Threshold-voltage control and enhancement-mode characteristics in multilayer tin disulfide field-effect transistors by gate-oxide passivation with an alkylphosphonic acid self-assembled monolayer

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We have synthesized crystals of two-dimensional layered tin disulfide (SnS_2) by chemical vapor transport and fabricated field-effect transistors based on mechanically exfoliated SnS_2 multilayer platelets. We demonstrate that the threshold voltage of these transistors can be modified by passivating the gate-oxide surface with a self-assembled monolayer of an alkylphosphonic acid, affording transistors with desirable enhancement-mode characteristics. In addition to a positive threshold voltage and a large on/off current ratio, these transistors also have a steep subthreshold swing of 4 V/decade. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4914488]

I. INTRODUCTION

Tin disulfide (SnS_2) is a two-dimensional layered metal dichalcogenide semiconductor.[1] Many of its electrical, optical, and catalytic properties are similar to those of molybdenum disulfide (MoS_2)[2] which has received significant attention mainly due to the large electron mobilities that have been measured in single- and multilayer MoS_2 field-effect transistors (FETs).[3–5] A potential advantage of SnS_2 over MoS_2 is its larger bandgap (greater than 2 eV for bulk SnS_2,[1] compared to 1.2 eV for bulk MoS_2, and 1.9 eV for single-layer MoS_2; see Ref. 2), which may translate into transistors having smaller off-state leakage currents and larger on/off current ratios. Recently, De *et al.*[6] and Song *et al.*[7] reported field-effect mobilities of 0.8 cm^2/V s for multilayer SnS_2 transistors[6] and 50 cm^2/V s for single-layer SnS_2 transistors.[7]

An undesirable feature of many of the previously reported MoS_2 and SnS_2 transistors is that they show depletion-mode behavior,[3–12] i.e., a significant charge-carrier density is present in the semiconductor channel even at a gate-source voltage of zero, so that a negative gate-source voltage must be applied in order to turn these transistors off. Depletion-mode behavior is undesirable for many FET applications, because it means that the circuit or system requires both a negative and a positive supply voltage.[10–12] The ability to control the threshold voltage during the device fabrication in order to obtain enhancement-mode characteristics is thus a valuable benefit in view of efficient circuit and system design. In single-crystalline silicon metal-oxide-semiconductor field-effect transistors (MOSFETs), the threshold voltage is usually adjusted by incorporating small amounts of either electron-donating or electron-accepting impurity atoms (e.g., phosphorus or boron) into the silicon lattice in the channel region of the transistors.

An alternative approach to control the threshold voltage during the fabrication is the passivation of the gate-oxide surface with an organic self-assembled monolayer (SAM).[13] By introducing a hydrophobic aliphatic SAM at the interface between the gate oxide and the semiconductor, the density of mobile charges otherwise present in the semiconductor channel at a gate-source voltage of zero can be greatly reduced by eliminating interfacial dipoles and trap states, thus providing a nearly charge-neutral semiconductor-dielectric interface[14] that leads to the desirable enhancement-mode characteristics.

Here, we demonstrate multilayer SnS_2 FETs in which enhancement-mode behavior is achieved by passivating the gate-oxide surface with an alkylphosphonic acid SAM prior to the deposition of the semiconductor. For comparison, we also fabricated multilayer SnS_2 FETs without SAM modification, and these devices show depletion-mode behavior. To our knowledge, this is the first report of SnS_2 FETs with enhancement-mode characteristics.

II. EXPERIMENT

Tin disulfide (SnS_2) crystals were synthesized by chemical vapor transport in vacuum-sealed ampoules using a horizontal tubular furnace at a temperature of 700 °C, starting from a pellet of elemental tin and a stoichiometric amount of sulfur and using iodine as a carrier agent.[15] Figure 1 shows several photographs and scanning electron microscopy (SEM) images of the vapor-transport-grown SnS_2 crystals. The two-dimensional layered structure consisting of covalently bound layers of edge-sharing SnS_2 octahedra weakly bound by van der Waals forces is clearly visible in the SEM images. The crystallinity of the SnS_2 platelets was also confirmed by x-ray diffraction (see Figure 2(a)). To estimate the

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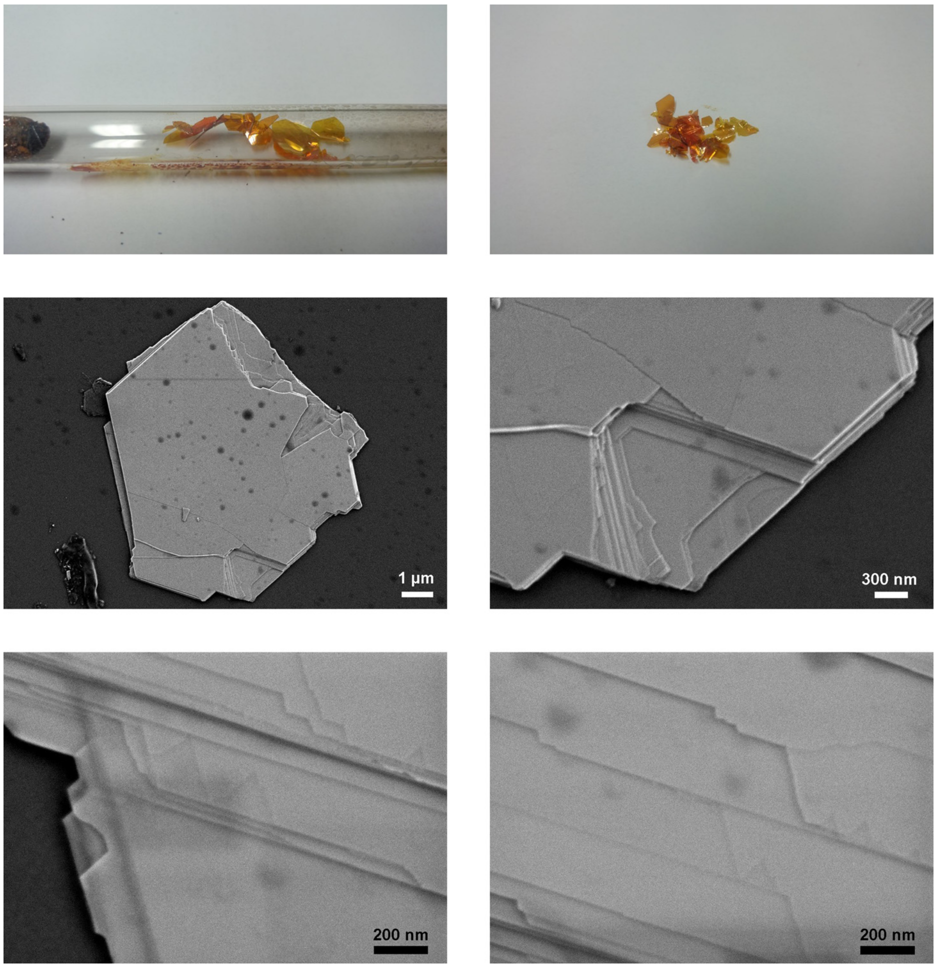

FIG. 1. Photographs and scanning electron microscopy images of SnS_2 crystals produced by chemical vapor transport.

bandgap of the SnS_2 crystals, a diffuse optical reflectance spectrum was measured for wavelengths from 400 to 800 nm (see Figure 2(b)). The reflectance spectrum was transformed according to the Kubelka-Munk formalism, and the bandgap was determined by a linear fit, indicating a bandgap of 2.2 eV.

Transistors were fabricated on heavily boron-doped, thermally oxidized silicon substrates, so that the doped silicon can be used as the gate electrode of the FETs. Prior to the deposition of the semiconductor, the surface of the thermally grown SiO_2 layer was functionalized with a thin layer of aluminum oxide (deposited by atomic layer deposition) and a solution-processed SAM of *n*-tetradecylphosphonic acid.[16] The chemisorption of the alkylphosphonic acid molecules on the Al_2O_3 surface leads to the spontaneous formation of a dense, hydrophobic monolayer, with the alkylphosphonic acid molecules being attached to the Al_2O_3 surface by strong covalent bonds.[17] A beneficial effect of the formation of the SAM is that essentially all hydroxyl groups initially present at the Al_2O_3 surface are eliminated, resulting in a clean, well-defined interface with a greatly reduced density of trap states.[17] The quality of the alkylphosphonic acid SAM was confirmed by contact-angle measurements, which consistently yielded contact angles for water of greater than 110°.[18] The SiO_2/Al_2O_3/SAM gate dielectric has a total thickness of 110 nm and a capacitance per unit area of 34 nF/cm^2.[19] Note that the SAM treatment was performed only in those (relatively small) areas of the substrate in which the

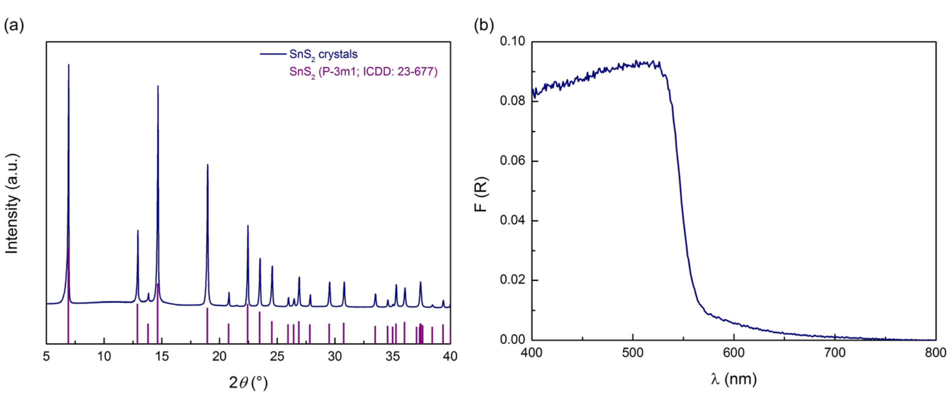

FIG. 2. (a) X-ray diffractogram of one batch of SnS_2 crystals employed in this work. The measured powder pattern is in good agreement with the reference (ICDD: file 23-677). (b) Diffuse optical reflectance spectrum of the same SnS_2 crystal, indicating a bandgap of 2.2 eV (corresponding to an absorption edge of 560 nm).

transistors were to be fabricated; the remainder of the substrate surface was left hydrophilic, since a completely hydrophobic substrate would have been difficult to uniformly coat with electron-beam resist (which is required for the patterning of the source and drain contacts on the surface of the SnS_2 platelets).

Crystalline SnS_2 platelets (flakes) with a thickness of a few hundred nanometers and lateral dimensions of a few tens of microns were then peeled from the SnS_2 crystals by mechanical exfoliation and deposited onto the SAM-functionalized $Si/SiO_2/Al_2O_3$ substrates. We also attempted to produce thinner platelets, but the result were always platelets with very small lateral dimensions, i.e., any platelets with a thickness of less than 100 nm had lateral dimensions of less than 1 μm and were thus not useful for device fabrication. (This problem was recently successfully addressed by Li *et al.*[20] who demonstrated that by exfoliating the flakes first onto a viscoelastic polymeric template and from there onto the hard silicon substrate, very large single-layer MoS_2 flakes can be obtained with excellent yield and quality.)

Finally, Ti/Au source and drain contacts were defined on the top surface of the SnS_2 platelets by electron-beam lithography, metal deposition by thermal evaporation in vacuum, and lift-off in organic solvents. All electrical measurements were performed in ambient air at room temperature.

III. RESULTS AND DISCUSSION

Figure 3 shows the schematic cross section and optical as well as SEM images of a transistor with a channel length of 5 μm and a channel width of 20 μm based on a SnS_2 platelet with a thickness of 380 nm. The thickness of the platelet was determined by atomic force microscopy (AFM). For comparison, we also fabricated transistors using SnS_2 platelets with similar dimensions and thickness, but without covering the gate-oxide surface with a SAM.

The effect of the SAM passivation of the gate-oxide surface on the threshold voltage of the transistors can be seen in Figure 4(a). The transistor in which the SAM treatment was omitted displays depletion-mode behavior, with a large negative threshold voltage (-10 V) and a significant drain current at a gate-source voltage of zero, similar to many of the previously reported MoS_2 and SnS_2 transistors.[3–12] In contrast, the transistor in which the gate oxide was passivated with an alkylphosphonic acid SAM shows desirable enhancement-mode characteristics, with a positive threshold voltage ($+20$ V) and a negligible drain current at zero gate-source voltage. Owing to the SAM passivation of the gate dielectric, the transistor can be completely turned off without the need for a negative gate-source voltage.

Figure 4(b) shows that the transistor with the SAM-functionalized gate oxide has an on/off current ratio of about 10^6 at a drain-source voltage of 10 V and 5×10^4 at a drain-source voltage of 30 V. From the transfer characteristics, maximum field-effect mobilities of 0.03 $cm^2/V\,s$ in the saturation regime (Figure 4(c)) and 0.04 $cm^2/V\,s$ in the linear regime (Figure 4(d)) can be extracted. At small drain-source voltages (1 V), the subthreshold swing is as steep as 4 V/decade (Figure 4(e)), which is a significant improvement over the

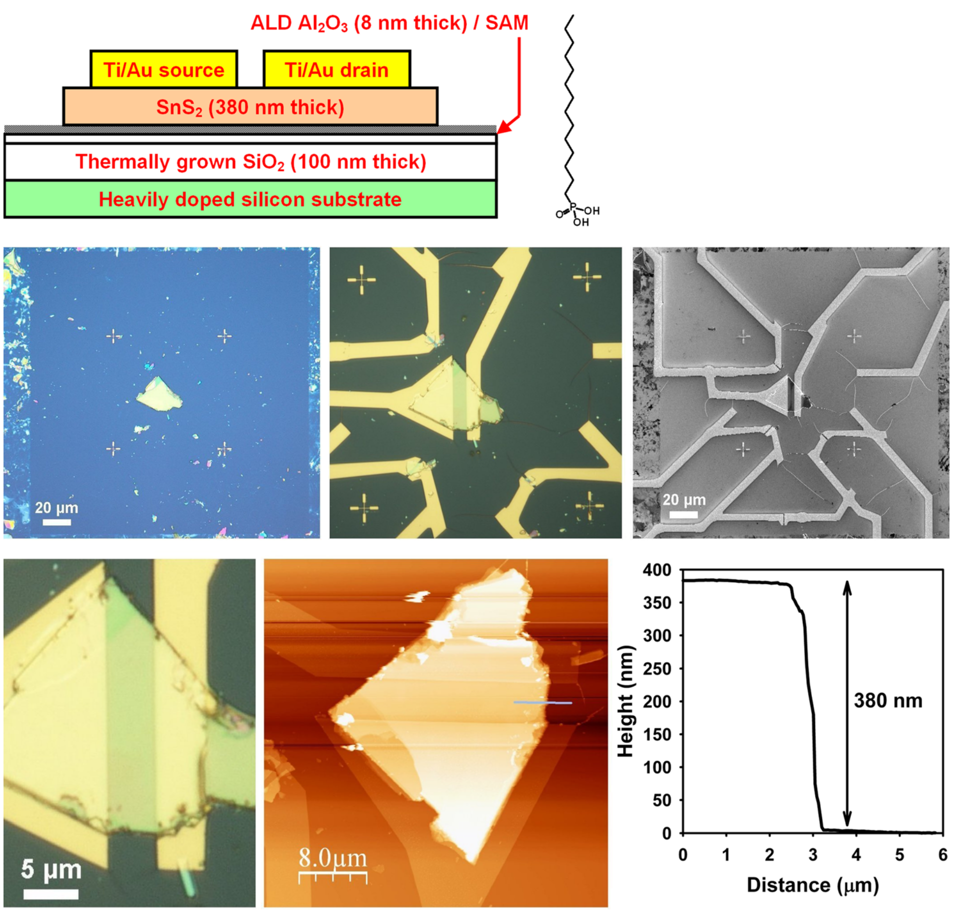

FIG. 3. Schematic cross section, optical micrographs, scanning electron microscopy image, and atomic force microscopy image of a multilayer SnS_2 field-effect transistor with a channel length of 5 μm and a channel width of 20 μm, based on a SnS_2 platelet with a thickness of 380 nm obtained by mechanical exfoliation from a single-crystal. Prior to depositing the SnS_2 platelet on the thermally oxidized silicon substrate, the SiO_2 substrate surface was functionalized with an 8-nm-thick aluminum oxide layer and a SAM of *n*-tetradecylphosphonic acid (the molecular structure of which is also shown). The Ti/Au source and drain contacts were patterned by electron-beam lithography on the SnS_2 platelet.

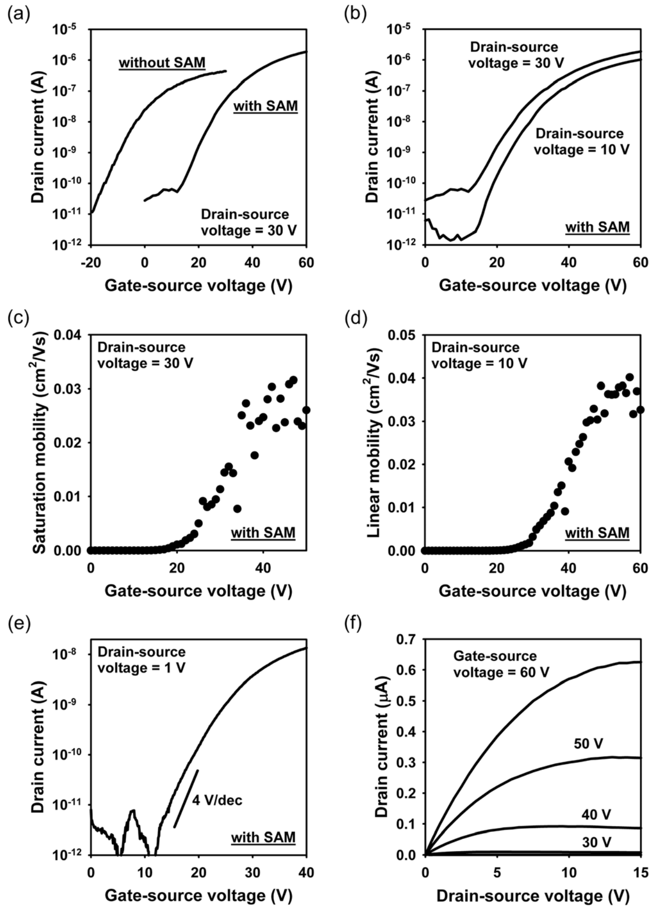

FIG. 4. (a) Transfer characteristics of multilayer SnS_2 FETs with and without SAM passivation of the gate oxide, both measured at a drain-source voltage of 30 V. (b) Transfer characteristics measured at drain-source voltages of 10 V and 30 V. (c) Field-effect mobility in the saturation region ($V_{DS} = 30$ V). (d) Field-effect mobility in the linear region ($V_{DS} = 10$ V). (e) Subthreshold characteristics ($V_{DS} = 1$ V). (f) Output characteristics.

10 V/decade reported in Ref. 6 for multilayer SnS_2 transistors, although it does not reach the 1.5 V/dec reported in Ref. 7 for single-layer SnS_2 transistors. The output characteristics (Figure 4(f)) display excellent linearity at small drain-source voltages and very good saturation at large drain-source voltages.

The fact that the field-effect mobility extracted from the current-voltage characteristics (0.04 cm^2/V s) is smaller by several orders of magnitude compared with the field-effect mobilities reported in the literature for FETs based on the same semiconductor (0.8 cm^2/V s for the multilayer SnS_2 transistors in Ref. 6; 50 cm^2/V s for the single-layer SnS_2 transistors in Ref. 7) is likely related to the substantially greater semiconductor thickness (380 nm in our work, compared to 15 nm in Ref. 6 and 2 nm in Ref. 7). Since the gate-induced carrier channel is located in close proximity to the semiconductor/dielectric interface (see Figure 3(c) in Ref. 20), a large semiconductor thickness implies that the charge carriers travel a significant distance from the source contact to the channel and from there to the drain contact through a highly resistive region essentially devoid of charge carriers (labeled "inactive layer" in Figure 3(c) in Ref. 20). Even if the carrier mobility in the crystal was isotropic, the fact that the carrier density is so much smaller in the inactive layer than in the gate-induced carrier channel would mean that the total resistance of the FET is dominated by the access resistance, rather than the channel resistance, resulting in a significantly reduced effective field-effect mobility. However, the layered structure of the SnS_2 crystals implies that the carrier mobility is highly anisotropic, with the out-of-plane mobility likely being substantially smaller than the in-plane mobility, which further reduces the effective mobility extracted from the current-voltage characteristics of FETs based on thicker platelets. For MoS_2 transistors, this trend was recently experimentally verified by Li *et al.* (see Figure 2 in Ref. 21). Our results further emphasize the significant benefit of utilizing thinner crystals (with a maximum thickness of approximately 30 nm) for FET fabrication.

Finally, we have also monitored the performance of the multilayer SnS_2 transistor with the SAM-passivated gate oxide over a period of four months during which the substrate was stored in ambient air with a humidity of about 50% under yellow laboratory light. Figure 5 shows that the performance of the transistor remains virtually unchanged over this period of time, indicating that these devices have good shelf-life stability under ambient conditions.

IV. CONCLUSION

We have synthesized two-dimensional layered tin disulfide (SnS_2) crystals by chemical vapor transport, confirmed their crystallinity and their relatively large bandgap (2.2 eV) by electron microscopy, x-ray diffraction and diffuse optical reflectance spectroscopy measurements, and fabricated field-effect transistors based on mechanically exfoliated SnS_2 platelets with a thickness of a few hundred nanometers. We have demonstrated that the passivation of the gate-oxide surface with an alkylphosphonic acid self-assembled monolayer prior to the deposition of the semiconductor results in FETs that display desirable enhancement-mode characteristics, whereas FETs in which the SAM treatment of the gate oxide

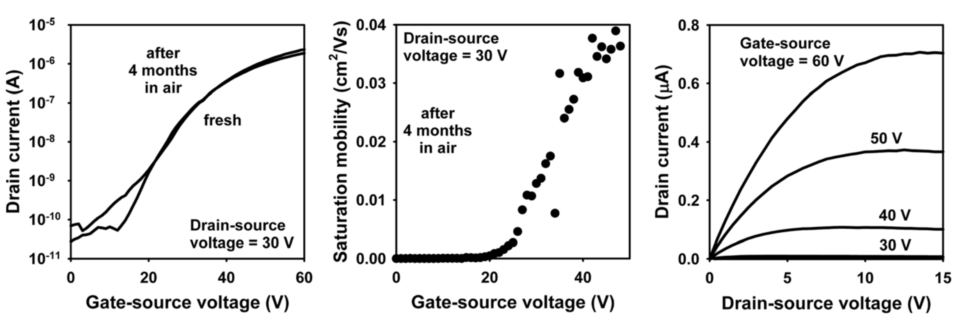

FIG. 5. Shelf-life stability of SnS_2 FETs: Transfer characteristics, saturation mobility, and output characteristics of the same TFT shown in Figures 4(b)–4(f) after four months of storage in ambient air.

is omitted show depletion-mode behavior. To our knowledge, this is the first time that enhancement-mode SnS_2 FETs have been reported. In addition, the transistors also have a large on/off current ratio (10^6) and a steep subthreshold swing (4 V/decade). The small field-effect mobility of our transistors is the result of the large thickness of the platelets (several hundred nanometers) which leads to a large access resistance between the gate-induced carrier channel (located at the semiconductor/dielectric interface) and the source and drain contacts, which further emphasizes the benefit of utilizing thinner crystals for FET fabrication.

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