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1 Introduction

The properties of single-walled carbon nanotubes (SWCNTs) have received significant attention since their discovery. Their electrical characteristics are usually investigated in a three-terminal device configuration: Two terminals contacting the nanotube (labelled source [S] and drain [D]) are used to apply a voltage along the tube, whereas the third terminal (labelled gate [G]) is electrically insulated from the tube and used to manipulate the electrostatic potential of the tube. The performance of SWCNT devices such as single-electron transistors (SETs) as well as field-effect transistors (FETs) depends critically on the properties of the gate dielectric. Different materials have been explored for this purpose [1–3]. Usually, a relatively thick (>100 nm) silicon oxide layer is utilised in a back-gate configuration, where the gate electrode also serves as the substrate. In these devices the gate coupling is relatively weak so that comparably high voltages have to be applied to the back gate to enable device operation [1]. Furthermore, these devices often suffer from a relatively large hysteresis in the drain current when sweeping the gate–voltage (e.g. 15 V for 500 nm thick SiO_2) and large threshold voltages [4]. Reducing the thickness of the insulating layer increases the gate coupling and can reduce the hysteresis, but often results in an increased leakage current through the gate dielectric [2]. Here, we present a very thin gate dielectric that can be made at low process temperatures and permits SWCNT-FETs operation at gate voltages of –2 V, with low gate leakage currents and a small hysteresis.

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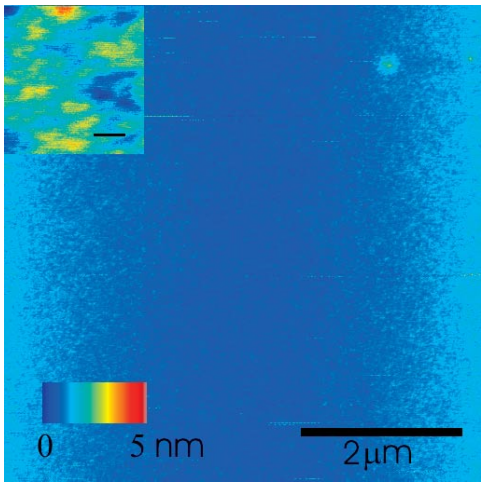

Fig. 1 (online colour at: www.pss-b.com) Tapping-mode AFM image of the silicon substrate covered by the SAM. The layer is very smooth over large areas. *Inset*: Close-up view. The scale bar here is 20 nm, and the colour scale ranges from 0 to 0.5 nm.

2 Experimental

Our approach relies upon an organic self-assembled monolayer (SAM) made of 18-phenoxyoctadecyltrichlorosilane that is used as a dielectric in a back-gate configuration. This SAM has been used previously as the gate dielectric for low-voltage, high-mobility pentacene organic thin film transistors [5]. A natively oxidized, heavily doped silicon wafer serves as the substrate and gate electrode. After a brief oxygen plasma treatment (100 W, 10 sec, substrate at room temperature) the silicon oxide has a thickness of about 4 nm, as determined by ellipsometry. The monolayer self-assembles on the plasma-treated silicon oxide surface from the vapour phase in a reduced-pressure nitrogen ambient at a temperature of 200 °C. An atomic force microscopy (AFM) image of the SAM covered substrate is shown in Fig. 1, which proves that the monolayer is molecularly flat across large areas. Due to the low process temperature, SAM gate dielectrics can be used on flexible substrates, such as metallized plastic foils [6].

Since the SAM is very hydrophobic, spin-coating of the electron-beam resist onto the SAM surface is only possible after evaporation of 0.3 nm Ti onto the surface prior to spin coating. The titanium immediately oxidizes and therefore does not contribute to the conduction between source and drain contacts as has been determined by electrical measurement. HiPCO (High Pressure CO Conversion) SWCNTs were dispersed in aqueous solution using a surfactant and deposited on the Ti-covered SAM. Source and drain contacts were then fabricated on top of the SWCNTs by standard e-beam lithography using an electron dose of 300 µC/cm^2. The metal contacts consist of 15 nm AuPd and have a contact spacing of 200 nm. A schematic depiction of the device structure is given in Fig. 2. Devices incorporating individual SWCNTs were identified by tapping-mode atomic force microscopy, followed by careful glue-bonding of metal wires onto the contact pads.

In addition to SWCNT devices, two types of test structures were fabricated to determine whether the electron exposure during lithography causes damage of the SAM. Both types of samples consist of a

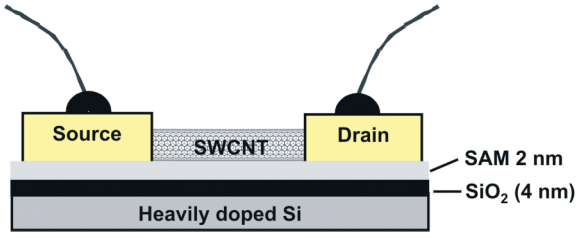

Fig. 2 (online colour at: www.pss-b.com) Schematic device setup. The heavily doped silicon wafer (shown in grey) is covered with a 4 nm thin SiO_2 layer (black). On top of the SAM (light grey) individual SWCNTs are connecting source and drain AuPd contacts. Thin metal wires are glue-bonded to the contacts.

heavily doped silicon wafer as back-gate, the insulating SAM and metal pads (200×200 μm^2) evaporated on top. The metal was patterned either through a shadow mask or by electron-beam lithography and lift-off. The leakage current through the SAM dielectric was found to be independent (10^{-7} A/cm^2) of whether the metal contact is patterned through the shadow mask or by e-beam lithography, indicating that an electron dose of 300 μC/cm^2 does not inflict significant damage on the SAM.

3 Results and discussion

Devices comprising individual metallic SWCNTs display single-electron charging phenomena at low temperature (Fig. 3). The ultra-small thinness of the SAM dielectric manifests itself in a small spacing of the Coulomb oscillation peaks of the nanotube dot [7]. The four-fold periodicity of the peaks, which is discernible in the current vs. gate voltage-plot, arises from the two-fold degenerate low-energy band structure of metallic SWCNTs combined with spin [8]. According to theory, the peak spacing is approximately given by $\Delta V_g = (U + \Delta E)/e\alpha$, where $U = e^2/C$ is the Coulomb charging energy, ΔE is the discrete level spacing, and $\alpha = C_g/C$ is the gate coupling constant. C corresponds to the total capacitance of the quantum dot and C_g is the gate capacitance [7]. Within each group the peak spacing between the first and second peak (as marked in Fig. 3) [9] is dominated by the Coulomb interaction [10]. Devices comprising the SiO_2 (4 nm)/SAM (2 nm)-dielectric like the one shown in Fig. 3 exhibit a peak spacing $\Delta V_g = e/C_g$ of ~24 mV, whereas a value of 120 mV was found for devices with a 200 nm thick thermally grown SiO_2 gate insulator. The peak spacing related to the SAM dielectric devices yields a gate capacitance of $\sim 7 \times 10^{-18}$ F, which agrees within a factor of two with the capacitance estimated from the transistor geometry by using the dependence $C_{gate} = 2\pi\varepsilon\varepsilon_0 L/[\cosh^{-1}(h/r)] \approx 2\pi\varepsilon\varepsilon_0 L/\ln(2h/r)$, where the dielectric constant $\varepsilon \sim 3$, the gate insulator thickness $h = 6$ nm, and the radius of the nanotube $r \sim 1$ nm [4].

Devices consisting of individual semiconducting SWCNTs showed FET behaviour. Figure 4a shows the output characteristics of such a device measured under ambient conditions. The device exhibits typical p-type behaviour with excellent saturation of the drain current (Fig. 4a). To our knowledge, these devices represent the first low-voltage individual SWCNT transistors with a low-temperature organic gate dielectric. In contrast to previous reports [11], no significant difference in the drain current was observed depending on the direction of current flow at high gate voltages (i.e., when the drain and source are exchanged; Fig. 4a). This finding indicates the absence of a significant asymmetry in the injection properties of the two contacts.

The transfer characteristics of the same device, also measured under ambient conditions, are shown in Fig. 4b. The drain current exceeds the gate leakage current by about three orders of magnitude, so it is justified to state that the gate leakage current is negligible. A transconductance of 0.5 μS at $V_{DS} = -1$ V

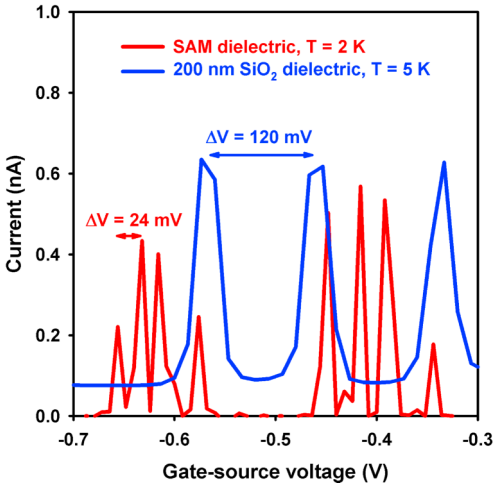

Fig. 3 (online colour at: www.pss-b.com) Coulomb oscillations due to single-electron tunnelling in devices made from individual metallic SWCNTs using two different gate dielectrics (4 nm SiO_2 plus organic SAM, or 200 nm thermal SiO_2). Indicated are the respective peak spacings within the groups consisting of four peaks.

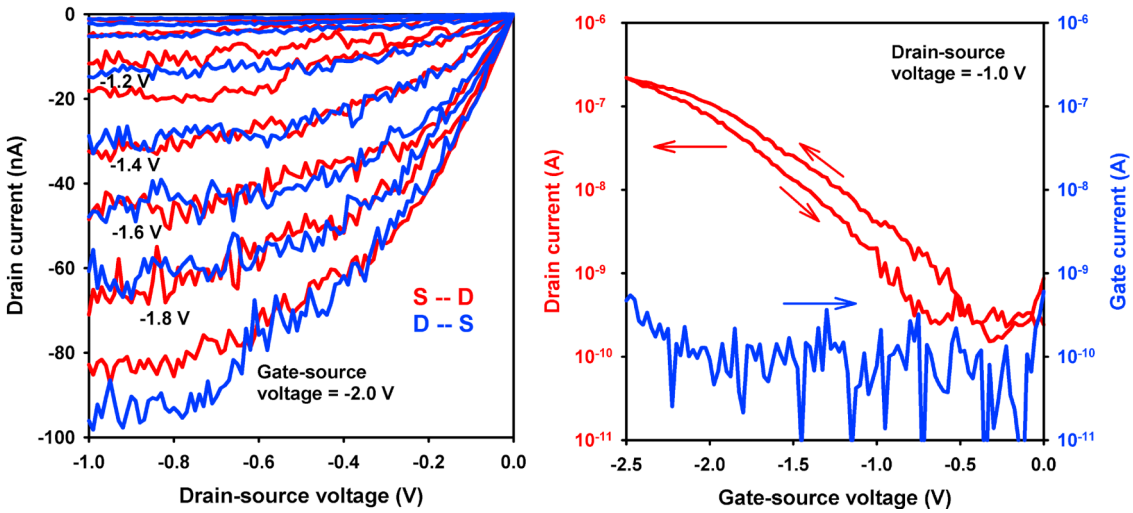

Fig. 4 (online colour at: www.pss-b.com) a) Output characteristic of a semiconducting SWCNT. Source and drain have been exchanged in the red and blue traces. b) Transfer characteristic of the same device. The gate voltage sweep rate was 250 mV/s. All curves are measured under ambient conditions.

and a relatively large on/off current ratio of about 10^4 are obtained. Moreover, the SWCNT-FET turns on at a gate-source voltage close to zero and has a threshold voltage of −1.1 V. The subthreshold swing has been determined to be 290 mV/dec at room temperature, which is a fair result considering that no attempts were made to reduce the contact resistance [12].

As in the case of virtually all individual SWCNT transistors reported in the literature, a hysteresis in the transfer characteristics can be observed (see Fig. 4b). Compared to most other FET devices, however, the hysteresis in our transistors is comparatively small (~200 mV under ambient conditions).

4 Conclusion

In summary, we have demonstrated that the implementation of an organic SAM gate dielectric strongly enhances the gate coupling. Two different types of transistors with a channel length of 200 nm were fabricated on this basis using e-beam lithography, namely single-electron transistors from individual metallic SWCNTs and FETs from individual semiconducting SWCNTs. The latter devices show good performance, including a very small hysteresis in the drain current (200 mV), a large transconductance of 0.5 μS, a small subthreshold swing of 290 mV/dec, and an on/off current ratio of 10^4 [13].

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