Organic Electronics 14 (2013) 3213–3221

Contents lists available at ScienceDirect

Organic Electronics

journal homepage: www.elsevier.com/locate/orgel

High-mobility organic thin-film transistors based on a small-molecule semiconductor deposited in vacuum and by solution shearing

Robert Hofmockel [a], Ute Zschieschang [a], Ulrike Kraft [a], Reinhold Rödel [a], Nis Hauke Hansen [b], Matthias Stolte [c], Frank Würthner [c], Kazuo Takimiya [d,e], Klaus Kern [a,f], Jens Pflaum [b], Hagen Klauk [a,*]

[a] Max Planck Institute for Solid State Research, Heisenbergstr. 1, 70569 Stuttgart, Germany
[b] Experimental Physics VI, University of Würzburg and Bavarian Center for Applied Energy Research (ZAE Bayern e.V.), Am Hubland, 97047 Würzburg, Germany
[c] Universität Würzburg, Institut für Organische Chemie and Röntgen Research Center for Complex Material Systems, Am Hubland, 97074 Würzburg, Germany
[d] Department of Applied Chemistry, Graduate School of Engineering, Institute for Advanced Materials Research, Hiroshima University, Higashi-Hiroshima, Japan
[e] Emergent Molecular Function Research Team, RIKEN Advanced Science Institute, Wako, Saitama, Japan
[f] École Polytechnique Fédérale de Lausanne, Institut de Physique de la Matière Condensée, 1015 Lausanne, Switzerland

ARTICLE INFO

Article history:
Received 29 May 2013
Received in revised form 15 August 2013
Accepted 2 September 2013
Available online 19 September 2013

Keywords:
Organic thin-film transistors
C_{10}-DNTT
Thin-film morphology
Contact resistance
Solution shearing

ABSTRACT

The small-molecule organic semiconductor 2,9-di-decyl-dinaphtho-[2,3-b:2′,3′-f]-thieno-[3,2-b]-thiophene (C_{10}-DNTT) was used to fabricate bottom-gate, top-contact thin-film transistors (TFTs) in which the semiconductor layer was prepared either by vacuum deposition or by solution shearing. The maximum effective charge-carrier mobility of TFTs with vacuum-deposited C_{10}-DNTT is 8.5 $cm^2/V\,s$ for a nominal semiconductor thickness of 10 nm and a substrate temperature during the semiconductor deposition of 80 °C. Scanning electron microscopy analysis reveals the growth of small, isolated islands that begin to coalesce into a flat conducting layer when the nominal thickness exceeds 4 nm. The morphology of the vacuum-deposited semiconductor layers is dominated by tall lamellae that are formed during the deposition, except at very high substrate temperatures. Atomic force microscopy and X-ray diffraction measurements indicate that the C_{10}-DNTT molecules stand approximately upright with respect to the substrate surface, both in the flat conducting layer near the surface and within the lamellae. Using the transmission line method on TFTs with channel lengths ranging from 10 to 100 μm, a relatively small contact resistance of 0.33 kΩ cm was determined. TFTs with the C_{10}-DNTT layer prepared by solution shearing exhibit a pronounced anisotropy of the electrical performance: TFTs with the channel oriented parallel to the shearing direction have an average carrier mobility of $(2.8 \pm 0.3)\ cm^2/V\,s$, while TFTs with the channel oriented perpendicular to the shearing direction have a somewhat smaller average mobility of $(1.3 \pm 0.1)\ cm^2/V\,s$.

1. Introduction

Organic thin-film transistors (TFTs) have gained great interest for their potential application in electronic components and products, for example in flexible active-matrix displays or flexible sensors [1–5]. One important requirement for most applications is a high charge-carrier mobility. In 2007, the small-molecule p-channel semiconductor dinaphtho-[2,3-b:2′,3′-f]-thieno-[3,2-b]-thiophene (DNTT) was introduced and showed a relatively high hole mobility up to 3 $cm^2/V\,s$, combined with excellent air stability [6,7]. More recently, the alkylated DNTT derivative C_{10}-DNTT

* Corresponding author.
E-mail address: H.Klauk@fkf.mpg.de (H. Klauk).

1566-1199/$ - see front matter © 2013 Elsevier B.V. All rights reserved.
http://dx.doi.org/10.1016/j.orgel.2013.09.003

(2,9-di-decyl-dinaphtho-[2,3-b:2′,3′;-f]-thieno-[3,2-b]-thiophene) showed even higher hole mobilities up to 12 cm^2/V s [8–11]. These results show that the strategic introduction of alkyl substituents into the molecular structure has an important effect on the crystal structure and/or thin-film morphology of organic semiconductors and thereby on the TFT performance. The structure of C_{10}-DNTT is shown in Fig. 1. The molecule has a calculated length of 39.3 Å, a (001) interlayer distance (d-spacing) deduced by structural X-ray analysis of 38.0 Å and a HOMO energy of −5.38 eV [8]. Here we investigate the evolution of the thin-film morphology of vacuum-deposited C_{10}-DNTT films as a function of the film thickness and the substrate temperature during the deposition and the correlation with the effective field-effect mobility and the contact resistance of the TFTs. In addition to C_{10}-DNTT TFTs with a vacuum-deposited semiconductor layer we have also prepared TFTs in which the semiconductor was deposited by solution shearing and investigated the in-plane spatial anisotropy of the charge transport in the solution-sheared semiconductor films.

2. Transistors with vacuum-deposited semiconductor

All organic TFTs were fabricated on p-doped thermally oxidized silicon substrates that simultaneously serve as global back-gates. For the TFTs with a vacuum-deposited semiconductor the gate dielectric consists of a 100-nm-thick layer of thermally grown silicon dioxide, an 8-nm-thick layer of aluminum oxide (by atomic layer deposition) and a self-assembled monolayer of n-tetradecylphosphonic acid (obtained by immersion in a 2-propanol solution) [7,12,13]. In this case, the gate dielectric has a total thickness of 110 nm and a capacitance per unit area of 34 nF cm^{-2}. The organic semiconductor was deposited in vacuum at a pressure of about 10^{-6} mbar. During the semiconductor deposition the temperature of the substrate holder was set to a specific value between room temperature and 180 °C, and the nominal thickness of the vacuum-deposited semiconductor layer was measured with a quartz crystal microbalance. The deposition rate was about 1 nm/min. The source and drain contacts were formed on the top surface of the semiconductor by evaporating gold in vacuum through a silicon stencil mask [13].

All electrical measurements were performed in ambient air at room temperature. The effective hole mobilities of the TFTs were calculated from the saturation transfer characteristics with the following formula [14]:

$$I_D = \frac{\mu C_i W}{2L}(V_{GS} - V_{th})^2, \quad (1)$$

where I_D is the drain current, μ is the effective field-effect mobility, C_i is the gate-dielectric capacitance per unit area, W is the channel width, L is the channel length, V_{GS} is the gate-source voltage, and V_{th} is the threshold voltage.

In a first series of experiments, the C_{10}-DNTT was deposited at a substrate temperature of 80 °C and the nominal thickness of the semiconductor layer was varied between 1 and 25 nm. The measured transfer characteristics and the effective mobility as a function of nominal semiconductor thickness are shown in Fig. 2. For a nominal semiconductor thickness of less than 4 nm the drain current is below the noise level. For a nominal thickness of 4 nm, which corresponds to the calculated length of the molecules, a small field effect with an on/off ratio of 10^2 and an effective mobility of about 10^{-5} cm^2/V s is measurable. Upon increasing the nominal C_{10}-DNTT thickness from 4 to 10 nm, the on-state drain current, the on/off ratio and the effective mobility increase. At a nominal thickness of 10 nm the maximum mobility of 8.5 cm^2/V s is reached. For a nominal C_{10}-DNTT thickness greater than 10 nm the mobility does not show a thickness dependence within the process fluctuations.

Interestingly, the vacuum-deposited C_{10}-DNTT films have a pronounced topology with extremely tall lamellae protruding from the surface. Even for a nominal thickness of less than 10 nm, these C_{10}-DNTT lamellae have elevations of over 100 nm, making it difficult to obtain useful AFM (atomic force microscopy) images of the surface. Therefore, the semiconductor morphology was investigated by scanning electron microscopy (SEM). Fig. 3 shows SEM images of C_{10}-DNTT vacuum-deposited at a substrate temperature of 80 °C with a nominal semiconductor thickness of 0.5 nm, 1.0 nm, 3.0 nm and 6.0 nm. In these images the bare substrate appears light gray and the lamellae appear white. In addition, the SEM images show dark gray regions which appear in the form of small, isolated islands when the nominal thickness is very small (e.g., 0.5 nm, 1.0 nm) and which begin to coalesce when the nominal thickness is increased to about 3 nm and form a connected and finally closed layer for a nominal thickness greater than about 4 nm respectively 10 nm. Since 4 nm is the nominal thickness at which the electrical measurements indicate the onset of a field effect (see Fig. 2), these dark gray regions are believed to represent the extent of the flat conducting channel layer formed by the C_{10}-DNTT molecules on the substrate surface. From the SEM images, the exact thickness of these conducting channel regions cannot be determined.

In a second series of experiments, C_{10}-DNTT layers with a nominal thickness of 10 nm were vacuum-deposited onto substrates held at temperatures between 40 and 180 °C. Fig. 4 shows the effective mobility as a function of substrate temperature during the C_{10}-DNTT deposition. As can be seen, the optimum range of substrate temperatures is about 60–80 °C, where the effective hole mobility exceeds 8 cm^2/V s, while for lower and higher substrate temperatures the effective mobility is smaller. A similar relationship between effective mobility and substrate temperature during the deposition has been reported for other

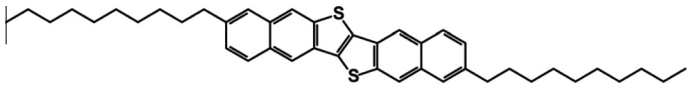

Fig. 1. Molecular structure of the organic semiconductor C_{10}-DNTT. The calculated length of the molecule is 39.3 Å [8].

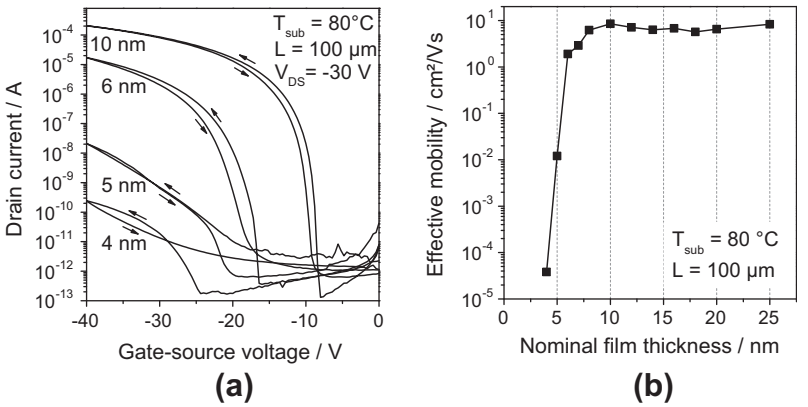

Fig. 2. (a) Transfer characteristics of C_{10}-DNTT TFTs with a vacuum-deposited semiconductor layer having a nominal thickness of 4 nm, 5 nm, 6 nm and 10 nm. The semiconductor was deposited onto substrates held at a temperature of 80 °C. (b) Effective field-effect mobility extracted from the transfer characteristics in the saturation regime as a function of the nominal C_{10}-DNTT thickness.

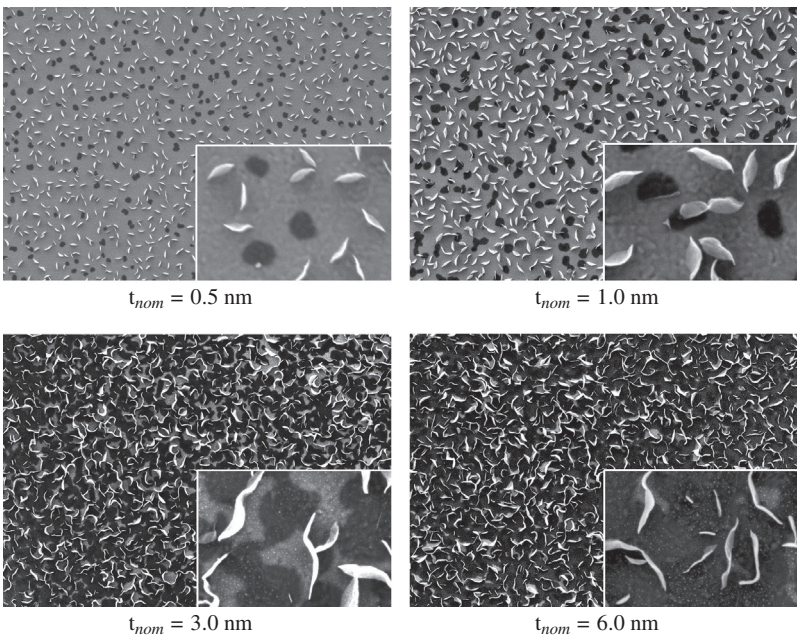

Fig. 3. Evolution of the thin-film morphology of vacuum-deposited C_{10}-DNTT when the nominal thickness is increased from 0.5 nm to 6.0 nm. The semiconductor was deposited at a substrate temperature of 80 °C. The images were obtained by scanning electron microscopy (SEM) with an acceleration voltage of 1.0 kV. The width of the large images corresponds to 10 µm and the width of the small images to 1 µm. The bare substrate appears light gray, the tall lamellae appear white and the flat channel layer appears dark gray.

organic semiconductors as well [15,16]. A possible explanation is that at lower substrate temperatures (<60 °C) the thermal energy is insufficient to induce long-range structural ordering within the semiconductor film, therefore leading to smaller grain sizes. At higher substrate temperatures (>80 °C) the charge-carrier transport between the grains is limited by the lack of inter-grain connectivity caused by partial dewetting of the organic molecules. This is confirmed by SEM observations which indicate the formation of macroscopic cracks at very high substrate temperatures (160 and 180 °C).

The analysis of the semiconductor morphology by SEM indicates that the number of lamellae per unit area is significantly smaller when the C_{10}-DNTT is deposited at higher substrate temperatures (see Fig. 5). This suggests that the lamellae are a metastable configuration, while the flat channel layer represents the thermodynamically stable configuration. At a substrate temperature of 180 °C the number of lamellae is sufficiently small so that the morphology of the flat conducting channel layer near the surface can be analyzed in a useful manner by AFM. The result is shown in Fig. 6. The AFM image shows that the

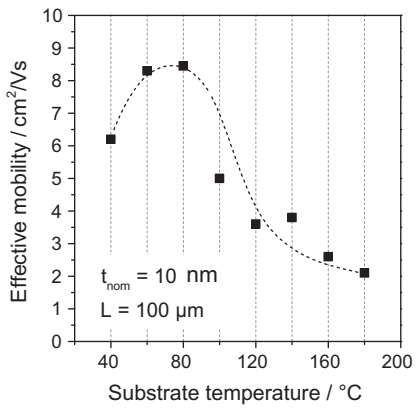

Fig. 4. Effective hole mobility in saturation as a function of the substrate temperature during the C_{10}-DNTT deposition. The nominal semiconductor thickness is 10 nm. As can be seen, the optimum substrate temperature is in the range of 60 to 80 °C. The dashed line is a guide-to-the-eye.

semiconductor grows primarily in the form of flat terraces with a step height of approximately 4 nm. This step height corresponds to the calculated length of a single C_{10}-DNTT molecule [8], suggesting that each terrace corresponds to a monolayer in which the molecules stand approximately upright with respect to the substrate surface.

To elucidate the structure of the vacuum-deposited semiconductor layers in more detail, X-ray diffraction (XRD) spectra were recorded on four C_{10}-DNTT layers deposited at substrate temperatures of 80 °C and 180 °C with nominal thicknesses of 10 nm and 100 nm (see Fig. 7). Since the films deposited at a substrate temperature of 180 °C are essentially devoid of lamellae, the peaks in the XRD spectra of these films can be assigned to the flat channel layer near the surface. In contrast, the nominally 100-nm-thick film deposited at a substrate temperature of 80 °C consist mainly of lamellae, so the peaks in the XRD spectra of this film can be unambiguously assigned to the lamellae. From the indexed Bragg peaks, average (0 0 1) interlayer spacings along the out-of-plane direction of (37.1 ± 0.7) Å for a substrate temperature of 80 °C and (38.3 ± 0.4) Å for a substrate temperature of 180 °C are calculated when the nominal thickness is 10 nm, whereas the average (0 0 1) interlayer spacings along the out-of-plane direction are (37.2 ± 0.1) Å for a substrate temperature of 80 °C and (37.5 ± 0.1) Å for a substrate temperature of 180 °C when the nominal thickness is 100 nm. These lattice constants agree satisfactorily with the XRD data reported by Kang et al. [8] as well as with our AFM results discussed above and further confirm that the molecules stand approximately upright with respect to the substrate surface, both in the flat conducting channel layer near the surface as well as in the lamellae. Assuming that the C_{10}-DNTT molecules have a length of 39.3 Å, as calculated by Kang et al. [8], these average d-spacings of (37.2 ± 0.1) Å and (37.5 ± 0.1) Å correspond to average molecular tilt angles of (18.8 ± 0.5)° at a substrate temperature of 80 °C and (17.4 ± 0.5)° at a substrate temperature of 180 °C.

The observation that the molecules within the flat channel layer stand approximately upright with respect to the substrate surface is not surprising; this has been reported for many other organic semiconductors [17,18]. On the other hand, based on kinetic considerations regarding the formation of the lamellae in the vacuum-deposited

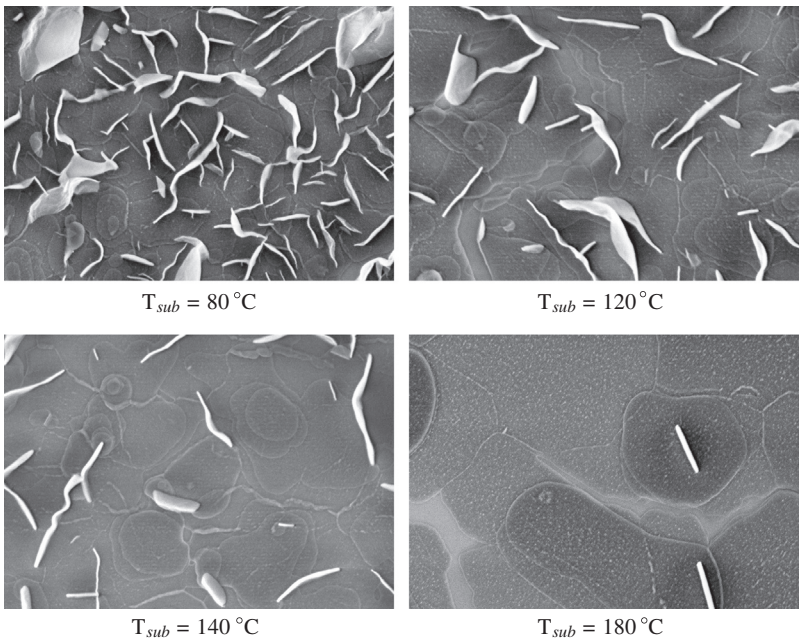

Fig. 5. SEM images of C_{10}-DNTT layers with a nominal thickness of 10 nm vacuum-deposited at substrate temperatures of 80 °C, 120 °C, 140 °C and 180 °C. As can be seen, the number of the tall lamellae per unit area is significantly smaller at higher substrate temperatures. The width of the images corresponds to 10 µm.

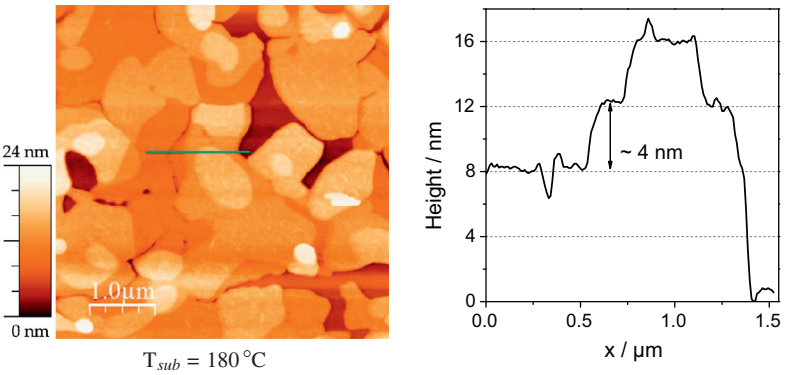

Fig. 6. Atomic force microscopy (AFM) image of the surface of a C_{10}-DNTT layer with a nominal thickness of 10 nm, vacuum-deposited at a substrate temperature of 180 °C. The green line indicates the line profile depicted on the right. Step heights of approximately 4 nm can be identified. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

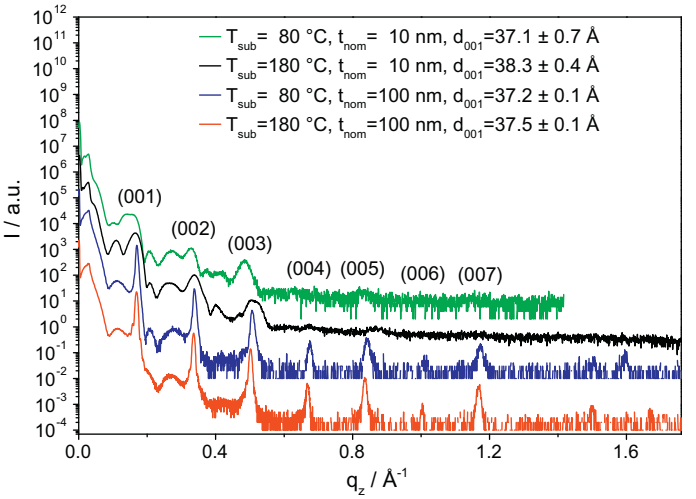

Fig. 7. X-ray diffraction spectra of C_{10}-DNTT layers vacuum-deposited at substrate temperatures of 80 °C and 180 °C with nominal thicknesses of 10 nm and 100 nm.

C_{10}-DNTT layers one may have been expecting that within the lamellae the molecules are oriented with their long axis parallel to the substrate surface. However, based on our XRD spectra, which extend to a scattering angle of 25° and thus allow us to resolve lattice spacings as small as 3.56 Å, we can rule out the existence of layers with a horizontal orientation of the molecules. The reason is that all Bragg peaks seen in our XRD spectra, regardless of the substrate temperature during the deposition, can be clearly assigned to molecular layers in which the C_{10}-DNTT molecules stand approximately upright with respect to the substrate surface.

Unfortunately, the extent to which the lamellae contribute to the charge transport in the TFTs is unknown at this point. We only know that the lamellae do not coalesce into a connected network (see Figs. 3 and 5) and therefore are unlikely to sustain lateral charge transport over macroscopic distances.

3. Contact resistance analysis

An important undesirable effect of all field-effect transistors including organic TFTs is the contact resistance [19,20]. To extract the contact resistance of our C_{10}-DNTT TFTs we have applied the transmission line method (TLM) [19–22]. For this purpose we fabricated TFTs with channel lengths ranging from 10 µm to 100 µm and determined the threshold voltage V_{th} individually from the transfer curve in the linear regime (at $V_{DS} = -0.1$ V) with the second-derivative method [23]. The total resistance $R = \frac{V_{DS}}{I_D}$, taken from the linear transfer curve at a specific overdrive voltage ($V_{GS} - V_{th} = -20$ V), was then normalized to the channel width and plotted as a function of the channel length (see data points in Fig. 8a). These measurement data were then fitted to the following equation (see red line in Fig. 8a):

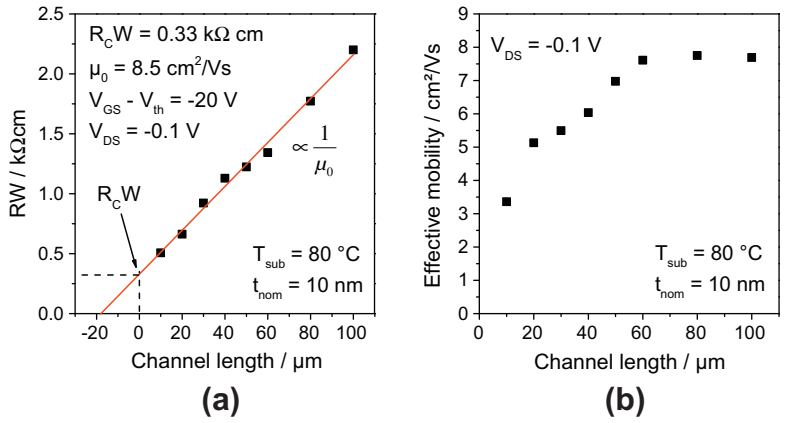

Fig. 8. (a) Transmission line method performed on vacuum-deposited C_{10}-DNTT TFTs with channel lengths ranging from 10 μm to 100 μm. The total width-normalized resistance of the TFTs is plotted as a function of the channel length. The TFTs have a contact length of 200 μm. The measurements were performed at a drain-source voltage of −0.1 V. The intercept of the fit (red line) with the *y*-axis defines the width-normalized contact resistance $R_C W$ and the slope yields the intrinsic mobility μ_0. (b) Effective field-effect mobility in the linear regime (drain-source voltage −0.1 V) as a function of the channel length. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

$$RW = R_C W + \frac{L}{\mu_0 C_i (V_{GS} - V_{th})}. \quad (2)$$

Extrapolating the fit to a channel length of zero yields the width-normalized contact resistance $R_C W$, and the slope of the fit gives the intrinsic mobility μ_0 (i.e., the hole mobility in the polycristalline channel without the influence of the contact resistance). For C_{10}-DNTT TFTs with a semiconductor layer deposited at a substrate temperature of 80 °C and a nominal thickness of 10 nm, a width-normalized contact resistance of 0.33 kΩ cm and an intrinsic mobility of 8.5 $cm^2/V\,s$ were extracted (see Fig. 8a). For comparison, the contact resistance of DNTT TFTs with the same contact length (the distance by which the gate electrode overlaps the source and drain contacts) is about 0.6 kΩ cm [24]. Despite the fact that the contact resistance is relatively small, its influence on the effective mobility for short channel lengths is evident (see Fig. 8b).

Fig. 9a shows the dependence of the contact resistance on the nominal semiconductor thickness; no distinct tendency can be identified. Richards et al. [25] previously reported that with greater semiconductor thickness the contact resistance increases, due to the greater distance between the top contacts and the conducting channel layer at the semiconductor/dielectric interface. However, in our vacuum-deposited C_{10}-DNTT TFTs most of the deposited semiconductor material goes into the lamellae which cover only a fraction of the substrate surface, so that the thickness of the flat conducting channel layer near the surface does not increase beyond a few monolayers and the contact metal is always close to the conducting channel layer. This can be nicely seen in Fig. 10, which shows SEM images of a C_{10}-DNTT layer with a nominal thickness of 22 nm vacuum-deposited at a substrate temperature of 80 °C and partially covered with a 30-nm-thick gold contact, showing that the gold is in direct contact with the flat conducting channel layer near the surface. In other words, the distance which the carriers have to travel from the top contacts to the channel does not increase significantly when the nominal semiconductor thickness is increased.

The width-normalized contact resistance as a function of the substrate temperature during the C_{10}-DNTT deposition

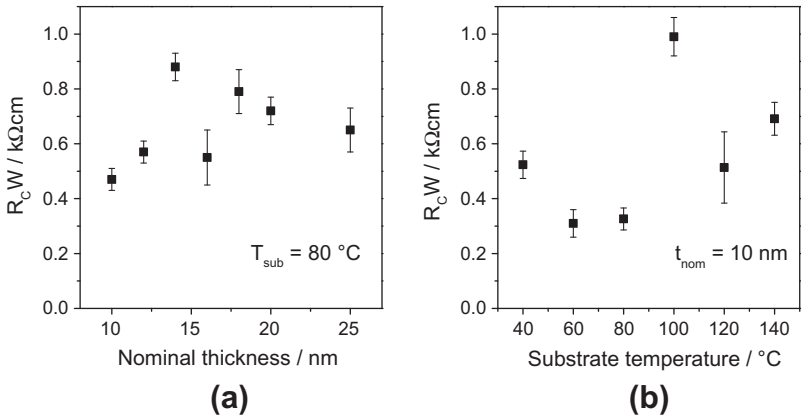

Fig. 9. Contact resistance of vacuum-deposited C_{10}-DNTT TFTs: (a) as a function of the nominal semiconductor thickness and (b) as a function of the substrate temperature during the deposition. In both cases no distinct correlation can be determined.

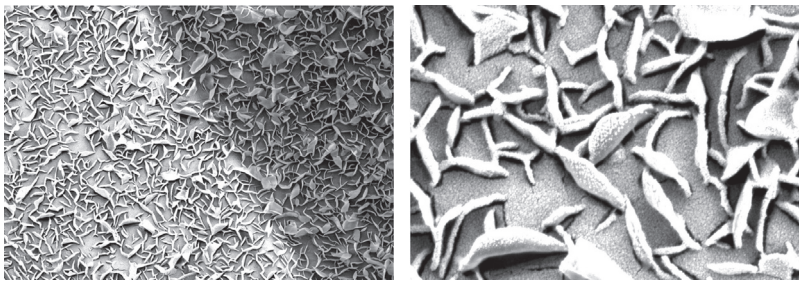

Fig. 10. SEM images of a C_{10}-DNTT layer with a nominal thickness of 22 nm vacuum-deposited at a substrate temperature of 80 °C and partially covered with a 30-nm-thick gold layer. In the left SEM image the gold layer is clearly visible in the lower left corner, while in the right image the entire area is covered with gold. As can be seen, the gold is in direct contact with the flat conducting channel layer near the surface, despite the large density of lamellae. This explains the observation that the contact resistance does not show a systematic increase with the nominal layer thickness.

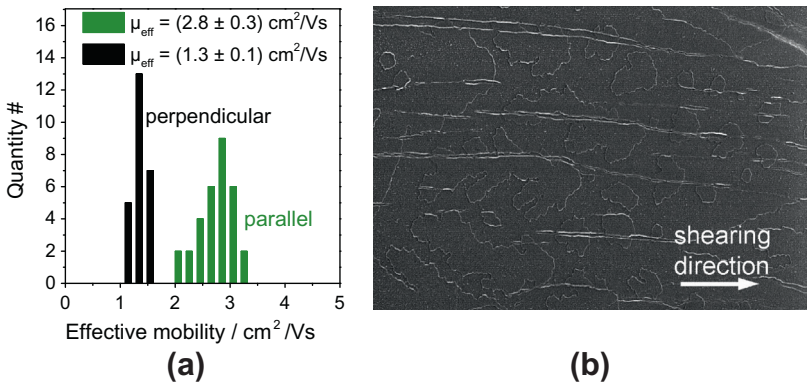

Fig. 11. (a) Distribution of the effective field-effect mobility of C_{10}-DNTT TFTs in which the semiconductor was deposited by solution shearing. The 30 TFTs in which the channel is oriented parallel to the shearing direction are indicated in green and the 25 TFTs in which the channel is oriented perpendicular to the shearing direction are indicated in black. All TFTs have a channel length of 100 μm. (b) SEM image of the relatively flat solution-processed C_{10}-DNTT film. The white arrow indicates the shearing direction. The width of the image corresponds to 10 μm. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

is shown in Fig. 9b. As can be seen, the variation of the contact resistance with the substrate temperature during the deposition is quite small, from 0.33 to 0.99 kΩ cm without any clear tendency. Nonetheless, it is noticeable that the substrate temperature at which the contact resistance has its minimum (60–80 °C) coincides with the substrate temperature for the maximum effective hole mobility as seen in Fig. 4.

The effects of the substrate temperature during the C_{10}-DNTT deposition and of the nominal semiconductor thickness on the intrinsic mobility μ_0 (not shown) are qualitatively similar to those on the effective mobility seen in Figs. 4 and 2b.

4. Transistors with semiconductor deposited by solution shearing

Unlike DNTT, which can only be deposited in vacuum, the alkylated derivative C_{10}-DNTT can also be deposited from solution. For example, Nakayama et al. and Uemura et al. have previously processed C_{10}-DNTT TFTs from solution using a stamp with an inclined surface under which the solvent is allowed to dry slowly and obtained mobilities up to 12 $cm^2/V\,s$ [10,26]. We have used an alternative method in which the semiconductor solution is sheared across the substrate surface using a flat, smooth shearing tool [27]. For this purpose we used the setup recently described by Stolte et al. [28]. The TFTs were fabricated on silicon substrates with a 100-nm-thick layer of thermally grown silicon dioxide as the gate dielectric. The C_{10}-DNTT was dissolved in *o*-dichlorobenzene with a concentration of 4 mg ml^{-1}, and the solution was stirred at 100 °C for better solubility. During the deposition, both the oxidized silicon substrate and the shearing tool were heated to a temperature of 130 °C. After dropping the semiconductor solution onto the substrate, the shearing tool was lowered close to the surface and sheared across the substrate with a speed of 5 mm min^{-1} while being held exactly parallel to the surface.

Difficulties occurred due to the poor solubility of the C_{10}-DNTT, so that not the entire substrate surface was coated homogeneously. To complete the transistors, gold source and drain contacts were deposited onto the semiconductor layer by vacuum deposition through a shadow mask. In an area of approximately 10 mm^2, in which a homogeneous semiconductor layer was obtained, 30 TFTs with the channel oriented parallel to the shearing direction

and 25 TFTs with the channel oriented perpendicular to the shearing direction were characterized. The results are summarized in Fig. 11a. The 30 TFTs with the channel oriented parallel to the shearing direction have an average saturation mobility of (2.8 ± 0.3) cm^2/V s and an on/off ratio of at least 10^7. In contrast, the 25 TFTs with the channel perpendicular to the shearing direction have an average mobility of (1.3 ± 0.1) cm^2/V s and an on/off ratio of at least 10^6. The observed anisotropy of the TFT performance indicates that the shearing induces a preferential grain boundary orientation and/or a spatially anisotropic extension of the grains that favor charge transport along the shearing direction (see SEM image in Fig. 11b). A similar degree of anisotropy in the field-effect mobility depending on the crystallization direction was recently reported for TFTs based on solution-deposited 6,13-bis (triisopropylsilylethynyl) (TIPS) pentacene [29].

5. Conclusion

In summary, we have fabricated organic TFTs based on the high-mobility small-molecule semiconductor C_{10}-DNTT. The effective field-effect mobility of TFTs in which the organic semiconductor layer was prepared by vacuum-deposition is as large as 8.5 cm^2/V s when the nominal semiconductor thickness is 10 nm and the substrate temperature during the semiconductor deposition is 80 °C. Analysis of the semiconductor morphology by scanning electron microscopy reveals the growth of small isolated islands that coalesce into a flat conducting channel layer when the nominal thickness exceeds about 4 nm. This analysis together with X-ray structural data also shows the formation of tall lamellae with a number per unit area that is strongly affected by the substrate temperature during the C_{10}-DNTT vacuum deposition. At very high substrate temperatures (180 °C) the number of lamellae is sufficiently small to allow the morphology of the flat channel layer to be analyzed by atomic force microscopy. The results of this analysis together with the XRD data indicate that the C_{10}-DNTT molecules stand approximately upright with respect to the surface. Using the transmission line method a relatively small contact resistance of 0.33 kΩ cm and an intrinsic hole mobility of 8.5 cm^2/V s were determined.

In addition to TFTs with a vacuum-deposited semiconductor layer we also fabricated C_{10}-DNTT TFTs in which the semiconductor layer was prepared by solution shearing. These TFTs exhibit a clear anisotropy of the in-plane charge transport depending on the orientation of the transistor channel with respect to the shearing direction: TFTs with the channel oriented parallel to the shearing direction have an average mobility of (2.8 ± 0.3) cm^2/V s, while TFTs with the channel oriented perpendicular to the shearing direction showed a somewhat smaller average mobility of (1.3 ± 0.1) cm^2/V s.

Acknowledgments

We thank Marion Hagel at the Max Planck Institute for Solid State Research for expert technical assistance. This work was partially funded by the German Ministry of Education and Research (Project KoSiF, FKZ: 1612000463).

References

[1] G. Gu, P.E. Burrows, S. Venkatesh, S.R. Forrest, M.E. Thompson, Vacuum-deposited, nonpolymeric flexible organic light-emitting devices, Optics Letters 22 (3) (1997) 172–174.
[2] T. Someya, Y. Kato, T. Sekitani, S. Iba, Y. Noguchi, Y. Murase, H. Kawaguchi, T. Sakurai, Conformable, flexible, large-area networks of pressure and thermal sensors with organic transistor active matrixes, Proceedings of the National Academy of Sciences of the United States of America 102 (35) (2005) 12321–12325.
[3] A. Loi, I. Manunza, A. Bonfiglio, Flexible, organic, ion-sensitive field-effect transistor, Applied Physics Letters 86 (10) (2005). 103512-103512.
[4] G. Gelinck, P. Heremans, K. Nomoto, T.D. Anthopoulos, Organic transistors in optical displays and microelectronic applications, Advanced Materials 22 (34) (2010) 3778–3798.
[5] T. Sekitani, T. Yokota, U. Zschieschang, H. Klauk, S. Bauer, K. Takeuchi, M. Takamiya, T. Sakurai, T. Someya, Organic nonvolatile memory transistors for flexible sensor arrays, Science 326 (5959) (2009) 1516–1519.
[6] T. Yamamoto, K. Takimiya, Facile synthesis of highly π-extended heteroarenes, dinaphtho [2,3-b: 2′,3′-f] chalcogenopheno [3,2-b] chalcogenophenes, and their application to field-effect transistors, Journal of the American Chemical Society 129 (8) (2007) 2224–2225.
[7] U. Zschieschang, F. Ante, D. Kälblein, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Someya, J. Blochwitz-Nimoth, H. Klauk, Dinaphtho [2,3-b:2,3-f] thieno [3,2-b] thiophene (DNTT) thin-film transistors with improved performance and stability, Organic Electronics 12 (8) (2011) 1370–1375.
[8] M.J. Kang, H. Mori, E. Miyazaki, K. Takimiya, M. Ikeda, H. Kuwabara, et al., Alkylated dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophenes (C_n-DNTTs): organic semiconductors for high-performance thin-film transistors, Advanced Materials 23 (10) (2010) 1222–1225.
[9] K. Niimi, M.J. Kang, E. Miyazaki, I. Osaka, K. Takimiya, General synthesis of dinaphtho [2,3-b:2,3-f] thieno [3,2-b] thiophene (DNTT) derivatives, Organic Letters 13 (13) (2011) 3430–3433.
[10] T. Uemura, K. Nakayama, Y. Hirose, J. Soeda, M. Uno, W. Li, M. Yamagishi, Y. Okada, J. Takeya, Band-like transport in solution-crystallized organic transistors, Current Applied Physics 12 (3) (2012) 87–91.
[11] W. Ou-Yang, T. Uemura, K. Miyake, S. Onish, T. Kato, M. Katayama, M. Kang, K. Takimiya, M. Ikeda, H. Kuwabara, M. Hamada, J. Takeya, High-performance organic transistors with high-k dielectrics: a comparative study on solution-processed single crystals and vacuum-deposited polycrystalline films of 2,9-didecyl-dinaphtho[2,3-b:2,3-f]thieno[3,2-b]thiophene, Applied Physics Letters 101 (22) (2012). 223304-223304.
[12] U. Zschieschang, M.J. Kang, K. Takimiya, T. Sekitani, T. Someya, T.W. Canzler, A. Werner, J. Blochwitz-Nimoth, H. Klauk, Flexible low-voltage organic thin-film transistors and circuits based on C_{10}-DNTT, Journal of Materials Chemistry 22 (10) (2012) 4273–4277.
[13] U. Zschieschang, R. Hofmockel, R. Rödel, U. Kraft, M.J. Kang, K. Takimiya, T. Zaki, F. Letzkus, J. Butschke, H. Richter, J.N. Burghartz, H. Klauk, Megahertz operation of flexible low-voltage organic thin-film transistors, Organic Electronics 14 (2013) 1516–1520.
[14] G. Horowitz, Organic field-effect transistors, Advanced Materials 10 (5) (1998) 365–377.
[15] Y. Hosoi, D. Tsunami, H. Ishii, Y. Furukawa, Air-stable n-channel organic field-effect transistors based on n,n'-bis (4-trifluoromethylbenzyl) perylene-3,4,9,10-tetracarboxylic diimide, Chemical Physics Letters 436 (1) (2007) 139–143.
[16] R. Schmidt, J.H. Oh, Y.-S. Sun, M. Deppisch, A.-M. Krause, K. Radacki, H. Braunschweig, M. Könemann, P. Erk, Z. Bao, F. Würthner, High-performance air-stable n-channel organic thin film transistors based on halogenated perylene bisimide semiconductors, Journal of the American Chemical Society 131 (17) (2009) 6215.
[17] S.E. Fritz, S.M. Martin, C.D. Frisbie, M.D. Ward, M.F. Toney, Structural characterization of a pentacene monolayer on an amorphous SiO_2 substrate with grazing incidence X-ray diffraction, Journal of the American Chemical Society 126 (13) (2004) 4084–4085.
[18] J. Soeda, T. Uemura, Y. Mizuno, A. Nakao, Y. Nakazawa, A. Facchetti, J. Takeya, High electron mobility in air for n, n-1h, 1h-perfluorobutyldicyanoperylene carboxydi-imide solution-crystallized thin-film transistors on hydrophobic surfaces, Advanced Materials 23 (32) (2011) 3681–3685.

[19] D. Gundlach, L. Zhou, J. Nichols, T. Jackson, P. Necliudov, M. Shur, An experimental study of contact effects in organic thin film transistors, Journal of Applied Physics 100 (2) (2006). 024509-024509.
[20] R. Rödel, F. Letzkus, T. Zaki, J.N. Burghartz, U. Kraft, U. Zschieschang, K. Kern, H. Klauk, Contact properties of high-mobility, air-stable, low-voltage organic n-channel thin-film transistors based on a naphthalene tetracarboxylic diimide, Applied Physics Letters 102 (2013) 233303.
[21] G. Reeves, H. Harrison, Obtaining the specific contact resistance from transmission line model measurements, IEEE, Electron Device Letters 3 (5) (1982) 111–113.
[22] F. Ante, D. Kälblein, U. Zschieschang, T. Canzler, A. Werner, K. Takimiya, M. Ikeda, T. Sekitani, T. Someya, H. Klauk, Contact doping and ultrathin gate dielectrics for nanoscale organic thin-film transistors, Small 7 (9) (2011) 1186–1191.
[23] D. Boudinet, G. Le Blevennec, C. Serbutoviez, J.-M. Verilhac, H. Yan, G. Horowitz, Contact resistance and threshold voltage extraction in n-channel organic thin film transistors on plastic substrates, Journal of Applied Physics 105 (8) (2009). 084510-084510.
[24] F. Ante, D. Kälblein, T. Zaki, U. Zschieschang, K. Takimiya, M. Ikeda, T. Sekitani, T. Someya, J. Burghartz, K. Kern, et al., Contact resistance and megahertz operation of aggressively scaled organic transistors, Small 8 (1) (2012) 73–79.
[25] T.J. Richards, H. Sirringhaus, Analysis of the contact resistance in staggered, top-gate organic field-effect transistors, Journal of Applied Physics 102 (9) (2007). 094510-094510.
[26] K. Nakayama, Y. Hirose, J. Soeda, M. Yoshizumi, T. Uemura, M. Uno, W. Li, M.J. Kang, M. Yamagishi, Y. Okada, et al., Patternable solution-crystallized organic transistors with high charge carrier mobility, Advanced Materials 23 (14) (2011) 1626–1629.
[27] H.A. Becerril, M.E. Roberts, Z. Liu, J. Locklin, Z. Bao, High-performance organic thin-film transistors through solution-sheared deposition of small-molecule organic semiconductors, Advanced Materials 20 (13) (2008) 2588–2594.
[28] M. Stolte, M. Gsänger, R. Hofmockel, S.-L. Suraru, F. Würthner, Improved ambient operation of n-channel organic transistors of solution-sheared naphthalene diimide under bias stress, Physical Chemistry Chemical Physics 14 (41) (2012) 14181–14185.
[29] C.M. Keum, J.H. Bae, M.H. Kim, H.L. Park, M.M. Payne, J.E. Anthony, S.D. Lee, Topography-guided spreading and drying of 6,13-bis(triisopropylsilylethynyl)-pentacene solution on a polymer insulator for the field-effect mobility enhancement, Applied Physics Letters 102 (19) (2013) 193307.