NANO LETTERS

2009
Vol. 9, No. 4
1335-1340

Highly Reliable Carbon Nanotube Transistors with Patterned Gates and Molecular Gate Dielectric

R. Thomas Weitz,*,† Ute Zschieschang,† Alicia Forment-Aliaga,†,§ Daniel Kälblein,† Marko Burghard,† Klaus Kern,†,‡ and Hagen Klauk†

Max Planck Institute for Solid State Research, Heisenbergstrasse 1, D-70569 Stuttgart, Germany, and Institut de Physique des Nanostructures, Ecole Polytechnique Fédérale de Lausanne, CH-1015 Lausanne, Switzerland

Received October 1, 2008; Revised Manuscript Received January 19, 2009

ABSTRACT

The prospect of realizing nanoscale transistors using individual semiconducting carbon nanotubes offers enormous potential, both as an alternative to silicon technology beyond conventional scaling limits and as a way to implement high-speed devices and circuits on flexible substrates. A significant challenge is the realization of low-voltage nanotube transistors with individually addressable gate electrodes that display large transconductance, steep subthreshold swing, and large on/off ratio. Their integration into circuits with large signal gain and good stability still needs to be demonstrated. Here, we demonstrate that these important goals can be achieved with the help of a bottom-gate device structure that combines patterned metal gates with a thin gate dielectric based on a molecular self-assembled monolayer. The obtained transistors operate with a gate-source voltage of 1 V and have a transconductance of 5 μS, a subthreshold swing of 68 mV/decade, and an on/off ratio of 10^7. To verify the excellent operational and shelf life stability, we show that the device performance does not degrade during 10 000 switching cycles and during storage under ambient conditions for more than 300 days. We also demonstrate that the device structure allows the implementation of unipolar logic circuits with good switching characteristics.

Some of the performance parameters of field-effect transistors (FETs) based on individual semiconducting single-walled carbon nanotubes (SWCNT) already rival those of state-of-the-art silicon FETs. For example, SWCNT FETs with a subthreshold swing close to the room-temperature limit of 60 mV/decade,[1−3] transconductance as large as 30 μS,[4−6] and an on/off ratio of 10^7 [refs 1 and 7], have been demonstrated. By utilizing large-capacitance gate dielectrics, SWCNT FETs can be operated with a gate-source voltage of 1 V.[2,3,5,6,8−10] Like silicon FETs, SWCNT transistors with individually addressable (i.e., patterned) gate electrodes can be connected into logic circuits.[11−15]

However, realizing transistors based on individual carbon nanotubes that display large transconductance, steep subthreshold swing and large on/off ratio simultaneously (i.e., in the same device) remains a significant challenge.

Here, we report on the performance and reliability of individual SWCNT field-effect transistors that comprise patterned aluminum gate electrodes functionalized with a self-assembled monolayer (SAM) gate dielectric. Transistors and circuits are manufactured on a silicon wafer covered with 100 nm of thermally grown silicon dioxide. The wafer serves only as a substrate and is not part of the final device (i.e., the silicon is not used as a gate, and the silicon dioxide is not used as a gate dielectric). The wafer is coated with poly(methyl metacrylate) (PMMA) resist, and areas for the local gate electrodes are opened in the resist by electron-beam lithography (see Figure 1a). A 20 nm thick layer of aluminum is deposited by thermal evaporation and then briefly exposed to an oxygen plasma. This creates a 3.6 nm thick layer of aluminum oxide terminated with hydroxyl groups.[16] The substrate is subsequently immersed in a 2-propanol solution containing 5 mM of *n*-octadecylphosphonic acid and then briefly baked on a hotplate at 60 °C so that a 2.1 nm thick molecular SAM is formed on the plasma-oxidized aluminum gate electrodes.[16] The result is a hybrid gate dielectric with a thickness of about 6 nm composed of plasma-grown aluminum oxide and a high-quality SAM (see Figure 1b). During the plasma treatment and SAM formation, the areas outside the aluminum gates remain covered by PMMA, so the hydrophobic SAM is formed only on the gate electrodes, while the rest of the substrate is left hydrophilic. The PMMA mask is then stripped to remove the aluminum outside of the gate areas. HiPCO single-walled carbon

* To whom correspondence should be addressed. E-mail: t.weitz@fkf.mpg.de.
† Max Planck Institute for Solid State Research.
‡ Ecole Polytechnique Fédérale de Lausanne.
§ Present address: Universidad de Valencia, Pol. La Coma s/n, 46980 Paterna, Spain.

10.1021/nl802982m CCC: $40.75
Published on Web 02/26/2009

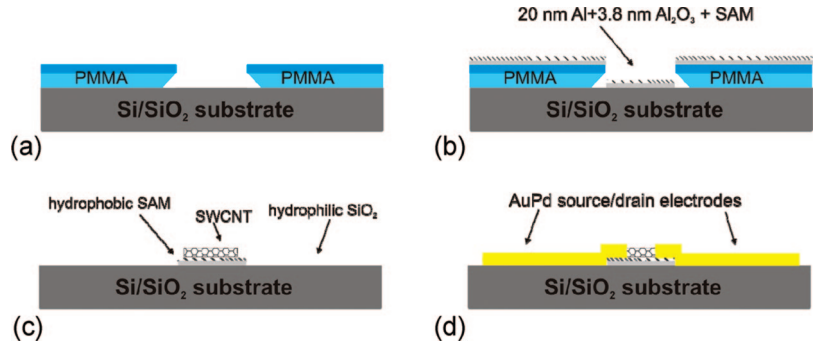

Figure 1. Fabrication process for carbon nanotube FETs with individual metal gate electrodes. (a) A thermally oxidized silicon wafer is coated with a double-layer PMMA resist, and areas for the gate electrodes are opened by electron-beam lithography. (b) A 20 nm thick layer of aluminum is deposited by vacuum evaporation and briefly exposed to an oxygen plasma. An organic monolayer is allowed to self-assemble on the plasma-oxidized aluminum from a solution of *n*-octadecylphosphonic acid. (c) The PMMA resist is stripped and the substrate is immersed in a suspension of HiPCO SWCNTs. (d) Gold/palladium source/drain contacts are created by electron beam lithography, evaporation and lift-off.

nanotubes were obtained from commercial sources and used without sorting of semiconducting and metallic nanotubes. These nanotubes are suspended in deionized water with 1 wt % sodium dodecyl-sulfate as a surfactant by sonication followed by centrifugation in order to remove nanotube bundles. The substrate is then immersed in the suspension which leads to a preferred deposition of carbon nanotubes on the hydrophobic, SAM-covered gate electrodes (see Figure 1c and Supporting Information, Figure S1). Using atomic force microscopy (AFM), individual carbon nanotubes are identified on the patterned gate electrodes. This step is necessary, since the location of the nanotubes on the gate electrodes is essentially random. The substrate is again coated with PMMA resist, areas for the source and drain contacts are opened by electron-beam lithography (so that one individual nanotube is contacted per transistor), and a 20 nm thick layer of gold/palladium is deposited by thermal evaporation. Finally, the PMMA is stripped to remove the metal outside of the contact areas (see Figure 1d). The electrical characteristics of all devices on the substrate are measured to identify those devices that are semiconducting, rather than metallic. All measurements are performed in air at room temperature.

An AFM image of a completed carbon nanotube transistor with a channel length of 100 nm is shown in Figure 2, where the patterned aluminum gate electrode and the overlapping Au/Pd source and drain contacts are visible. Figure 3a shows the output and transfer characteristics of this device. Owing to the large capacitance of the thin gate dielectric (0.7 μF/cm^2, see ref 16), the transistor can be operated with a relatively small gate-source voltage of 1 V. Immediately after fabrication the transistor has a transconductance of 4 μS, a subthreshold swing of 77 mV/decade, an on/off current ratio of 10^7, and a gate leakage current of about 10^{-13} A. To our knowledge, this is the first time that a transconductance greater than 1 μS, a subthreshold swing better than 100 mV/decade, and an on/off ratio greater than 10^5 have been achieved simultaneously for a p-channel SWCNT transistor. Javey et al. reported a transconductance of 20 μS, a subthreshold swing of 70 mV/decade, and an on/off ratio of 10^6 for chemically n-doped SWCNT transistors;[6] Appenzeller et al. and Chen et al. reported subthreshold swings of less than 70 mV/decade and on/off ratios of 10^7 for p-channel SWCNT transistors, but with a transconductance below 1 μS [refs 1 to 7].

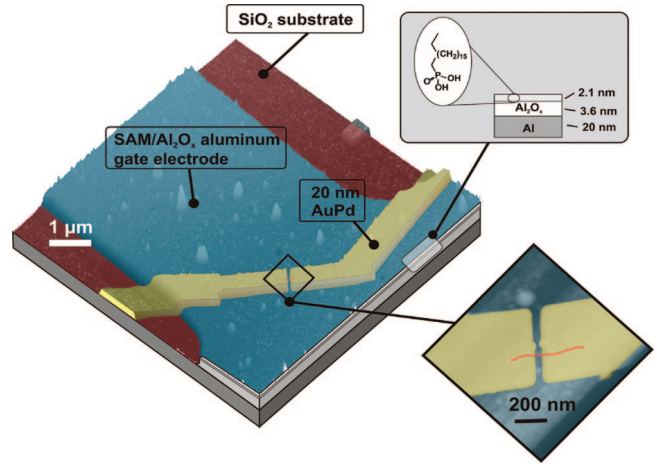

Figure 2. False colored AFM image of a completed carbon nanotube FET. The patterned aluminum gate electrode (blue), the carbon nanotube (red), and the overlapping source and drain AuPd contacts (yellow) are clearly visible. The gate stack is sketched in the top inset. A zoom showing the channel of the FET in greater detail is shown in the bottom inset. The SWCNT has been colored in red to enhance its visibility.

As can be seen in Figure 3a, the threshold voltage of the transistor depends on the drain-source voltage. This phenomenon is due to the systematic lowering of the energy barrier between the source contact and the semiconductor by the drain potential, referred to as drain-induced barrier lowering (DIBL), and is commonly observed in FETs with short channel length. In the case of the SWCNT FET in Figure 3a, the DIBL is $\Delta V_{th}/\Delta V_{DS} = 700$ mV/V, which is similar to previously reported carbon nanotube FETs with similar channel length.[9,13] Theoretical work has shown that DIBL in short-channel SWCNT FETs can be reduced by implementing a double-gate, triple-gate, or surround-gate device structure.[17]

Combining patterned bottom gate electrodes[12] with a thin, SAM-based gate dielectric[16] offers a number of advantages.

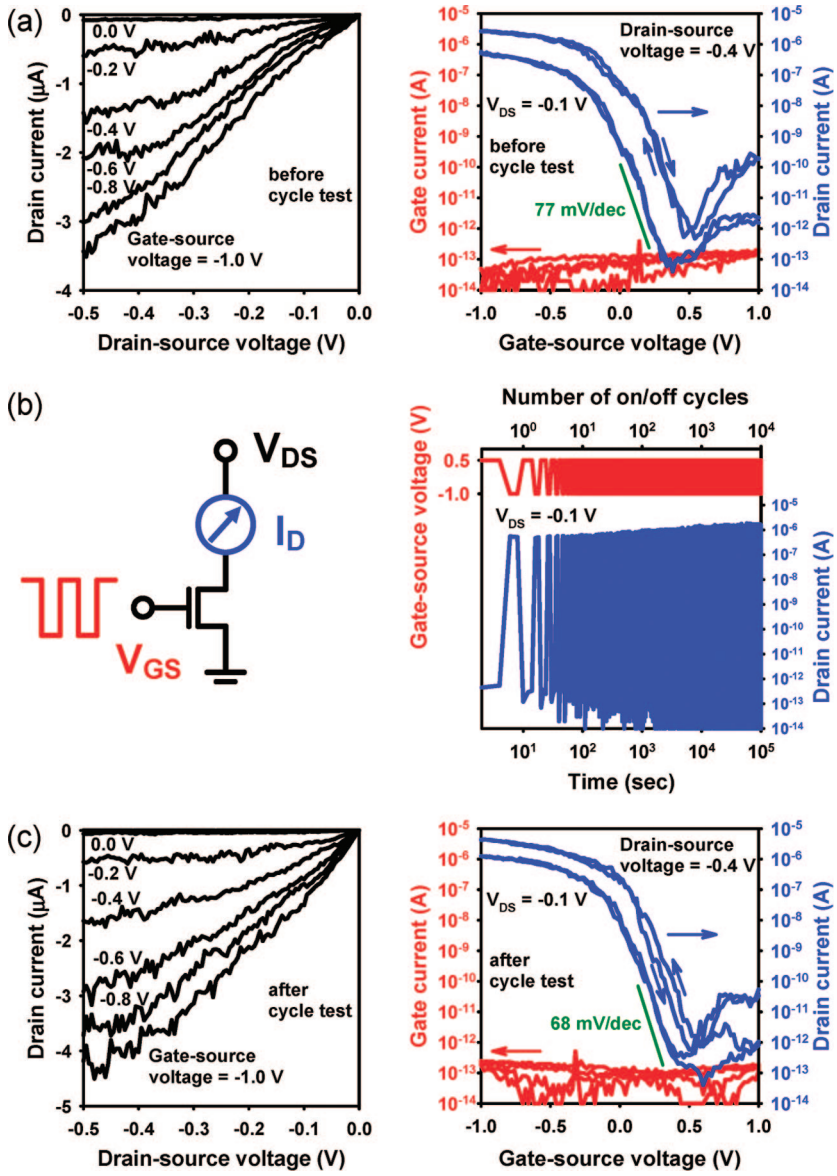

Figure 3. Operational stability of a SWCNT FET with patterned aluminum gate and SAM-based gate dielectric. (a) Electrical characteristics of the FET prior to the cycle test. (b) Recorded drain current while the FET is cycled 10^4 times between on-state ($V_{GS} = -1$ V) and off-state ($V_{GS} = 0.5$ V). (c) Electrical characteristics of the FET after the cycle test.

First, it allows the integration of individually addressable, low-voltage transistors into large-scale integrated circuits on arbitrary substrates, including glass or flexible plastics, which is not possible with a global, unpatterned gate (and hence not possible with a SiO_2 dielectric that is thermally grown on a doped silicon wafer). Second, the surface energy contrast between the hydrophobic SAM-covered gate electrodes and the hydrophilic substrate surface results in a preferred deposition of the nanotubes on the gate electrodes when the substrate is immersed in an aqueous nanotube suspension, thereby enabling the controlled nanotube placement in the desired transistor locations. Several methods for the deposition of carbon nanotubes in hydrophilic areas have been described, which exploit either the dewetting of nanotube-containing droplets from hydrophobic regions[18−20] or the specific adsorption of carbon nanotubes onto amino-functionalized (i.e., hydrophilic) surfaces.[21−23] In contrast, our process takes advantage of the preferred deposition of the (hydrophobic) carbon nanotubes on the (hydrophobic) SAM-covered metal electrodes,[24] which efficiently guides the nanotubes to the transistor locations (see Supporting Information, Figure S1 for an AFM image). The third advantage of combining patterned metal gates with a SAM-based gate dielectric is that the hydrophobic character of the gate dielectric significantly reduces the undesirable hysteresis in the current−voltage characteristics of the transistors, which is related to the presence of water near the nanotube/dielectric interface in the case of hydrophilic gate dielectrics.[3] In addition, the SAM gate dielectric provides for a lower interface state density and thereby improves the subthreshold swing compared with purely inorganic oxide gate dielectrics.[3,12] Finally, the patterned gate electrode is partially overlapped by the source and drain contacts and thus controls the entire carrier channel from source to drain. This eliminates the need for electrostatic or chemical doping of the contact regions required in top-gate transistors with

nonoverlapping contacts,[1,4,6,7] while providing a steeper subthreshold swing and a larger on/off ratio than any top-gated transistors with overlapping contacts reported thus far.[5,11,25]

In view of practical applications of carbon nanotube transistors, the stability of the devices with respect to ambient species (oxygen, water vapor, etc.) needs to be studied. To evaluate the operational stability of our SWCNT transistors, the FETs were cycled 10^4 times between on-state ($V_{GS} = -1$ V) and off-state ($V_{GS} = +0.5$ V). During the cycle tests, the drain-source voltage was held constant ($V_{DS} = -0.1$ V) and the drain current was recorded continuously (see Figure 3b). Over the course of the cycle test, the on-state drain current increased from 0.5 to 1.3 μA (measured at $V_{GS} = -1$ V, $V_{DS} = -0.1$ V) and the transconductance increased from 4 to 5 μS, while the threshold voltage remained unchanged and the slope of the I_D versus V_{DS} curves (output conductance) at small drain-source voltage ($V_{DS} \rightarrow 0$) increased (Figure 3c). These observations suggest that the performance of the source and drain contacts, that is, the efficiency of injecting and extracting carriers at the metal/nanotube interfaces, improved during the cycle test.[26] This may be related to thermal annealing as a result of local Joule heating at the contacts due to the large current densities. In addition, the subthreshold swing improved from 77 to 68 mV/decade during the cycle test, which possibly reflects a reduction in the density of trap states at the nanotube/dielectric interface. A subthreshold swing of 68 mV/decade for a dielectric capacitance of 0.7 μF/cm^2 corresponds to an interface trap state density of 6.2×10^{11} cm^{-2}V^{-1} [ref 3].

Another indicator of the excellent stability of the transistors is the observation that the off-state drain current and the gate leakage current remained essentially constant during the cycle test, both at about 10^{-13}A. The unchanged gate current is indicative of the high quality and excellent reliability of the gate dielectric, despite its small thickness and its preparation at low temperature (60 °C). The observation that the off-state drain current remains small suggests that the nanotube retains its intrinsic electronic properties, that is, the nanotube is apparently not doped during the cycle test, despite the local heating and exposure to air during the cycle test.

After completing the cycle test, the transistors were kept in ambient air at room temperature for one year, during which the current−voltage characteristics were measured occasionally. Figure 4a shows that there is essentially no change in transconductance during that time. The electrical characteristics of the transistor after 327 days are shown in Figure 4b. The transconductance is 6 μS, the subthreshold swing is 75 mV/decade, and the on/off ratio is 10^7.

The excellent stability of the carbon nanotube transistors during the cycle and shelf life tests is owed to the chemical inertness of defect-free carbon nanotubes. This is in contrast to many aromatic oligomers, such as pentacene, that are employed as the semiconductor in high-mobility organic thin-film transistors. Pentacene thin-film transistors (TFTs) show excellent initial performance with carrier mobility around 1 cm^2/Vs, transconductance exceeding 40 μS/mm, subthreshold swing of 100 mV/decade, and on/off ratio of 10^7 or greater.[16]

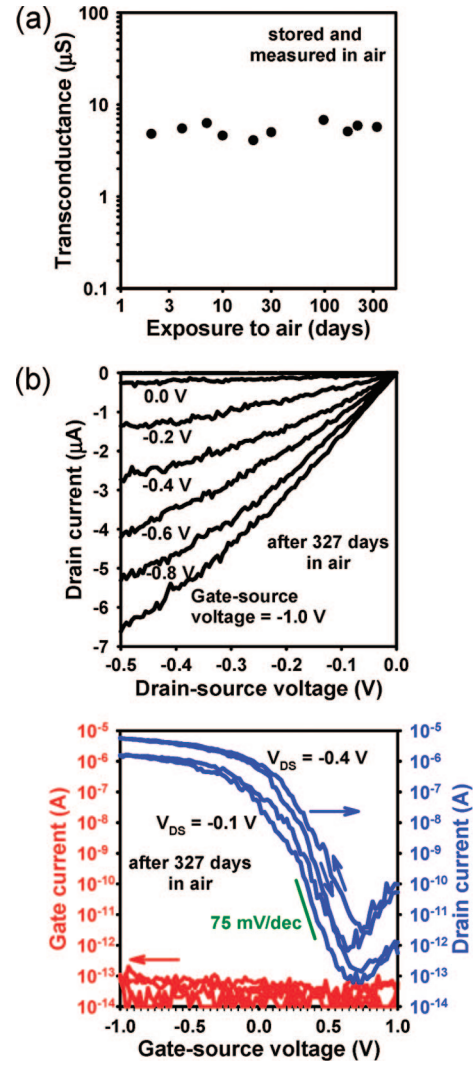

Figure 4. Shelf life stability of the same SWCNT FET. The shelf life test was started after completion of the cycle test; the characteristics of the FET at the beginning of the shelf life test are shown in Figure 2c. (a) Transconductance of the FET during the shelf life test, while the substrate was kept in ambient air at room temperature. (b) Electrical characteristics of the FET after 327 days in air.

But pentacene is readily oxidized in the presence of ambient species, yielding molecules such as 6,13-pentacenequinone, which act as charge traps or scattering sites in the semiconductor.[27] Consequently, the transconductance of pentacene transistors exposed to air decays rapidly and significantly.[28] Carbon nanotubes, in contrast, are much more stable against chemical reactions, due to the lack of −CH═ moieties. In addition, charge transport in carbon nanotubes is expected to be ballistic under the conditions of the cycle test (i.e., channel length about 100 nm, drain-source voltage −0.1 V; see references 29 and 30), which means that interactions between the carriers and the nanotube will be small and effects that might accelerate structural changes of the nanotube, such as Joule heating caused by coupling between carriers and optical phonons, will be greatly suppressed.

The present device structure with patterned metal gate electrodes and a low-temperature gate dielectric allows SWCNT transistors to be integrated into circuits without the

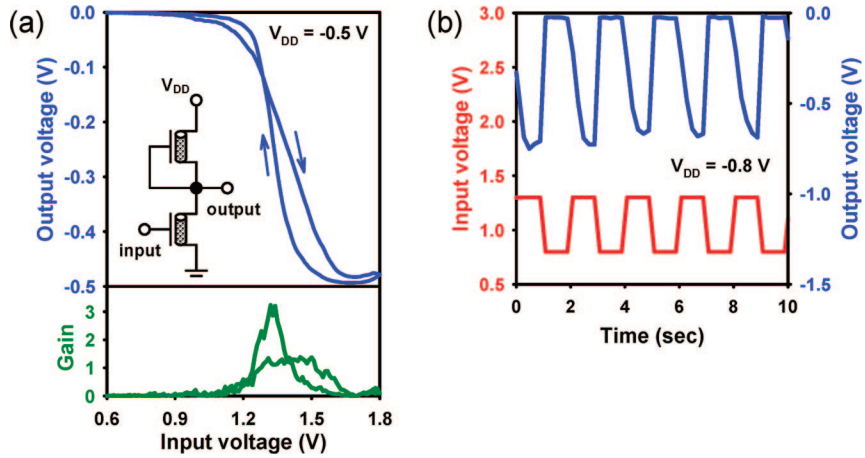

Figure 5. (a) Static and (b) dynamic characteristics of a unipolar inverter-like circuit composed of two SWCNT FETs with patterned metal gates and SAM-based gate dielectric on the same substrate.

use of a global silicon back gate. As a proof-of-concept, we have connected two transistors that were prepared on the same substrate into a logic circuit. One of the transistors serves as the drive transistor (and has its gate connected to the input node of the circuit), the other serves as a load (having its gate connected to the output node). The electrical connections between the transistors were realized by wire bonding, although they could also be realized by lithography and metal deposition. The schematic and the static transfer characteristics of the circuit are shown in Figure 5a. The switching of the output voltage between the two logic states, 0 and −0.5 V, is clearly observed, and the maximum small-signal gain is about 3. Because of the positive threshold voltage of the transistors, the circuit requires positive input voltages, but since the output signal is zero or negative, the input and output voltages do not match and the circuit cannot be used as a true inverter. Implementing inverters with compatible input and output range using only p-channel transistors with positive threshold voltage is possible using a level-shift design,[31] although we have not yet realized this with carbon nanotube FETs. Figure 5b shows the result of a dynamic test of the circuit in which the input voltage was cycled over a range of 0.5 V, causing the output voltage to change over a range of 0.7 V, that is, the large-signal gain is greater than unity. When the drive transistor switches from the conducting to the nonconducting state, the output node is charged through the load transistor. Because the circuit was built on a conducting silicon substrate covered with a 100 nm thick SiO_2 layer, and because the measurement was performed with passive probes, the output node has a capacitance of about 10^{-10} F. The resistance of the load transistor is on the order of 10^9 Ω, yielding a signal delay on the order of 0.1 s. Large-scale integrated circuits with operating frequencies beyond 10^6 Hz will be possible by utilizing low-capacitance substrates, such as glass or plastic.

In summary, we have reported a manufacturing process for low-voltage carbon nanotube transistors with excellent static performance that allow the implementation of integrated circuits on nonconducting substrates. In addition, we have also shown that the carbon nanotube transistors have excellent operational and shelf life stability, showing no degradation after 10 000 switching cycles and more than 300 days in ambient storage.

Acknowledgment. A.F.-A. is grateful to the Conselleria d'Educació de la Generalitat Valenciana for a postdoctoral fellowship. We thank Benjamin Stuhlhofer at the Max Planck Institute for Solid State Research for expert technical assistance.

Supporting Information Available: An atomic force microscopy image of a SiO_2 coated silicon wafer with a patterned, SAM-covered aluminum gate electrode onto which nanotubes have been deposited from suspension. This material is available free of charge via the Internet at http://pubs.acs.org.

References

(1) Appenzeller, J.; Lin, Y. M.; Knoch, J.; Avouris, P. *Phys. Rev. Lett.* **2004**, *93* (19), 196805.
(2) Lu, Y.; Bangsaruntip, S.; Wang, X.; Zhang, L.; Nishi, Y.; Dai, H. *J. Am. Chem. Soc.* **2006**, *128* (11), 3518–3519.
(3) Weitz, R. T.; Zschieschang, U.; Effenberger, F.; Klauk, H.; Burghard, M.; Kern, K. *Nano Lett.* **2007**, *7* (1), 22–27.
(4) Javey, A.; Guo, J.; Farmer, D. B.; Wang, Q.; Wang, D. W.; Gordon, R. G.; Lundstrom, M.; Dai, H. J. *Nano Lett.* **2004**, *4* (3), 447–450.
(5) Javey, A.; Guo, J.; Farmer, D. B.; Wang, Q.; Yenilmez, E.; Gordon, R. G.; Lundstrom, M.; Dai, H. *Nano Lett.* **2004**, *4* (7), 1319–1322.
(6) Javey, A.; Tu, R.; Farmer, D. B.; Guo, J.; Gordon, R. G.; Dai, H. *Nano Lett.* **2005**, *5* (2), 345–348.
(7) Chen, J.; Klinke, C.; Afzali, A.; Avouris, P. *Appl. Phys. Lett.* **2005**, *86* (12), 123108.
(8) Appenzeller, J.; Knoch, J.; Derycke, V.; Martel, R.; Wind, S.; Avouris, P. *Phys. Rev. Lett.* **2002**, *89* (12), 126801.
(9) Klinke, C.; Hannon, J. B.; Afzali, A.; Avouris, P. *Nano Lett.* **2006**, *6* (5), 906–910.
(10) Yang, M. H.; Teo, K. B. K.; Gangloff, L.; Milne, W. I.; Hasko, D. G.; Robert, Y.; Legagneux, P. *Appl. Phys. Lett.* **2006**, *88* (11), 113507.
(11) Chen, Z. H.; Appenzeller, J.; Lin, Y. M.; Sippel-Oakley, J.; Rinzler, A. G.; Tang, J. Y.; Wind, S. J.; Solomon, P. M.; Avouris, P. *Science* **2006**, *311* (5768), 1735–1735.
(12) Bachtold, A.; Hadley, P.; Nakanishi, T.; Dekker, C. *Science* **2001**, *294* (5545), 1317–1320.
(13) Javey, A.; Kim, H.; Brink, M.; Wang, Q.; Ural, A.; Guo, J.; McIntyre, P.; McEuen, P.; Lundstrom, M.; Dai, H. J. *Nat. Mater.* **2002**, *1* (4), 241–246.
(14) Javey, A.; Wang, Q.; Ural, A.; Li, Y. M.; Dai, H. J. *Nano Lett.* **2002**, *2* (9), 929–932.
(15) Hu, Y. F.; Yao, K.; Wang, S.; Zhang, Z. Y.; Liang, X. L.; Chen, Q.; Peng, L. M.; Yao, Y. G.; Zhang, J.; Zhou, W. W.; Li, Y. *Appl. Phys. Lett.* **2007**, *90* (22), 223116.

(16) Klauk, H.; Zschieschang, U.; Pflaum, J.; Halik, M. *Nature* **2007**, *445* (7129), 745–748.
(17) Fiori, G.; Iannaccone, G.; Klimeck, G. *IEEE Trans. Electron Devices* **2006**, *53*, 1782–1788.
(18) Yerushalmi, R.; Ho, J. C.; Jacobson, Z. A.; Javey, A. *Nano Lett.* **2007**, *7*, 2764–2768.
(19) Tsukruk, V. V.; Ko, H.; Peleshanko, S. *Phys. Rev. Lett.* **2004**, *92* (6), 065502.
(20) Bardecker, J. A.; Afzali, A.; Tulevski, G. S.; Graham, T.; Hannon, J. B.; Jen, A. K. Y. *J. Am. Chem. Soc.* **2008**, *130* (23), 7226–7227.
(21) Liu, J.; Casavant, M. J.; Cox, M.; Walters, D. A.; Boul, P.; Lu, W.; Rimberg, A. J.; Smith, K. A.; Colbert, D. T.; Smalley, R. E. *Chem. Phys. Lett.* **1999**, *303* (1−2), 125.
(22) Choi, K. H.; Bourgoin, J. P.; Auvray, S.; Esteve, D.; Duesberg, G. S.; Roth, S.; Burghard, M. *Surf. Sci.* **2000**, *462* (1−3), 195.
(23) Rao, S. G.; Huang, L.; Setyawan, W.; Hong, S. H. *Nature* **2003**, *425* (6953), 36–37.
(24) Burghard, M.; Duesberg, G.; Philipp, G.; Muster, J.; Roth, S. *Adv. Mater.* **1998**, *10* (8), 584–588.
(25) Wind, S. J.; Appenzeller, J.; Martel, R.; Derycke, V.; Avouris, P. *Appl. Phys. Lett.* **2002**, *80* (20), 3817–3819.
(26) Gundlach, D. J.; Jia, L. L.; Jackson, T. N. *IEEE Electron Device Lett.* **2001**, *22* (12), 571–573.
(27) Jurchescu, O. D.; Baas, J.; Palstra, T. T. M. *Appl. Phys. Lett.* **2004**, *84* (16), 3061–3063.
(28) Klauk, H.; Zschieschang, U.; Weitz, R. T.; Meng, H.; Sun, T.; Nunes, G.; Keys, D. E.; Fincher, C. R.; Xiang, Z. *Adv. Mater.* **2007**, *19* (22), 3882–3887.
(29) Yao, Z.; Kane, C. L.; Dekker, C. *Phys. Rev. Lett.* **2000**, *84* (13), 2941–2944.
(30) Javey, A.; Guo, J.; Paulsson, M.; Wang, Q.; Mann, D.; Lundstrom, M.; Dai, H. J. *Phys. Rev. Lett.* **2004**, *92* (10), 106804.
(31) Klauk, H.; Halik, M.; Zschieschang, U.; Eder, F.; Schmid, G.; Dehm, C. *Appl. Phys. Lett.* **2003**, *82* (23), 4175–4177.

NL802982M

Supporting Information for

"Highly reliable carbon nanotube transistors with patterned gates and molecular gate dielectric"

R. Thomas Weitz, Ute Zschieschang, Alicia Forment-Aliaga, Daniel Kälblein,

Marko Burghard, Klaus Kern and Hagen Klauk

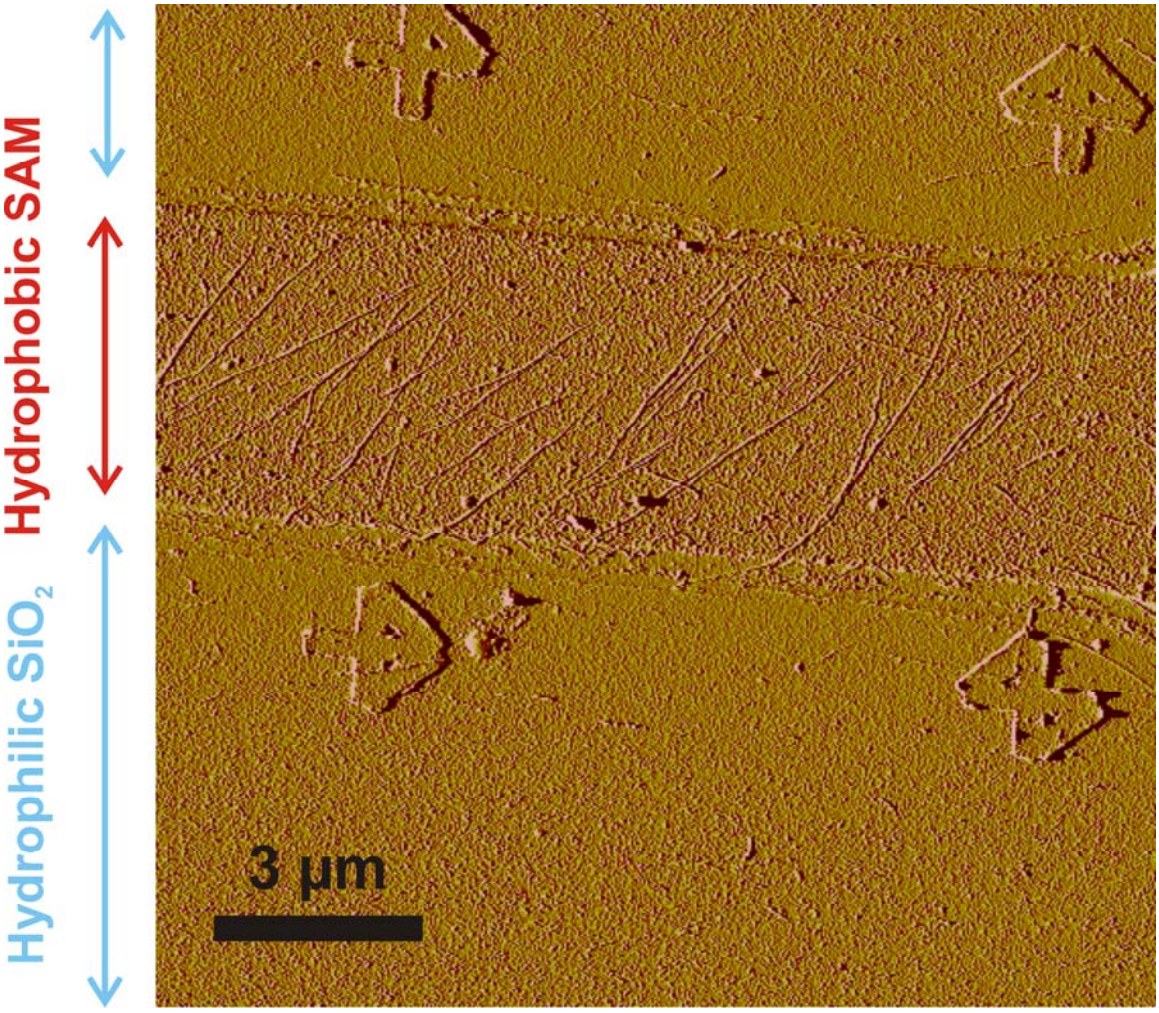

Figure S1: Atomic Force Microscopy (AFM) amplitude image of a silicon dioxide coated silicon wafer (marked in blue) with a patterned aluminum gate electrode (marked in red). The aluminum electrode is covered with a hydrophobic self assembled monolayer (SAM). Single walled carbon nanotubes are deposited by immersing the substrate into an aqueous solution of SWCNTs (sodium dodecyl-sulfate was utilized as surfactant). Subsequently the substrate is taken out of solution, dried under a nitrogen stream and thoroughly rinsed with water. As can be discerned from the image, SWCNTs can be preferably found on the hydrophobic patterned gate electrode.