Low-voltage organic thin-film transistors with large transconductance

Hagen Klauk[a] and Ute Zschieschang
Max Planck Institute for Solid State Research, Heisenbergstrasse 1, 70569 Stuttgart, Germany

Marcus Halik
Institute of Polymer Materials, Friedrich-Alexander University Erlangen-Nürnberg, Martensstrasse 7, 91058 Erlangen, Germany

(Received 6 March 2007; accepted 20 August 2007; published online 12 October 2007)

We have developed an organic thin-film transistor (TFT) technology that aims at providing a good balance of static and dynamic performance parameters. An inverted staggered (bottom-gate, top-contact) device structure with patterned metal gates, a room-temperature-deposited gate dielectric providing a capacitance of 0.7 μF/cm^2, and vacuum-deposited pentacene as the semiconductor were employed. The TFTs have a channel length of 10 μm, a carrier mobility of 0.4 cm^2/V s, an on/off current ratio of 10^7, a subthreshold swing of 100 mV/decade, and a transconductance per channel width of 40 μS/mm. Ring oscillators operate with supply voltages as low as 2 V and with signal propagation delays as low as 200 μs per stage. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2794702]

I. INTRODUCTION

One of the challenges in the development of high-performance organic thin-film transistors (TFTs) is the simultaneous optimization of the various performance parameters while maintaining general manufacturability. A good example is the difficult compromise between carrier mobility, channel length, contact resistance, and cutoff frequency. The highest-mobility organic semiconductors are vacuum-deposited oligomers[1,2] which are known to irreversibly degrade when exposed to process chemicals[3] and, thus, require the use of an inverted (bottom-gate) TFT structure. Manufacturing TFTs with a sufficiently short channel, on the other hand, is usually accomplished by employing wet-chemistry-based high-resolution patterning methods, such as photolithography. This leads directly to the inverted coplanar (bottom-gate, bottom-contact) TFT structure which is usually associated with a significant contact resistance.[4] The contact resistance limits the transconductance (g_m) attainable at a given mobility and channel length, which in turn limits the cutoff frequency (f_T) (Ref. 5),

$$g_m = \frac{\partial I_D}{\partial V_{GS}}, \tag{1}$$

$$f_T = \frac{g_m}{2\pi C_{gate}}. \tag{2}$$

As a result, transconductance and cutoff frequency of organic TFTs often do not scale with channel length as expected, since the simplified equations do not take into account the effect of the contact resistance,[5]

$$\left.\begin{aligned} I_D &= \frac{\mu C_{diel} W}{L}\left[(V_{GS}-V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right], \\ g_m &= \frac{\mu C_{diel} W}{L} V_{DS}, \end{aligned}\right\} \quad \text{for } |V_{GS}-V_{th}| > |V_{DS}| > 0 \tag{3}$$

$$\text{(i.e., in the linear regime)}, \tag{4}$$

$$\left.\begin{aligned} I_D &= \frac{\mu C_{diel} W}{2L}(V_{GS}-V_{th})^2, \\ g_m &= \frac{\mu C_{diel} W}{L}(V_{GS}-V_{th}), \end{aligned}\right\} \quad \text{for } |V_{DS}| > |V_{GS}-V_{th}| > 0 \tag{5}$$

$$\text{(i.e., in the saturation regime)}. \tag{6}$$

Improvements in transconductance and cutoff frequency are possible using chemical contact treatments to reduce the contact resistance associated with the bottom-contact structure,[6] or by employing electron-beam lithography to define channel lengths below 100 nm.[6–10] However, from a manufacturability standpoint (considering throughput and substrate size), electron-beam lithography may be of limited use for high-volume, large-area manufacturing.

Another challenging compromise is that between the

[a]Electronic mail: h.klauk@fkf.mpg.de

 © 2007 American Institute of Physics

Downloaded 19 Oct 2007 to 134.105.227.101. Redistribution subject to AIP license or copyright, see http://jap.aip.org/jap/copyright.jsp

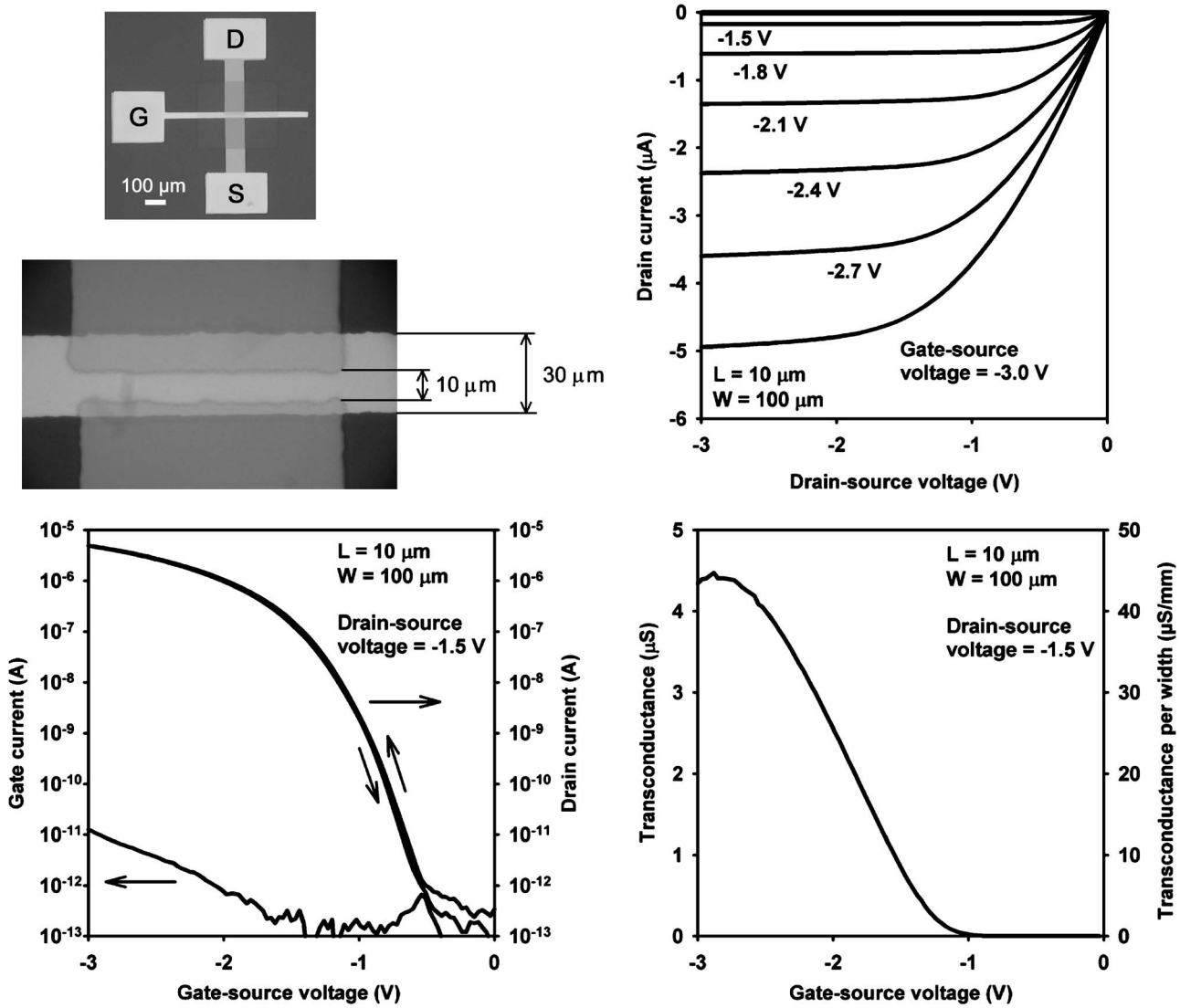

FIG. 1. Characteristics of a pentacene TFT with a channel length of 10 μm and a channel width of 100 μm.

gate dielectric capacitance and the gate leakage current density. To allow organic TFTs to operate with voltages in the range of 2–3 V, the gate capacitance should be in the range of 0.5 μF/cm^2. Given the typical permittivity of organic dielectrics (i.e., $\varepsilon_r \sim 3 \cdots 5$), this means that the gate insulator should be less than 10 nm thick. Despite this small thickness, the gate leakage through the dielectric must be kept to a minimum, but at the same time, it must be possible to deposit and pattern the gate dielectric at substrate temperatures sufficiently low to allow the use of flexible substrates.

Here, we demonstrate an organic TFT process that achieves a useful balance between gate capacitance, operating voltage, gate leakage, carrier mobility, channel length, contact resistance, on/off current ratio, interface trap density, transconductance, cutoff frequency, and manufacturability and provides organic TFTs with good overall static and dynamic performance.

II. DEVICE MANUFACTURING

The TFTs and circuits were manufactured on glass substrates using an inverted staggered (bottom-gate, top-contact) TFT structure.[11] To prepare the gate electrodes, aluminum was deposited through a shadow mask to a thickness of 20 nm. The gate dielectric consists of a thin layer of aluminum oxide (3.6 nm thick, created by oxygen plasma treatment of the aluminum gate electrodes) covered by an organic self-assembled monolayer of *n*-octadecylphosphonic acid (2.1 nm thick, prepared from a 2-propanol solution at room temperature). For the organic semiconductor, a 30 nm thick film of pentacene (purified by temperature-gradient sublimation) was deposited in vacuum. Finally, 30 nm thick gold source/drain contacts were prepared by evaporation. The metal and semiconductor layers were patterned using polymer shadow masks that were manually aligned under an optical microscope. To define vias in the gate dielectric for electrical probing and for interconnects, a simple process that exploits the specific surface selectivity of the self-assembling organic molecules during the solution-based adsorption process was employed.[11] The maximum temperature during the device manufacturing process was 60 °C (the substrate temperature during the pentacene deposition). All electrical mea-

Downloaded 19 Oct 2007 to 134.105.227.101. Redistribution subject to AIP license or copyright, see http://jap.aip.org/jap/copyright.jsp

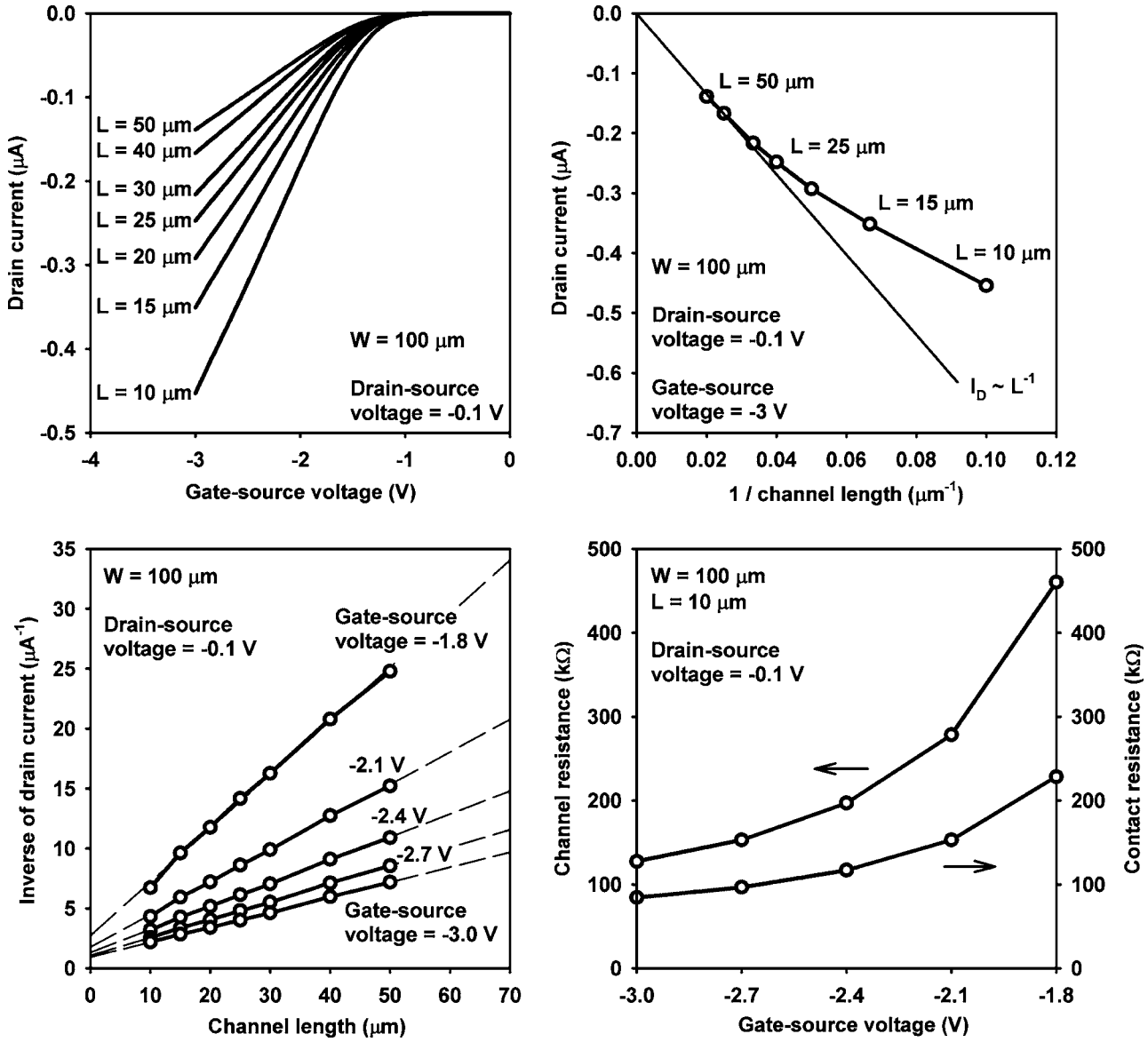

FIG. 2. Contact resistance analysis for a series of pentacene TFTs with a channel width of 100 μm.

surements were carried out at room temperature in ambient air under yellow light.

III. CURRENT-VOLTAGE CHARACTERISTICS

Two photographs and the electrical characteristics of a TFT with a channel length (L) of 10 μm and a channel width (W) of 100 μm are shown in Fig. 1. The gate dielectric has a total thickness of 5.7 nm (measured by small-angle x-ray reflectivity) and provides a gate capacitance (C_{diel}) of 0.7 μF/cm^2 (measured by impedance spectroscopy and indicating an effective permittivity of 4.5). The current density through the gate dielectric, measured in metal/dielectric/metal capacitors manufactured on the same substrate, is less than 5×10^{-6} A/cm^2 at an applied voltage of 3 V. The maximum gate and drain currents are 15 pA and 5 μA, respectively, both at a gate-source voltage of −3 V. The off-state drain current at a gate-source voltage of 0 V is about 0.5 pA, and the on/off current ratio is about 10^7. The transconductance according to Eq. (1) has a maximum around 4 μS (40 μS per millimeter channel width). The carrier mobility (μ) extracted from the $\sqrt{I_D}$ versus V_{GS} data in the saturation regime ($V_{DS}=-1.5$ V, $V_{GS}\sim-2.0\cdots-2.5$ V) is 0.4 cm^2/V s.

The TFT has a threshold voltage (V_{th}) of −1.2 V, so at a gate-source voltage of −3 V, the overdrive voltage ($V_{GS}-V_{th}$) is −1.8 V. At this gate-source voltage, the induced channel charge density $[C_{diel}\times(V_{GS}-V_{th})/q]$ is 8×10^{12} cm^{-2}. For comparison, a TFT with a 100 nm thick SiO_2 gate dielectric ($C_{diel}=0.035$ μF/cm^2) requires an overdrive voltage of 36 V to obtain the same charge density in the carrier channel.

For gate-source voltages between the threshold voltage ($V_{th}=-1.2$ V) and the switch-on voltage ($V_{so}\sim-0.5$ V) (Ref. 12), the drain current depends exponentially on the gate-source voltage,[5]

$$I_D = I_0 \exp\left(\frac{q|V_{GS}-V_{th}|}{nkT}\right). \tag{7}$$

From the slope of the $\log(I_D)$ versus V_{GS} curve in the subthreshold region—or from its inverse, the subthreshold

Downloaded 19 Oct 2007 to 134.105.227.101. Redistribution subject to AIP license or copyright, see http://jap.aip.org/jap/copyright.jsp

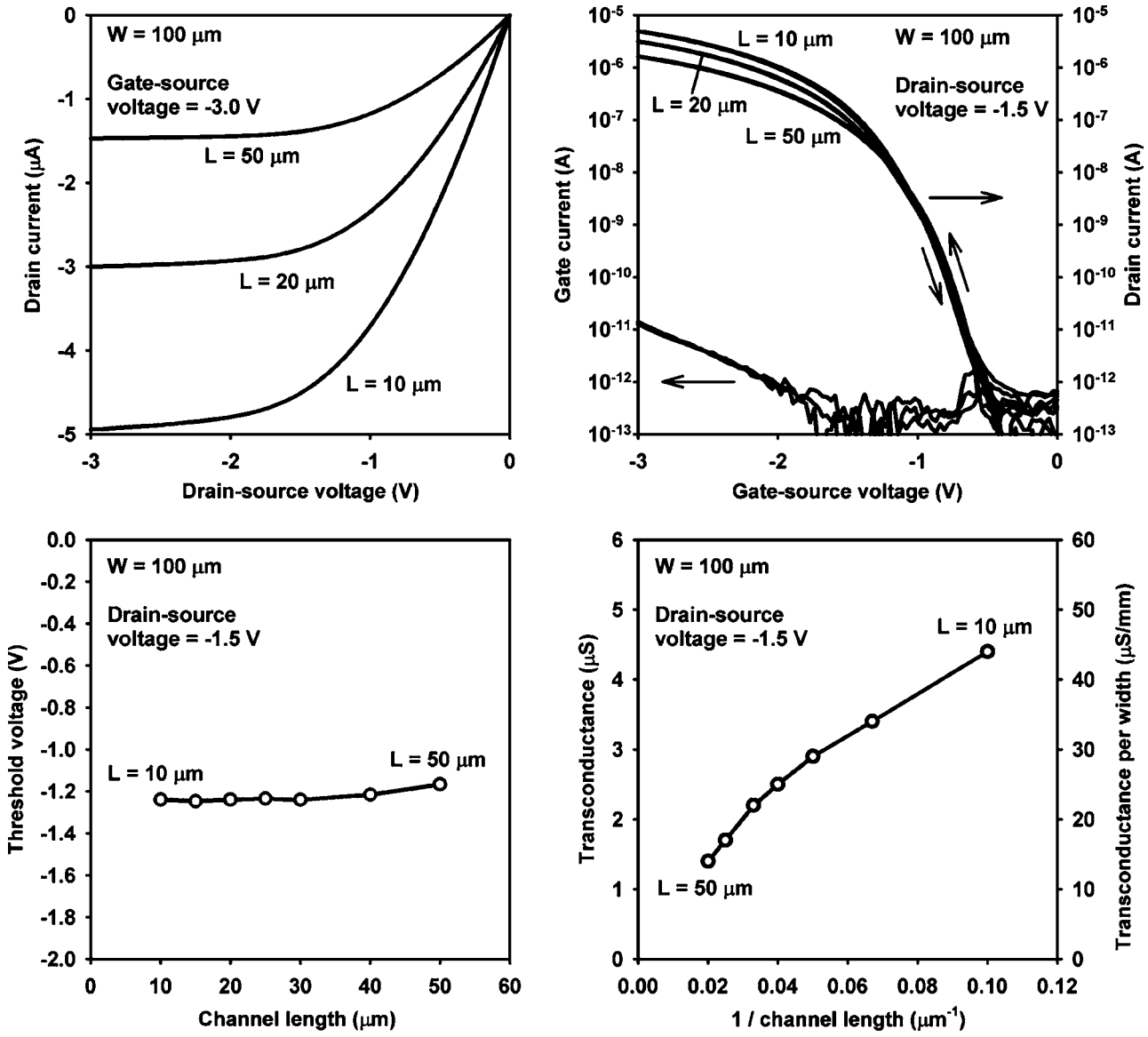

FIG. 3. Channel length scaling behavior of top-contact pentacene TFTs.

swing (S)—the density of trap states at the semiconductor/dielectric interface (N_{it}) can be calculated,[5]

$$S = \frac{\partial V_{GS}}{\partial(\log_{10} I_D)} = \frac{kT}{q} \ln 10\left(1 + \frac{qN_{it}}{C_{diel}}\right). \quad (8)$$

The TFT in Fig. 1 has a subthreshold swing of 100 mV/decade, from which an interface trap density of 3×10^{12} cm^{-2} V^{-1} is calculated. Although this is several orders of magnitude higher than the interface trap density of high-quality silicon[5] or carbon nanotube[13] field-effect transistors, it is similar to the best values reported for organic TFTs.[14–16]

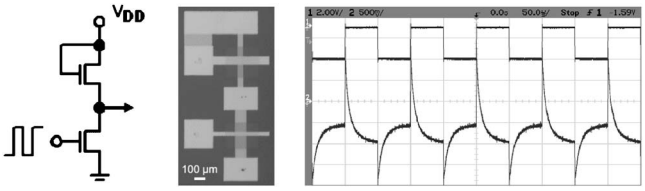

FIG. 4. Dynamic response of a pentacene inverter with saturated load to a 10 kHz square-wave input signal. The drive TFT has a channel length of 10 μm and a channel width of 100 μm, the load TFT has a channel length and width of 50 μm.

IV. CONTACT RESISTANCE

An important advantage of the top-contact TFT structure compared with the bottom-contact TFT structure is the smaller contact resistance, which is mainly due to the larger area available for charge injection from the metal into the carrier channel.[4] In order to estimate the contact resistance of the technology presented here, we have characterized TFTs with a channel width of 100 μm and with channel length ranging from 10 to 50 μm.

The results are summarized in Fig. 2. As can be seen, the maximum drain current scales with channel length approximately as predicted by Eq. (3) for channel lengths between 50 and about 25 μm. Below about 20 μm, the effect of the

Downloaded 19 Oct 2007 to 134.105.227.101. Redistribution subject to AIP license or copyright, see http://jap.aip.org/jap/copyright.jsp

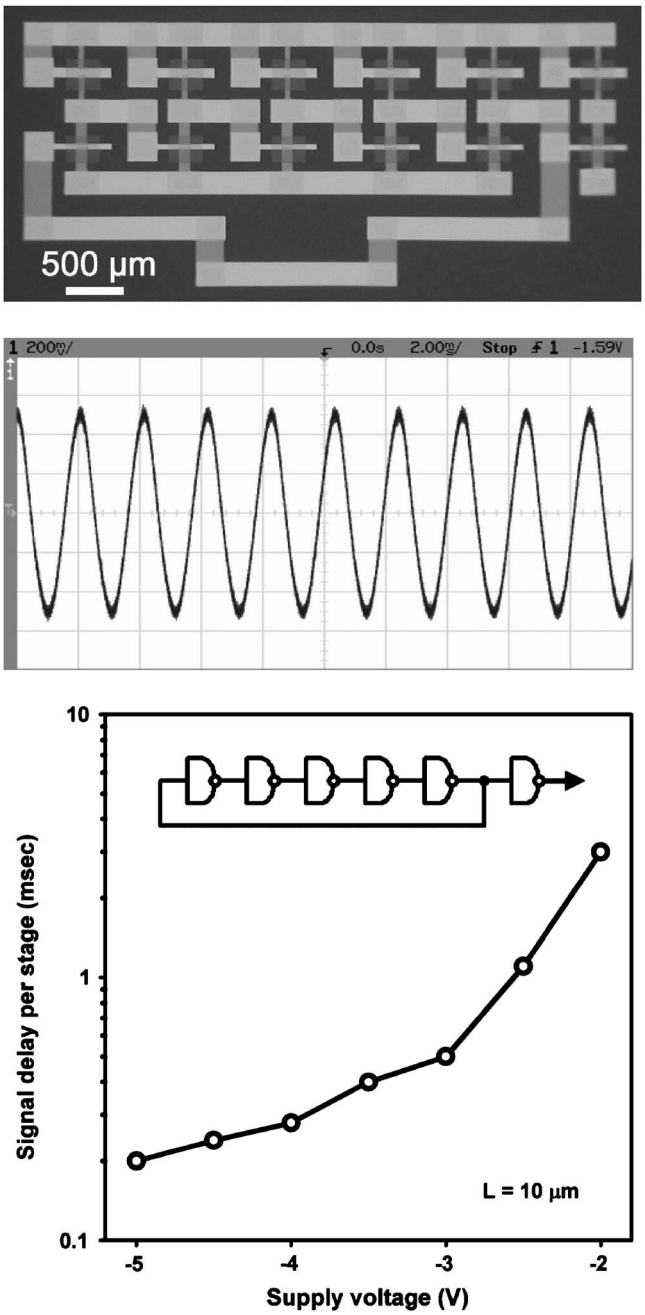

FIG. 5. Characteristics of a pentacene five-stage ring oscillator. The drive TFTs have a channel length of 10 μm and a channel width of 100 μm, the load TFTs have a channel length and width of 50 μm.

contact resistance on the drain current becomes evident, as the increase in drain current with decreasing channel length becomes smaller than expected.

In order to calculate the contact resistance, the inverse of the drain current is plotted as a function of channel length, extrapolated to a channel length of zero (where the channel resistance disappears) and multiplied by the drain-source voltage.[17] For a gate-source voltage of −3 V and a drain-source voltage of −0.1 V (linear regime), this yields a contact resistance of 85 kΩ. Assuming that the contact resistance is inversely proportional to the channel width, this corresponds to a contact resistance multiplied by the channel width of 850 Ω cm in the linear regime.

To calculate the channel resistance per channel length, the slope of the inverse of drain current versus channel length curve is multiplied by the drain-source voltage.[17] For a drain-source voltage of −0.1 V, a gate-source voltage of −3 V, and a channel length of 10 μm, this yields a channel resistance of 130 kΩ or 1.3 kΩ cm in the linear regime.

For comparison, in the saturation regime (gate-source voltage of −3.0 V, drain-source voltage of −3.0 V), we have found a contact resistance of 1.2 kΩ cm and a channel resistance per 10 μm channel length of 1.8 kΩ cm. Thus, both the contact resistance and the channel resistance are about 40% larger when the TFT is operated in the saturation regime, compared with the linear regime.

As the channel length is reduced, the channel resistance decreases, but since the contact resistance is independent of channel length, there is a certain channel length below which the channel resistance is smaller than the contact resistance. In this case, the drain current is no longer limited by the channel, but rather by the contacts. In bottom-contact TFTs with large contact resistance, this crossover between channel-limited and contact-limited behavior can occur for channel lengths greater than 30 μm (Ref. 4). In contrast, our top-contact TFTs are channel limited down to the smallest channel length of 10 μm (linear regime: contact resistance of 850 Ω cm, channel resistance of 1.3 kΩ cm; saturation regime: contact resistance of 1.2 kΩ cm, channel resistance of 1.8 kΩ cm). The crossover from channel-limited to contact-limited transport is projected to a channel length between 6 and 7 μm.

V. CHANNEL LENGTH SCALING

As the channel length is reduced, certain short-channel effects may appear, including less pronounced saturation of the drain current, threshold voltage roll-off (in the case of *p*-channel TFTs, this means the threshold voltage becomes more positive as the channel length is reduced), and a less rapid increase in transconductance with decreasing channel length.[5]

As can be seen in Fig. 3, the saturation of the drain current is indeed less pronounced as the channel length is reduced from 50 to 10 μm. For a channel length of 50 μm, the differential output conductance ($\delta I_D / \delta V_{DS}$ at $V_{GS} = -3$ V and for $V_{DS} \rightarrow -3$ V) is 20 nS; for a channel length of 20 μm, the differential output conductance is 50 nS; and for a channel length of 10 μm, the differential output conductance is 100 nS. This increase in differential output conductance with decreasing channel length illustrates the less pronounced saturation.

On the other hand, the threshold voltage is essentially the same for all channel lengths between 50 and 10 μm, i.e., the threshold voltage roll-off is not observed for this technology and for this range of channel lengths.

Finally, the transconductance scales as predicted by Eq. (6) only for channel lengths between 50 and about 25 μm. For channel lengths below about 20 μm, the transconductance still increases with decreasing channel length, but the increase is somewhat smaller than expected.

Downloaded 19 Oct 2007 to 134.105.227.101. Redistribution subject to AIP license or copyright, see http://jap.aip.org/jap/copyright.jsp

TABLE I. Summary of the main TFT parameters.

Semiconductor layer	Vacuum-deposited pentacene
Gate dielectric capacitance per area	0.7 μF/cm^2
Operating voltage	3 V
Carrier mobility	0.4 cm^2/V s
Channel length	10 μm
Gate-to-contact overlap	10 μm
Maximum gate current per channel width	150 pA/mm
Maximum drain current per channel width	50 μA/mm
Minimum drain current per channel width	5 pA/mm
On/off current ratio	10^7
Subthreshold swing	100 mV/decade
Contact resistance×channel width	850 Ω cm
Transconductance per channel width	40 μS/mm
Cutoff frequency (estimated)	40 kHz
Maximum operating frequency (measured)	10 kHz (inverter); 5 kHz (ring oscillator)

VI. DYNAMIC PERFORMANCE

An important limitation of the top-contact organic TFT structure is that it does not permit the use of high-resolution wet-chemistry patterning methods for the definition of the source/drain contacts, since this would irreversibly degrade the organic semiconductor layer.[3] To pattern metal contacts on top of the pentacene film, we have employed a simple shadow-mask process that allows the definition of a channel length of 10 μm and a gate-to-contact overlap (ΔL) of 10 μm (see Fig. 1). Thus, the lateral dimensions critical in determining the cutoff frequency of the transistors are a factor of about 5 larger compared with photolithographically patterned bottom-contact devices.[18]

The TFT shown in Fig. 1 has a transconductance of 4 μS and a total gate capacitance of about 15 pF [$C_{\text{gate}} \sim C_{\text{diel}} \times (L+\Delta L) \times W$]. According to Eq. (2), a cutoff frequency of approximately 40 kHz would be expected. Figure 4 shows the dynamic response of a pentacene inverter with a saturated load to a square-wave input signal with a frequency of 10 kHz. The drive TFT has a channel length of 10 μm and a channel width of 100 μm, the load TFT has a channel length and width of 50 μm. The highest input frequency for which a useful output signal is obtained is about 10 kHz, which is within a factor of 4 of the estimated cutoff frequency.

We have also prepared five-stage ring oscillators with integrated output buffer based on inverters with saturated load (see Fig. 5). The measured signal propagation delay is 500 μs per stage at a supply voltage of −3 V and 200 μs per stage at a supply voltage of −5 V. Although this is a factor of 8–20 slower than the estimated cutoff frequency, it is to our knowledge the smallest signal delay reported for an organic circuit operating with a supply voltage of 5 V or less.

VII. CONCLUSIONS

We have presented an organic TFT technology that provides a good balance of static and dynamic device characteristics. The main transistor parameters are summarized in Table I. Owing to the use of a gate dielectric that provides a large capacitance (0.7 μF/cm^2), a small leakage current density ($\sim 10^{-6}$ A/cm^2), and a low interface trap density (3×10^{12} cm^{-2} V^{-1}) the transistors and circuits can be operated with relatively low voltages of about 3 V. By combining a vacuum-deposited small-molecule semiconductor with good carrier mobility (0.4 cm^2/V s), a top-contact device structure with small contact resistance (850 Ω cm), and a relatively simple manufacturing process capable of defining critical dimensions of 10 μm, we have obtained TFTs with a transconductance per channel width of 40 μS/mm and an estimated cutoff frequency of 40 kHz. We have also designed and manufactured digital organic circuits that employ a saturated-load design and operate with supply voltages in the range of 2–5 V and with signal propagation delays as low as 100 μs per stage for individual inverters and as low as 200 μs per stage for ring oscillators.

Many previous publications have reported organic circuits that operate at frequencies higher than those presented here,[19–29] with propagation delays as low as about 1 μs per stage.[22,23,27–29] However, these circuits operate with significantly larger voltages, typically between 20 and 100 V. For certain applications, such as small portable devices, organic TFTs and circuits with supply voltages in the range of 2–3 V may be desirable. In general, circuits operated at lower voltages have lower circuit speed, unless the lateral transistor dimensions are also reduced. (This is because g_m is proportional to the voltage, while the effects of C_{diel} on g_m and C_{gate} cancel each other, so that f_T is proportional to the voltage, but independent of C_{diel}.) Strategies for increasing the circuit speed without increasing the operating voltage include improvements in carrier mobility, more aggressive scaling of the critical lateral dimensions (L and ΔL), and ideally the use of a complementary circuit design employing p-channel and n-channel organic TFTs with large, balanced carrier mobilities.[30]

ACKNOWLEDGMENTS

The authors thank Benjamin Stuhlhofer at the Max Planck Institute for Solid State Research for expert technical assistance and Richard Rook at CADiLAC Laser for providing high-quality shadow masks. One of the authors (M.H.) acknowledges financial support by the Deutsche Forschungsgemeinschaft.

Downloaded 19 Oct 2007 to 134.105.227.101. Redistribution subject to AIP license or copyright, see http://jap.aip.org/jap/copyright.jsp

[1]T. W. Kelley, L. D. Boardman, T. D. Dunbar, D. V. Muyres, M. J. Pellerite, and T. P. Smith, J. Phys. Chem. B **107**, 5877 (2003).
[2]S. Lee, B. Koo, J. Shin, E. Lee, H. Park, and H. Kim, Appl. Phys. Lett. **88**, 162109 (2006).
[3]D. J. Gundlach, T. N. Jackson, D. G. Schlom, and S. F. Nelson, Appl. Phys. Lett. **74**, 3302 (1999).
[4]D. J. Gundlach, L. Zhou, J. A. Nichols, T. N. Jackson, P. V. Necliudov, and M. S. Shur, J. Appl. Phys. **100**, 024509 (2006).
[5]K. K. Ng, *Complete Guide to Semiconductor Devices*, 2nd ed. (Wiley, New York, 2002).
[6]G. S. Tulevski, Q. Miao, A. Afzali, T. O. Graham, C. R. Kagan, and C. Nuckolls, J. Am. Chem. Soc. **128**, 1788 (2006).
[7]J. Collet, O. Tharaud, A. Chapoton, and D. Vuillaume, Appl. Phys. Lett. **76**, 1941 (2000).
[8]Y. Zhang, J. R. Petta, S. Ambily, Y. Shen, D. C. Ralph, and G. G. Malliaras, Adv. Mater. (Weinheim, Ger.) **15**, 1632 (2003).
[9]L. Wang, D. Fine, T. Jung, D. Basu, H. von Seggern, and A. Dodabalapur, Appl. Phys. Lett. **85**, 1772 (2004).
[10]J. Lee, P. C. Chang, J. A. Liddle, and V. Subramanian, IEEE Trans. Electron Devices **52**, 1874 (2005).
[11]H. Klauk, U. Zschieschang, J. Pflaum, and M. Halik, Nature (London) **445**, 745 (2007).
[12]E. J. Meijer, C. Tanase, P. W. M. Blom, E. van Veenendaal, B. H. Huisman, D. M. de Leeuw, and T. M. Klapwijk, Appl. Phys. Lett. **80**, 3838 (2002).
[13]R. T. Weitz, U. Zschieschang, F. Effenberger, H. Klauk, M. Burghard, and K. Kern, Nano Lett. **7**, 22 (2007).
[14]L. A. Majewski, R. Schroeder, and M. Grell, Adv. Mater. (Weinheim, Ger.) **17**, 192 (2005).
[15]M. McDowell, I. G. Hill, J. E. McDermott, S. L. Bernasek, and J. Schwartz, Appl. Phys. Lett. **88**, 073505 (2006).
[16]H. W. Zan, K. H. Yen, P. K. Liu, K. H. Ku, C. H. Chen, and J. Hwang, Org. Electron. **8**, 450 (2007).
[17]H. Klauk, G. Schmid, W. Radlik, W. Weber, L. Zhou, C. D. Sheraw, J. A. Nichols, and T. N. Jackson, Solid-State Electron. **47**, 297 (2003).
[18]G. H. Gelinck, G. H. Gelinck, H. E. A. Huitema, E. van Veenendaal, E. Cantatore, L. Schrijnemakers, J. B. P. H. van der Putten, T. C. T. Geuns, M. Beenhakkers, J. B. Giesbers, B. H. Huisman, E. J. Meijer, E. M. Benito, F. J. Touwslager, A. W. Marsman, B. J. E. van Rens, and D. M. de Leeuw, Nat. Mater. **3**, 106 (2004).
[19]G. H. Gelinck, T. C. T. Geuns, and D. M. de Leeuw, Appl. Phys. Lett. **77**, 1487 (2000).
[20]M. G. Kane, J. Campi, M. S. Hammond, F. P. Cuomo, B. Greening, C. D. Sheraw, J. A. Nichols, D. J. Gundlach, J. R. Huang, C. C. Kuo, L. Jia, H. Klauk, and T. N. Jackson, IEEE Electron Device Lett. **21**, 534 (2000).
[21]B. K. Crone, A. Dodabalapur, R. Sarpeshkar, R. W. Filas, Y. Y. Lin, Z. Bao, J. H. O'Neill, W. Li, and H. E. Katz, J. Appl. Phys. **89**, 5125 (2001).
[22]W. Fix, A. Ullmann, J. Ficker, and W. Clemens, Appl. Phys. Lett. **81**, 1735 (2002).
[23]P. Baude, D. A. Ender, M. A. Haase, T. W. Kelley, D. V. Muyres, and S. D. Theiss, Appl. Phys. Lett. **82**, 3964 (2003).
[24]T. D. Anthopoulos, D. M. de Leeuw, E. Cantatore, P. van 't Hof, J. Alma, and J. C. Hummelen, J. Appl. Phys. **98**, 054503 (2005).
[25]H. Klauk, M. Halik, U. Zschieschang, F. Eder, D. Rohde, G. Schmid, and C. Dehm, IEEE Trans. Electron Devices **52**, 618 (2005).
[26]S. H. Han, S. M. Cho, J. H. Kim, J. W. Choi, J. Jang, and M. H. Oh, Appl. Phys. Lett. **89**, 093504 (2006).
[27]T. D. Anthopoulos, B. Singh, N. Marjanovic, N. S. Sariciftci, A. Montaigne Ramil, H. Sitter, M. Cölle, and D. M. de Leeuw, Appl. Phys. Lett. **89**, 213504 (2006).
[28]C. Rolin, S. Steudel, K. Myny, D. Cheyns, S. Verlaak, J. Genoe, and P. Heremans, Appl. Phys. Lett. **89**, 203502 (2006).
[29]B. Yoo, T. Jung, D. Basu, A. Dodabalapur, B. A. Jones, A. Facchetti, M. R. Wasielewski, and T. J. Marks, Appl. Phys. Lett. **88**, 082104 (2006).
[30]M. Kitamura and Y. Arakawa, Appl. Phys. Lett. **91**, 053505 (2007).

Downloaded 19 Oct 2007 to 134.105.227.101. Redistribution subject to AIP license or copyright, see http://jap.aip.org/jap/copyright.jsp