S. Guiriec,[35] Y. Hanabata,[36] A.K. Harding,[21] M. Hayashida,[3] E. Hays,[21] A. B. Hill,[28] L. Hjalmarsdotter,[4,5] D. Horan,[17] R. E. Hughes,[12] M. S. Jackson,[5,37] G. Jóhannesson,[3] A. S. Johnson,[3] T. J. Johnson,[21,33] W. N. Johnson,[1] T. Kamae,[3] H. Katagiri,[36] N. Kawai,[38,39] M. Kerr,[18] J. Knödlseder,[42] M. L. Kocian,[3] E. Koerding,[7] M. Kuss,[6] J. Lande,[3] L. Latronico,[6] M. Lemoine-Goumard,[29,30] F. Longo,[8,9] F. Loparco,[15,16] B. Lott,[29,30] M. N. Lovellette,[1] P. Lubrano,[13,14] G. M. Madejski,[3] A. Makeev,[1,41] L. Marchand,[42] M. Marelli,[20] W. Max-Moerbeck,[43] M. N. Mazziotta,[16] N. McColl,[42] J. E. McEnery,[21,33] C. Meurer,[26,5] P. F. Michelson,[3] S. Migliari,[44] W. Mitthumsiri,[3] T. Mizuno,[36] C. Monte,[15,16] M. E. Monzani,[3] A. Morselli,[45] I. V. Moskalenko,[3] S. Murgia,[3] P. L. Nolan,[3] J. P. Norris,[46] E. Nuss,[24] T. Ohsugi,[36] N. Omodei,[6] R. A. Ong,[42] J. F. Ormes,[46] D. Paneque,[3] D. Parent,[29,30] V. Pelassa,[24] M. Pepe,[13,14] M. Pesce-Rollins,[6] F. Piron,[24] G. Pooley,[47] T. A. Porter,[48] K. Pottschmidt,[21] S. Rainò,[15,16] R. Rando,[10,11] P. S. Ray,[1] M. Razzano,[6] N. Rea,[19,49] A. Readhead,[43] A. Reimer,[50,3] O. Reimer,[50,3] J. L. Richards,[43] L. S. Rochester,[3] J. Rodriguez,[7] A. Y. Rodriguez,[19] R. W. Romani,[3] F. Ryde,[37,5] H. F.-W. Sadrozinski,[48] A. Sander,[12] P. M. Saz Parkinson,[48] C. Sgrò,[6] E. J. Siskind,[51] D. A. Smith,[29,30] P. D. Smith,[12] P. Spinelli,[15,16] J.-L. Starck,[7] M. Stevenson,[43] M. S. Strickman,[1] D. J. Suson,[52] H. Takahashi,[36,11] T. Tanaka,[3] J. B. Thayer,[3] D. J. Thompson,[21] L. Tibaldo,[10,11,7] J. A. Tomsick,[53] D. F. Torres,[54,19] G. Tosti,[13,14] A. Tramacere,[3,55] Y. Uchiyama,[3] T. L. Usher,[3] V. Vasileiou,[22,23] N. Vilchez,[40] V. Vitale,[45,56] A. P. Waite,[3] P. Wang,[3] J. Wilms,[57] B. L. Winer,[12] K. S. Wood,[1] T. Ylinen,[37,58,5] M. Ziegler[48]

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Organic Nonvolatile Memory Transistors for Flexible Sensor Arrays

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Using organic transistors with a floating gate embedded in hybrid dielectrics that comprise a 2-nanometer-thick molecular self-assembled monolayer and a 4-nanometer-thick plasma-grown metal oxide, we have realized nonvolatile memory arrays on flexible plastic substrates. The small thickness of the dielectrics allows very small program and erase voltages (≤6 volts) to produce a large, nonvolatile, reversible threshold-voltage shift. The transistors endure more than 1000 program and erase cycles, which is within two orders of magnitude of silicon-based floating-gate transistors widely employed in flash memory. By integrating a flexible array of organic floating-gate transistors with a pressure-sensitive rubber sheet, we have realized a sensor matrix that detects the spatial distribution of applied mechanical pressure and stores the analog sensor input as a two-dimensional image over long periods of time.

Electronic devices are traditionally fabricated using inorganic semiconductors, rigid substrates, and high-temperature manufacturing methods. In contrast, organic semiconductors can be processed at low temperatures and on large-area polymeric substrates. This has allowed for the development of a variety of electronic devices on flexible plastic substrates, including solar cells (*1*), light-emitting diode displays (*2*), field-effect transistors (*3*), transponders (*4*), sensors (*5*), actuators (*6*), and nonvolatile memory transistors (*7*–*11*). Nonvolatile memory transistors are potentially useful to individualize radio-frequency transponders or to store data obtained by large-area sensor arrays for later read-out. Most of the organic memory transistors reported to date exploit the electric field–induced remnant polarization in ferroelectric polymer films (*7*–*11*). A considerable limitation of ferroelectric polymer memory transistors is that the coercive field required to reverse the macroscopic polarization increases with decreasing film thickness (*12*), which makes it difficult to obtain a large enough memory window with program and erase voltages below about 20 V. Also, due to the substantial surface roughness of the ferroelectric polymer films, the carrier field-effect mobility in these transistors is usually quite low (<0.1 cm^2/Vs).

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A floating-gate transistor is a field-effect transistor with two gate electrodes. In addition to the control gate, similar to that in a regular transistor, it has a floating gate embedded in the gate dielectric. When the dielectric is thin enough, electronic charge can be brought onto the floating gate by quantum tunneling or thermal emission when a large enough program voltage is applied between the control gate and the source contact. Charging the floating gate changes the transistor's threshold voltage, because the charge on the floating gate partially screens the electric field between the control gate and the semiconductor. This threshold voltage shift can be detected by measuring the drain current at a certain gate-source voltage. Because the floating gate is completely isolated by the dielectric, charge stored on the floating gate remains there without the need for any applied voltage (nonvolatile memory). To erase the memory, a voltage of opposite polarity is applied, discharging the floating gate through the dielectric.

In silicon-based floating-gate transistors, the dielectric is a silicon dioxide layer with a thickness of a few nanometers. The exact thickness is a

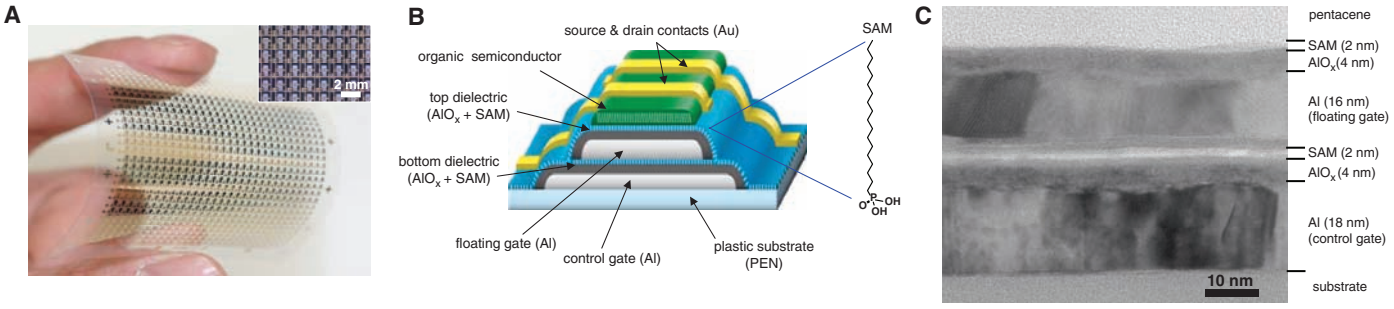

Fig. 1. (**A**) Photograph of an organic floating-gate transistor sheet comprising 26 by 26 memory cells. The array has an effective area of 50 by 50 mm^2. The inset shows a magnified image of the array. (**B**) Schematic cross section of the floating-gate transistors. The substrate is flexible PEN. The control and floating gates are 20-nm-thick layers of evaporated aluminum. The top and bottom dielectrics are each a combination of a 4-nm-thick layer of AlO_x and a 2-nm-thick SAM. The organic semiconductor is a 50-nm-thick layer of pentacene, and the source and drain contacts are 50-nm-thick layers of evaporated gold. (**C**) Cross-sectional TEM images of a flexible floating-gate transistor. The specimen was prepared using a focused ion beam and imaged by TEM (300 kV).

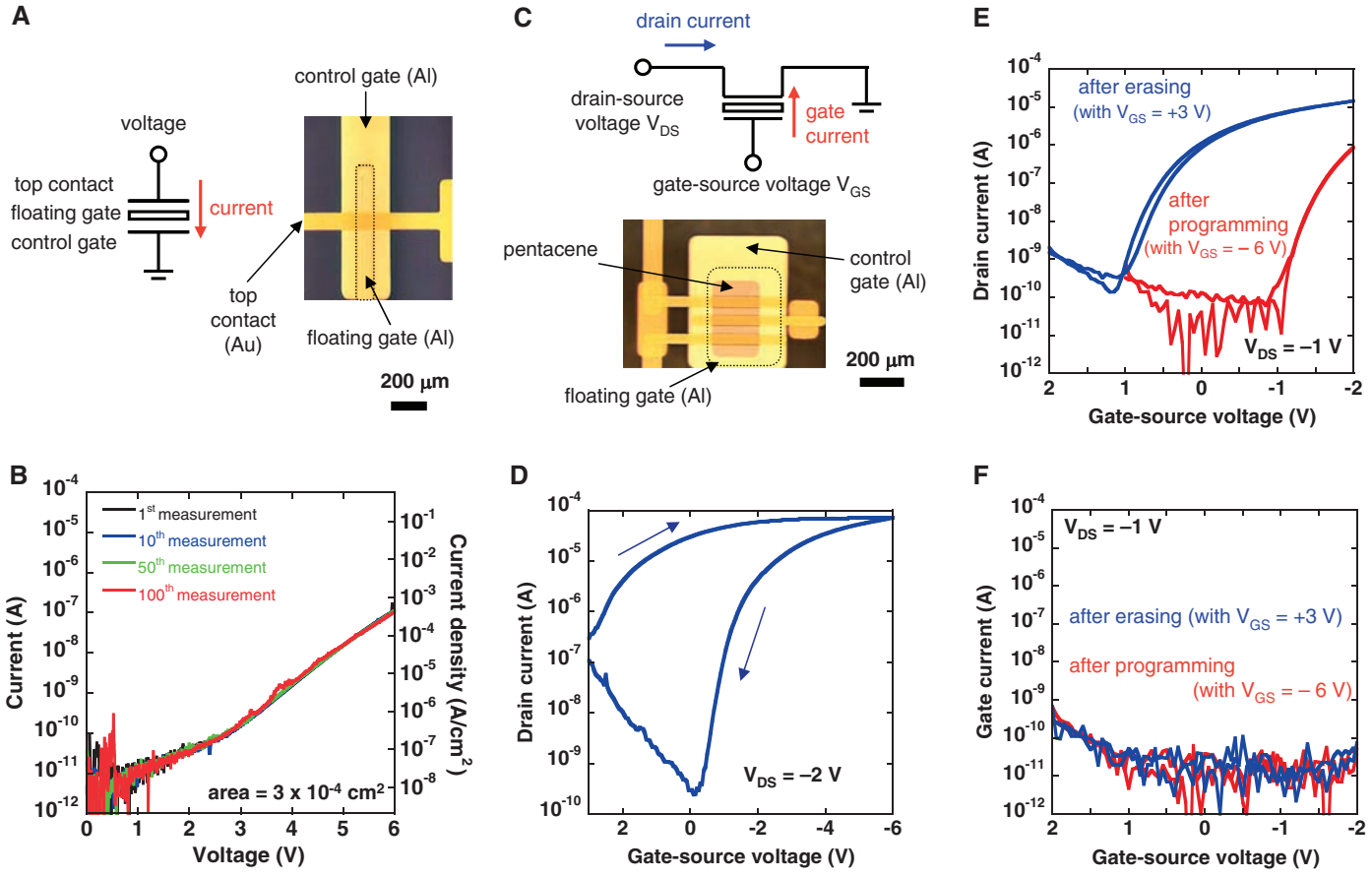

Fig. 2. Static electrical performance of the floating-gate memory devices. (**A**) Photograph of a floating-gate capacitor used for characterizing the voltage-dependent current through the AlO_x/SAM dielectrics. (**B**) Current through the AlO_x/SAM dielectrics as a function of applied voltage. Up to 6 V, the current does not cause irreversible changes in the dielectrics. (**C**) Photograph of a pentacene floating-gate memory transistor. (**D**) Drain current as a function of the voltage applied between control gate and source contact. When the applied voltages are –6 V and +3 V, the floating gate is charged and discharged, causing a threshold-voltage shift and hysteresis in the current-voltage characteristics. (**E**) Read-out operation performed on a floating gate transistor after programming and after erasing for 1 s. The threshold-voltage shift induced by the program and erase operations is clearly observed. (**F**) Gate current of a floating-gate transistor measured during read-out. For read-out voltages up to ±2 V, the gate current reaches about 100 pA.

compromise between the voltage required to bring enough charge onto the floating gate and the charge leakage from the floating gate, which sets an upper limit on the retention time. Silicon-based floating-gate transistors typically have program and erase voltages of 10 to 20 V (*13*, *14*) and retention times of several years. Because the defect density in the thin dielectric increases with every program and erase operation, the endurance is usually limited to ~10^6 program and erase cycles (*14*).

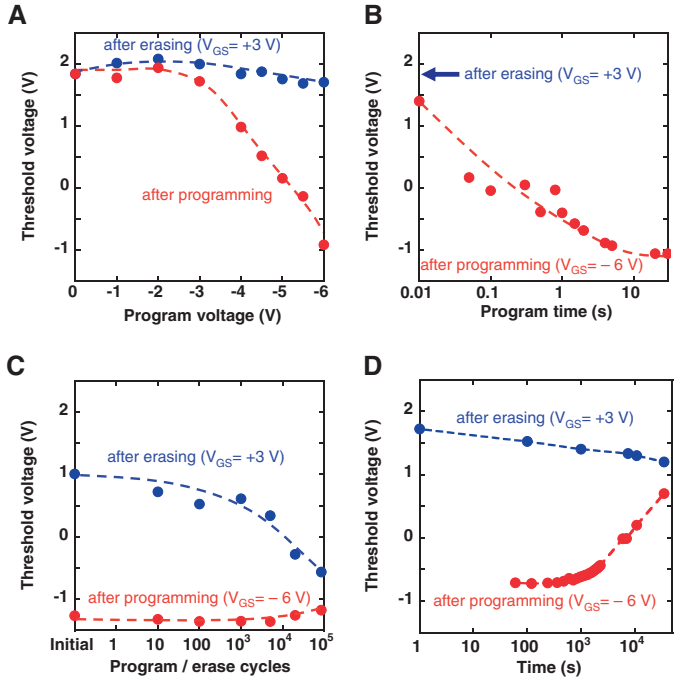

Fig. 3. Threshold voltage of organic floating-gate transistors. (**A**) Threshold-voltage shift as a function of program voltage. The program voltage is applied for 1 s. At the maximum program voltage of –6 V, a threshold-voltage shift of about 2.5 V is obtained. The threshold voltage after erasing with +3 V is independent of the program voltage. (**B**) Threshold-voltage shift as a function of the duration of the program pulse. The program voltage is –6 V. (**C**) Endurance of the memory transistors. The threshold-voltage window is greater than 2 V after 10^3 program and erase (–6 to +3 V) cycles and greater than 1 V after 10^4 cycles. (**D**) Retention characteristics of the memory transistors. The threshold voltage window is greater than 2 V after 10^3 s and greater than 1 V after 10^4 s. For each data point, the threshold voltage was obtained by measuring the complete transfer characteristics [sweeping gate-source voltage (V_{GS}) from +2 to –2 V; drain-source voltage (V_{DS}) = –1 V].

Although silicon floating-gate transistors are excellent for high-density data storage, flexible organic floating-gate transistors are potentially useful for large-area sensors and actuators with integrated nonvolatile memory capability. There are very few reports of organic floating-gate transistors, most of which use rigid substrates, thick dielectrics (10 to 50 nm) and large program and erase voltages (15 to 50 V), and none of which have demonstrated integration of these transistors into memory arrays (*15*–*18*). The main challenge in reducing the program and erase voltages and in demonstrating high yield and sufficient uniformity in large-area memory arrays on flexible plastic substrates is to develop a dielectric that can be prepared below the glass transition temperature of plastic film (<150°C) and which combines small film thickness with good reproducibility and small defect density. By taking advantage of the excellent properties of a low-temperature hybrid dielectric based on a thin metal oxide and a self-assembled monolayer (SAM), we have developed flexible floating-gate transistors with small program and erase voltages (–6 V to +3 V). Figure 1A shows a photograph of a plastic sheet with 676 organic floating-gate transistors arranged in a 26 by 26 array on a 125-μm-thick plastic film. The schematic device cross section is shown in Fig. 1B; the fabrication process is outlined in the Supporting Online Material. The two dielectrics that isolate the floating gate from the control gate and the organic semiconductor are a combination of a thin aluminum oxide (AlO_x) layer grown in an oxygen plasma at room temperature and an alkyl-phosphonic acid SAM

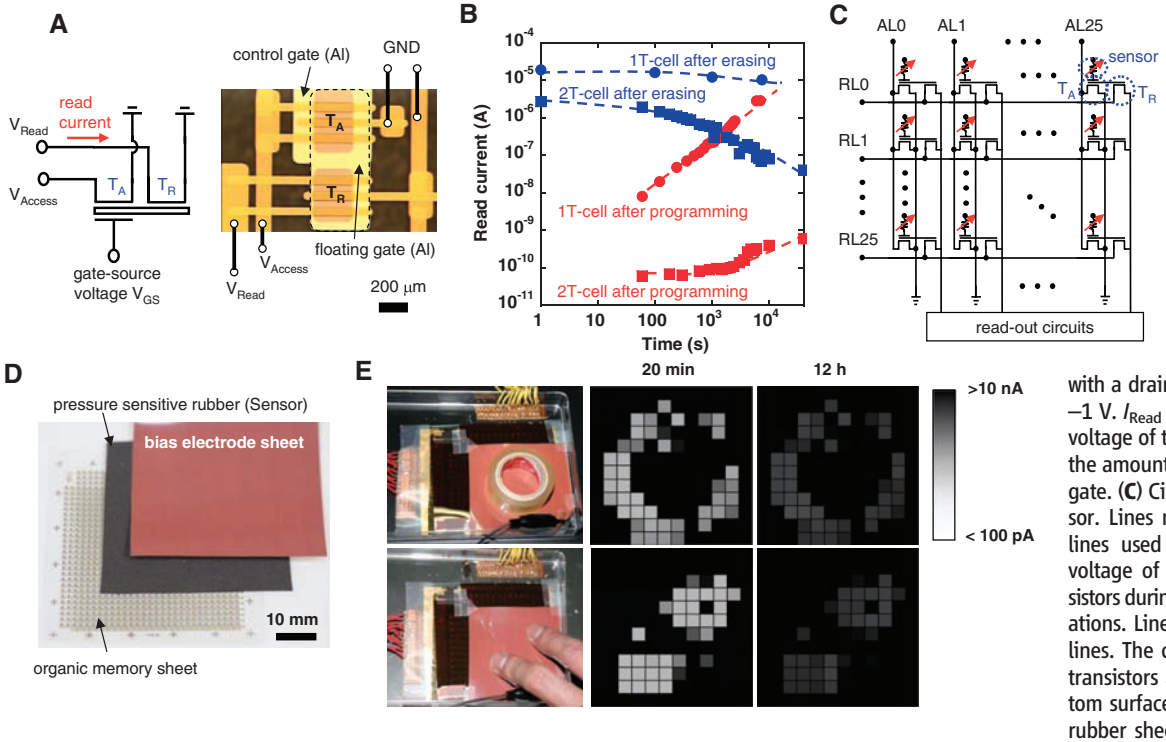

Fig. 4. Flexible pressure-sensor array. (**A**) Schematic and photograph of a two-transistor (2T) memory cell in which an access transistor (T_A) and a read-out transistor (T_R) share a large floating gate. (**B**) Retention characteristics of a 2T cell in comparison with that of a 1T cell. The read current (I_{Read}) is the drain current of T_R measured with a drain-source voltage (V_{Read}) of –1 V. I_{Read} depends on the threshold voltage of the transistors and thus on the amount of charge on the floating gate. (**C**) Circuit schematic of the sensor. Lines marked AL are the access lines used to apply a drain-source voltage of –2 V to the access transistors during program and erase operations. Lines marked RL are the read lines. The control gates of all access transistors are connected to the bottom surface of the pressure-sensitive rubber sheet. (**D**) Photograph of the three individual sheets before lamination. Bottom, 125-μm-thick PEN sheet with 676 2T memory cells; center, 500-μm-thick pressure-sensitive rubber sheet; top, 125-μm-thick PEN sheet with copper electrode. (**E**) Demonstration of the sensor array. The spatial distribution of mechanical pressure applied using two different objects is stored in the organic floating-gate transistors and can be retrieved even after the pressure and voltages have been removed.

prepared from solution at room temperature, with a total thickness of about 6 nm and a capacitance of 0.6 to 0.65 μF/cm^2 (*19*–*22*). The semiconductor is a thin layer of vacuum-deposited pentacene.

Figure 1C shows a cross-sectional electron microscopy (EM) image of a completed device. The specimen was prepared using a focused ion beam (FIB) (FB-2100, Hitachi High-Technologies Corp., Tokyo, Japan) and imaged by transmission electron microscopy (TEM) (HF-3300 Cold-FE TEM, 300 kV, Hitachi High-Technologies Corp.). The control gate, the floating gate, and the two dielectric layers can be clearly distinguished in the TEM image. Perhaps most notably, the 2-nm-thick organic SAM of the bottom dielectric that separates the control gate from the floating gate is clearly resolved. The TEM image confirms the structure of the organic floating-gate transistors.

To characterize the electric current through the dielectrics during program and erase operations, floating-gate capacitors were prepared without the semiconductor (Fig. 2A). Figure 2B shows that when the voltage between the control gate and the top contact increases, the current also increases, reaching 0.5 mA/cm^2 at 6 V. This measurement was repeated 100 times without any changes in the current-voltage curves, showing that the dielectric can sustain this current. Beyond 6.3 V, however, an irreversible increase in current was observed, indicating damage to the dielectric (fig. S3A).

Figure 2C shows a photograph of a pentacene floating-gate memory transistor. Initially, the threshold voltage (V_{th}) is between +1 and +2 V (Figs. 2 and 3). For programming, a voltage of –6 V is applied between the control gate and the source contact. This creates a gate current of 1 μA (fig. S3B), which charges the floating gate and shifts V_{th} to –1 V. To erase, a voltage of +3 V is applied to discharge the floating gate and recover the initial threshold voltage. Cycling the gate-source voltage between +3 V and –6 V produces the hysteresis seen in Fig. 2D. The exact V_{th} shift depends on the voltage and duration of the program pulse (Fig. 3, A and B, and figs. S4 and S5). To read the stored information, V_{th} is determined, for example, by measuring the drain current as a function of gate-source voltage. Figure 2E shows the result of two read-out operations, one on a transistor programmed at –6 V, the other on a transistor erased at +3 V. The threshold voltage window and the device-to-device uniformity (fig. S6) are sufficient for unambiguous read-out. Figure 2F shows that if read-out is performed with a gate-source voltage of ±2 V, the gate current reaches 100 pA. This causes a small portion of the stored charge to be lost and V_{th} to shift slightly during each read-out operation (destructive read-out) (fig. S7, A and B). In contrast, if read-out is performed with a gate-source voltage of 0 V, there is no charge loss and no V_{th} shift (nondestructive read-out) (fig. S7C).

Modern silicon-based flash memory is typically rated for 10^6 program and erase cycles (*14*), after which the memory characteristics degrade. To evaluate the endurance of the organic memory transistors, a device was subjected to 10^5 program and erase cycles (–6 V to +3 V, 1 Hz). The results in Fig. 3C and in fig. S8 show that the threshold voltage window is constant at 2 V up to 10^3 cycles. Beyond that, the positive threshold voltage shift during the erase operation becomes smaller, so the initial threshold voltage of +1 V is no longer recovered and the threshold voltage window becomes smaller. Nonetheless, after 10^4 cycles, the threshold voltage window is still 1 V, sufficient for unambiguous read-out. After 10^5 cycles, the threshold voltage window is 0.5 V. Interestingly, the initial threshold voltage of +1 V can be recovered by annealing the transistors at 140°C in dry nitrogen, which suggests that the endurance is limited not by irreversible structural damage but by reversible carrier trapping.

Unlike dynamic random access memory (DRAM), nonvolatile memories retain information in the absence of external voltages. In floating-gate transistors, this requires that the charge on the floating gate is prevented from leaking away through the dielectric. Data retention experiments on an individual pentacene device (shown in Fig. 3D) suggest that the retention time is only a few hours (threshold voltage window is 1.1 V after 3 hours, 0.6 V after 12 hours). However, most of the charge loss in this case occurred during read-out. To improve retention, we have therefore designed and fabricated a two-transistor memory cell in which an access transistor (with control gate) and a read-out transistor (without control gate) share a floating gate with an area of 400 by 1000 μm^2 (Fig. 4A). Read-out is performed with a drain-source voltage of –1 V applied to the read-out transistor for 0.1 s or less, with no voltage applied on the control gate. This resulted in a significant improvement in retention time: After 3 hours, the read-current ratio is less than 2 for the one-transistor cell, but 2×10^2 for the two-transistor cell. After 12 hours, the two-transistor cell still has a usably large read-current ratio of 10^2 (Fig. 4B).

To demonstrate the potential of organic floating-gate transistors and the two-transistor memory cell design, we fabricated a large-area flexible sensor that measures the spatial distribution of mechanical pressure applied to it and retains this data for more than 12 hours after the pressure and voltages have been removed. The sensor was fabricated by laminating three sheets: a polyethylene naphthalate (PEN) sheet with 676 two-transistor memory cells arranged in a 26 by 26 array, a pressure-sensitive rubber sheet, and a PEN sheet with a copper electrode. The circuit schematic is shown in Fig. 4C, a photograph of the three individual sheets before lamination is shown in Fig. 4D, photographs of the memory array are shown in fig. S10A, and a cross section of the laminated stack is shown in fig. S10B. The control gates of all 676 memory cells are connected to the bottom surface of the rubber sheet, and the top surface of the rubber sheet is in contact with the copper electrode. When mechanical pressure is applied to the rubber sheet, the electrical resistance between the rubber's top and bottom surfaces decreases (fig. S10C). By applying a program voltage to the copper electrode and an access voltage to all memory cells, the copper electrode supplies the program voltage to the floating-gate transistors in those positions where pressure is applied, and the pressure distribution is stored in the memory array.

Figure 4E shows a demonstration of the sensor. Pressure was applied using two different objects: a roll of tape and two fingers. The stored information was read out after 20 min and again after 12 hours with a multichannel drive system. As can be seen, the contrast between the programmed cells and the background deteriorates over time due to charge loss (Fig. 4B), but even 12 hours after removing the mechanical pressure and the electric voltages, the stored information showing the spatial distribution of the applied pressure was still successfully recovered.

References and Notes

1. D. Gebeyehu *et al.*, *Synth. Met.* **118**, 1 (2001).
2. L. Zhou *et al.*, *Appl. Phys. Lett.* **88**, 083502 (2006).
3. G. H. Gelinck *et al.*, *Nat. Mater.* **3**, 106 (2004).
4. P. F. Baude *et al.*, *Appl. Phys. Lett.* **82**, 3964 (2003).
5. T. Someya *et al.*, *Proc. Natl. Acad. Sci. U.S.A.* **102**, 12321 (2005).
6. T. Sekitani *et al.*, *Nat. Mater.* **6**, 413 (2007).
7. C. A. Nguyen, S. G. Mhaisalkar, J. Ma, P. S. Lee, *Org. Electron.* **9**, 1087 (2008).
8. K. H. Lee, G. Lee, K. Lee, M. S. Oh, S. Im, *Appl. Phys. Lett.* **94**, 093304 (2009).
9. T. Sekitani *et al.*, *IEEE Trans. Electron. Dev.* **56**, 1027 (2009).
10. R. Schroeder, L. A. Majewski, M. Grell, *Adv. Mater.* **16**, 633 (2004).
11. R. C. G. Naber *et al.*, *Nat. Mater.* **4**, 243 (2005).
12. H. Kliem, R. Tadros-Morgane, *J. Phys. D Appl. Phys.* **38**, 1860 (2005).
13. K. Takeuchi, *IEEE J. Solid-State Circuits* **44**, 1227 (2009).
14. R. Bez, E. Camerlenghi, A. Modelli, A. Visconti, *Proc. IEEE* **91**, 489 (2003).
15. Z. Liu, F. Xue, Y. Su, Y. M. Lvov, K. Varahramyan, *IEEE Trans. NanoTechnol.* **5**, 379 (2006).
16. L. Zhen, W. Guan, L. Shang, M. Liu, G. Liu, *J. Phys. D Appl. Phys.* **41**, 135111 (2008).
17. W. Wang, J. Shi, D. Ma, *IEEE Trans. Electron. Dev.* **56**, 1036 (2009).
18. M.-F. Chang, P.-T. Lee, S. P. McAlister, A. Chin, *Appl. Phys. Lett.* **93**, 233302 (2008).
19. H. Klauk, U. Zschieschang, J. Pflaum, M. Halik, *Nature* **445**, 745 (2007).
20. H. Ma *et al.*, *Appl. Phys. Lett.* **92**, 113303 (2008).
21. T. Sekitani, Y. Noguchi, U. Zschieschang, H. Klauk, T. Someya, *Proc. Natl. Acad. Sci. U.S.A.* **105**, 4976 (2008).
22. P. H. Wöbkenberg *et al.*, *Appl. Phys. Lett.* **93**, 013303 (2008).

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Supporting Online Material

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Materials and Methods
SOM Text
Figs. S1 to S10

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1. Device fabrication (Figure S1)

Fig. 1A shows a photograph of a plastic sheet with 676 organic floating-gate transistors arranged in a 26 × 26 array fabricated on 125 μm thick flexible polyethylene naphthalate (PEN) film. A schematic cross section of the floating-gate transistors is shown in Fig. 1B.

In the first step of the fabrication process, the control gates are prepared by evaporating aluminium (Al) onto the PEN substrate to a thickness of 20 nm through a shadow mask. A layer of aluminum oxide (AlO_x) with a thickness of about 4 nm is created on the Al surface by oxygen plasma treatment (150 W, 10 min). The substrate is immersed in a 2-propanol solution of n-octadecylphosphonic acid to create a densely packed self assembled monolayer (SAM) with a thickness of 2 nm on the surface of the oxidized Al layer.

The dielectric between the control gate and the floating gate is therefore a combination of an AlO_x layer grown in an oxygen plasma at room temperature and a SAM prepared from solution at room temperature, with a total thickness of about 6 nm and a capacitance of 0.6–0.65 μF/cm^2. On top of this bottom dielectric, a 20 nm thick floating gate is prepared by evaporating Al to a thickness of 20 nm through a shadow mask. The top dielectric is again a combination of a plasma-grown AlO_x layer (with a thickness of about 4 nm) and a SAM of n-octadecylphosphonic acid (with a thickness of 2 nm). A cross-sectional image without pentacene can be seen in Fig. S1. The specimen was prepared using a focused ion beam (FIB; FB-2100, Hitachi High-Technologies Corp.) and imaged by transmission electron microscopy (TEM; HF-3300 Cold-FE TEM, 300 kV, Hitachi High-Technologies Corp.).

On top of the top dielectric, a 50 nm thick layer of the conjugated organic semiconductor pentacene is deposited by vacuum sublimation through a shadow mask. The source and drain contacts are formed on top of the organic semiconductor by evaporating gold (Au) to a thickness of 50 nm through a shadow mask.

Finally, the substrate is coated with a hybrid organic/metal passivation layer (a 300 nm thick layer of parylene followed by a 150 nm thick layer of gold) to protect the transistors from air-induced degradation. Consequently, all measurements were carried out in ambient air.

2. Transistor characteristics (Figure S2)

Fig. S2 summarizes results on the performance and the stability of a pentacene thin-film transistor that was prepared without a floating gate on flexible PEN. (**A**) Schematic cross-section of a pentacene transistor without a floating gate. Transistors without floating gate cannot be used as memory devices; they were manufactured here only for evaluation purposes and were not utilized in the pressure sensor array. (**B**) Output characteristics and (**C**) transfer characteristics of a flexible pentacene transistor with a channel length of 50 μm and a channel width of 500 μm. Owing to the small thickness of the AlO_x/SAM gate dielectric, the transistor can be operated with small gate-source and drain-source voltages. The transistor has a field-effect mobility of 0.5 cm^2/Vs, an on/off current ratio of 10^5, and a subthreshold swing of 120 mV/decade. Despite the small thickness of the gate dielectric, the gate current at a gate-source voltage of -2 V is less than 1 nA. (**D**) Shelf-life test on a flexible pentacene transistor, showing that the encapsulated devices are stable in air for long periods of time, owing to the excellent gas-barrier properties of the organic/metal passivation layer.

3. Electric currents through the AlO_x/SAM dielectrics (Figure S3)

(**A**) Current flowing through a floating-gate capacitor as a function of applied voltage. Up to 6 V, the current does not cause electrical damage in the AlO_x/SAM dielectrics (see also Fig. 2B). But when the voltage exceeds 6.3 V, an irreversible increase in current is observed, indicating damage to the dielectric. Therefore, the maximum program and erase voltages for the floating-gate transistors are 6 V. (**B**) Gate current of a pentacene floating-gate transistor as a function of voltage applied between the control gate and the source contact. At a program voltage of -6 V, the gate current reaches 1 μA.

4. Influence of the program voltage on the threshold-voltage shift (Figure S4)

(**A**) Transfer characteristics of a floating-gate transistor after program operations performed with program voltages ranging from -1 V to -6 V. The duration of each program voltage pulse was 1 s. As can be seen, larger program voltages yield larger threshold-voltage shifts. (**B**) Transfer characteristics of a floating-gate transistor after a program operation immediately followed by an erase operation. The program operation was performed with program voltages ranging from -1 V to -6 V; the subsequent erase operation was performed with an erase voltage of +3 V. The duration of each program-voltage pulse and each erase-voltage pulse was 1 s. As can be seen, the initial threshold voltage of -1 V is always recovered by the erase operation, regardless of the program voltage during the program operation. (**C**) Drain current of a floating-gate transistor measured at zero gate-source voltage (V_{GS} = 0, V_{DS} = -1 V) after a program operation performed with program voltages ranging from -1 V to -6 V (red curve), and after a program operation followed immediately by an erase operation (blue curve). (**D**) Transfer characteristics of a

floating-gate transistor obtained by applying maximum gate-source voltages ranging from -2 V to -6 V. As can be seen, the hysteresis due to the threshold-voltage shift increases as the maximum gate-source voltage is increased.

5. Influence of the program pulse duration on the threshold-voltage shift (Figure S5)

Transfer characteristics of a floating-gate transistor after program operations performed with voltages pulses ranging in duration from 0.05 s to 20 s. The program voltage was -6 V in all cases. As can be seen, longer pulse durations yield larger threshold-voltage shifts.

6. Device-to-device uniformity (Figure S6)

(**A**) Drain current as a function of gate-source voltage of 15 floating-gate transistors (randomly selected from the same substrate) after erasing (blue curve) and after programming (red curve). (**B**) Threshold voltage and (**C**) drain current at V_{GS} = 0 V and V_{DS} = -1 V of the 15 transistors after erasing (blue data) and after programming (red data). Good uniformity has been achieved because the gate dielectrics, which are the most important component of floating-gate transistors, are formed by molecular self-assembly and plasma-growth without the need for alignment or thickness control.

7. Data retention during read-out operations (Figure S7)

(**A**) Drain current as a function of gate-source voltage of a pentacene floating-gate memory transistor before (blue curve) and after (red curve) programming with a program voltage of -6 V, and after each of ten successive read-out operations during which the gate-source voltage is swept between -2 and +2 V (as shown in Fig. 2E). The gate-source voltage applied during

read-out causes a small gate current (see Fig. 2F) that changes the amount of charge on the floating gate. As a result, the threshold voltage shifts slightly during each read-out operation (destructive read-out). (**B**) Threshold voltage after each of ten successive read-out cycles. V_{th} shifts towards more positive values during each read-out operation. The dashed lines are guides to the eye. (**C**) Evolution of the drain current after as many as 500 read-out operations performed with pulsed read-out voltages (pulse with 100 ms). When read-out is performed with V_{GS} = -2 V and V_{DS} = -1 V, the memory ratio decreases with each read-out pulse, from 10^2 after 10 read-out operations to 10^1 after 100 read-out operations. On the other hand, when read-out is performed with V_{GS} = 0 V and V_{DS} = -1 V, the data retention during read-out is much better, because there is essentially no charge loss during read-out. The results indicate that the data is not lost even after 100~1000 read-out operations when read-out is performed using specific pulsed voltages. We believe in mass storage applications the stored data must survive 10^6 read-out operations, but organic floating-gate transistors are of interest for large-area sensors and actuators where the number of read-out cycles will be much smaller.

8. Endurance (Figure S8)

(**A**) Transfer characteristics (read-out operations) of a floating-gate transistor after 10, 100, 1000, 5000, 20,000, and 85,000 program/erase cycles. Each program/erase cycle was performed with a program voltage of -6 V, an erase voltage of +3 V, and a pulse duration of 1 s. The last operation before the transfer curve was measured was an erase operation. (**B**) Transfer characteristics (read-out operations) of a floating-gate transistor after 10, 100, 1000, 5000, 20,000, and 85,000 program/erase cycles (-6 V/+3 V; 1 s). The last operation before the transfer curve was measured was a program operation. (**C**) Drain current of a floating-gate transistor measured at zero

gate-source voltage (V_{GS} = 0, V_{DS} = -1 V) after 10, 100, 1000, 5000, 20,000, and 85,000 program/erase cycles (-6 V/+3 V; 1 s). The last operation before the drain current was measured was an erase operation (blue curve) or a program operation (red curve). (**D**) Drain current as a function of the voltage applied between control gate and source contact. Measurements were performed after 1, 10, 50, and 100 cycles sweeping from + 3 V to -6 V. When the applied voltages are -6 V and +3 V, the floating gate is charged and discharged, causing a threshold-voltage shift and hysteresis in the current-voltage characteristics.

9. Influence of the erase voltage on the threshold-voltage shift (Figure S9)

(**A**) Transfer characteristics of a floating-gate transistor after a program operation performed with a voltage of -6 V (red curve), after an erase operation performed with a voltage of +3 V, (blue curve), and after "over-erasing" with a voltage of +4.5 V (black curve). The duration of each voltage pulse was 1 s. "Over-erasing" shifts the threshold voltage beyond the initial threshold voltage to large positive values. (**B**) Retention characteristics after programming (V_{GS} = -6 V, 1s), after erasing (V_{GS} = +3 V, 1s), and after "over-erasing" (V_{GS} = +4.5 V, 1s). This result indicates that the threshold-voltage shift is symmetric with respect to its initial value and that this initial value is recovered after sufficiently long time.

10. Structure of the flexible pressure-sensor array (Figure S10)

(**A**) Photographs of the memory array. The substrate is a 125-µm-thick sheet of polyethylene naphthalate (PEN). The 676 two-transistor cells are arranged in a 26 × 26 array with access and read lines. The effective area of the array is 50 × 50 mm^2. (**B**) Schematic cross section of the sensor. The commercially available pressure-sensitive rubber sheet has a thickness of 500 µm

(PCR Technical Co. Ltd, Japan) (**C**) Electrical resistance measured between the top and bottom surfaces of the rubber sheet as a function of mechanical pressure. When pressure is applied to the rubber sheet, the resistance decreases from 1 MΩ at 100 Pa to 100 Ω at 10^4 Pa.

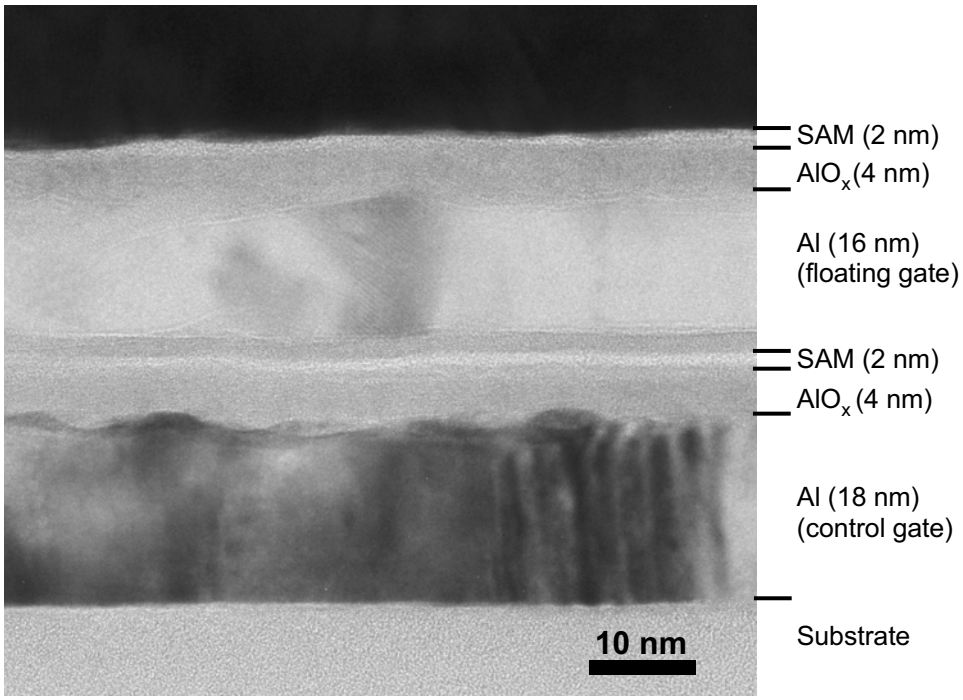

Fig. S1. A cross-sectional image without pentacene. The specimen was prepared using FIB and imaged by TEM.

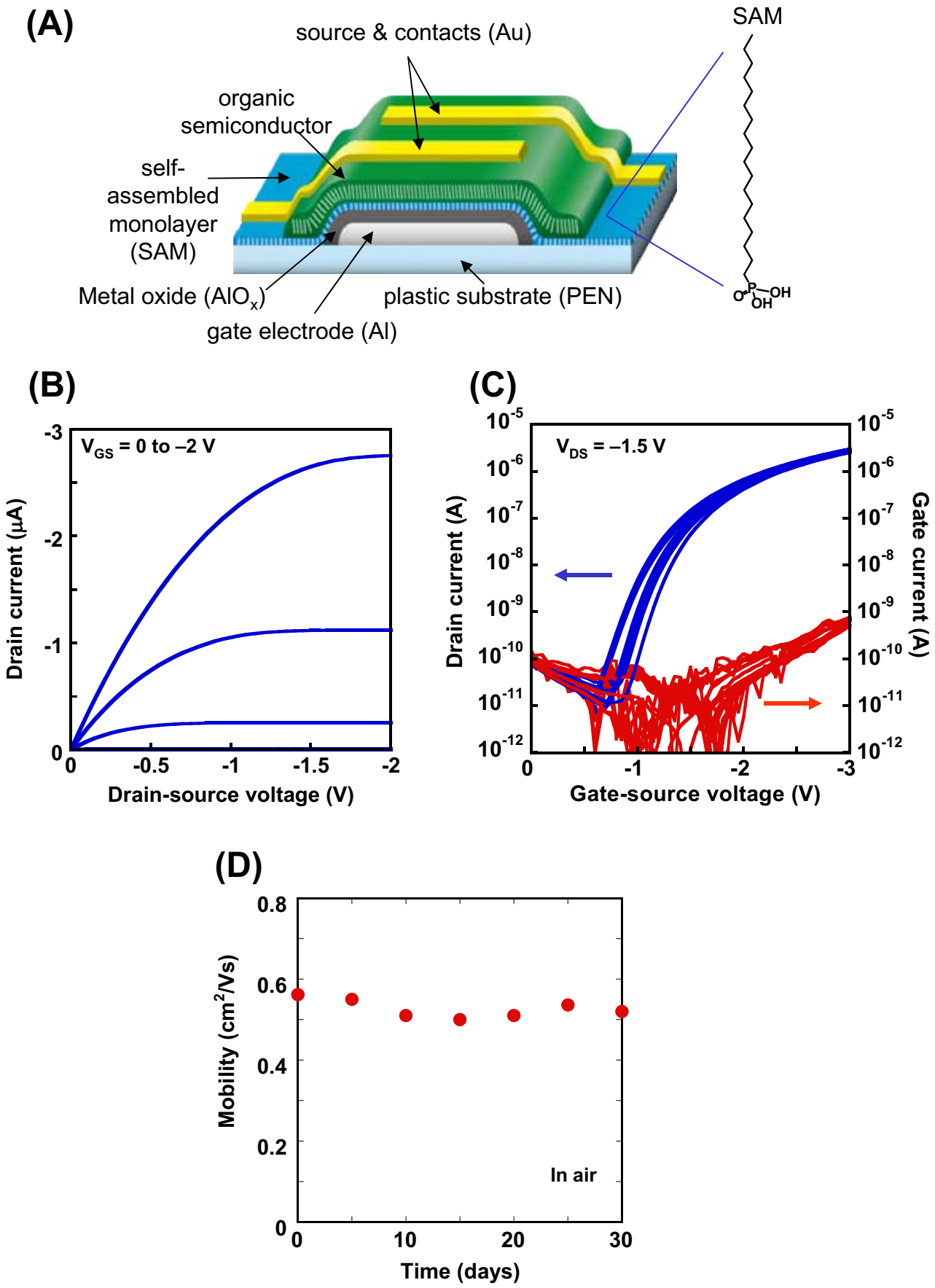

Fig. S2. Transistor characteristics without a floating gate.

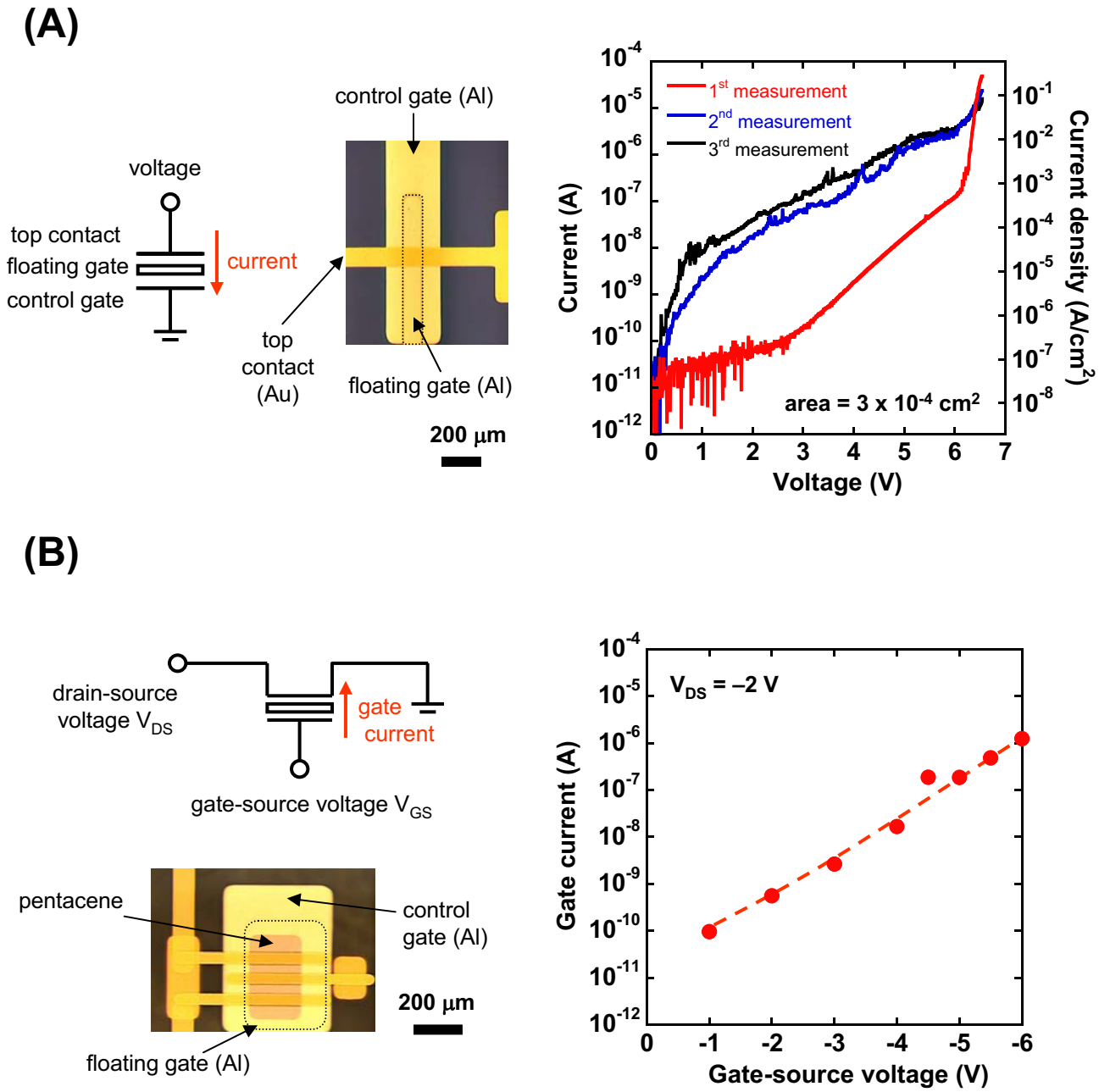

Fig. S3. Electric currents through the AlO_x/SAM dielectrics

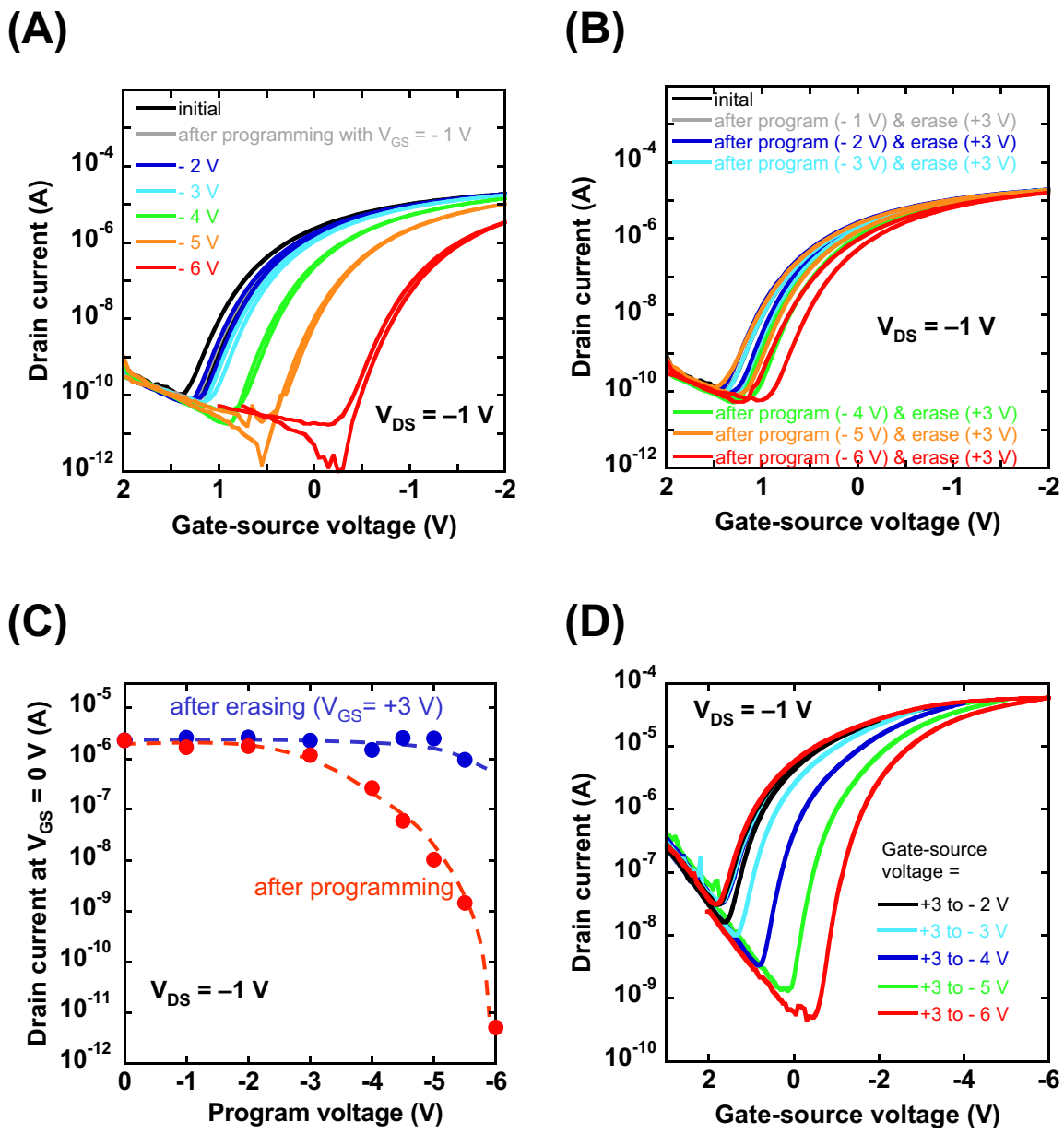

Fig. S4. Influence of the program voltage on the threshold-voltage shift.

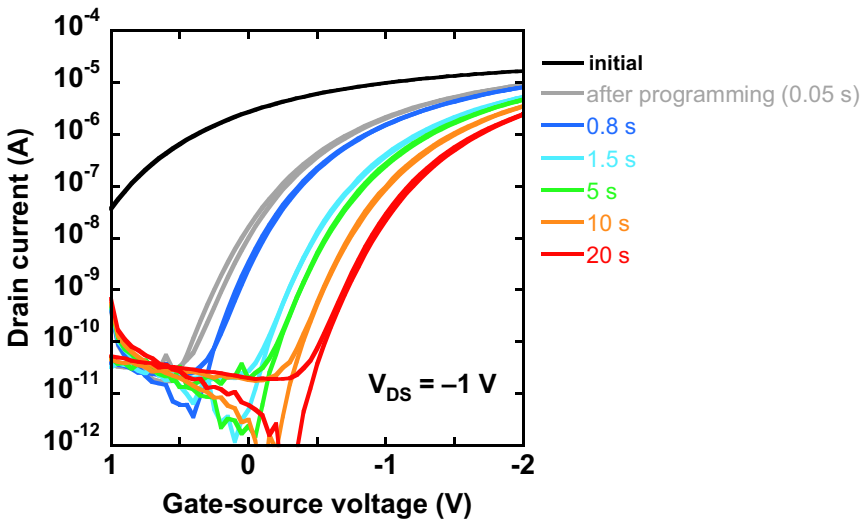

Fig. S5. Influence of the program pulse duration on the threshold-voltage shift.

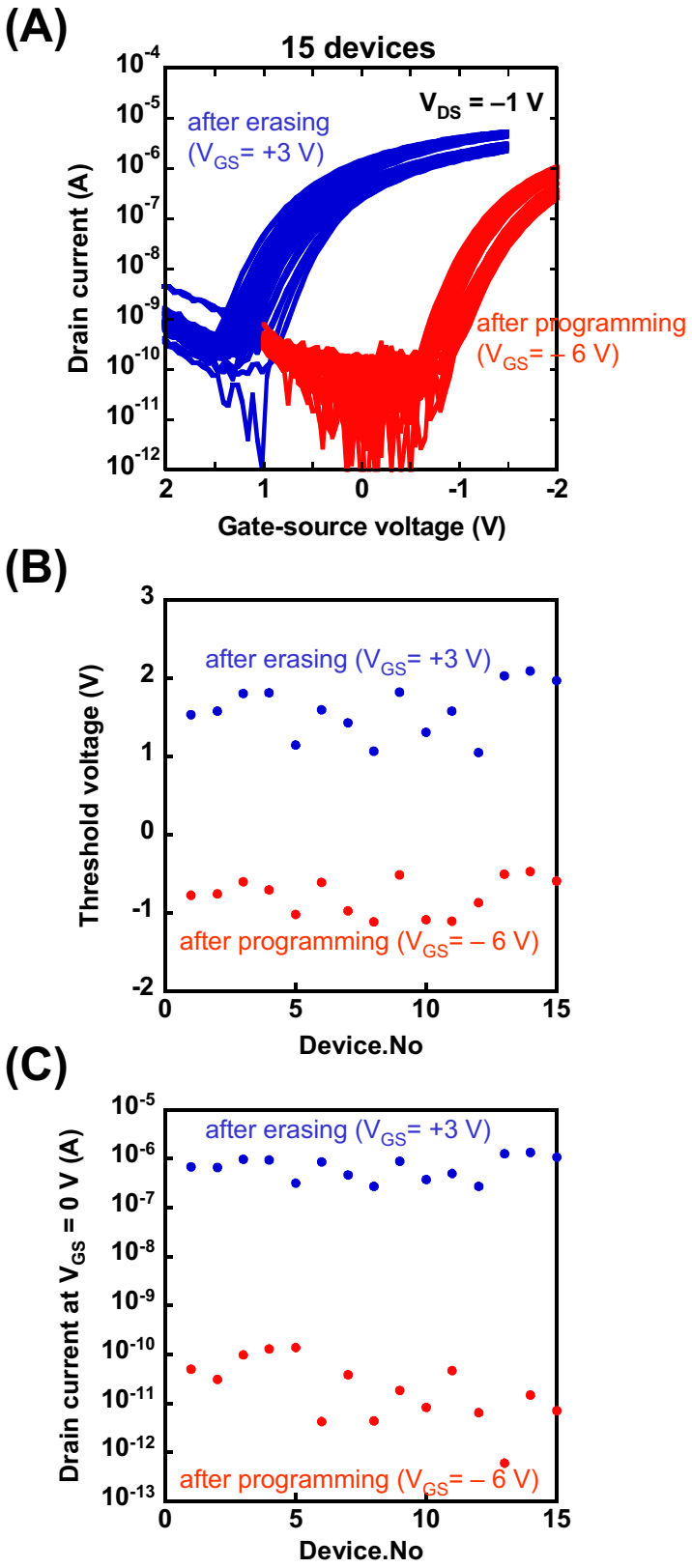

Fig. S6. Device-to-device uniformity.

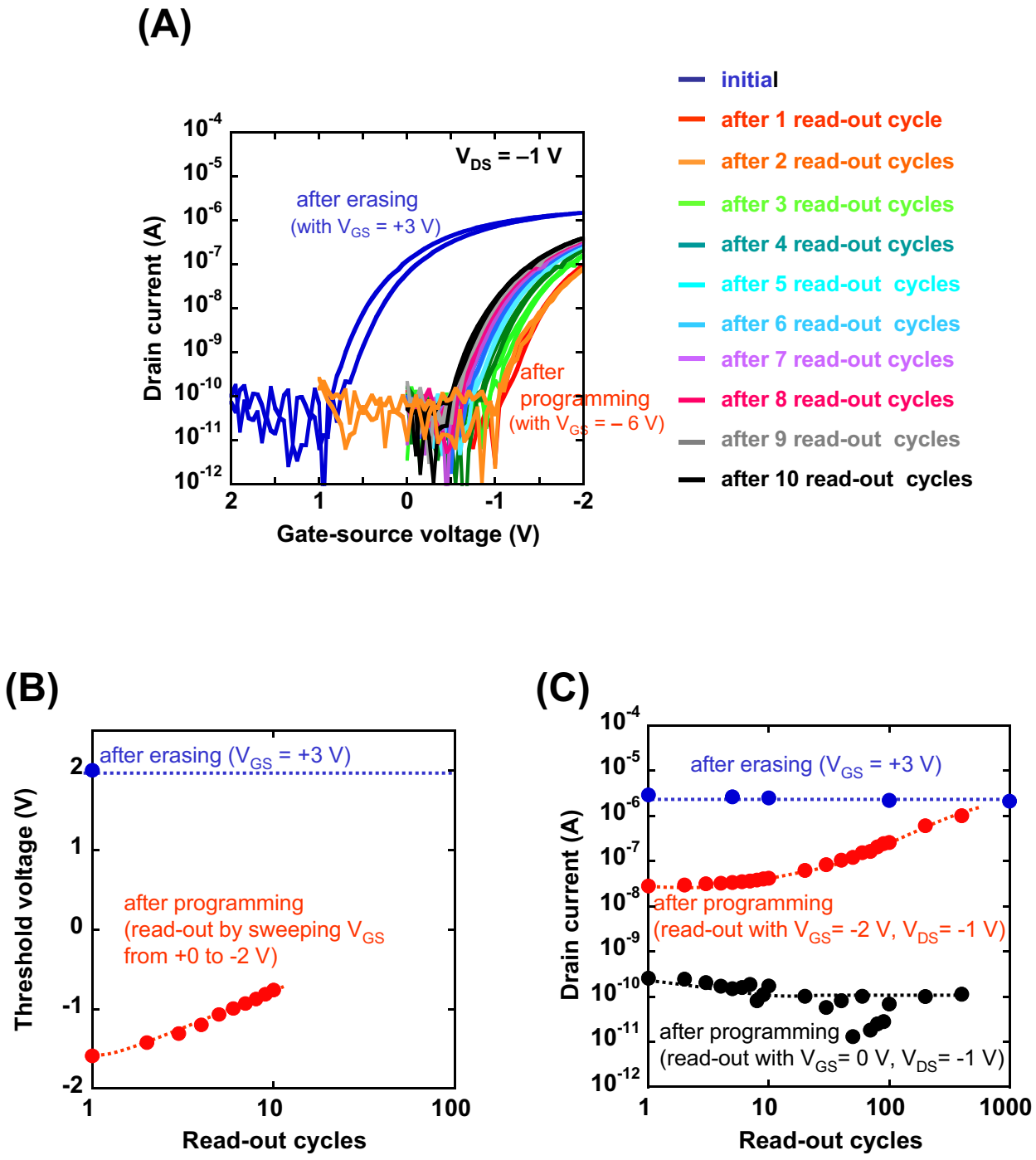

Fig. S7. Data retention during read-out operations.

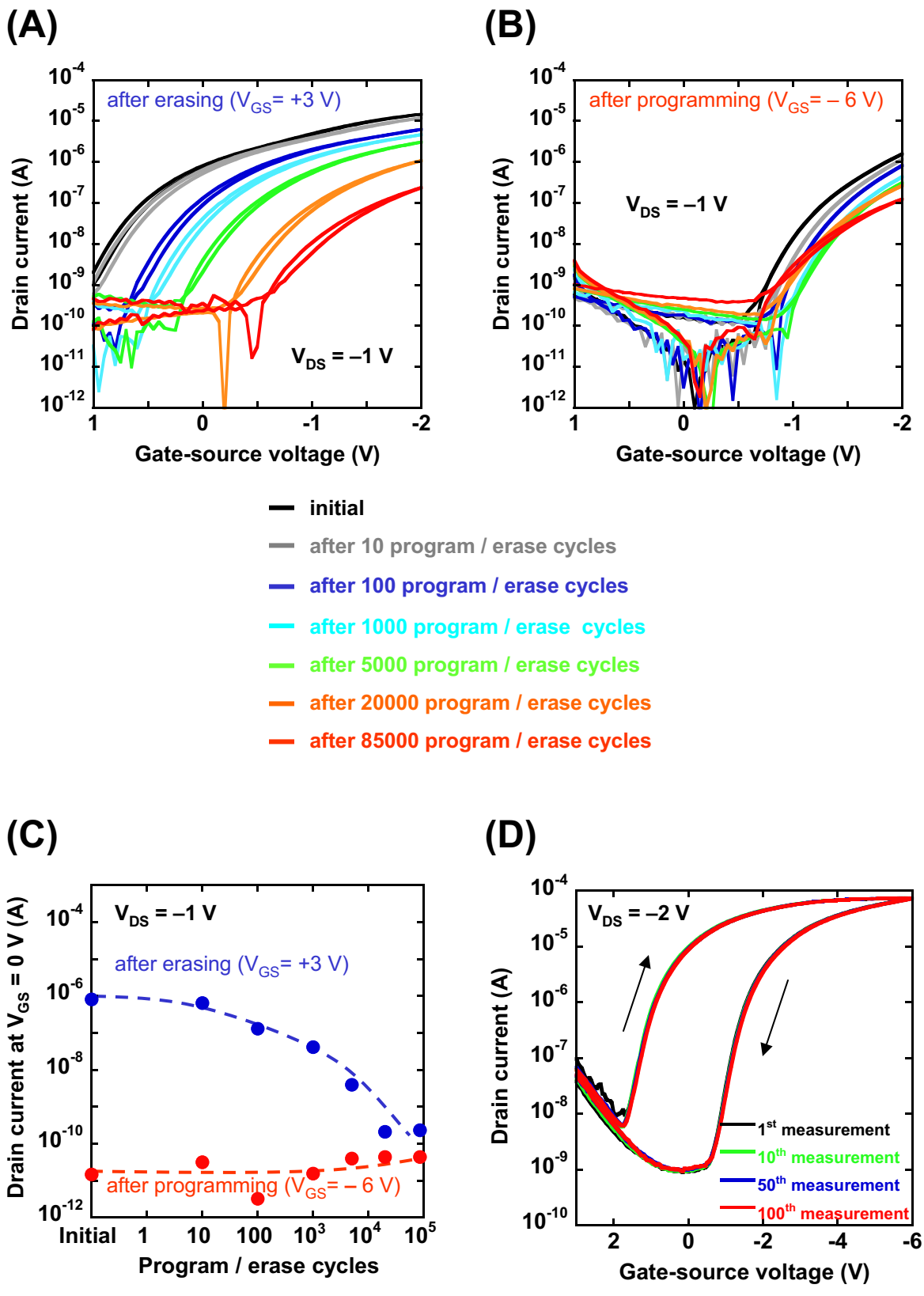

Fig. S8. Endurance.

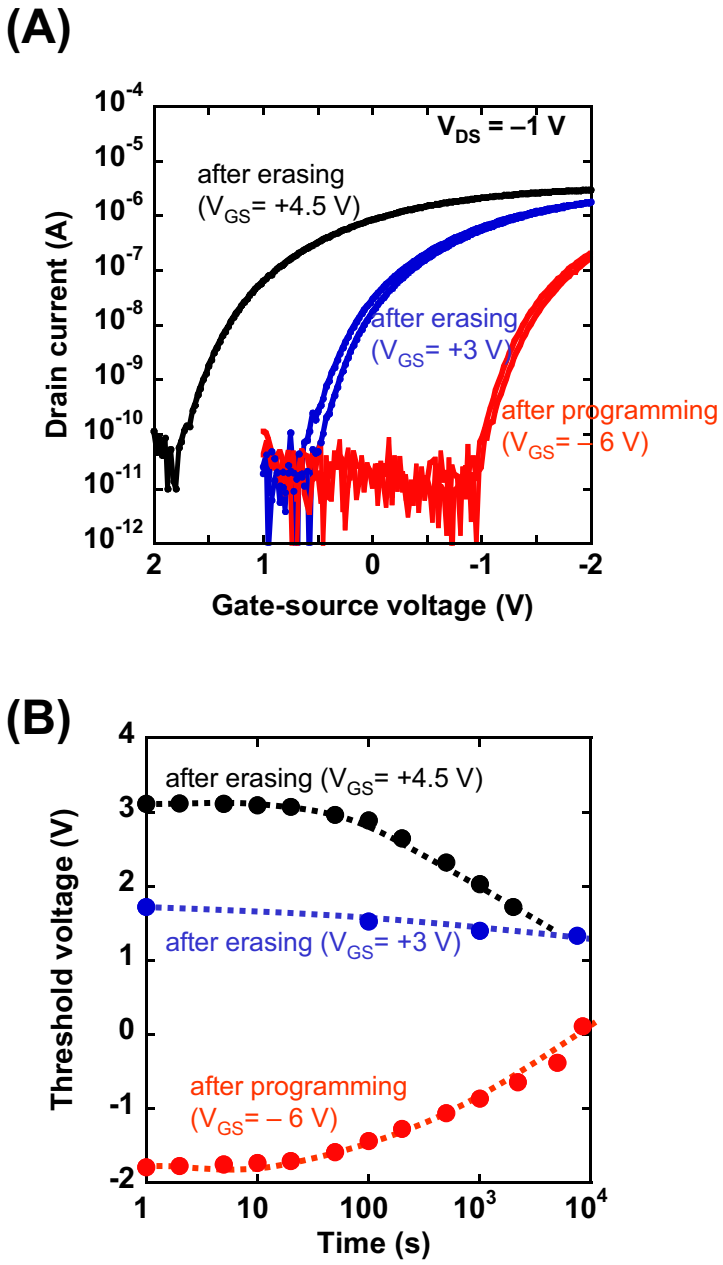

Fig. S9. Influence of the erase voltage on the threshold-voltage shift.

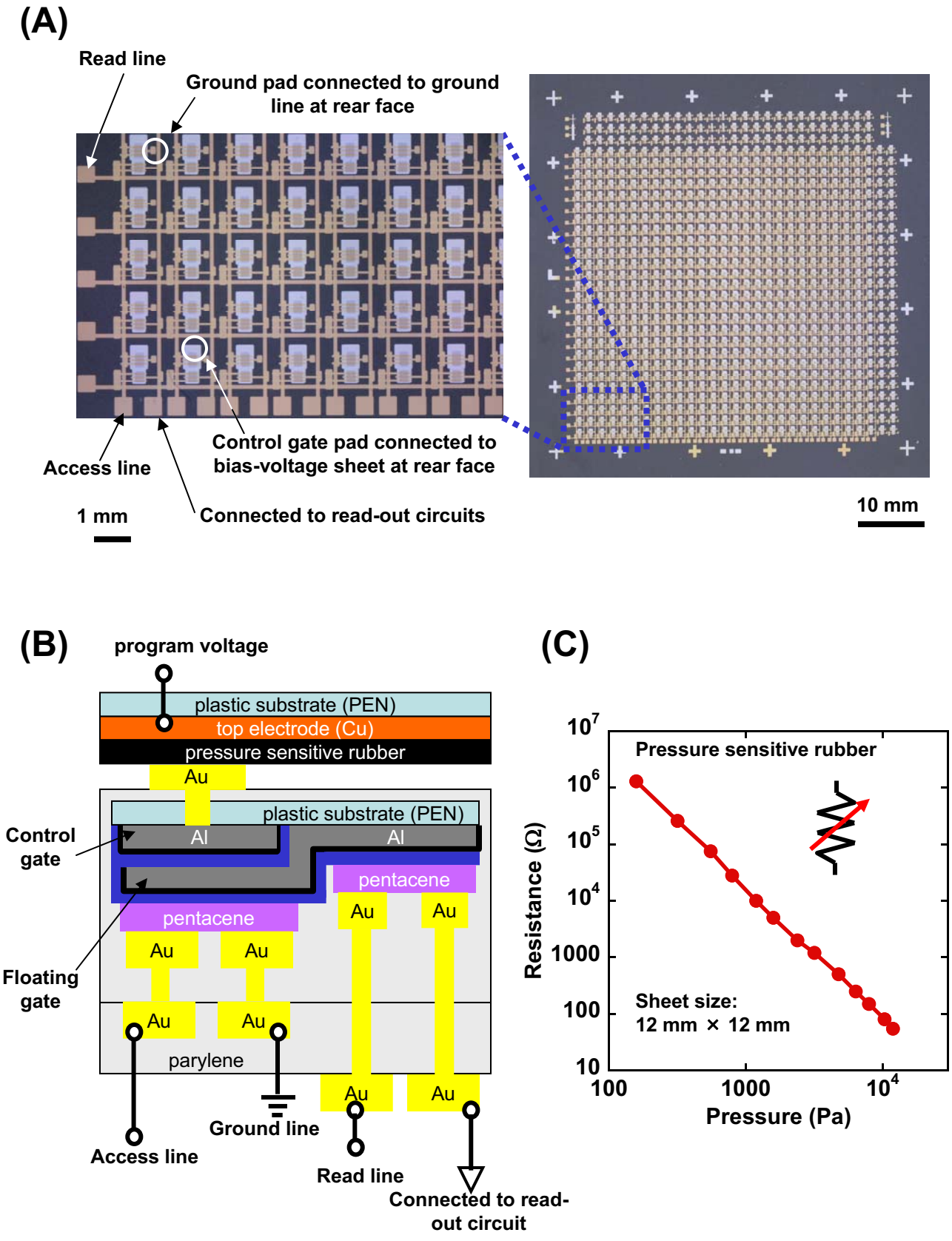

Fig. S10. Structure of the flexible pressure-sensor array.