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High-Performance Carbon Nanotube Field Effect Transistors with a Thin Gate Dielectric Based on a Self-Assembled Monolayer

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ABSTRACT

Individual single-walled carbon nanotube (SWCNT) field effect transistors (FETs) with a 2 nm thick silane-based organic self-assembled monolayer (SAM) gate dielectric have been manufactured. The FETs exhibit a unique combination of excellent device performance parameters. In particular, they operate with a gate–source voltage of only −1 V and exhibit good saturation, large transconductance, and small hysteresis (≤100 mV), as well as a very low subthreshold swing (60 mV/dec) under ambient conditions. The SAM-based gate dielectric opens the possibility of fabricating transistors operating at low voltages and constitutes a major step toward nanotube-based flexible electronics.

During the past few years, single-walled carbon nanotubes (SWCNTs) have emerged as highly promising components of nanoscale electrical devices. Among these, SWCNT-based field effect transistors (FETs) have attracted especially strong interest due to their excellent device characteristics. Three crucial factors that govern the performance of SWCNT-FETs are the chemical nature, the structural quality, and the thickness of the gate dielectric. In the most widely used configuration, a highly doped silicon substrate covered with thermally grown SiO_2 (typical thickness 100−200 nm; growth temperature >700 °C) serves as a macroscopic back-gate.[1] In order to achieve increased capacitive coupling, alternative gate dielectrics of ultrathin thickness (e.g., Al_2O_3)[2] or high dielectric permittivity (e.g., ZrO_2)[3,4] have been investigated, in some cases employing a top-gate geometry. While the corresponding FETs exhibit very high transconductance and carrier mobility, they often suffer from pronounced hysteresis in the transfer characteristic.[5] Back-gated FETs based on random SWCNT networks have recently been reported using a thin (16 nm) organic self-assembled multilayer gate dielectric.[6,7] Devices reported in that work show a greatly reduced hysteresis, but—since they are based on SWCNT networks—show inferior on/off drain current ratio and mobility. In addition, such devices display relatively large gate leakage currents.

Here we investigate individual semiconducting SWCNT-FETs that employ a simpler gate dielectric comprised of a 2 nm thick organic self-assembled monolayer (SAM) prepared in a single process step on a 4 nm thick SiO_2 layer on a silicon substrate used as a back-gate. The SiO_2 layer results from a brief oxygen plasma step required to create a sufficient density of hydroxyl groups for organic self-assembly. The SAM is based on (18-phenoxyoctadecyl)-trichlorosilane, which has been shown to be a suitable gate dielectric for the fabrication of low-voltage, high-mobility pentacene organic thin-film transistors.[8] Owing to their low formation temperature of less than 200 °C, SAM gate dielectrics are compatible with unconventional substrates such as metalized plastic foils, thereby enabling electronics on flexible substrates.[9] One important question is whether the SAM is stable under the conditions of electron-beam (e-beam) lithography, which is required for fabricating transistors with a channel length of 200 nm. To date there has only been a single report of FETs obtained through e-beam lithography on top of a SAM-based dielectric. In this pioneering work on molecular gate dielectrics, oligothiophene-based organic thin-film transistors with carboxyl group-terminated silane-based SAM dielectrics were fabricated on silicon substrates.[10] However, no systematic study of the effect of different electron doses on the structural integrity of the SAM has been performed.

The structure of our SWCNT-FET devices is apparent from Figure 1. The SAM self-assembles subsequent to a brief

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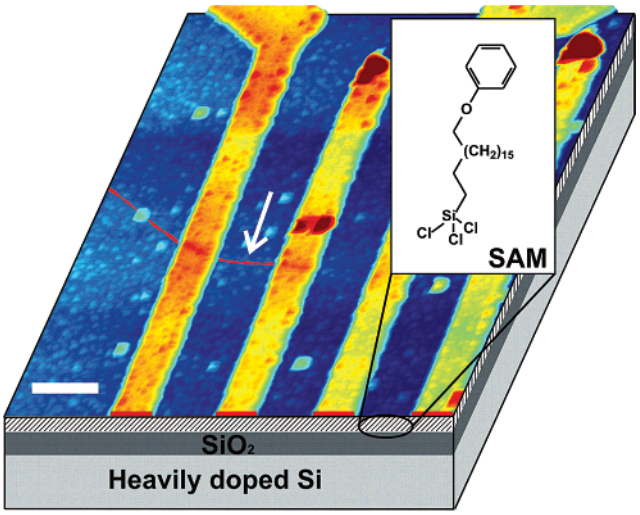

Figure 1. AFM image of the SWCNT-FET device structure. The 4 nm thin SiO_2 layer on top of the highly doped silicon wafer (light gray) is shown in dark gray. Four AuPd electrode lines are deposited onto the SAM (hatched layer) that has formed on the SiO_2 surface. A 0.3 nm layer of titanium is evaporated on top of the monolayer to enable spin coating of PMMA. The individual SWCNT in the AFM image has been colored to enhance its visibility. The scale bar is 200 nm. Inset: Chemical structure of the silane molecule used for SAM formation.

oxygen plasma treatment (0.1 mbar, 100 W, 10 s, substrate at room temperature) of a p^+-doped silicon wafer serving as the substrate and gate electrode from the vapor phase (low-pressure nitrogen atmosphere) at a temperature of 200 °C. Ellipsometry revealed that the plasma activation resulted in a ~4 nm thick SiO_2 coating of the silicon substrate. We note that plasma activation is required for high-quality molecular self-assembly in order to generate a sufficient density of functional groups at the surface. During the plasma treatment the substrate remains at room temperature which in principle opens up the possibility of implementing the devices on flexible substrates (in which case a natively oxidizing metal would be used instead of silicon). Compared with silicon dioxide formed by thermal oxidation above 700 °C (ref 11), our room-temperature plasma-grown SiO_2 is of lower quality, but as far as gate leakage and interface state density are concerned, this deficiency is compensated by the SAM which is also created at low temperature (200 °C). Although the SAM adds only ~2 nm to the total dielectric thickness (as determined by ellipsometry), it reduces the leakage current by more than 3 orders of magnitude, from 10^{-4} to 10^{-7} A/cm^2 (measured at a gate field of 2 MV/cm). For a thin (6 nm), low-temperature (200 °C), large-area dielectric this is an exceptionally small current density. The SAM-covered substrate is smooth over large areas as shown by atomic force microscopy (Figure S1, Supporting Information). Scanning tunneling microscopy studies have shown that the SAM is essentially free of pinholes.[8]

The capacitance of the dielectric stack, in which the SAM accounts for the majority of the insulating properties, has been determined by impedance spectroscopy to be 0.5 μF/cm^2. The relative permittivity of the dielectric is estimated to be about 3.3 and is determined mostly by the permittivities of the SAM and the SiO_2. Due to the strongly hydrophobic character of the SAM-modified surface, a 0.3 nm thick layer of titanium had to be evaporated onto the samples to allow spin-coating of the electron-beam resist (PMMA). The titanium does not form a closed layer as confirmed by atomic force microscopy (AFM) measurements. Due to the small thickness and fast oxidation of the titanium layer upon air exposure, it does not contribute to the electrical conduction between source and drain, as has been confirmed by electrical measurement. The contribution of the capacitance of the oxidized titanium to the total capacitance of the dielectric stack can be ignored, since titanium oxide has a very large permittivity (>50) in comparison to the SiO_2/SAM stack (adding the titanium oxide reduces the total capacitance by about 1%).

Carbon nanotubes (CNI, Houston, TX) were dispersed in an aqueous surfactant solution (1 wt % sodium dodecyl sulfate) and then purified by centrifugation and deposited on the substrate after the deposition of the 0.3 nm Ti. Source and drain contacts were then fabricated on top of the SWCNTs by e-beam lithography using a standard double-layer poly(methyl methacrylate) (PMMA) resist with a thickness of 200 nm, an electron energy of 25 keV, and an electron beam dose of 300 μC/cm^2. Electrodes with a separation of 200 nm were formed through thermal evaporation of 0.3 nm Ti/15 nm AuPd (60/40) and subsequent lift-off in acetone. Thin metal wires were carefully glue-bonded to the contact pads to establish reliable electrical connections between the device terminals and the chip carrier. The electrical measurements were carried out at room temperature in air.

In order to determine the extent to which the e-beam exposure during lithography causes structural damage of the SAM as well as to evaluate the contribution of the SAM to the insulating properties of the SiO_2/SAM-dielectric, five different types of test structures were investigated. These samples consist of a heavily doped silicon substrate covered by a thin dielectric (bare or SAM-modified 4 nm plasma-grown SiO_2, with or without 0.3 nm oxidized Ti) and a top metal contact (patterned either through an evaporation mask or by e-beam lithography). In Figure 2, the results of current−voltage ($I-V$) measurements performed on the respective samples under ambient conditions are shown. The SiO_2 dielectric without SAM has very poor insulating properties, as apparent from the substantial current density of about 10^{-4} A/cm^2 at an electric field of 2 MV/cm applied between the silicon gate and the metal contact. The leakage current does not decrease significantly upon evaporating 0.3 nm of Ti onto the 4 nm thick plasma-grown SiO_2 and allowing the Ti to oxidize prior to depositing the contact pads. The large leakage currents in the devices without SAM originate from the poor quality of plasma-grown SiO_2 as compared to high-quality SiO_2 grown by thermal oxidation.[11]

In comparison, the test structures including a SAM exhibit a significantly reduced leakage current density of less than 10^{-7} A/cm^2 at the same electric field. This confirms the crucial role of the SAM in determining the insulating properties of the dielectric stack, despite its small thickness.

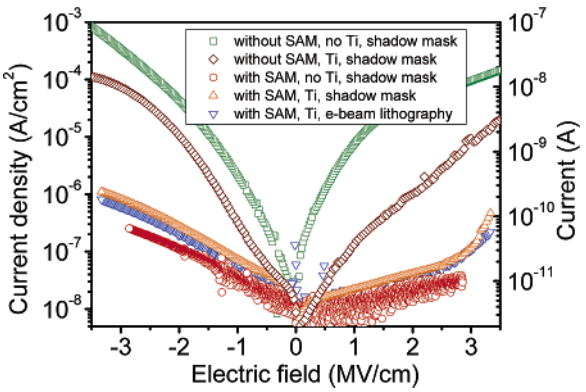

Figure 2. Current density through the gate dielectric vs bias field measured at room temperature on sandwich structures with and without the organic SAM. In the devices incorporating the SAM, the top gold contacts were patterned either by e-beam lithography or by evaporation through a shadow mask. The absolute current is displayed on the right axis.

A similar conclusion has previously been drawn for organic SAM-containing sandwich devices.[8,12,13] Comparing the SAM devices with and without a 0.3 nm thick Ti layer evaporated on top of the SAM shows an increase in leakage current by a factor of about 2 as a result of the titanium deposition. If the SAM was significantly damaged or destroyed by the Ti, as has been reported in the literature,[14] we would expect a more significant increase in leakage current. In our case however we believe that the 0.3 nm Ti oxidizes sufficiently fast (due to its very small thickness and the residual gas in our evaporator) to not inflict substantial damage on the SAM.

More intriguingly, the leakage current through the SAM dielectric is found to be virtually the same ($\sim 10^{-7}$ A/cm^2 at 2 MV/cm) regardless of whether the top metal contact is patterned by a shadow-mask technique or by electron-beam lithography, which demonstrates that the electron dose of 300 μC/cm^2 does not significantly damage the SAM. Due to its small thickness the electron absorption in the oxidized Ti can be ignored, especially since our AFM measurements suggest that the oxidized Ti does not form a closed layer. At first glance, the good stability of the SAM under e-beam exposure appears to be in contrast to literature reports of considerable damage involving bond rapture and partial desorption of molecular fragments after e-beam irradiation of thiol-based SAMs on Au substrates.[15] However, it has to be taken into account that the electron energy of 25 keV in the present study is much higher than the 10−100 eV used in case of the thiol-based monolayers. It is well-documented that higher-energy electron irradiation causes less damage in thin organic films than lower-energy irradiation.[16] This difference can be attributed to the lower stopping power of higher-energy electrons, whereby only little energy is deposited in thin films. First signs of electron-induced damage of our PMMA resist-covered SAMs, manifested by increased leakage currents ($\geq 10^{-6}$ A/cm^2), were detected for doses larger than 1800 μC/cm^2.

Building upon the excellent process stability and insulating properties of the SAM-based dielectric, we were able to obtain excellent FETs from individual semiconducting

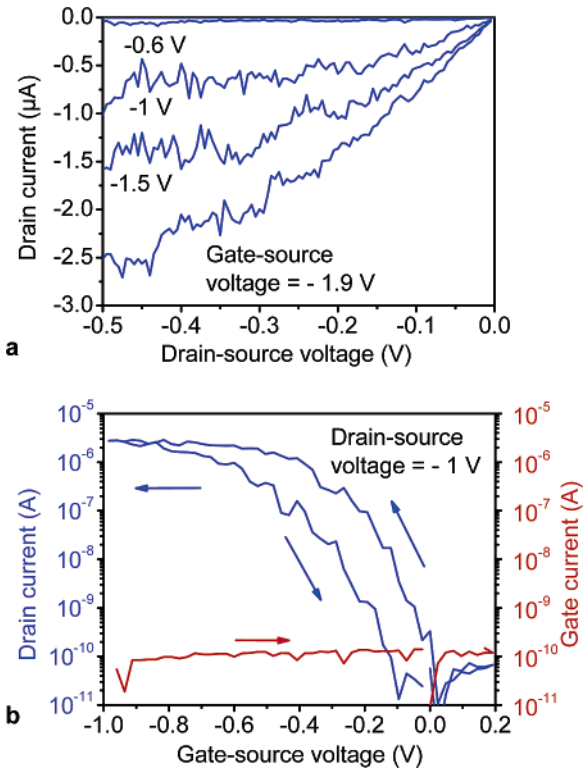

Figure 3. (a) Output characteristics of a FET device with a SAM-based gate dielectric comprising an individual semiconducting SWCNT as channel. (b) Transfer characteristics of the same device. The gate voltage sweep rate was 150 mV/s. All measurements were performed under ambient conditions. The measured gate leakage current resolution is limited by the measurement setup in this experiment. Data for the leakage current density should be taken from Figure 1 which shows measurements of the gate leakage current with a higher accuracy.

SWCNTs. The output characteristics of an exemplary device (tube diameter 1.2 nm) shown in Figure 3a display p-type behavior, a common feature of SWCNT-FETs that were not subjected to further treatment.[2,17] The drain current vs drain−source voltage characteristic resembles that of conventional p-type metal-oxide-semiconductor FETs (MOSFETs). One of these features is the saturation of the drain current at higher V_{ds}. For the present device, saturation occurs for example at a drain−source voltage of approximately −0.3 V and a gate−source voltage of −1.5 V (also see Figure 4a for a different device showing good saturation). From the transfer characteristics, shown in Figure 3b, one finds a transconductance[18] $g_m = dI_d/dV_{gs}$ of about 20 μS at $V_{ds} = -1$ V. This value is similar to the highest reported so far for SWCNT-FETs[19] and testifies to the superior gate coupling and to a large carrier field-effect mobility. The device exhibits a threshold voltage between −0.05 and −0.5 V, depending on whether the threshold voltage is estimated from the plot of the square root of the drain current versus gate−source voltage or from the plot of the drain current versus drain−source voltage. Moreover, the large on/off drain current ratio of about 10^5 (at $V_{ds} = -1$ V) is particularly remarkable in view of the small thickness of the gate dielectric and theoretical predictions on drain voltage scaling in SWCNT-FETs.[4,20−22] Finally, evaluation of the subthreshold swing $S = [dV_{gs}/d(\log$

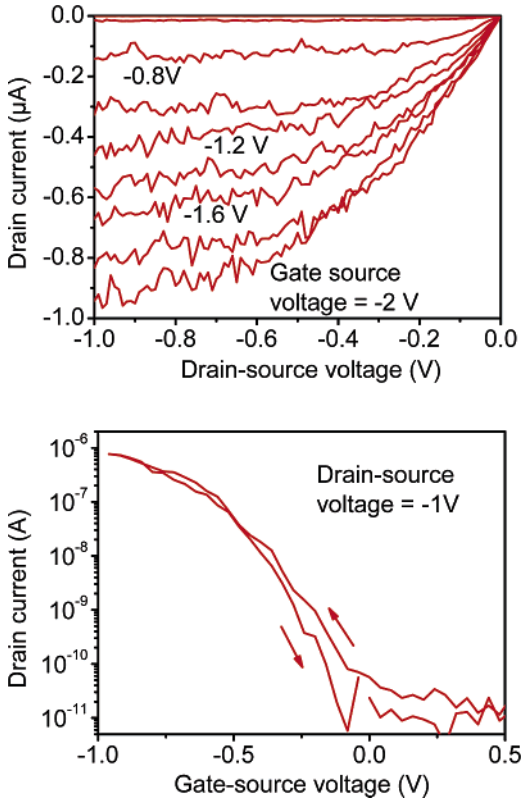

Figure 4. Output (a) and transfer (b) curve of a device at a drain−source voltage of −1 V. Negligible hysteresis is measured under ambient conditions. The gate voltage sweep rate was 210 mV/s.

I_{ds})] within the model for MOSFETs[18] yields the value of 60 mV/decade in the subthreshold region (between about 10^{-10} and 10^{-8} A), close to the theoretical limit of the subthreshold swing at room temperature.[18] Such a low value has not been previously reported for undoped Schottky-barrier SWCNT FETs with low operating voltages,[3,23−26] and its realization within the present devices is notable considering that no attempts were made to reduce the contact resistance[27] and we work with a global back-gate structure. Previous publications have reported subthreshold swings of 60−70 mV/decade for SWCNT FETs in which the channel conductance was controlled with a local gate field while the contact regions were either chemically doped[23] or electrostatically "doped" by applying a large static field from a global back-gate.[3,26] It is known, that in such devices the subthreshold swing is not limited by the gate dielectric.[26,28] In our devices the low-voltage back-gate controls the entire nanotube and the low subthreshold swing is an indication for the high quality of the gate dielectric used in this work. From the subthreshold swing the interface state density $N = (\log(e)\, q\, S/k_B T - 1)^* C/q$ of the SAM/SWCNT interface can be calculated where q is the electron charge, k_B Boltzmann's constant, T the temperature, and C the gate capacitance per area.[29] The obtained value of $N = 6 \times 10^{10}$ cm^{-2} V^{-1} is more than 1 order of magnitude lower compared to other SWCNT transistors[4,17,19,21] and underlines the high structural quality of the SAM (see Figure S2 within Supporting Information). It should be stressed, that in order to achieve a minimal subthreshold swing, both the capacitance of the gate dielectric and the interface state density have to be optimized. While in most works using high-permittivity dielectrics a large capacitive coupling is realized, the interface trap density is often high in comparison to dielectrics with lower permittivity like the one used in this work (see Figure S2 within Supporting Information). It is furthermore relevant that the device exhibits a very low gate leakage current (∼100 pA at $V_{gs} = -1$ V) that is smaller than the drain current by more than 4 orders of magnitude. This leakage current is an upper limit of the actual leakage since the minimum resolution of our measurement device in this measurement is about 100 pA. Figure 2 gives a better idea of the real leakage current through the gate dielectric.

While the electrical characteristics presented above belong to one of the best devices, we note that only a relatively small variation in performance was observed from sample to sample. In particular, all of the devices displayed saturation of the drain current in the output characteristic. The lowest transconductance and on/off ratio found among the investigated devices were 0.5 μS and 10^4, respectively, while subthreshold swings as large as 300 mV per decade were measured.

The transfer characteristics of the investigated devices (Figure 3b) disclose a hysteresis. This phenomenon is common to SWCNT-FETs. It has been ascribed to traps located within the bulk SiO_2 gate insulator or near the nanotube/SiO_2 interface, which get filled with electrons from the nanotube channel upon sweeping to more positive gate voltages.[22,30] Similar to other SWCNT-FETs, the present devices show forward-type hysteresis.[5] Its magnitude (defined as the separation between the forward and backward curves at 50% of the maximum source−drain current) depends on temperature as well as the V_{gs} sweep rate and range, whereas it is only weakly affected by V_{ds}. We find a room-temperature hysteresis of 900 mV when sweeping the gate voltage between 1.5 and −1.5 V at a rate of 7.5 mV/s. Its value decreases down to 100 mV upon increasing the sweep rate to 350 mV/s. Such a decrease in hysteresis with rising sweep rate of the gate voltage indicates the presence of trap charging on a time scale on the order of several hundreds of milliseconds. Moreover, the hysteresis experiences a significant reduction when the devices are cooled, similar to the behavior of SWCNT-FETs with a pure SiO_2 gate insulator.[30,31]

Hysteresis in SWCNT-FETs has previously been considered mostly from the viewpoint of potential memory applications.[30−32] This task still requires a better control over the hysteretic effect, although the first promising steps have already been taken in this direction, for instance via removal of the water layer from the SiO_2 gate insulator surface.[5] A prerequisite for efficient operation as a FET, by contrast, is the absence of hysteresis. In this regard, it is pertinent to note that some of our devices exhibit essentially no hysteresis even when measured under ambient conditions, i.e., with the CNT channel exposed to air (Figure 4). This result is outstanding since a vanishing hysteresis has only been achieved so far with the nanotube protected from air either by inorganic ALD dielectrics[21] or when working with a liquid

gate.[25] We attribute the small or absent hysteresis in our SWCNT-FETs to two major factors. A first contribution may arise from the low operation voltage enabled by the strong gate coupling, as has been put forward previously.[6] Second, the SAM-modified dielectric surface should adsorb only small amounts of water, despite the thin oxidized titanium layer covering the SAM.[8] This is further supported by the finding that the hysteresis of our devices is not significantly reduced upon transfer of the device into vacuum. Since water is known to enhance hysteretic behavior,[5] the predominantly hydrophobic character of the surface should help to reduce the hysteresis. To prove that really the monolayer is responsible for the reduction of a hysteresis, we fabricated devices with a 100 nm thick thermal SiO_2 gate dielectric covered by the SAM and 0.3 nm of Ti. We found the hysteresis to be between 0 and about 20% of the maximum gate voltage window. In Figure S3 (Supporting Information) such a transfer curve is compared with a device that does not have a SAM covering the thermal SiO_2. In the device with the SAM the hysteresis is significantly reduced. To evaluate the extent to which the SAM reduces the hysteresis, we compare our data taken from the work by Kim et al.[5] Since the hysteresis is known to depend on gate voltage sweep rate and the maximum applied gate field, not the absolute value of the hysteresis can be compared but it has to be set in relation to the maximum gate field and the sweep rate. When in the FET comprising the SAM-covered SiO_2 the gate field is swept at a speed of 3.8×10^4 V/(cm•s) across a gate field of $\pm 1 \times 10^6$ V/cm (± 10 V) a hysteresis of 12% of the maximum gate field window (i.e., the difference between the maximum and minimum gate field) can be observed. In Kim et al. 's work a thermally grown SiO_2 is used without any surface functionalization.[5] The gate field is for example swept at a speed of 1.1×10^5 V/(cm•s) between a maximum field of $\pm 2 \times 10^5$ V/cm (± 10 V). A hysteresis of 38% of the maximum gate field window was observed. In comparison with our results it can be seen that even when a device with SAM is swept across a larger gate electric field at a low sweep speed the hysteresis in the drain current is still lower than in devices that do not include the SAM. It has to be noted that the hysteresis is known to increase when the gate voltage sweep rate is increased and the maximum of the applied gate voltage is increased.

In summary, we have demonstrated that the integration of a high-quality gate dielectric based on an organic self-assembled monolayer into nanotube-based electronic devices permits strong gate coupling. The high stability of the SAM against electron exposure during electron-beam lithography has enabled the fabrication of field-effect transistors with a channel length of 200 nm from individual semiconducting SWCNTs. Back-gated SWCNT-FETs obtained in this manner not only exhibit an unprecedented combination of excellent performance parameters but also approach the room-temperature limit of 60 mV/dec for the subthreshold swing which is a key performance parameter of FETs. It is equally important to stress that the low temperature used for incorporating the organic SAM makes the fabrication process compatible with flexible polymeric substrates.

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Supporting Information Available: An AFM image of a SAM-covered silicon substrate; a comparison between literature data of the interface state density of SWCNT FETs with different gate insulator materials and the data obtained in this work; transfer curves of SWCNT FETs with a 100 nm thick thermally grown SiO_2 gate dielectric with and without a silane SAM covering the oxide layer.

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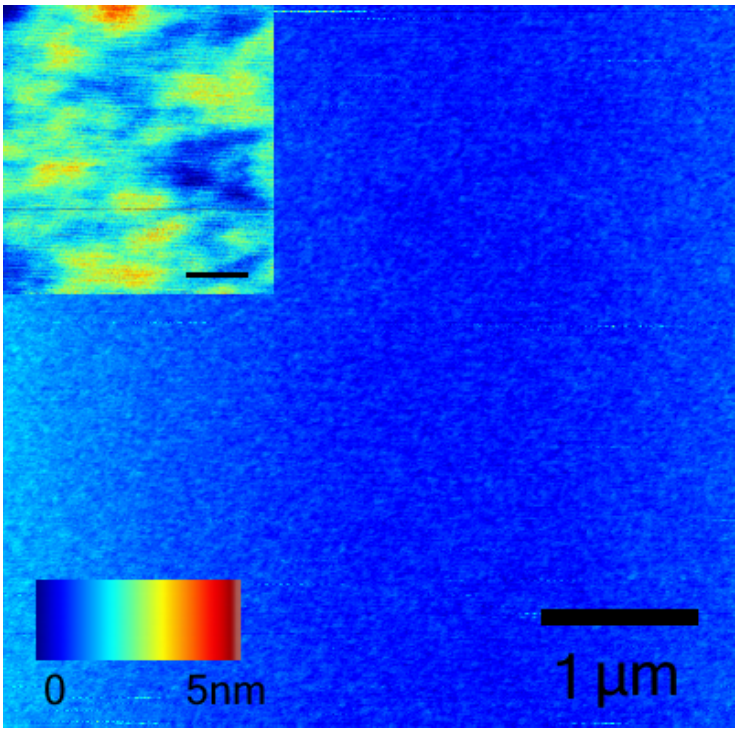

Figure S1 Tapping-mode atomic force microscopy (AFM) image of the silicon substrate covered by the SAM. The layer is very smooth and pinhole free across large areas. **Inset** Zoom. The scale bar here is 20 nm, and the colour scale ranges from 0 to 0.5 nm.

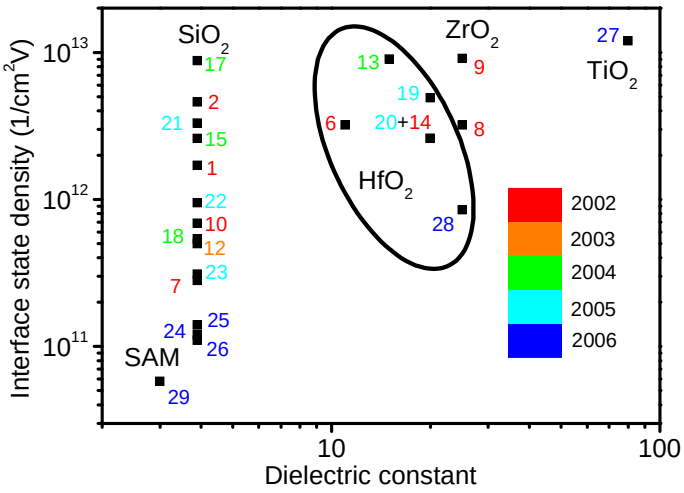

Figure S2 Comparison of the interface state density of gate insulator materials with different dielectric constants. The interface state density N was calculated from the subthreshold swing S at room temperature and the capacitance per unit area C of the gate dielectric by the formula $N = (\log(e)*q*S/k_BT-1)*C/q$ with q as the electron charge, k_B Boltzmann's constant and T as the temperature. The color scale indicates the respective year of the publication. It can be clearly observed that for materials of lower dielectric constant the interface state density is also lower. Furthermore a trend towards a lower interface state density over the years due to higher quality dielectrics is visible.

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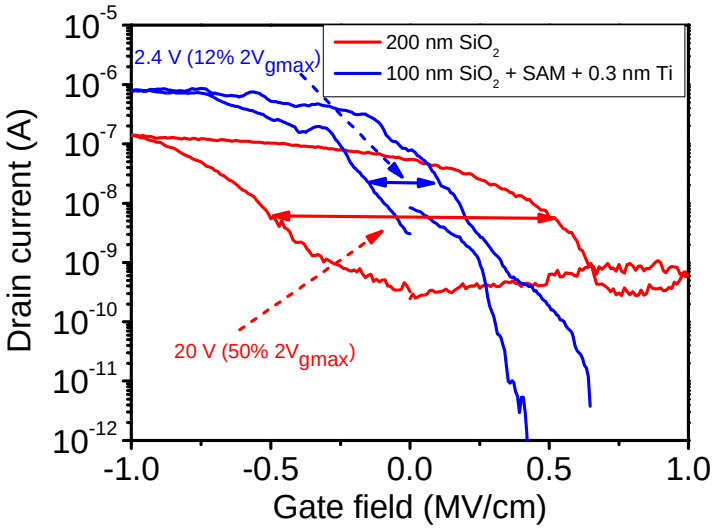

Figure S3 Transfer curve of two devices: In red a SWCNT FET with a 200 nm SiO_2 dielectric. In blue a SWCNT FET with a 100 nm SiO_2 and a SAM on top. The hysteresis in this case is only 12% of the gate voltage window (determined by the difference between the minimum and maximum gate voltage) at a gate voltage sweep rate of 0.38 V/s (3.8 x 10^4 V/cm s).