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Top-Gate ZnO Nanowire Transistors and Integrated Circuits with Ultrathin Self-Assembled Monolayer Gate Dielectric

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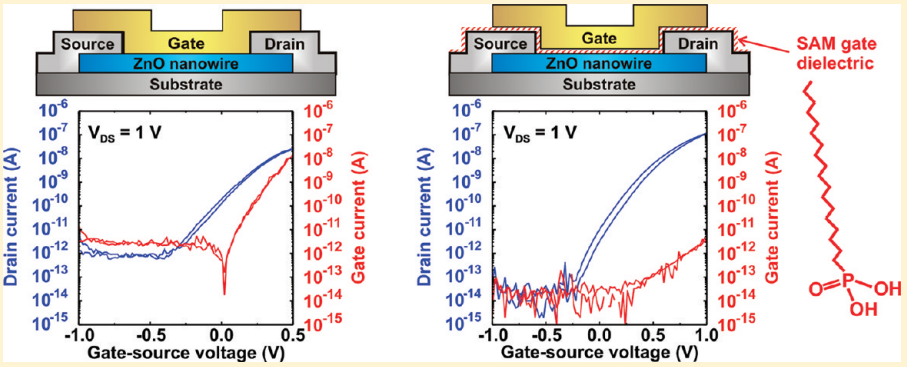
Supporting Information

ABSTRACT:



A novel approach for the fabrication of transistors and circuits based on individual single-crystalline ZnO nanowires synthesized by a low-temperature hydrothermal method is reported. The gate dielectric of these transistors is a self-assembled monolayer that has a thickness of 2 nm and efficiently isolates the ZnO nanowire from the top-gate electrodes. Inverters fabricated on a single ZnO nanowire operate with frequencies up to 1 MHz. Compared with metal−semiconductor field-effect transistors, in which the isolation of the gate electrode from the carrier channel relies solely on the depletion layer in the semiconductor, the self-assembled monolayer dielectric leads to a reduction of the gate current by more than 3 orders of magnitude.

KEYWORDS: Wet-chemical synthesis, zinc oxide, nanowire transistor, self-assembled monolayer dielectric, integrated circuit

Semiconductor nanowires represent the preferred device geometry for next-generation, aggressively scaled metal−oxide−semiconductor field-effect transistors (MOSFET) in silicon CMOS integrated circuit technology.[1,2] In addition, single-crystal semiconductor nanowires are also useful to realize high-performance field-effect transistors on unconventional substrates, such as glass, plastics, and paper.[3−5] The synthesis of single-crystalline nanowires often requires high temperatures, but the nanowires can usually be synthesized on a temperature-compatible growth substrate and then be transferred to the target substrate for FET assembly. If the temperature during FET manufacturing is below ∼150 °C, high-mobility nanoscale FETs can therefore be realized on polymeric substrates for flexible active-matrix displays or integrated circuits.

Semiconductors that have shown potential for nanowire FETs include Si,[1,2,6] In_2O_3,[5,7] GaN,[8] CdS,[9,10] and ZnO.[11−13] Among these, ZnO is of particular interest, because it is a nontoxic, environmentally friendly material and because ZnO nanowires can be synthesized in large quantities by low-cost, wet-chemical growth methods[14] on a variety of substrates, including commercially available zinc foil.[15]

The realization of more than one transistor on a single nanowire requires local gating. In general, local gate electrodes can be realized in a bottom-gate[5,16] or a top-gate geometry.[13,17] For FETs based on nanowires, the top-gate geometry is preferable, since a top-gate electrode can wrap around the nanowire circumference and hence enable a more efficient control of the channel conduction.[18] The realization of a top-gate geometry requires a gate dielectric that can be grown or deposited on the nanowire surface.[10] This gate dielectric should provide conformal coverage of the nanowire surface with low defect density and ideally provide a large capacitance per unit area, so that the transistors can be operated at low voltages. For this purpose, we have developed a very thin gate dielectric that consists of a single monolayer of

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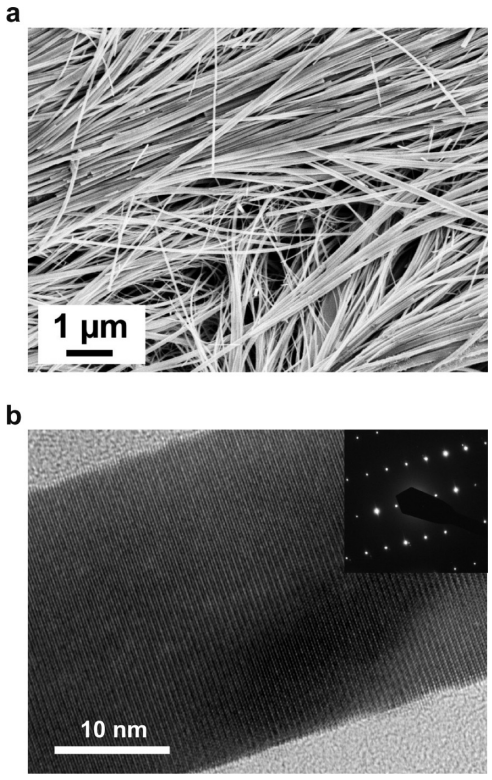

Figure 1. Electron microscopy images of hydrothermally grown ZnO nanowires. (a) Scanning electron microscopy image of a dense carpet of ZnO nanowires covering the surface of a piece of zinc foil after hydrothermal nanowire growth. The ZnO nanowires are as long as several tens of micrometers and have diameters ranging from 20 nm up to several hundred nanometers. (b) Transmission electron microscopy image of a wet-chemically grown ZnO nanowire. The inset confirms the single-crystalline structure of the ZnO nanowires with lattice constants of a = 0.322 nm and c = 0.526 nm.

alkylphosphonic acid molecules that self-assemble spontaneously in solution at room temperature on the nanowire surface.

We report on the synthesis of single-crystalline ZnO nanowires by hydrothermal growth on zinc foil, on the reduction of the intrinsic conductivity of the as-grown ZnO nanowires by thermal annealing, and on the static and dynamic performance of low-voltage top-gate field-effect transistors and circuits fabricated on a single ZnO nanowire. These transistors and circuits can in principle be fabricated on flexible polymeric substrates, because the high-temperature anneal (600 °C) that is required to reduce the conductivity of the as-grown nanowires can be performed prior to dispersing the nanowires on the device substrate, and the maximum temperature during the fabrication of the transistors and circuits is well below the glass transition temperature of plastic substrates.

ZnO nanowires are synthesized on commercially available zinc foil, using the hydrothermal method reported by Lu et al.[15] A Teflon beaker is filled with an aqueous solution of sodium hydroxide (0.48 mol/L) and ammonium persulfate (0.095 mol/L), and a 1 × 1 cm^2 piece of 250 μm thick zinc foil is placed at the bottom. The beaker is placed in a stainless-steel autoclave and heated to 150 °C. After 48 h the zinc foil is removed and rinsed several times with deionized water. Figure 1a shows that a large density of ZnO nanowires, many of them several tens of micrometers long, with diameters between 20 and 200 nm are obtained by this method. The aspect ratio of the nanowires can be as large as 500. The nanowires are harvested by a short sonication in 2-propanol. Transmission electron microscopy (TEM) analysis (Figure 1b) confirms the single-crystalline structure, the hexagonal lattice reconstruction, and the c-axis orientation of the wet chemically grown ZnO nanowires.

To determine the electrical properties of the as-grown ZnO nanowires, about 5 μL of the ZnO nanowire suspension is dropped onto a heavily doped, thermally oxidized silicon substrate. To obtain a homogeneous distribution of the nanowires on the substrate surface, the substrate is briefly heated to 130 °C during the deposition.[19] Dark-field optical microscopy images are used to locate the nanowires on the substrate with respect to an array of unique alignment markers. A pair of aluminum source and drain contacts that overlap the nanowire surface is then fabricated for each nanowire by electron-beam lithography, vacuum evaporation of 80 nm thick aluminum, and lift-off in *N*-methyl-2-pyrrolidone (NMP). Immediately prior to the evaporation of the aluminum contacts, the contact areas are briefly exposed to an argon plasma (reactive ion etching, 30 sccm Ar, 15 mTorr, 100 W, 20 s). This step is performed to clean the surface of the ZnO nanowires in the contact areas prior to metal deposition.

Before fabricating top-gate ZnO nanowire FETs, we were interested in the electrical properties of the wet-chemically grown nanowires. Using the doped silicon substrate as a gate electrode and the 200 nm thick silicon dioxide (SiO_2) as the gate dielectric, the electric current through the ZnO nanowire is measured as a function of the gate-source voltage in a bottom-gate field-effect transistor configuration. All electrical measurements are performed in ambient air, using an Agilent 4156C parameter analyzer. Panels a, b and c of Figure 2 show an atomic force microscopy image and the transfer and output characteristics of a bottom-gate FET based on an as-grown ZnO nanowire, with a diameter of about 50 nm. The channel length defined by electron-beam lithography is 3 μm. As can be seen, the as-grown nanowire has a large electrical conductivity (10^3 S/m) that shows almost no dependence on the electric field from the silicon back gate. The large conductivity of the as-grown wires is believed to be due to a high density of dopants that are unintentionally incorporated into the ZnO lattice during hydrothermal growth. To make the nanowires useful for FETs, the charge-carrier density must be dramatically reduced. This is achieved by annealing the nanowires in a quartz-tube furnace in ambient air. (To avoid oxidation of the aluminum source and drain contacts during annealing, the anneal is always performed prior to the fabrication of the contacts.) Figure 2d shows the transfer characteristics of three back-gate FETs based on ZnO nanowires annealed at temperatures of 200, 400, and 600 °C. As can be seen, the temperature of 600 °C is sufficient to cause a dramatic reduction in the doping density and off-state conductivity of the nanowires and a dramatic increase in the gate-field dependence of the drain current. For ZnO, n-type doping is easily achieved by incorporation of extrinsic dopants, such as Al, Ga,[20] and In[21] on a zinc lattice site. Furthermore, intrinsic defects (like zinc interstitials and oxygen vacancies[22]) as well as hydrogen have been discussed as possible sources of unintentional n-type doping in ZnO. Hydrogen can act as a donor in ZnO when it is incorporated on an interstitial lattice site (H_i) or on an oxygen vacancy (H_O).[23] The observed strong reduction of the doping concentration in the temperature range of 400−600 °C coincides with theoretical calculations of the outdiffusion temperature of H_O from the ZnO lattice.[24] This observation therefore indicates that H_O might be

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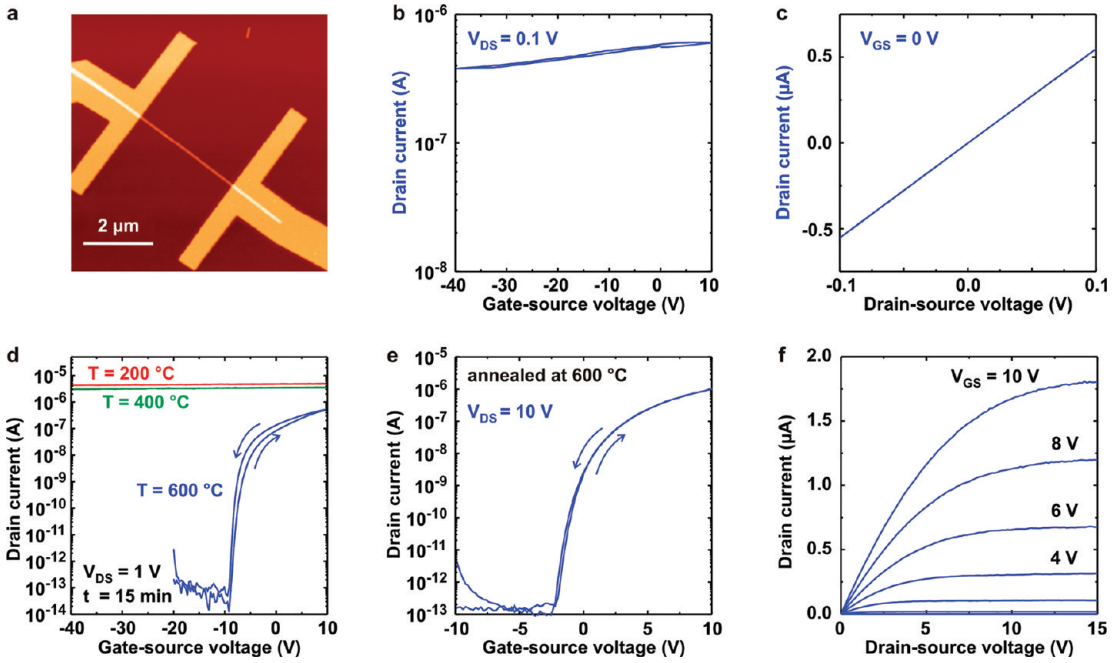

Figure 2. Electrical characteristics of ZnO nanowire FETs in the global back-gate configuration. (a) Atomic force microscopy image, (b) transfer characteristics, and (c) output characteristics of an as-grown ZnO nanowire with Al source and drain contacts. The nanowire has a large conductivity, which makes it difficult to modulate the drain current with the electric field from the back gate. (d) Transfer characteristics of three ZnO nanowire FETs based on nanowires annealed at 200 °C (red), 400 °C (green), and 600 °C (blue) for a drain−source voltage V_{DS} = 1 V. All annealing steps were performed in ambient air for 15 min. In the temperature range between 400 and 600 °C, most of the unintentional incorporated dopants are passivated and a dramatic increase in the gate dependence is observed. (e) Transfer and (f) output characteristics of a ZnO nanowire FET based on a nanowire annealed at 600 °C in air for 15 min (L = 5 μm, d = 45 nm). At V_{DS} = 10 V the FET shows an on/off current ratio of 10^7 and a maximum transconductance of 0.2 μS. The calculated field-effect mobility is 40 $cm^2/(V\ s)$.

the cause for the large conductivity of the as-grown ZnO nanowires. However, since the source materials for the hydrothermal synthesis are only about 98% pure, it is also possible that large amounts of extrinsic dopants (like Al) are unintentionally incorporated during the hydrothermal growth, and doping by these contaminants cannot be ruled out. Panels e and f of Figure 2 show the transfer and output characteristics of a back-gate FET based on a ZnO nanowire annealed at 600 °C. The FET has an on/off current ratio of 10^7, a transconductance of 0.2 μS, and a subthreshold swing of 0.4 V/decade. The field-effect mobility is 40 $cm^2/(V\ s)$. (The formalism used to calculate this mobility is explained in the Supporting Information.)

To fabricate FETs and integrated circuits based on individual ZnO nanowires, the back-gate FET process described in the previous two paragraphs is not suitable, since the global back-gate does not allow the nanowires to be addressed individually. Therefore we have developed the top-gate transistor process outlined in Figure 3a. In the first step, aluminum source and drain contacts are defined on the randomly dispersed and annealed ZnO nanowires by electron-beam lithography, argon plasma cleaning of the nanowire surface, aluminum evaporation (80 nm thick), and lift-off; this step is similar to the fabrication of the back-gate FETs. In preparation for the self-assembly of the alkylphosphonic acid monolayer gate dielectric, the ZnO nanowire and the aluminum source and drain contacts are briefly exposed to a low-power oxygen plasma (reactive ion etching, 30 sccm O_2, 10 mTorr, 50 W, 20 s). The oxygen plasma increases the density of hydroxyl groups on the surface of the ZnO nanowires and on the surface of the aluminum source and drain contacts, which is beneficial for the formation of a high-quality alkylphosphonic acid self-assembled monolayer.[25,26] Immediately after the oxygen plasma treatment, the substrate is immersed in a 2-propanol solution of 1 mmol of octadecylphosphonic acid. The molecules (Figure 3a) adsorb on the hydroxyl-terminated ZnO and aluminum surfaces and form a densely packed self-assembled monolayer (SAM). This monolayer has a thickness of approximately 2 nm[25] and serves as the gate dielectric of the top-gate nanowire FETs. Finally, gold gate electrodes are fabricated on top of the SAM gate dielectric by electron-beam lithography, gold evaporation (80 nm thick), and lift-off. A scanning electron microscopy (SEM) image of a top-gate ZnO nanowire FET with a channel length of 1 μm is shown in Figure 3b. Because the SAM gate dielectric covers not only the ZnO nanowire but also the plasma-oxidized aluminum, the gold gate electrode is allowed to overlap the source and drain contacts by about 100 nm. This small overlap is advantageous because it allows the top gate to control the entire channel from source to drain without the need of additional back-gating, as is necessary for accumulation-mode FETs with nonoverlapping gate electrodes.[27,28] The cross-sectional TEM image shown in Figure 3c indicates that the gold top-gate covers three of the six facets of the circumference of the ZnO nanowire. The maximum temperature during the top-gate fabrication process is 160 °C, which is necessary to bake the resist for the electron-beam lithography. Therefore it is possible to realize these top-gate FETs not only on silicon or glass substrates but also on flexible plastic substrates (see Figure S1 in the Supporting Information for the characteristics of a top-gate ZnO nanowire FET fabricated on a flexible poly(ethylene naphthalate) (PEN) substrate).

Figure 4 shows the transfer and output characteristics of a top-gate FET with a channel length of 2 μm based on a ZnO

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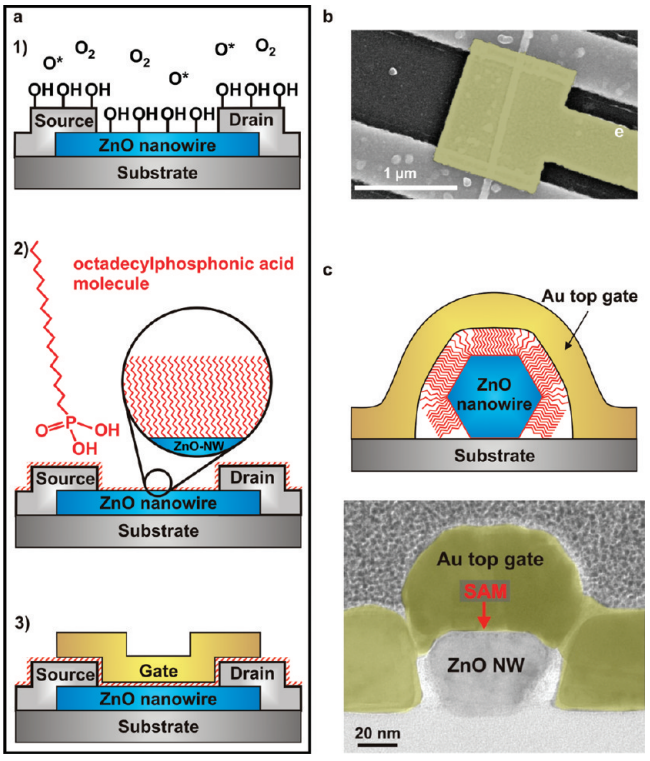

Figure 3. Fabrication and imaging of top-gate ZnO nanowire FETs. (a) Fabrication process. (1) A ZnO nanowire with aluminum source and drain contacts defined by electron beam lithography (EBL) is exposed to a soft oxygen-plasma treatment (30 sccm O_2, 10 mTorr, 50 W, 30 s). The procedure removes organic adsorbents from the surface and increases the density of hydroxyl groups on the contact and nanowire surfaces. (2) The formation of the self-assembled monolayer (SAM) gate dielectric is performed from a solution of 2-propanol containing 1 mmol of octadecylphosphonic acid. The insulating SAM readily assembles on the surfaces of the aluminum source and drain contacts and the ZnO nanowire. (3) Patterning of the top-gate electrode is performed by EBL, evaporation of gold, and lift-off of excess metal. (b) SEM image of a top-gated ZnO nanowire FET with a channel length of 1 μm. The overlap between the top-gate electrode and the source and drain contacts is around 100 nm. (c) Schematic cross section and transmission electron microscopy image of the channel region of a top-gate ZnO nanowire FET. The gold top-gate electrode covers three of the six facets of the SAM-covered hexagonal ZnO nanowire.

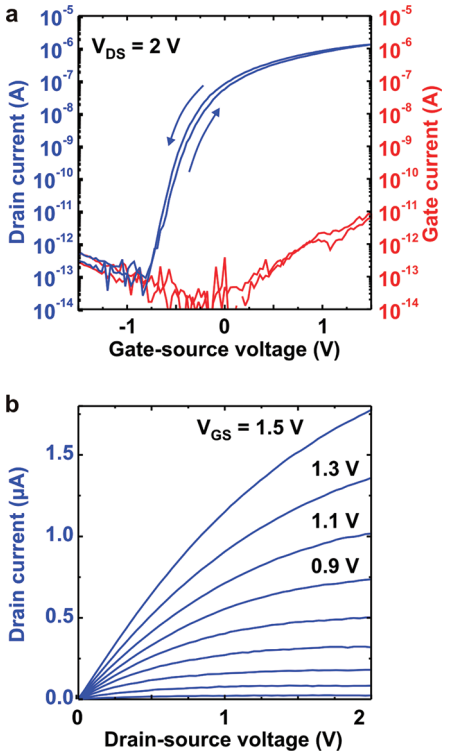

Figure 4. Transfer and output characteristics of a top-gate ZnO nanowire FET. (a) Drain current (blue) and gate current (red) as a function of the gate−source voltage at a drain−source voltage V_{DS} = 2 V. The transistor has an on/off current ratio of 10^7, a transconductance of 1 μS, and a steep subthreshold swing of 90 mV/decade. Due to the small thickness of the SAM gate dielectric, the transistor can be operated with low voltages. (b) Output characteristics of the transistor.

nanowire with a diameter of 40 nm, fabricated on a Si/SiO_2 substrate. The small thickness of the SAM gate dielectric (2 nm) makes it possible to operate the transistor with low gate-source voltages of around 1 V. The transistor has an on/off ratio of 10^7, a subthreshold swing of 90 mV/decade and a transconductance of 1 μS. The gate current is below 10 pA, even at the maximum gate-source voltage of 1.5 V. Given the small thickness of the SAM gate dielectric and the importance of minimizing the gate current, a further investigation of the contributions to the gate current and of the role of the SAM on the FET characteristics is appropriate.

The two contributions to the gate current are the overlap between the gate electrode and the source and drain contacts and the overlap between the gate electrode and the ZnO nanowire. In those regions where the gate electrode overlaps the source and drain contacts, the dielectric is a stack of ~3 nm thick AlO_x[25] and about 2 nm thick alkylphosphonic acid SAM. In those areas were the gate electrode overlaps the ZnO nanowire, the gate dielectric is only the alkylphosphonic acid SAM. On the basis of the fact that the overlap area between the gate electrode and the source and drain contacts is very small (10^{-9} cm^2) and the fact that the current density through the AlO_x/SAM dielectric is less than 10^{-5} A/cm^2 at 1 V[25] the absolute current flowing between the gate electrode and the source and drain contacts is expected to be no more than 10 fA. Therefore its contribution to the total gate current can be safely neglected, and in the following we will focus on the overlap between the gate electrode and the ZnO nanowire.

The different work functions of the gold gate electrode (5.1 eV) and the ZnO (~4.2 eV for n-type ZnO) lead to the formation of a Schottky barrier along the channel, and therefore to a depletion of the ZnO nanowire. In principal, FETs can be implemented in the form of a metal−semiconductor FET (MESFET) or in the form of a metal−insulator−semiconductor FET (MISFET, with the MOSFET being a special case). In a MESFET the density of free charge carriers and therefore the conductivity of the semiconductor is modulated via the depletion width of the Schottky contact between the metal gate electrode and the semiconductor.[9,29] This implies that the alkylphosphonic acid SAM gate dielectric is not strictly necessary for transistor operation. If the SAM dielectric was omitted, it would still be possible to operate the device as a MESFET. However, a substantial drawback of the MESFET approach is that the maximum drain current and the transconductance are limited by the intrinsic doping level of the semiconductor and the built-in potential barrier between the metal gate and the semiconductor.[30] In contrast, in a MISFET the presence of a gate dielectric allows the

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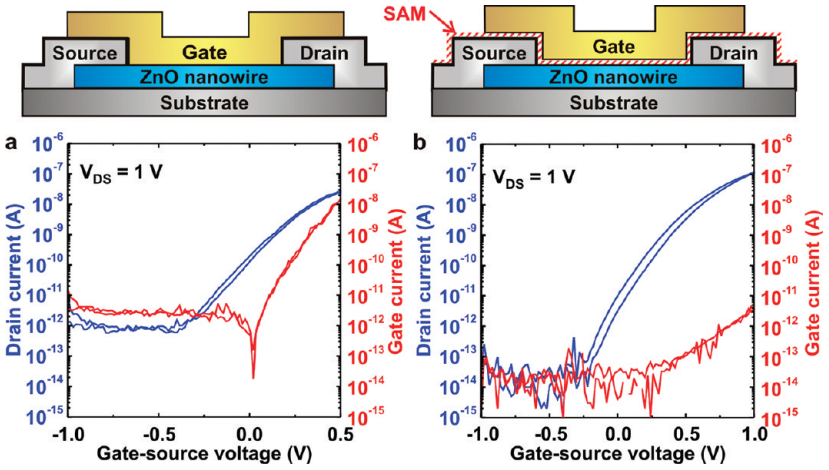

Figure 5. Comparison between the transfer characteristics of a ZnO nanowire FET without SAM gate dielectric (MESFET) and one with SAM gate dielectric (MISFET). (a) Drain and gate current of a ZnO nanowire FET without SAM gate dielectric. The gate-bias dependence of the gate current displays the characteristics of a Schottky diode. For negative gate bias a constant saturation current of I_S = 5 pA is measured. For positive gate bias the gate current increases exponentially and is approaching the drain current. This shows the device is working as a metal−semiconductor field-effect transistor (MESFET). (b) Drain and gate current of a ZnO nanowire FET with SAM gate dielectric. The gate current is near the resolution limit over nearly the entire gate-bias range. For positive gate bias V_{GS} > 0.5 V the gate current shows a slight increase, but not as pronounced as for the MESFET. Both devices shown have the same channel length of L = 1.5 μm.

gate-controlled accumulation of excess carriers, and therefore potentially much larger drain current and transconductance.

To understand the influence of the SAM gate dielectric on the transistor characteristics, we specifically compared ZnO nanowire devices with a gold top-gate electrode and either without SAM gate dielectric (MESFET) or with a SAM gate dielectric (MISFET). Panels a and b of Figures 5 show the transfer characteristic of a MESFET (without SAM gate dielectric) and of a MISFET (with SAM gate dielectric), respectively. Both FETs have a channel length of L = 1.5 μm. As expected, the gate current of the MESFET shows the characteristic Schottky-diode behavior. For negative gate voltages, the Schottky barrier between the gold gate electrode and the ZnO nanowire is biased in reverse direction and hence the gate current corresponds to the voltage-independent saturation current of the Schottky junction (5 pA). Positive gate−source voltages result in an exponential increase of the gate current due to increasing current across the built-in Schottky barrier. At V_{GS}= 0.5 V the gate current reaches the drain current, which makes FET operation impractical for gate−source voltages beyond 0.5 V. In comparison to the MESFET, the gate current in the MISFET (Figure 5b) is smaller by several orders of magnitude, both for negative and especially for positive gate−source voltages. For V_{GS} < 0.5 V the gate current is near the resolution limit of the measurement system (0.1 pA). For V_{GS} > 0.5 V the gate current increases approximately exponentially with gate−source voltage, but the slope is significantly smaller than in the MESFET. A statistical analysis of the gate currents of 25 MISFETs fabricated on four different substrates and 16 MESFETs on two different substrates is included in the Supporting Information. This comparison of the gate currents in a MESFET and a MISFET demonstrates the pronounced insulating properties of the octadecylphosphonic acid SAM on the ZnO nanowires. An important benefit of the SAM gate dielectric is that the MISFETs can be operated with substantially larger positive gate−source voltages and thus provide larger drain currents and larger transconductance than the MESFETs.

Many of the wet-chemically grown ZnO nanowires are sufficiently long to allow more than one FET, and hence simple integrated circuits, to be fabricated on a single nanowire. In order to eliminate the parasitic capacitance from the conducting substrate, the circuits are fabricated on glass substrates, rather than on silicon substrates. Panels a and b of Figure 6 show the circuit schematic, an SEM image and the static transfer characteristics of an inverter with a saturated load realized on a single ZnO nanowire. The nanowire has a length of 12 μm. The drive FET has a channel length of 1 μm, and the load FET has a channel length of 4 μm. The dynamic response of the inverter to a square wave input signal at a frequency of 1 MHz is shown in Figure 6c. To the best of our knowledge this is the highest switching frequency reported for an FET based on an individual metal oxide nanowire.

Since our ZnO nanowire FETs usually have a negative threshold voltage, the inverter requires a slightly negative input voltage in order to switch the output to the logic "1" state. However, since the output only produces positive potentials, these inverters cannot be cascaded. To allow cascading and obtain larger small-signal gain, we have also designed and fabricated inverters with an integrated level-shift stage on a single ZnO nanowire. These inverters consist of four top-gate FETs with a channel length of 1.5 μm and a gate-to-contact overlap of 100 nm, all of which were fabricated on a ZnO nanowire with a diameter of 60 nm. Figure 7 shows the circuit schematic, an SEM image, and the static transfer characteristics of such an inverter. The additional supply voltages V_{SS} and V_{GG} are chosen to produce a symmetric transfer curve with matching input and output potentials. This inverter has a small-signal gain of 12. The matching input and output levels of the inverters with integrated level-shift stage allow cascading of several inverters, as shown in Figure 7b. Cascading two inverters produces a maximum small-signal gain of 35 and a large-signal gain of 9.

In conclusion, we have fabricated field-effect transistors and integrated circuits based on individual single-crystalline ZnO nanowires with diameters around 50 nm synthesized by a

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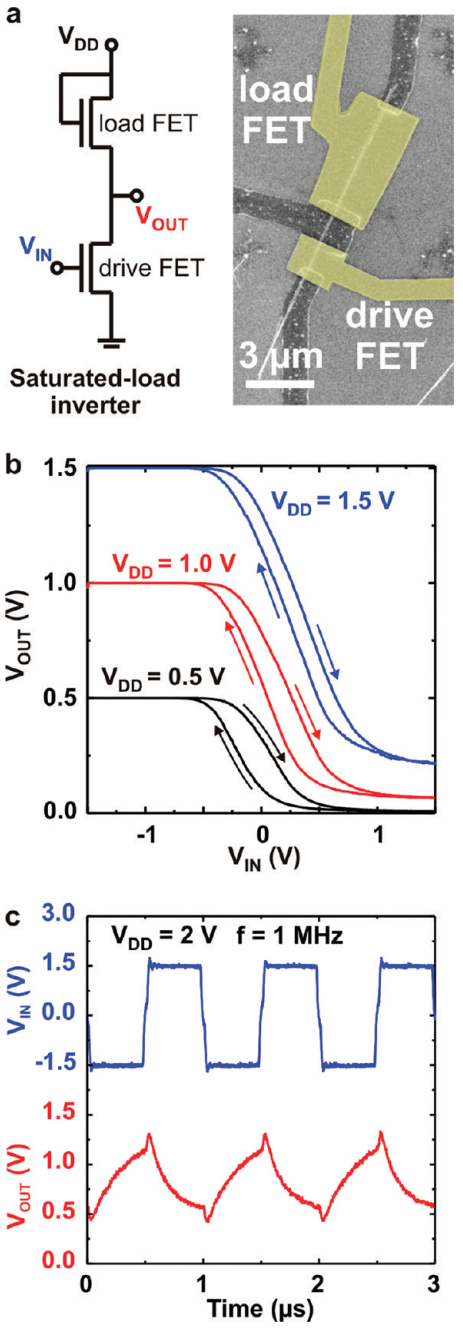

Figure 6. Static and dynamic characteristics of an inverter with saturated load realized on a single ZnO nanowire. (a) Circuit schematic and SEM image of an inverter with saturated load realized on a single ZnO nanowire having a length of 12 μm (L_{Load} = 4 μm, L_{Drive} = 1 μm). (b) Static transfer characteristics of a saturated-load inverter for three different supply voltages (V_{DD}). (c) Input and output characteristics of a ZnO nanowire inverter with saturated load fabricated on a glass substrate, operated at a frequency of 1 MHz (V_{DD} = 2 V).

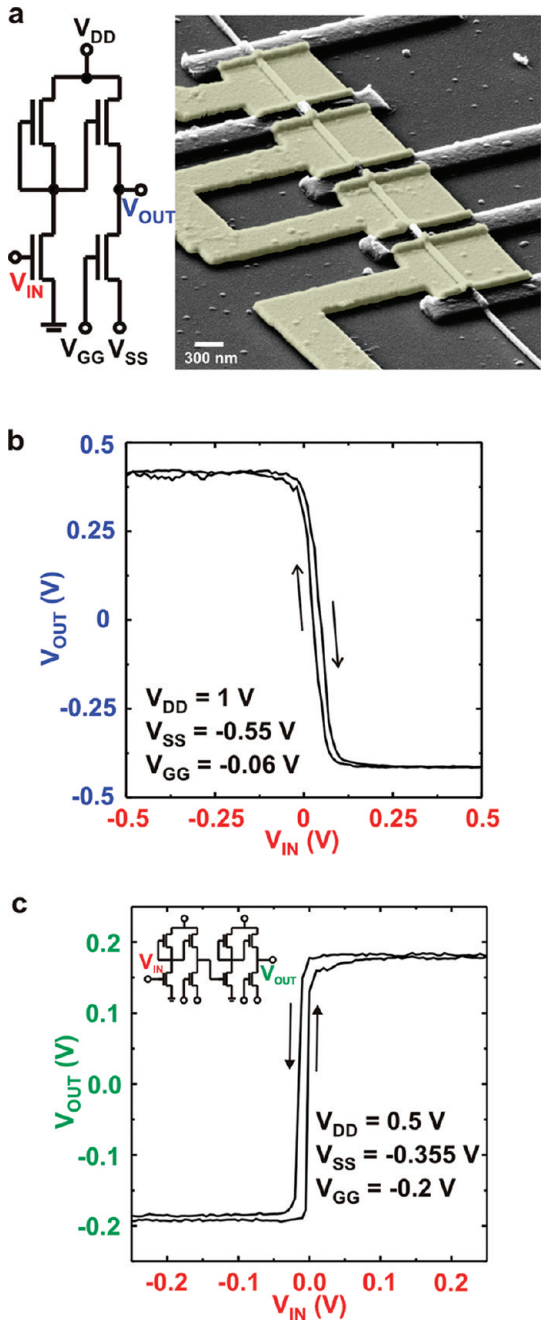

Figure 7. ZnO nanowire inverters with integrated level-shift stage. (a) Circuit schematic and tilted SEM image of an inverter with integrated level-shift stage. Four top-gate FETs are realized on a 12 μm long ZnO nanowire. The channel length of each FET is L = 1.5 μm. (b) Static transfer characteristics of an inverter with integrated level-shift stage. Due to the additional supply voltages V_{SS} and V_{GG}, the input and output voltage levels of the inverter are matching. (c) Static transfer characteristics of a cascade of two ZnO nanowire inverters with integrated level-shift stage. The inset shows the circuit schematic. This experiment confirms that the inverters with level shifting can be successfully cascaded.

low-temperature hydrothermal growth method. The transistors employ aluminum source and drain contacts, a molecular self-assembled monolayer gate dielectric with a thickness of 2 nm, and thermally evaporated gold top-gate electrodes. Compared with transistors without SAM gate dielectric (MESFETs), the SAM reduces the gate current by about 3 orders of magnitude. The transistors have an on/off current ratio of 10^7, a subthreshold swing of 90 mV/decade, and a transconductance of 1 μS. Inverter circuits fabricated on a single ZnO nanowire operate at frequencies as high as 1 MHz.

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■ ASSOCIATED CONTENT

Supporting Information. Calculation of the field-effect mobility of ZnO nanowire FETs on a global back gate, top-gate ZnO nanowire transistors with SAM gate dielectric on a plastic substrate, and statistical analysis of the gate currents of top-gate ZnO nanowire MESFETs and MISFETs. This material is available free of charge via the Internet at http://pubs.acs.org.

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Supporting Information

Top-Gate ZnO-Nanowire Transistors and Integrated Circuits with Ultrathin Self-Assembled Monolayer Gate Dielectric

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1. Calculating the field-effect mobility of ZnO-nanowire FETs on a global back gate

For large positive gate-source voltages, the ZnO-nanowire FETs operate in the accumulation regime. Therefore, the field-effect mobility is calculated according to the equations of the charge-sheet approximation [S1]. The field-effect mobility in the linear regime is given by

$$\mu_{lin} = \frac{g_m \cdot L^2}{C \cdot V_{DS}} \quad (1)$$

and in the saturation regime by

$$\mu_{sat} = \frac{2 \cdot L^2}{C} \left(\frac{d\sqrt{I_D}}{dV_{GS}} \right)^2 \quad (2)$$

with the channel length L, the transconductance g_m, and the gate capacitance C. To account for the geometry of the ZnO-nanowire FET, the gate capacitance C is calculated with the help of the metallic-cylinder-on-an-infinite-metal-plate model [S2]

$$C = \frac{2 \cdot \pi \cdot \varepsilon_0 \cdot \varepsilon_{eff} \cdot L}{\cosh^{-1}\left(1 + \frac{t_{ox}}{r_{NW}}\right)} \quad (3)$$

with the thickness of the gate dielectric t_{ox}, the nanowire radius r_{NW} and the effective dielectric constant ε_{eff} of the gate dielectric under consideration of the geometry (nanowire on a flat SiO_2 insulator $\varepsilon_{eff} = 2.5$ [S3]).

2. Top-gate ZnO-nanowire transistors with SAM gate dielectric on a plastic substrate

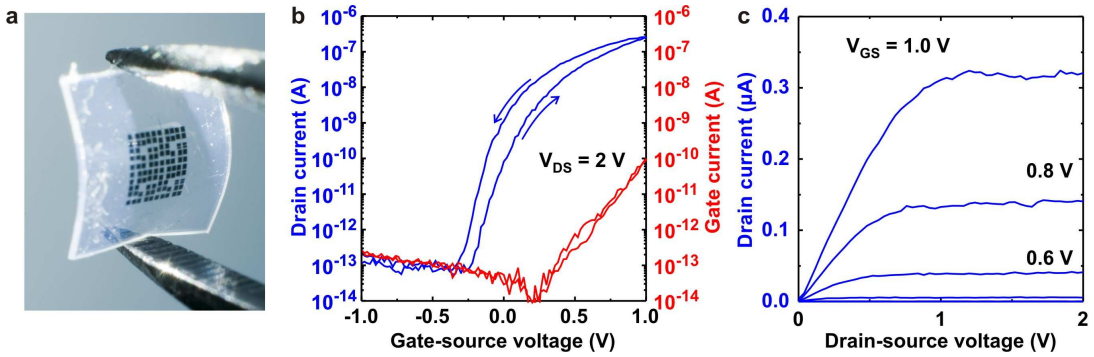

Figure S1: Electrical characteristics of a top-gate ZnO-nanowire FET on a flexible polyethylene naphthalate substrate

(a) Photograph of flexible polyethylene naphthalate (PEN) device substrate.

(b) Drain current (blue) and gate current (red) as a function of the gate-source voltage at a drain-source voltage V_{DS} = 2 V. The transistor has an on/off current ratio of 10^6, a transconductance of 0.5 μS, and a subthreshold swing of 80 mV/decade.

(c) Output characteristics of the transistor.

3. Statistical analysis of the gate currents of top-gate ZnO-nanowire MESFETs and MISFETs

In order to quantify and better understand the observed reduction of the gate current as a consequence of the SAM gate dielectric layer, the gate currents of 16 MESFETs fabricated on two different substrates (Figure S2a, red curves) and of 25 MISFETs fabricated on four different substrates (Figure S2a, blue curves) are compared. The gate currents were measured at a drain-source voltage of V_{DS} = 1 V and normalized to the channel length which determines the overlap area between the gold top-gate electrode and the ZnO nanowire. As can be seen, the gate currents are subject to considerable fluctuations and spread over two orders of magnitude. The fluctuations are most likely caused by the variations in the electrical properties of the wet-chemically grown ZnO nanowires.

For a MESFET the gate current resembles the current of a Schottky diode. Therefore, the gate currents of the 16 MESFETs are fitted with the help of the thermionic-emission equation [S1]:

$$I_G^{MESFET}(V) = I_S \cdot \exp\left(\frac{q \cdot V}{\eta \cdot k \cdot T}\right) \text{ and } \quad (4)$$

$$I_S = A \cdot A^* \cdot T^2 \cdot \exp\left(\frac{q \cdot \Phi_B}{k \cdot T}\right) \quad (5)$$

with the voltage-independent saturation current I_S, the Boltzmann constant k, the temperature T, the junction area A, the Richardson constant A^* (336710 $AK^{-2}m^{-2}$ in the case of ZnO), and the height of the energy barrier Φ_B at the metal/semiconductor interface. The junction ideality factor η is introduced to account for deviations from the thermionic emission theory.

Figure S2b and S2c show the distributions of the barrier height and of the ideality factors extracted from the gate current versus gate-source voltage characteristics of the 16 MESFETs (Figure S2a, red curves). The average height of the potential barrier is 0.55 eV and therefore significantly smaller than the maximum possible value of Φ_{ms} = 0.9 eV given by the difference of the work functions of gold and ZnO. Further, the junction ideality factor for most of the Schottky diodes is above two, which indicates gate-current contributions from mechanisms other than thermionic emission. Ideality factors much larger than one and barrier heights smaller than the work-function difference are commonly observed for gold-ZnO Schottky junctions [S4, S5, S6]. Possible explanations are a Gaussian

distribution of Φ_B along the nanowire channel [S7] and the presence of an interfacial layer between gold and ZnO that introduces a distribution of interface states [S1].

Regardless of the device-to-device fluctuations, the substantial difference between the gate currents of the MESFETs and the MISFETs is apparent in Figure S2a. Over the entire gate-bias range, the gate currents of the investigated MISFETs are much smaller compared to the gate currents of the MESFETs. Figure S2d shows the distribution of the normalized gate currents measured for a gate-source voltage of 0.5 V. The peak of the distribution for the MESFETs is in the range of 10^{-9} A/µm to 10^{-8} A/µm, while the peak for the MISFETs is between 10^{-13} A/µm and 10^{-12} A/µm. The average gate current at $V_{GS} = 0.5$ V for the MISFETs is therefore more than three orders of magnitude smaller compared to the MESFETs, which confirms the significant influence of the SAM.

The gate current reduction in consequence of the coverage with the SAM can be understood in the framework of the Metal-Insulator-Semiconductor (MIS) Schottky-diode model, which describes the influence of a thin insulating layer between semiconductor and metal on the current-voltage characteristics of a Schottky-diode [S8]. The thickness of the SAM gate dielectric is about 2 nm, which means that electrons can tunnel through the dielectric. According to the MIS Schottky-diode model, the insulating tunnel barrier modifies the current-voltage characteristics of an ideal Schottky diode by reducing the overall magnitude of the gate current described by a tunnel attenuation factor:

$$I_G^{\text{MIS-Schottky}} = I_G^{\text{MESFET}}(V) \cdot \exp(-\sqrt{\Phi_t} \cdot d_t) \qquad (6)$$

with the height of the tunnel barrier Φ_t and the thickness of the tunnel barrier d_t. The MIS-Schottky model has been successfully employed to describe the change in the current-voltage characteristics of Si/Hg Schottky diodes when the silicon was modified with an insulating SAM [S9]. The introduction of a tunnel barrier (in our case the octadecylphosphonic acid SAM on ZnO) leads to a smaller gate current over the entire gate-bias range (see Figure S2a, blue curves). However, since the gate currents of the MISFETs is near or below the resolution limit for most of the accessible range of gate-source voltages, an extraction of the parameters Φ_t and d_t is impractical.

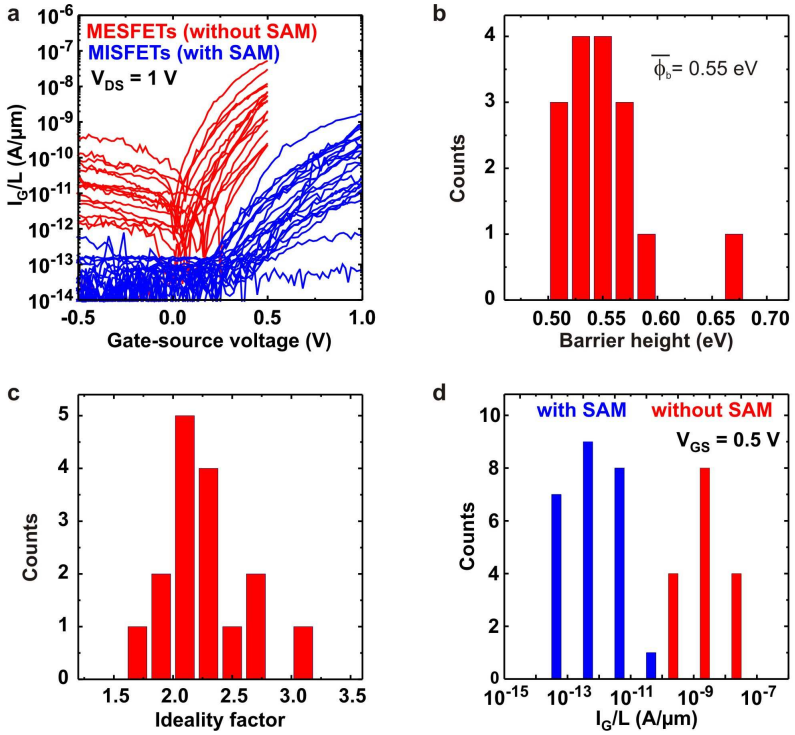

Figure S2: Statistical analysis of the gate currents of ZnO-nanowire MESFETs and MISFETs

(a) Gate currents normalized to the FET channel length L versus the gate-source voltage. The gate currents of the MISFETs (blue curves) and the MESFETs (red curves) are subject to considerable fluctuations and are spread over two orders of magnitude. The fluctuations are most probably caused by variations in the electrical properties of the wet-chemically grown ZnO nanowires.

(b) Distribution of the Schottky-barrier heights Φ_B extracted from the 16 MESFETs of figure S1a. The average barrier height is smaller than the maximum expected from the work function difference between gold and ZnO (Φ_{ms} = 0.9 eV).

(c) Distribution of the Schottky-junction ideality factors η extracted from the 16 MESFETs of figure S1a. For most MESFETs the ideality factors are above two, which indicates gate current contributions from other mechanism than thermionic emission and/or the presence of an interfacial layer between gold and ZnO that introduces a distribution of interface states.

(d) Distribution of the normalized gate currents obtained for V_{GS} = 0.5 V. In consequence of the SAM gate dielectric, the gate currents of the MISFETs are reduced by three orders of magnitude compared to the gate currents of the MESFETs.

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