Organic thin-film transistors†

Hagen Klauk

Received 21st October 2009
First published as an Advance Article on the web 16th April 2010
DOI: 10.1039/b909902f

Over the past 20 years, organic transistors have developed from a laboratory curiosity to a commercially viable technology. This *critical review* provides a short summary of several important aspects of organic transistors, including materials, microstructure, carrier transport, manufacturing, electrical properties, and performance limitations (200 references).

1. Introduction

Organic transistors are metal-insulator-semiconductor (MIS) field-effect transistors (FETs) in which the semiconductor is a conjugated organic material. In all MISFETs, regardless whether organic or inorganic, the semiconductor is separated from the metal gate electrode by a thin insulating layer, the gate dielectric. When a voltage is applied between the gate and the semiconductor, a thin sheet of mobile electronic charges is created in the semiconductor in close vicinity of the semiconductor/dielectric interface. This charge layer balances the charge (of opposite polarity) located on the gate electrode. By tuning the gate voltage, the charge density in the semiconductor channel can be modulated over a wide range, and as a result the electric conductivity of the charge-carrier channel changes dramatically. With two metal contacts attached to the semiconductor (the source contact and the drain contact), the electric current flowing through the transistor can therefore be efficiently controlled over a wide range, simply by adjusting the gate voltage.

Max Planck Institute for Solid State Research, Heisenbergstr. 1, 70569 Stuttgart, Germany
† Part of the Conducting Polymers for Carbon Electronics themed issue.

Hagen Klauk

Hagen Klauk received the Diplomingenieur degree in Electrical Engineering from Chemnitz University of Technology, Germany, in 1995 and the PhD degree in Electrical Engineering from the Pennsylvania State University in 1999. From 1999 to 2000 he was a post-doctoral researcher at the Center for Thin Film Devices at Penn State University. In 2000 he joined Infineon Technologies in Erlangen, Germany. Since 2005 he has been leading the Organic Electronics group at the Max Planck Institute for Solid State Research in Stuttgart, Germany. His research focuses on flexible transistors and circuits based on organic semiconductors, carbon nanotubes and inorganic semiconductor nanowires.

In mainstream semiconductor technology, the MISFET is by far the most important electronic device, forming the backbone of virtually all microprocessors, solid-state memories (DRAM, Flash, *etc.*), graphics adapters, mobile communication chips, active-matrix displays, and a wealth of other electronic products. In the year 2009, approximately 10^{19} MISFETs were produced worldwide, with a total value of about 200 billion US-dollars. More than 99% of all MISFETs are manufactured on the surface of single-crystalline silicon wafers, with the silicon serving both as the substrate and as the semiconductor. Silicon wafers with a diameter up to 300 mm are produced in large quantities by cutting cylindrical, single-crystalline ingots pulled from molten silicon (Czochralski process) into slices with a thickness of about 750 μm. Because the gate insulator in single-crystalline silicon MISFETs is usually an oxide (traditionally silicon dioxide, more recently also hafnium-based oxides), they are often called MOSFETs. In state-of-the-art microprocessors, the gate oxide is only about 2 nm thick.

Second to the silicon MOSFET in terms of commercial significance is the hydrogenated amorphous silicon (a-Si : H) transistor.[1] Hydrogenated amorphous silicon is a semiconductor that is produced in the form of thin films by plasma-enhanced chemical-vapor deposition (PECVD). The ability to grow semiconductor films in a gas-phase reaction facilitates the realization of MISFETs on substrates other than silicon wafers, most notably on glass substrates. The preferred gate dielectric for a-Si : H transistors is silicon nitride, which is also conveniently deposited by PECVD and which is usually a few hundred nanometres thick. The most important commercial product enabled by a-Si : H transistors is the active-matrix liquid-crystal display (AMLCD). In an AMLCD, each of the picture elements (pixels) contains an a-Si : H transistor that isolates the electric charge on the pixel during the frame time and thus facilitates high image resolution and high image fidelity. In 2009, more than 10^9 AMLCDs with a total area of about 10^8 m^2 and a total value of about 80 billion US-dollars were produced worldwide.

Unlike silicon-based transistors, which typically require fairly high process temperatures (>800 °C for single-crystalline silicon transistors, >200 °C for hydrogenated amorphous silicon transistors), organic transistors can usually be manufactured at or near room temperature, and thus on flexible polymeric substrates and even on paper. This opens the possibility of creating a wide range of novel products, such

as foldable, bendable, or rollable high-resolution color displays and electronic functionality on arbitrary, unbreakable surfaces, and this has spurred significant commercial and academic interest in organic transistors.

2. Charge-carrier transport

The fundamental property that allows organic molecules to conduct electronic charge is molecular conjugation, *i.e.* the presence of alternating single and double bonds between covalently bound carbon atoms. Conjugation causes the delocalization of one of the four valence electrons of each carbon atom that participates in the conjugated system, and this allows the efficient transport of electronic charge along a conjugated molecule.

The dimensions of organic transistors usually far exceed the dimensions of an individual molecule. Therefore, organic transistors typically utilize a thin film in which a large number of conjugated molecules are arranged in a more or less ordered fashion. Because the intermolecular bonds in organic solids are due to relatively weak van der Waals interactions, the electronic wave functions usually do not extend over the entire volume of the organic solid, but are localized to a finite number of molecules, or even to individual molecules. The mobility of electrons travelling through the organic semiconductor is therefore determined by the ease with which electrons are transported from one molecule to the next under the influence of the applied electric field. In other words, charge transport through the organic semiconductor is limited by trapping in localized states, which means that the charge-carrier mobilities in organic semiconductors are expected to be thermally activated and in general expected to be much smaller than the mobilities in inorganic semiconductor crystals.[2]

In reality, carrier mobilities observed in organic solids vary greatly depending on the choice of material, its chemical purity, and the microstructure of the solid. Semiconducting polymers that arrange in amorphous films when prepared from solution usually have room-temperature mobilities in the range of 10^{-6} to 10^{-3} cm^2/Vs. (For comparison, the carrier mobilities in single-crystalline silicon are above 10^2 cm^2/Vs at room temperature.) Through molecular engineering and by inducing semicrystalline order through better control of the film formation, the mobilities of certain semiconducting polymers can be increased to about 1 cm^2/Vs.[3] Small-molecule organic semiconductors, on the other hand, often spontaneously arrange into polycrystalline films when deposited by vacuum sublimation, which results in room-temperature mobilities as large as about 6 cm^2/Vs.[4] Reports on carefully prepared single-crystals of highly purified oligoacenes suggest that mobilities measured by the time-of-flight technique can exceed 30 cm^2/Vs at room temperature[5] and 100 cm^2/Vs at cryogenic temperatures.[6]

Because no single transport model can account for this wide a range of observed carrier mobilities, several different models for charge transport in organic semiconductors have been developed, two of which (the variable-range hopping model and the multiple trapping and release model) will be briefly discussed in the following.

The model of variable-range hopping (VRH) assumes that charge carriers hop between localized electronic states by quantum-mechanical tunneling through energy barriers and that the probability of a hopping event is determined by the hopping distance and by the energy distribution of the localized states. Specifically, carriers either hop over short distances with large activation energies, or over long distances with small activation energies. Since the hopping is thermally activated, the mobility increases with increasing temperature. With increasing gate voltage, carriers accumulated in the channel fill the lower-energy states, thus reducing the activation energy and increasing the mobility. As M. C. J. M. Vissenberg and M. Matters have shown in ref. 7, the tunneling probability depends strongly on the overlap of the electronic wave functions of the hopping sites. This result is consistent with the observation that the carrier mobility is significantly greater in semiconductors characterized by a larger degree of overlap of the delocalized molecular orbitals of neighboring molecules. Thus, the mobility is dependent on temperature, gate voltage, and molecular arrangement in the solid state, as shown in Fig. 1. The variable-range hopping model is usually discussed in the context of amorphous semiconductor films with room-temperature mobilities below about 10^{-2} cm^2/Vs.

Many small-molecule organic semiconductors have, however, a strong tendency to form polycrystalline films. As an example, Fig. 2 shows the crystal structure of the thin-film polymorph of pentacene (as determined by Stefan Schiefer and co-workers using grazing-incidence X-ray diffraction[8]) as well as the shape of the highest occupied molecular orbitals (HOMO) of the molecules within the (001) plane of the pentacene crystal (as determined by Alessandro Troisi and Giorgio Orlandi using quantum-mechanical calculations[9]). As a result of the regular molecular arrangement, the delocalized orbitals of neighboring molecules partially overlap, thereby facilitating more efficient intermolecular charge-carrier transfer and carrier mobilities that are much larger than in amorphous films, usually well above 10^{-2} cm^2/Vs. Such large mobilities are not easily explained with the variable-range hopping model.

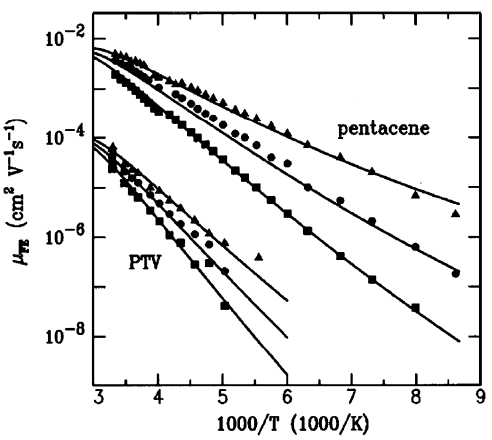

Fig. 1 Carrier mobility in solution-processed, amorphous films of polythienylene vinylene (PTV) and thermally converted precursor pentacene as a function of temperature for different gate voltages (squares: 5 V, circles: 10 V, triangles: 20 V). (Reprinted with permission from ref. 7: M. C. J. M. Vissenberg *et al.*, *Phys. Rev. B*, 1998, **57**, 12964. Copyright 1998 by the American Physical Society.)

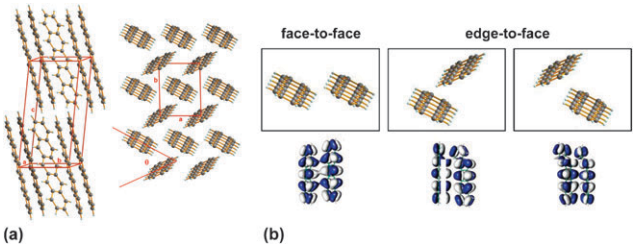

Fig. 2 (a) Crystal structure of the thin-film polymorph of pentacene, as determined by S. Schiefer and co-workers using X-ray diffraction[8] (a = 0.596 nm, b = 0.760 nm, c = 1.56 nm, α = 81.2°, β = 86.6°, γ = 89.8°, $\theta \sim 55°$). The (001) plane is oriented parallel to the substrate surface. (b) Shape of the highest occupied molecular orbitals (HOMO) of the molecules within the (001) plane of the pentacene crystal, as determined by A. Troisi and G. Orlandi using quantum-mechanical calculations.[9] (Reprinted with permission from ref. 9: A. Troisi and G. Orlandi, *J. Phys. Chem. B*, 2005, **109**, 1849. Copyright 2005 by the American Chemical Society.)

In contrast to the variable-range hopping model, the multiple trapping and release (MTR) model adapted for organic transistors by Gilles Horowitz and co-workers[10] is based on the assumption that most of the charge carriers in the channel are trapped in localized states (that are associated with structural or chemical defects), and that carriers cannot move directly from one state to another. Instead, carriers are temporarily promoted to an extended-state band in which charge transport occurs. The number of carriers available for transport then depends on the difference in energy between the trap level and the extended-state band, as well as on the temperature and on the gate voltage (see Fig. 3).

Although the existence of an extended-state transport band in organic semiconductors, as postulated by the MTR model, is often debated, the MTR model appears to properly describe transport in organic semiconductors with a microstructure that favors a high degree of intermolecular orbital overlap, such as polycrystalline films of small-molecule and certain polymeric semiconductors with room-temperature mobilities that approach or exceed 0.1 cm^2/Vs. Indeed, quantum-mechanical calculations of the charge-carrier dynamics in defect-free pentacene crystals suggest that carriers propagating through

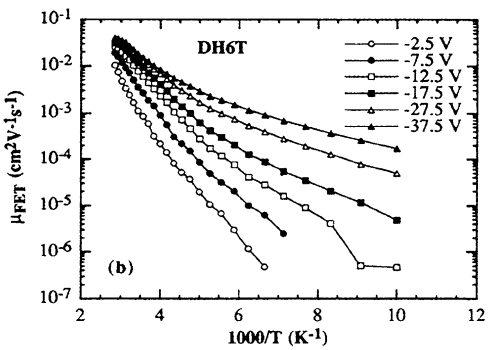

Fig. 3 Temperature-dependent and gate voltage-dependent carrier mobility in a vacuum-deposited polycrystalline dihexylsexithiophene (DH6T) film. (Reprinted with permission from ref. 10: G. Horowitz *et al.*, *J. Phys. III France*, 1995, **5**, 355. Copyright 1995 by EDP Sciences.)

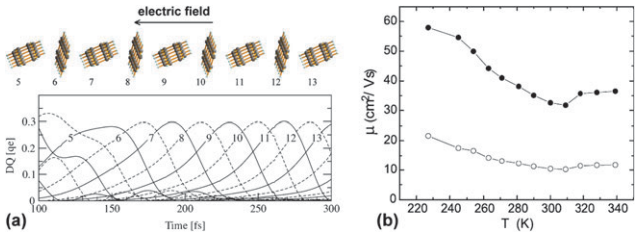

Fig. 4 (a) Time evolution of the net charge (ΔQ) per pentacene molecule due to an access electron propagating through the pentacene crystal in the [110] direction (intermolecular transfer integral J = 50 meV, electric field $E = 5 \times 10^4$ V cm^{-1}). (Reprinted with permission from ref. 11: M. Hultell *et al.*, *Chem. Phys. Lett.*, 2006, **428**, 446. Copyright 2006 by Elsevier.) (b) Hole mobility in a highly purified pentacene single-crystal measured with a time-of-flight technique as a function of temperature, showing evidence for band-like transport. (Reprinted with permission from ref. 5: O. Jurchescu *et al.*, *Appl. Phys. Lett.*, 2004, **84**, 3061. Copyright 2004 by the American Institute of Physics.)

the molecular lattice under the influence of an external electric field are delocalized over a significant number of molecules (see Fig. 4a), and that the carrier drift velocity is within a factor of two of the saturation velocity in single-crystalline silicon.[11] Furthermore, temperature-dependent time-of-flight mobility measurements on highly purified pentacene crystals have shown clear evidence for charge transport in extended states with a hole mobility that is within an order of magnitude of the hole mobility in single-crystalline silicon and is limited by phonon scattering, rather than thermal activation[5] (see Fig. 4b).

3. Materials

Organic semiconductors essentially come in two flavors: conjugated polymers and conjugated small-molecule materials. The prototypical semiconducting polymer is polythiophene (see Fig. 5a). While genuine polythiophene is insoluble and thus difficult to deposit in the form of thin films,[12] alkyl-substituted polythiophenes, such as poly(3-hexylthiophene) (P3HT) (see Fig. 5b) have excellent solubility in a variety of organic solvents,[13] and thin films are readily prepared by spin-coating, dip-coating, drop-coating, screen printing, or inkjet printing.

Generic polythiophenes usually form amorphous films with virtually no long-range structural order, very short π-conjugation length, and consequently poor carrier mobilities, typically below 10^{-3} cm^2/Vs. Obtaining usefully large mobilities in the polythiophene system requires highly purified derivatives

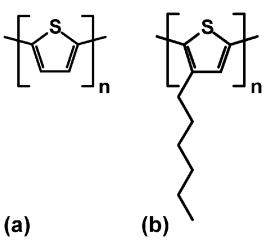

Fig. 5 Early conjugated polymers for organic transistors. (a) Polythiophene. (b) Poly(3-hexylthiophene) (P3HT).

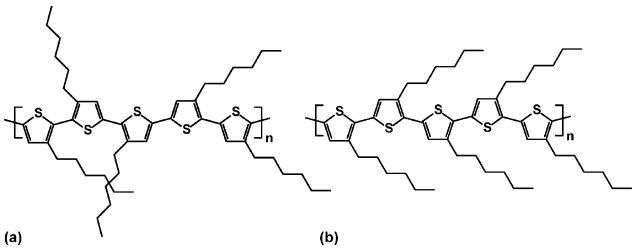

Fig. 6 (a) Schematic representation of regiorandom poly(3-hexylthiophene) (P3HT). (b) Schematic representation of regioregular P3HT.

specifically synthesized to allow the molecules to self-organize into crystalline lamella with a microstructure that favors intermolecular orbital overlap and charge transfer. An early example of such an engineered polythiophene is regioregular head-to-tail poly(3-hexylthiophene), initially synthesized by Richard McCullough and co-workers in 1993[14] and first employed for transistor fabrication by Zhenan Bao and co-workers in 1996.[15] In regioregular P3HT, the strong interactions between the regularly oriented alkyl side chains lead to a three-dimensional lamellar structure in which the thienylene moieties along the polymer backbone are held in coplanarity (see Fig. 6). The coplanarity of the thienylene moieties greatly increases the extent of π-conjugation along the molecular backbone and the ability to form well-ordered lamellar domains. One consequence is a substantially increased carrier mobility (0.05 to 0.1 cm^2/Vs) compared with regiorandom P3HT (where the mobility is usually below 10^{-3} cm^2/Vs).

The microstructure of regioregular P3HT films, its dependence on the degree of regioregularity, molecular weight, and deposition conditions, and the relationship between microstructure and carrier mobility have been studied in great detail. Henning Sirringhaus and co-workers found that the orientation of the lamellar domains with respect to the substrate surface is influenced by the molecular weight (*i.e.*, the average polymer chain length), by the degree of regioregularity, and by the deposition conditions (*i.e.*, whether the film formation occurred quickly or slowly).[16] The formation of ordered lamellae leads to a substantial overlap of the delocalized molecular orbitals of neighboring P3HT molecules (π–π stacking), but only in the direction perpendicular to the lamella plane. As a result, charge-carrier transport and mobility in ordered P3HT films are highly anisotropic. In field-effect transistors, the electric current usually flows parallel to the substrate, so the orientation of the lamellae with respect to the substrate surface is critical for the electrical performance of the transistors. Sirringhaus *et al.* were able to show that the transistor-friendly, edge-on orientation of the lamellae (shown in the left part of Fig. 7a) can be induced by selecting a polymer with a high degree of regioregularity (see Fig. 7b) and—to a lesser extent—by choosing deposition conditions that favor a slow crystallization of the film.

Joe Kline and co-workers later showed that the carrier mobility in regioregular P3HT films also depends critically on the interconnectivity between the individual lamellar domains, and that a higher molecular weight leads to smaller domain size, but significantly improved interconnectivity between the domains and thus larger carrier mobility (see Fig. 8a).[17]

Using a directional crystallization technique, Leslie Jimison and co-workers have prepared regioregular P3HT films in which most of the lamellar domains are oriented in the same direction and form well-ordered fibers that span several microns in length (see Fig. 8b), with profound consequences on the charge transport (especially its anisotropy) within the film.[18]

Unfortunately, the large extent of the π-conjugation in regioregular poly(3-hexylthiophene) also leads to a significantly reduced ionization potential that makes the material very susceptible to photoinduced oxidation, and this explains the commonly observed instability of P3HT transistors when operated in ambient air without encapsulation. A successful route to environmentally more stable self-organizing high-mobility polythiophene derivatives was devised by Beng Ong and co-workers.[19] They recognized that the strategic placement of unsubstituted moieties along the polymer backbone and the resulting torsional deviations from co-planarity would reduce the effective π-conjugation length sufficiently to increase the ionization potential (and thus greatly improve oxidation resistance and environmental stability) while compromising the mobility only slightly, if at all. A particularly successful

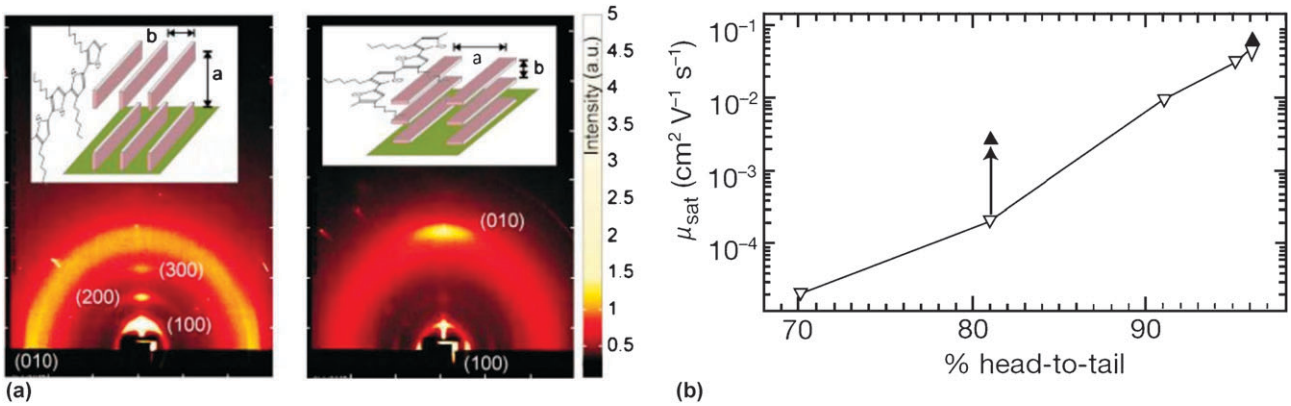

Fig. 7 (a) Upon deposition on a flat substrate, regioregular poly(3-hexylthiophene) (P3HT) forms ordered lamellar domains, the orientation of which with respect to the substrate surface depends on the degree of regioregularity, the molecular weight, and the deposition conditions. (b) Relationship between the degree of regioregularity (quantified as the head-to-tail ratio) and the carrier mobility of P3HT transistors. (Reprinted with permission from ref. 16: H. Sirringhaus *et al.*, *Nature*, 1999, **401**, 685. Copyright 1999 by Macmillan Publishers Ltd.)

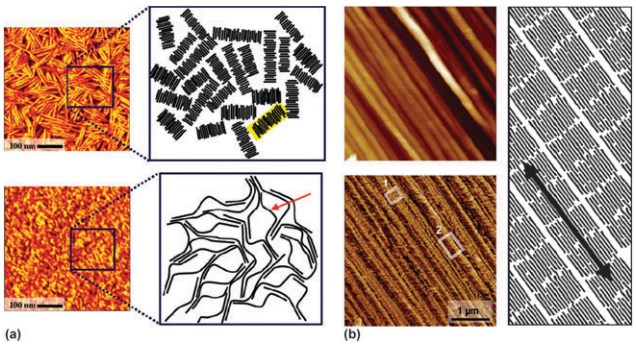

Fig. 8 (a) Microstructure of regioregular poly(3-hexylthiophene) (P3HT) films based on low molecular weight (top) and high molecular weight (bottom). In the low-molecular-weight film, charge-carrier transport is very efficient within the lamellar domains (one of which is highlighted in yellow), but the mobility in the film is severely limited by the disorder and the poor interconnectivity between the domains. In the high-molecular-weight film, the size of the lamellar domains is much smaller, but long polymer chains bridge the ordered regions and soften the boundaries (marked with a red arrow), thereby increasing the mobility in the film (Reprinted with permission from ref. 17: R. J. Kline *et al.*, *Macromolecules*, 2005, **38**, 3312. Copyright 2005 by the American Chemical Society.) (b) Microstructure of a regioregular P3HT film prepared by directional crystallization, showing a regular arrangement of the lamellar domains (Reproduced with permission from ref. 18: L. H. Jimison *et al.*, *Adv. Mater.*, 2009, **21**, 1568. Copyright 2009 by Wiley-VCH Verlag GmbH & Co. KGaA.)

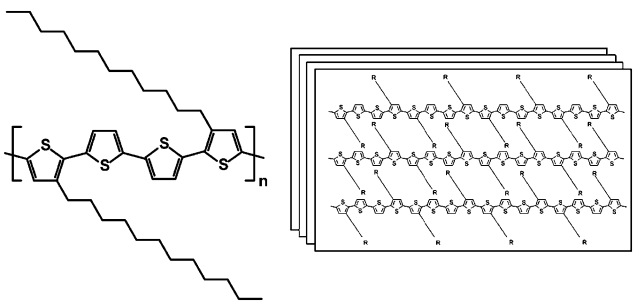

Fig. 9 Chemical structure of poly(3,3‴-didodecylquaterthiophene) (PQT-12) and a schematic representation of the lamellar π-stacking arrangement (Reprinted with permission from ref. 19: B. Ong *et al.*, *J. Am. Chem. Soc.*, 2004, **126**, 3378. Copyright 2004 by the American Chemical Society.)

material that emerged from this line of work is poly(3,3‴-didodecylquaterthiophene), better known as PQT-12 (see Fig. 9). PQT-12 has shown air-stable carrier mobilities as large as 0.2 cm^2/Vs and has been employed successfully in the fabrication of functional organic circuits and displays.

To further improve the performance and stability of alkyl-substituted polythiophenes, Iain McCulloch and co-workers incorporated thieno[3,2-*b*]thiophene moieties in the polymer backbone, yielding poly(2,5-bis(3-alkylthiophen-2-yl)thieno-[3,2-*b*]thiophene (pBTTT)[20] (see Fig. 10). The effect is two-fold: The delocalization of carriers from the fused aromatic unit is less favorable than from a single thiophene unit, so the effective π-conjugation length is further reduced and the ionization potential becomes even larger than for polyquaterthiophene. Second, the rotational invariance of the thieno[3,2-*b*]thiophene

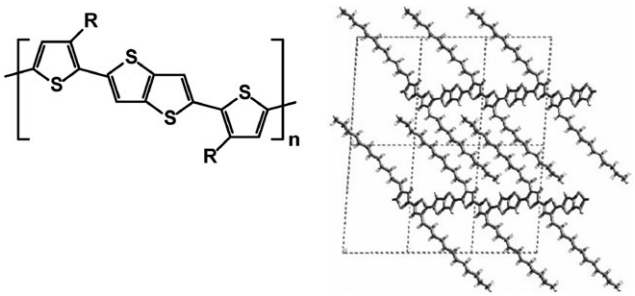

Fig. 10 Chemical structure of poly(2,5-bis(3-alkylthiophen-2-yl)thieno-[3,2-*b*]thiophene (pBTTT) and a schematic representation of the lamellar π-stacking arrangement (Reproduced with permission from ref. 20: I. McCulloch *et al.*, *Adv. Mater.*, 2009, **21**, 1091. Copyright 2009 by Wiley-VCH Verlag GmbH & Co. KGaA.)

unit in the backbone promotes the formation of highly ordered crystalline domains with an extent not previously seen in semiconducting polymers. The molecular ordering is induced by annealing the films in their liquid-crystalline phase and subsequent crystallization upon cooling. Transistors based on pBTTT typically have excellent stability, and carrier mobilities as large as 1.1 cm^2/Vs have been reported.[3]

Among the small-molecule organic semiconductors, the most widely studied materials include pentacene, sexithiophene and copper phthalocyanine (see Fig. 11). Many small-molecule organic semiconductors are insoluble in common organic solvents, but they often can be conveniently deposited by thermal sublimation in vacuum[4,10] or by organic vapor phase deposition.[21–23] In most cases, small-molecule organic semiconductors readily self-organize into well-ordered polycrystalline films upon deposition (see Fig. 12).

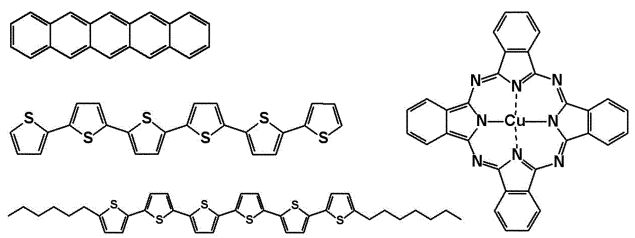

Fig. 11 Conjugated small-molecule organic semiconductors. (a) Pentacene. (b) Sexithiophene (6T). (c) Dihexylsexithiophene (DH6T, Hex-6T-Hex). (d) Copper phthalocyanine.

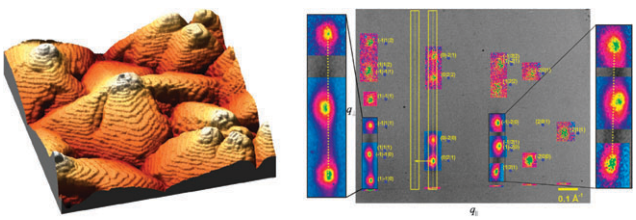

Fig. 12 Atomic force microscopy (AFM) image and grazing-incidence X-ray diffraction (GIXD) pattern of a thin pentacene film deposited by vacuum sublimation (Reprinted with permission from ref. 8: S. Schiefer *et al.*, *J. Am. Chem. Soc.*, 2007, **129**, 10316. Copyright 2007 by the American Chemical Society.)

The use of vacuum-deposited films of conjugated small-molecule materials for organic transistors was pioneered in the late 1980s by Kazuhiro Kudo and co-workers using merocyanines,[24] by M. Madru and C. Clarisse using metal phthalocyanines,[25,26] and by Gilles Horowitz and Francis Garnier using oligothiophenes.[27,28] Initial carrier mobilities were around 10^{-3} cm^2/Vs but quickly improved to about 0.1 cm^2/Vs. In 1996 Tom Jackson predicted and demonstrated that the carrier mobility of many organic semiconductors can be substantially improved by growing the films on low-energy surfaces.[29,30] Inorganic dielectrics, such as silicon dioxide, are usually characterized by large surface energies favoring two-dimensional growth of the organic layer. Two-dimensional film growth typically results in large crystalline grains, and it was long believed that this was desirable to achieve good transistor performance. The surface energy of inorganic dielectrics is readily reduced by covering the surface with a self-assembled monolayer (SAM) of a methyl-terminated alkylsilane, such as octadecyltrichlorosilane (OTS). Growth of small-molecule organic semiconductor films on low-energy SAM surfaces is distinctly three-dimensional, with much smaller grains and significantly more grain boundaries, yet the transistor mobilities were found to be significantly larger (by as much as an order of magnitude) compared with the large-grain films grown on high-energy surfaces. One explanation for the apparent discrepancy between grain size and mobility is that two-dimensional growth results in voids between disconnected grains, reducing the effective channel width of the transistor, and that such voids are efficiently filled when three-dimensional growth is favored.[31,32] Carrier mobilities on high-energy surfaces (such as bare silicon dioxide) peak around 0.5 cm^2/Vs, while mobilities on low-energy surfaces (SAM-treated oxides or polymer dielectrics) have reached 1 cm^2/Vs for dialkyl-oligothiophenes[33] and 6 cm^2/Vs for pentacene.[4,34–36] Ajay Virkar and co-workers have studied the relationship between the packing density of the alkylsilane monolayer and the microstructure of the vacuum-deposited small-molecule organic semiconductor layer and found that the mobility improves by as much as a factor of two if the semiconductor films grow on highly compressed, extremely well-ordered monolayers.[37,38] The concept of improving the carrier mobility in organic semiconductor films by controlling the semiconductor film growth using alkylsilane self-assembled monolayers, which was initially demonstrated for small-molecule semiconductors[29,30] was later also extended to polymeric semiconductors.[39]

Although a substantial number of small-molecule semiconductors have emerged, pentacene consistently provides the largest carrier mobilities, due to its favorable crystal structure that provides excellent overlap of the frontier molecular orbitals in the (001) lattice plane, and the fact that the grain boundaries in polycrystalline pentacene films do not cause significant impediment of the carrier transport through the film. Unfortunately, pentacene is easily oxidized when exposed to oxygen (including water, ozone, and other air-borne species). When pentacene oxidizes, the hydrogen atoms at the 6 and 13 positions (*i.e.*, at the central benzene ring of the molecule) are replaced with oxygen. Unlike the hydrogen that is replaced, oxygen forms double bonds with the carbon atoms, and this destroys the conjugation of the central benzene ring and substantially reduces the extent of the conjugated π-system of the molecule. The result of the oxidation is therefore a molecule with different orbital energies that no longer participates in the charge-carrier transport of the transistor. As more and more pentacene molecules are oxidized while the transistor is exposed to air, the carrier mobility therefore decreases monotonically and irreversibly. The rate at which the mobility degrades depends on the gate dielectric, the pentacene film thickness, and other factors, but it can be as high as one order of magnitude within a few weeks.[40–42]

Small-molecule semiconductors with a larger ionization potential and thus better oxidation resistance than pentacene have been proposed,[43–46] but at the expense of a less favorable crystal structure, so that the initial mobilities of these materials are inferior to that of pentacene. Two examples of conjugated molecules that have a larger ionization potential and thus better air stability compared with pentacene, but adopt a crystal structure with excellent orbital overlap (resulting in mobilities similar to or larger than those of pentacene) are 2,6-di[2-(4-phenyl)vinyl]anthracene (DPVAnt; see Fig. 13a), which was first synthesized by Hong Meng and co-workers,[47,48] and dinaphtho-[2,3-*b*:2′,3′-f]thieno[3,2-*b*]thiophene (DNTT; see Fig. 13b), which was developed by Tatsuya Yamamoto and Kazuo Takimiya.[49,50] Both semiconductors provide initial mobilities that are similar to that of pentacene transistors, but show much better air stability than pentacene (see Fig. 13c).

An interesting alternative to solution-processed polymers and vacuum-deposited small-molecule semiconductors was developed by Peter Herwig and Klaus Müllen in the early 1990s in the form of solution-processed pentacene.[51] The idea was to combine the simplicity of solution-processing with the large carrier mobility of pentacene. Herwig and Müllen (and later Ali Afzali and co-workers;[52] see Fig. 14) synthesized a soluble pentacene precursor that was spin-coated and subsequently converted to pentacene at elevated temperature. Carrier field-effect mobilities in thermally converted pentacene films are between 0.1 and 1 cm^2/Vs, depending on the conversion temperature (130 to 200 °C).

The concept of solution-processable, high-mobility, small-molecule organic semiconductors was further developed by John Anthony and co-workers. They designed and synthesized a number of soluble pentacene and anthradithiophene derivatives that do not require chemical conversion after deposition. Three particularly successful examples, triisopropylsilylethynyl pentacene (TIPS pentacene,[53–55]), triethylsilylethynyl anthradithiophene (TESADT,[56–58]), and difluoro-triethylsilylethynyl

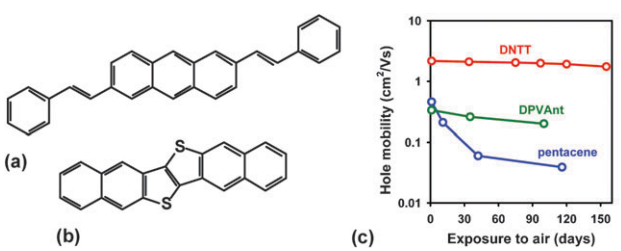

Fig. 13 Small-molecule organic semiconductors with improved air stability. (a) 2,6-Di[2-(4-phenyl)vinyl]anthracene (DPVAnt).[48] (b) Dinaphtho-[2,3-*b*:2′,3′-f]thieno[3,2-*b*]thiophene (DNTT).[49] (c) Comparison of the air stability of pentacene, DPVAnt, and DNTT.

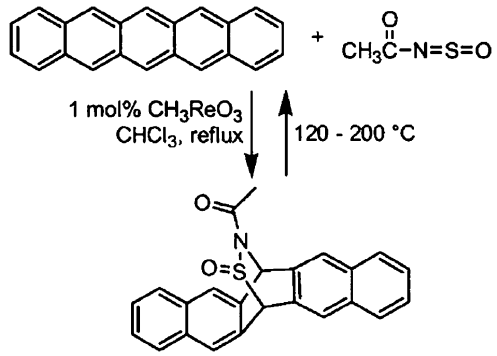

Fig. 14 Synthesis of a soluble pentacene precursor and thermally induced conversion of the precursor to pentacene (Reprinted with permission from ref. 52: A. Afzali *et al*., *J. Am. Chem. Soc*., 2002, **124**, 8812. Copyright 2002 by the American Chemical Society.)

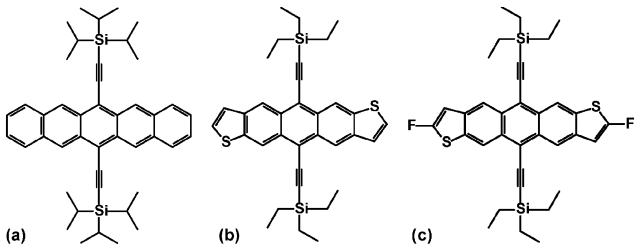

Fig. 15 Soluble pentacene derivatives. (a) Triisopropylsilylethynyl pentacene (TIPS pentacene). (b) Triethylsilylethynyl anthradithiophene (TESADT). (c) Difluoro-triethylsilylethynyl anthradithiophene (diF-TESADT).

anthradithiophene (diF-TESADT,[59–62]), are shown in Fig. 15. In addition to providing a high degree of solubility in common organic solvents, the functionalization of pentacene and anthradithiophene at the center rings can be utilized to strategically tune the molecular packing in the solid state in order to induce π-stacking with reduced intermolecular distances. Depending on the choice of substituents, the molecules adopt a one-dimensional ("slipped") or two-dimensional π-stacking arrangement. With optimized deposition, carrier mobilities between 1 and 2.5 cm^2/Vs have been achieved with these materials.[55,57,60,62,63] Because the central aromatic ring of the molecules is protected from oxidation, they also provide better air stability than pentacene.

Organic transistors prepared with any of the semiconductors described so far operate efficiently only as *p*-channel transistors, *i.e*. the currents in these transistors are due to positively charged carriers (holes in the highest occupied molecular orbital, HOMO). In contrast, currents due to negative carriers (electrons in the lowest unoccupied molecular orbital, LUMO) are usually very small in these materials, or these currents can only be measured when the transistors are operated in vacuum or in an inert gas. This has several reasons. One is that the energy barrier between the Fermi level of the source/drain contacts and the HOMO of the semiconductor is usually much smaller than the energy barrier between the Fermi level of the contacts and the LUMO. For example, pentacene has an ionization potential (HOMO energy) of about 4.5 eV and an electron affinity (LUMO energy) of about 2.5 eV. When pentacene is contacted with an air-stable metal, such as gold (with a workfunction or Fermi energy of about 5 eV), the barrier between the Fermi level of the metal and the HOMO of the pentacene is only a few hundred meV, while the barrier between the Fermi level of the metal and the LUMO of the pentacene is more than 2 eV. As a result, the exchange of positive carriers between the contacts and the HOMO is much more efficient than the exchange of negative carriers between the contacts and the LUMO, so the current through the semiconductor is greatly dominated by holes.

A second reason is that in many organic semiconductors negative charge carriers are trapped more frequently than positive carriers, either at the semiconductor/gate dielectric interface,[64] or at grain boundaries within the semiconductor, or by environmental traps which are presumably generated by oxygen or water entering the semiconductor layer from the environment.

As a result, most organic transistors show *p*-channel, but not *n*-channel behavior. However, the realization of many electronic applications benefits greatly from the availability of both *p*-channel and *n*-channel field-effect transistors, because this allows the implementation of complementary circuits with low static power consumption and sufficient robustness against device parameter variations and electronic noise that is always present in electronic systems. Consequently, substantial effort has gone into the development of organic *n*-channel transistors.

The fabrication of organic *n*-channel transistors requires that the energy barrier between the Fermi level of the source/drain contacts and the LUMO of the organic semiconductor is as small as possible (and much larger than the barrier to the HOMO). For semiconductors with a small electron affinity, such as pentacene and poly(3-hexylthiophene), this can be achieved by employing contacts based on a low-workfunction metal. For example, Marcus Ahles and co-workers have reported *n*-channel operation in pentacene transistors with calcium source and drain contacts.[65] Calcium has a workfunction of about 2.8 eV, so the energy barrier between the Fermi level of the calcium contacts and the LUMO of pentacene is only a few hundred meV, allowing efficient exchange of negative charge carriers. To reduce the density of the electron traps available at the semiconductor/dielectric interface, Ahles *et al*. deposited a small amount of calcium on the surface of the gate dielectric prior to depositing the pentacene. Electron mobilities as large as 0.2 cm^2/Vs were reported.[65] However, these transistors can only be operated in vacuum or in an inert gas; they immediately and irreversibly degrade when exposed to air. Lay–Lay Chua and co-workers have reported *n*-channel operation in a variety of conjugated polymers (including poly(3-hexylthiophene), poly(9,9-dioctyfluorene) and poly(*p*-phenylenevinylene)), with electron mobilities approaching 0.01 cm^2/Vs.[66] To minimize the energy barrier between the Fermi level of the contacts and the LUMO of the polymers, Chua *et al*. also utilized calcium contacts. To reduce the electron trapping rate at the semiconductor/dielectric interface, polymer gate dielectrics without hydroxyl groups were employed. Again, these transistors can only be operated in an inert environment.

Compared with pentacene and poly(3-hexylthiophene), the fullerene C_{60} (see Fig. 16a) has a somewhat larger electron affinity, and C_{60} *n*-channel transistors have been prepared

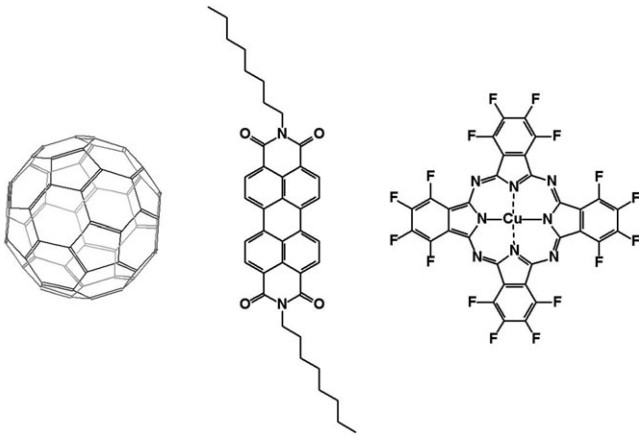

Fig. 16 Conjugated small-molecule semiconductors for organic *n*-channel transistors. (a) The fullerene C_{60}. (b) Dioctyl–perylene tetracarboxylic diimide (PTCDI-C_8H_{17}). (c) Hexadecafluorocopperphthalocyanine (F_{16}CuPc).

using a variety of high-workfunction and low-workfunction contact metals, such as gold[67–69] lithium fluoride,[70] aluminium,[71,72] and calcium.[72] Although Xiao-Hong Zhang and Bernard Kippelen found clear evidence that calcium provides substantially better contact performance than aluminium for C_{60} transistors,[72] no systematic correlation between the choice of metal and the C_{60} transistor performance is apparent from the results of other groups, with electron mobilities reported between 2 and 6 cm^2/Vs for metals with workfunctions ranging from 3 to 5 eV. The lack of a monotonic relationship between the workfunction of the contact metal and the contact performance may be related to a variety of phenomena occurring at the interface between the organic semiconductor and the metal, such as the Coulomb repulsion between the electrons at the surfaces of the two materials (the so-called ''pillow effect''), the presence of a thin oxide or contamination layer, a large density of electronic gap states at the interface, or the presence of an interface dipole.[73] Regardless of the contact metal, C_{60} transistors show acceptable performance only as long as they are kept under vacuum or in an inert gas. Reports of C_{60} transistors that can be operated in air are rare. Kazunaga Horiuchi and co-workers have encapsulated C_{60} *n*-channel transistors with a sputter-deposited aluminium oxide layer and reported stable transistor operation in air for up to 40 min; however, the electron mobility was only 0.1 cm^2/Vs.[68] Junhyuk Jang and co-workers have employed a fluoropolymer (Cytop™) as the gate dielectric, which leads to a dramatic reduction in the density of trap states at the semiconductor/dielectric interface compared with more common organic or inorganic dielectrics, allowing the transistors to operate in air without encapsulation; however, the electron mobility was only 0.05 cm^2/Vs.[74]

Electron mobilities as large as 1.7 cm^2/Vs and 2.1 cm^2/Vs have been reported for *n*-channel transistors based on dioctyl–perylene tetracarboxylic diimide (PTCDI–C_8H_{17}; see Fig. 16b) and ditridecyl–perylene tetracarboxylic diimide (PTCDI–$C_{13}H_{27}$), respectively.[75,76] These semiconductors have electron affinities of about 3.4 eV,[77] so the best *n*-channel transistor performance might have been expected for low-workfunction-metal contacts, but in fact the transistor performance is strongly limited by the contacts regardless of the choice of metal, as reported by David Gundlach and co-workers.[78] Again, these transistors were reported to operate only when protected from ambient air. Electron mobilities of 6.2 cm^2/Vs in an inert ambient and 0.4 cm^2/Vs in air have been measured for *n*-channel transistors based on cyclohexyl–naphthalene tetracarboxylic diimide (NTCDI–C_6H_{11}).[79]

The first breakthrough towards air-stable organic *n*-channel transistors came in 1998, when Zhenan Bao and co-workers synthesized hexadecafluorocopperphthalocyanine (F_{16}CuPc; see Fig. 16c).[80] By substituting all 16 hydrogen atoms of copper phthalocyanine (CuPc) with fluorine atoms, the electron affinity of the molecule was increased by almost 2 eV, to about 4.5 eV.[81] For the first time, this allowed organic *n*-channel transistors to be operated in air without encapsulation. In fact, F_{16}CuPc transistors can usually be stored in air for several months without significant degradation of the performance.[80,82] Also, the large electron affinity means that non-oxidizing, high-workfunction metals, such as gold, can be employed for the source and drain contacts without introducing a significant energy barrier between the contacts and the LUMO of the semiconductor. Unfortunately, the electron mobilities in F_{16}CuPc transistors are quite small, only about 0.03 cm^2/Vs, *i.e.* smaller by one or two orders of magnitude compared with the best organic *p*-channel transistor mobilities. Also, unlike most other conjugated semiconductors, F_{16}CuPc appears to not benefit significantly from deposition onto low-energy surfaces, so that the mobility of F_{16}CuPc transistors is not easily improved by optimizing the gate dielectric surface. A possible explanation for the low mobility was reported by Dimas de Oteyza and co-workers who found that F_{16}CuPc typically forms a disordered interface layer during the early stages of film growth.[83,84] This disordered interface layer is buried under polycrystalline material during the later stages of film growth, so that X-ray diffraction experiments performed on thicker films typically suggest a well-ordered film with the apparent potential for large carrier mobilities. However, the carrier channel of a field-effect transistor is located in close vicinity of the semiconductor/gate dielectric interface, and in the case of F_{16}CuPc this means that the current flows in the disordered interface layer, which explains the relatively poor mobilities of transistors based on F_{16}CuPc (and most other phthalocyanines).

The idea of substituting hydrogen with fluorine to create conjugated semiconductors for air-stable organic *n*-channel transistors was extended to the naphthalene tetracarboxylic diimide (NTCDI) system by Howard Katz and co-workers.[85,86] They examined four different fluorocarbon substitutions and six different hydrocarbon substitutions on the imide positions of the molecule. None of the hydrocarbon-substituted compounds showed transistor activity in air. In contrast, three of the four fluorocarbon-substituted compounds showed electron mobilities above 0.01 cm^2/Vs in air (see Fig. 17), with a maximum mobility in air of 0.12 cm^2/Vs. Unlike the phthalocyanines, where the fluorine substitution introduced by Bao *et al.* has a massive effect on the electron affinity of the molecule, the substitutions investigated by Katz *et al.* have little, if any, effect on the orbital energies of the NTCDI

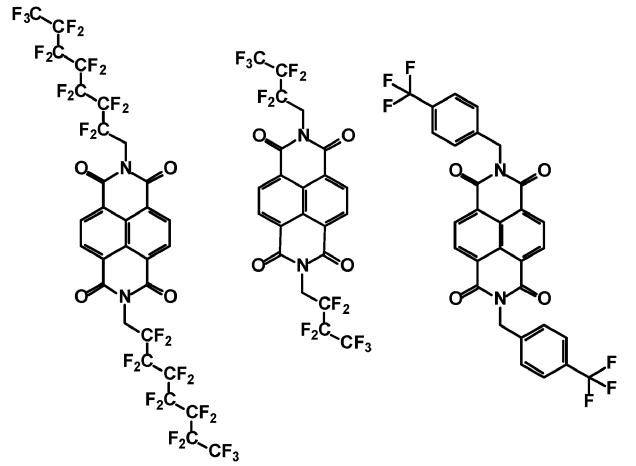

Fig. 17 Fluorocarbon-substituted naphthalene tetracarboxylic diimide (NTCDI) derivatives for air-stable organic *n*-channel transistors.[85,86]

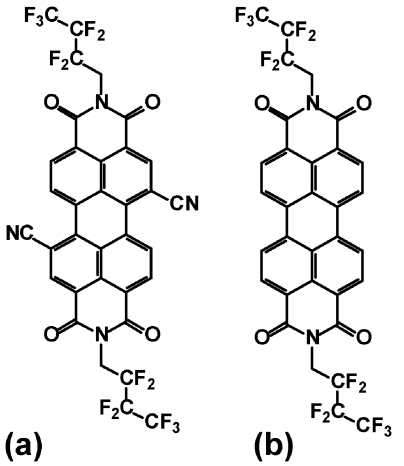

Fig. 18 Conjugated semiconductors for high-mobility, air-stable organic *n*-channel transistors. (a) Bis(2,2,3,3,4,4,4-heptafluorobutyl)-dicyano-perylene tetracarboxylic diimide (PTCDI–$(CN)_2$–$CH_2C_3F_7$).[97] (b) Bis(2,2,3,3,4,4,4-heptafluorobutyl)-perylene tetracarboxylic diimide (PTCDI-$CH_2C_3F_7$).[100]

compounds, because the fluorine atoms are not directly connected to the conjugated core. In other words, genuine NTCDI, hydrocarbon-substituted NTCDI, and fluorocarbon-substituted NTCDI all have approximately the same electron affinity—one that is too small to expect air stability. In order to explain the fact that the transistors with the fluorocarbon-substituted NTCDI can nonetheless be operated in air, Katz *et al*. hypothesized that the fluorocarbon-substituted molecules perhaps pack more densely in the solid state, compared with genuine or hydrocarbon-substituted NTCDI, and that this might create a barrier protecting the conjugated cores from ambient species, such as water and oxygen. But the authors also pointed out that denser packing was to be expected only for two of the three air-stable compounds, not including the one that showed the largest mobility. Whether the mobility degrades when the transistors are stored in air for extended periods of time was not reported.

Antonio Facchetti and co-workers systematically investigated the effect of various fluoroalkyl and fluoroarene substitutions on the transport characteristics of a wide variety of oligothiophenes and phenylene–thiophene oligomers.[87–94] For many of these compounds, the fluorination indeed led to the observation of efficient electron transport. One of these semiconductors, diperfluorohexylcarbonyl-quaterthiophene (DFHCO-4T) showed an electron mobility as large as 1.7 cm^2/Vs.[94] However, in all of these reports the transistors were either protected from ambient air, or the electron mobilities were below 0.1 cm^2/Vs.

Applying the concept of fluorination to the conjugated hydrocarbon with the largest hole mobility, pentacene, proved more challenging. In 2004, Youichi Sakamoto and co-workers successfully synthesized perfluoropentacene ($C_{22}F_{14}$) in a difficult six-step reaction.[95] Replacing the fourteen hydrogen atoms of pentacene with fluorine increases the electron affinity by 1 eV, but because pentacene has a relatively small electron affinity to begin with (2.4 eV), the fluorination effect is insufficient to produce a molecule that is useful for air-stable *n*-channel transistors. The maximum reported electron mobility of perfluoropentacene *n*-channel transistors is 0.22 cm^2/Vs when the transistors are operated in vacuum or in an inert gas, but less than 0.01 cm^2/Vs when the devices are exposed to air.[96]

The second breakthrough towards air-stable organic *n*-channel transistors with large carrier mobility was made in 2004, when Brooks Jones and co-workers synthesized bis(2,2,3,3,4,4,4-heptafluorobutyl)-dicyano-perylene tetracarboxylic diimide (PTCDI–$(CN)_2$–$CH_2C_3F_7$; see Fig. 18a) and found that *n*-channel transistors based on this compound operated with a record mobility of 0.64 cm^2/Vs in air.[97] In addition to the fluoroalkyl substituents at the imide positions, the PTCDI–$(CN)_2$–$CH_2C_3F_7$ molecule has two highly electronegative cyano groups attached to the bay positions of the conjugated core, which increases the electron affinity to about 4.3 eV. The large mobility strongly suggests that this molecule forms well-ordered films with a crystal structure that favors a high degree of orbital overlap between neighboring molecules in the direction parallel to the substrate surface.

The 2004 report by Jones *et al*. sparked a wave of new efforts to better understand the complex relationships between substitution pattern, electron affinity, air stability, film morphology, and electron mobility in PTCDI and NTCDI derivatives. For example, Thomas Weitz and co-workers investigated five different dicyano–PTCDI derivatives with various fluoroalkyl and fluoroarene substitutions at the imide positions of the PTCDI–$(CN)_2$ molecule and investigated how the substituents affect the film morphology, the electron mobility, and the rate at which the mobility degrades when the transistors are exposed to air for extended periods of time.[98] They found that the substitution pattern has indeed a profound effect on the film morphology. If the fluoroalkyl substituent is too short (CH_2CF_3), the molecules form either disordered or discontinuous films, and mobilities are below 10^{-5} cm^2/Vs. If the fluoroalkyl substituent is too long ($CH_2C_7F_{15}$), well-ordered films are obtained, but the mobilities are no greater than 0.05 cm^2/Vs. For the optimum fluoroalkyl length ($CH_2C_3F_7$), excellent film morphology and an electron mobility of 0.1 cm^2/Vs were obtained. Cyclic substituents

cause films to be less ordered and result in mobilities around 10^{-3} cm^2/Vs. Weitz *et al.* also showed that for all five dicyano–PTCDI derivatives the electron mobility measured in the vacuum-deposited films degrades with the same rate of about one order of magnitude per year when the transistors are stored in air. However, when the transistors are made using single-crystalline ribbons, rather than vacuum-deposited films, the air-induced mobility degradation is completely eliminated, which suggests that the grain boundaries present in vacuum-deposited films (but not in single-crystalline ribbons) play an important role in determining the air stability of organic semiconductors.[99]

Rüdiger Schmidt and co-workers synthesized and investigated 14 different PTCDI derivatives with six different fluorocarbon substituents at the imide positions and five different substitution patterns at the conjugated core.[100] Unlike Jones[97] and Weitz,[98,99] who employed cyano groups, Schmidt *et al.* substituted fluorine, chlorine, or bromine atoms at the bay positions of the conjugated core. Depending on the substituents, the electron affinity varied between 3.7 and 4.2 eV. Nine of the 14 compounds yielded *n*-channel transistor operation in air with electron mobilities above 0.01 cm^2/Vs. Ironically, the largest electron mobility in air (1.2 cm^2/Vs) was found for a derivative without core substituents and with simple fluoroalkyl substituents at the imide positions (PTCDI–$CH_2C_3F_7$; see Fig. 18b). The air stability of this material (and several others from the series) is excellent, with no detectable degradation of the electron mobility after continuous exposure to air for 60 days. Schmidt *et al.* convincingly showed that placing substituents at the bay positions of the conjugated core causes the core to twist as a result of steric hindrance, with profound consequences for the π-stacking of the molecules in the solid state. This explains why the largest mobility was obtained for a molecule without core substituents. The exact reason for the excellent air stability is still unclear.

For virtually all small-molecule organic semiconductors, the thin-film morphology is affected by the temperature of the substrate during film growth. This feature is useful to obtain optimum morphology and maximum mobility simply by adjusting the substrate temperature during the deposition. However, if the thin-film morphology is too sensitive with respect to the substrate temperature, it becomes difficult to maintain device-to-device uniformity over large substrates and substrate-to-substrate uniformity in large manufacturing volumes. Compared with many other small-molecule semiconductors, the carrier mobility in films of NTCDI and PTCDI derivatives appears to depend much stronger on the substrate temperature during deposition (see Fig. 19). This suggests that these compounds adopt a variety of crystal structures, depending on the kinetics during film formation.

The semiconductor films in all of the organic *n*-channel transistors discussed above were prepared by vacuum deposition. Because C_{60}, $F_{16}CuPc$, and all derivatives of NTCDI, PTCDI and thiophene or phenylene–thiophene oligomers with small substituents (or without any substituents) are insoluble in common organic solvents, they can usually not be deposited from solution. Some of the NTCDI, PTCDI and phenylene–thiophene derivatives with long or bulky substituents have good solubility, and a few of them have been used to prepare

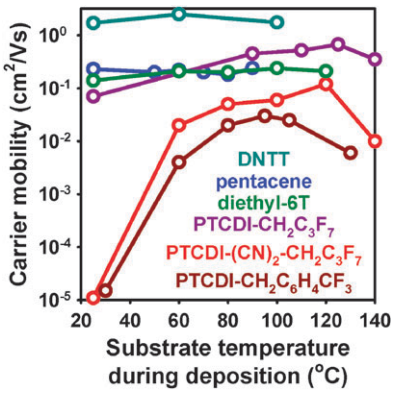

Fig. 19 Relationship between the carrier mobility in the transistor channel and the substrate temperature during the deposition of the organic semiconductor layer for five different small-molecule organic semiconductors. (Data from the following references: DNTT:[49], pentacene:[101], diethyl-sexithiophene[102], PTCDI–$CH_2C_3F_7$,[100] PTCDI–$(CN)_2$–$CH_2C_3F_7$,[98] PTCDI–$CH_2C_6H_4CF_3$.[103])

n-channel transistors by drop-casting or spin-coating, with mobilities around 0.1 cm^2/Vs and good air stability in some cases.[104–107] A number of soluble fullerene derivatives, such as phenyl–C_{61}–butyric acid methyl ester (PCBM), have also been employed to prepare organic *n*-channel transistors with solution-deposition methods.[108,109] Electron mobilities can reach 0.25 cm^2/Vs, but like C_{60} transistors, the performance of these devices degrades rapidly and substantially upon air exposure.

Finally, organic *n*-channel transistors have also been made using polymers. For example, Amit Babel and Samson Jenekhe have synthesized ladder poly(benzobisimidazobenzophenanthroline) (BBL; see Fig. 20a) and reported electron mobilities as large as 0.1 cm^2/Vs for *n*-channel transistors with a spin-coated active layer operating in air.[110,111] Sven Hüttner and co-workers have prepared poly(perylene bisimide acrylate) (PPerAcr; see Fig. 20b) and measured electron mobilities of 0.001 cm^2/Vs in devices with a spin-coated semiconductor operated in nitrogen.[112] Transistors with spin-coated films of poly{[bis(decyltetradecyl)-perylene diimide-diyl]-alt-(dithienothiophene-diyl)} (see Fig. 20c) prepared by Xiaowei Zhan and co-workers showed a mobility of 0.013 cm^2/Vs in nitrogen.[113]

By far the best performance for a polymer-based *n*-channel transistor has been realized by Zhihua Chen, He Yan and co-workers, who synthesized poly{[bis(octyldodecyl)-naphthalene-bis(dicarboximide)-diyl]-alt-(bithiophene)} (see Fig. 20d) and prepared transistors not only on glass, but also on flexible polymeric substrates, employing a variety of deposition methods, including spin-coating, gravure printing, and inkjet printing.[114,115] Record mobilities as large as 0.85 cm^2/Vs were achieved. In addition to providing fantastic electron mobilities, the semiconductor also has excellent air stability, in part due to the large electron affinity (4 eV). This clearly shows the enormous potential of conjugated polymers specifically synthesized for high-performance, air-stable transistors.

From a materials perspective, the carrier mobility is the most important electrical parameter of organic transistors. Fig. 21 summarizes the development of the field-effect mobility of *p*-channel and *n*-channel transistors based on small-molecule and polymeric semiconductors, beginning with the first reports

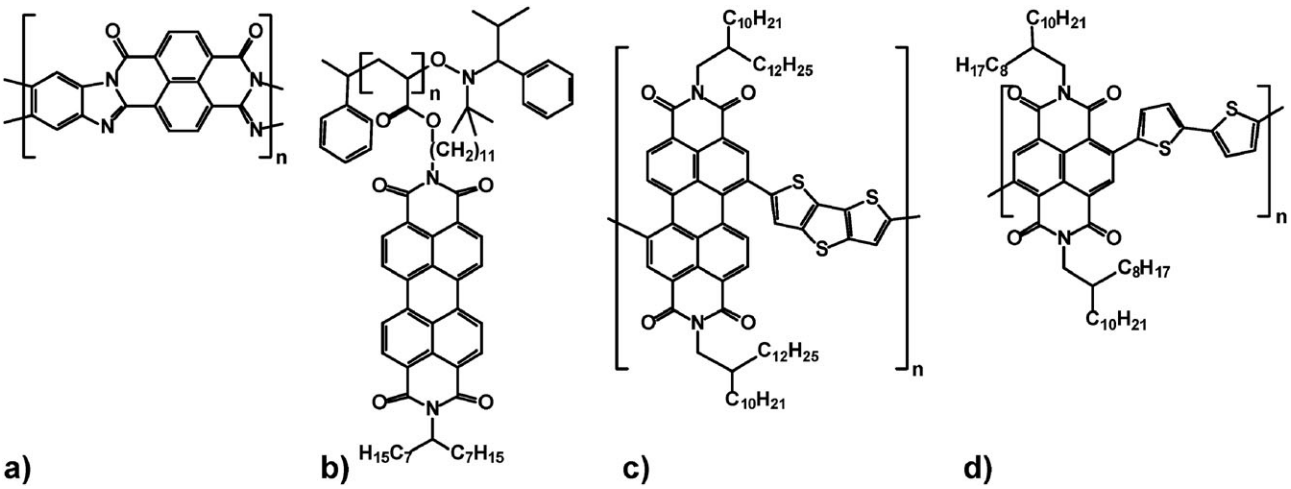

Fig. 20 Conjugated polymers for *n*-channel transistors. (a) Ladder poly(benzobisimidazobenzophenanthroline) (BBL).[110,111] (b) Poly(perylene bisimide acrylate) (PPerAcr).[112] (c) Poly{[bis(decyltetradecyl)-perylene diimide-diyl]-alt-(dithieno-thiophene-diyl)}.[113] (d) Poly{[bis(octyldodecyl)-naphthalene-bis(dicarboximide)-diyl]-alt-(bithiophene)}.[114,115]

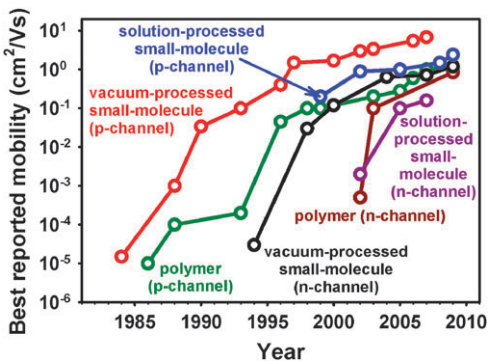

Fig. 21 Development of the carrier field-effect mobility (measured in ambient air) of *p*-channel and *n*-channel transistors based on small-molecule and polymeric semiconductors. The largest mobility for each of the six categories was taken from the following references: polymer *p*-channel transistors:[3] polymer *n*-channel transistors:[115] vacuum-processed small-molecule *p*-channel transistors:[4] vacuum-processed small-molecule *n*-channel transistors:[100] solution-processed small-molecule *p*-channel transistors:[62] solution-processed small-molecule *n*-channel transistors:[104,106]

by Kazuhiro Kudo and co-workers in 1984[24] and Akira Tsumura and co-workers in 1986.[12] As can be seen, mobilities have improved by about five orders of magnitude over the past 26 years and reached $\sim$1 cm^2/Vs for both *p*-channel and *n*-channel and both small-molecule and polymer transistors. For each material system, initial progress in mobility was quite rapid, but eventually slowed down.

Under certain conditions it is possible to operate the same field-effect transistor either as a *p*-channel transistor or as an *n*-channel transistor, simply by reversing the polarity of the applied gate-source and drain-source voltages. Field-effect transistors that can be operated in either *p*-channel or *n*-channel mode, depending on the polarity of the applied voltages, are called ambipolar transistors. Ambipolar transistors require that the energy barrier between the Fermi level of the source/drain contacts and the HOMO of the semiconductor as well as the barrier between the source/drain contacts and the LUMO of the semiconductor are *both* sufficiently small to permit balanced and efficient charge transfer of both positive and negative carriers. This means that if the semiconductor layer is composed of a single material, the HOMO–LUMO gap (or bandgap) of this material must be quite small, *i.e.* no greater than a few hundred meV. Most conjugated semiconductors, however, have much larger HOMO–LUMO gaps, usually greater than 1.5 eV, so that the injection of one carrier type is favored over that of the other, and this is why most organic transistors are not ambipolar. Ambipolar transistor operation can be achieved either by using a semiconductor with a small HOMO–LUMO gap,[116] or by employing a blend of two different semiconductors,[117] or by utilizing a heterostructure (bilayer) of two different semiconductors.[118] For integrated-circuit applications, ambipolar transistor behavior is undesirable, since it causes large off-state drain currents, small noise margins, and large power consumption. Ambipolar transistor do, however, present a unique opportunity to study light-emitting field-effect devices.[119]

4. Manufacturing

The most useful organic transistor implementation for practical applications is the thin-film transistor (TFT). The TFT concept was initially proposed and developed by Paul Weimer in the 1960s for transistors based on polycrystalline inorganic semiconductors, such as evaporated cadmium sulfide.[120] The concept was later extended to TFTs based on plasma-enhanced chemical-vapor deposited (PECVD) hydrogenated amorphous silicon (a-Si : H) TFTs.[121] Today, a-Si : H TFTs are widely employed as the pixel drive devices in active-matrix liquid-crystal displays (AMLCDs) on glass substrates.[1] Organic TFTs were first reported in the 1980s.[12,24,26,122] To make an organic TFT, the organic semiconductor and the other materials required (gate electrode, gate dielectric, source and drain contacts) are deposited as thin layers on the surface of an electrically insulating substrate, such as glass or plastic foil. The total thickness of the devices can be less than 50 nm. Depending on the sequence in which the materials

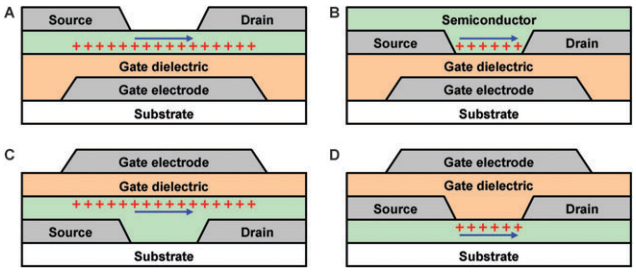

Fig. 22 Schematic cross-sections of the four principle thin-film transistor (TFT) structures. The carrier channel is schematically shown in red. (a) Bottom-gate (inverted) staggered TFT. (b) Bottom-gate (inverted) coplanar TFT. (c) Top-gate staggered TFT. (d) Top-gate coplanar TFT.

are deposited, four different TFT architectures can be distinguished, as shown in Fig. 22.

Each of the four TFT structures shown in Fig. 22 has certain advantages and disadvantages. For example, the presence of an energy barrier at the interfaces between the organic semiconductor and the source and drain contacts is expected to impede the exchange of charge carriers between the contacts and the semiconductor. Experiments and simulations have shown that for the same energy barrier height, TFTs with a staggered structure (**A**, **C**) have the advantage of being less affected by this energy barrier than TFTs with a coplanar structure (**B**, **D**).[123–127] However, in case of the bottom-gate coplanar structure (**B**), the effect of the energy barrier on the carrier exchange efficiency can be substantially reduced by modifying the surface of the source and drain contacts with a thin organic monolayer carrying an appropriate dipole moment[57,61,86,97,128,129] or with a thin metal oxide.[130–133]

An important advantage of the bottom-gate coplanar structure (**B**) is that the gate dielectric layer and the source and drain contacts are prepared *before* the organic semiconductor is deposited. The reason why this is important is that many high-mobility organic semiconductors, especially vacuum-deposited small-molecule materials, but also many high-mobility polymers, adopt a thin-film microstructure that is very sensitive to external perturbations. For example, vacuum-deposited pentacene films undergo an irreversible phase transition, associated with a substantial drop in carrier mobility, when exposed to organic solvents, such as those employed for the solution-based deposition of polymer gate dielectrics and in photolithographic contact patterning processes.[134] With the bottom-gate coplanar structure (**B**), methods involving solvents and/or thermal treatments can be safely employed to prepare the gate dielectric and the contacts without harming the semiconductor layer.

A variety of methods exist for the deposition and patterning of the individual layers of the TFT. For example, gate electrodes and source and drain contacts are often prepared using inorganic metals. Non-noble metals, such as aluminium or chromium, are suitable for the gate electrodes in the inverted device structures, since these metals have excellent adhesion on glass and plastic substrates. Noble metals, most notably gold, are a popular choice for the source and drain contacts, since they tend to provide better contact performance than other metals, at least for most *p*-channel TFTs, but also for many *n*-channel TFTs. The metals are conveniently deposited by thermal evaporation in vacuum and patterned either by photolithography in combination with lift-off[135] or wet-chemical etching,[136] by deposition through a shadow mask,[137] by digital lithography using an inkjet-printed wax-based etch resist,[138] or by inkjet-printing of a metal nanoparticle suspension (followed by drying of the solvent and sintering of the nanoparticles).[139] The key parameter for the patterning of the source and drain contacts is the minimum achievable feature size, which ideally should be as small as possible. With shadow-masking it is in principle possible to produce feature sizes well below 1 μm,[140] although 5 to 10 μm is a more realistic lower limit for shadow masks compatible with large-area substrates.[141] Photolithography reliably produces features of approximately 1 or 2 μm or slightly below.[142] The feature size achievable by inkjet-printing depends heavily on the droplet volume and can be as small as about 1 or 2 μm (see Fig. 23[143,144]). Self-aligned inkjet-printing that exploits the selective dewetting from hydrophobic surfaces has been employed to produce organic transistors with a channel length as small as 100 nm.[145–147] High-resolution inkjet printing is a relatively slow process. To alleviate this limitation and achieve acceptable manufacturing throughput, it may be useful to apply high-resolution inkjet printing only to the most demanding features (source/drain contacts) and utilize patterning techniques with lower resolution (but greater speed) for all of the less demanding features (row and column lines, interconnect lines, semiconductor layer, vias, passivation, *etc.*).

An alternative to inorganic metals are conducting polymers, such as polyaniline (PANI) and poly(3,4-ethylenedioxythiophene):poly(styrene sulfonic acid) (PEDOT:PSS, see Fig. 24). These are chemically doped conjugated polymers that have electrical conductance in the range between 0.1 and 1000 S cm^{-1}. Conducting polymers can be processed from organic solutions (PANI) or from aqueous dispersions (PEDOT:PSS), so the gate electrodes and the source and drain contacts of

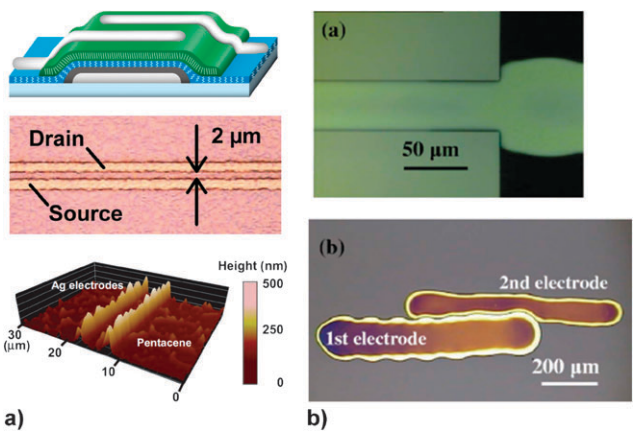

Fig. 23 (a) Subfemtoliter inkjet printing of metal source and drain contacts for inverted staggered pentacene TFTs. (Reprinted with permission from ref. 143: T. Sekitani *et al.*, *Proceedings of the National Academy of Sciences*, 2008, **105**, 4976. Copyright 2008 by the National Academy of Sciences, USA) (b) Self-aligned inkjet printing of metal source and drain contacts for top-gate polymer TFTs. (Reprinted with permission from ref. 147: N. Zhao *et al.*, *J. Appl. Phys.*, 2007, **101**, 064513. Copyright 2007 by the American Institute of Physics.)

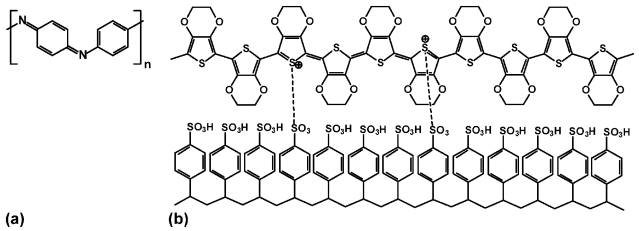

Fig. 24 Conducting polymers for the gate electrodes and the source and drain contacts of organic transistors. (a) Polyaniline (PANI). (b) Poly(3,4-ethylenedioxythiophene):poly(styrene sulfonic acid) (PEDOT:PSS).

organic TFTs can be conveniently prepared by spin-coating and photolithography,[142,148] or by direct inkjet-printing.[145] Fig. 25 shows a scanning electron microscopy (SEM) image of a bottom-gate coplanar pentacene TFT with spin-coated and photolithographically patterned PEDOT:PSS gate electrode and source and drain contacts.[148]

The gate dielectric material and the processing conditions for the gate dielectric (*i.e.*, temperature, plasma, organic solvents, *etc.*) must be compatible with the substrate and in case of the top-gate structures (**C**, **D**) also with the previously deposited organic semiconductor layer. For example, chemical-vapor-deposited (CVD) silicon oxide and silicon nitride, which are popular gate dielectric materials for amorphous and polycrystalline silicon TFTs, may not be suitable for use on flexible polymeric substrates, since the high-quality growth of these dielectrics often requires temperatures that exceed the glass transition temperature of conventional polymeric substrate materials. Insulating polymers, such as polystyrene or polyimide, are usually suitable for bottom-gate TFTs and even for top-gate TFTs based on certain polymeric semiconductors not affected by the solvents from which the dielectric is deposited.

The thickness of the gate dielectric layer is usually a compromise between the competing requirements for large gate coupling, low operating voltages, and small leakage currents. Large gate coupling (*i.e.*, a large gate dielectric capacitance per unit area) means that the transistors can be operated with low voltages, which is important when the TFTs are designed for portable or handheld devices that are powered by small batteries or by near-field radio-frequency coupling. Also, a large dielectric capacitance ensures that the carrier density in

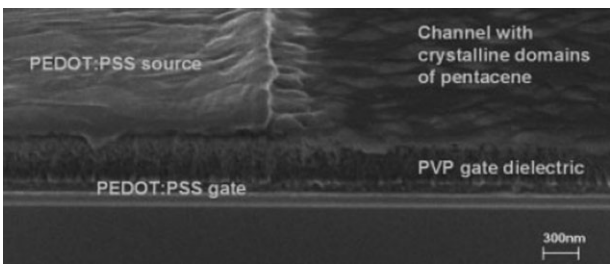

Fig. 25 Scanning electron microscopy (SEM) image of a bottom-gate coplanar pentacene TFT with spin-coated and photolithographically patterned PEDOT:PSS gate electrode and source and drain contacts (Reproduced with permission from ref. 148: M. Halik *et al.*, *Adv. Mater.*, 2002, **14**, 1717. Copyright 2002 by Wiley-VCH Verlag GmbH & Co. KGaA.)

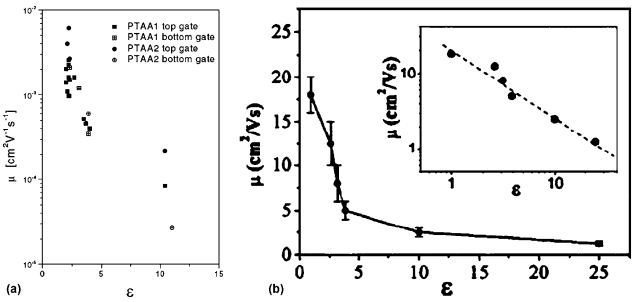

Fig. 26 Relationship between the permittivity of the gate dielectric and the carrier mobility in the channel of organic transistors. (a) Polytriarylamine TFT (Reproduced with permission from ref. 149: J. Veres *et al.*, *Adv. Funct. Mater.*, 2003, **13**, 199. Copyright 2003 by Wiley-VCH Verlag GmbH & Co. KGaA.) (b) Rubrene single-crystal field-effect transistor (Reprinted with permission from ref. 150: A. F. Stassen *et al.*, *Appl. Phys. Lett.*, 2004, **85**, 3899. Copyright 2004 by the American Institute of Physics.)

the channel is controlled by the gate-source voltage, and not by the drain-source voltage, which is especially critical for TFTs with short channel length. One way to obtain a large gate dielectric capacitance is to employ a dielectric material with large permittivity ε (since $C_{diel} = \varepsilon \cdot \varepsilon_0 / t$, where C_{diel} is the gate dielectric capacitance per unit area, ε_0 is the permittivity of free space, and t is the gate dielectric thickness), for example a transition metal oxide (TiO_2, ZrO_2, HfO_2). However, as several authors have shown,[36,149–151] the carrier mobility in organic field-effect transistors is systematically reduced as the permittivity of the gate dielectric is increased, presumably due to enhanced localization of carriers by local polarization effects (see Fig. 26).

As an alternative to high-permittivity metal oxides, low-permittivity dielectrics with very small thickness or thin multilayer dielectrics with specifically tailored properties may be employed. The greatest concern with thin dielectrics is the inevitable increase in gate leakage due to defects and quantum-mechanical tunnelling as the dielectric thickness is reduced. A number of promising paths towards high-quality thin dielectrics with low gate leakage for low-voltage organic TFTs have recently emerged. One such approach is the use of very thin cross-linked polymer films deposited by spin-coating.[152–154] With a thickness of around 10 to 20 nm these dielectrics provide capacitances as large as 0.3 $\mu F/cm^2$, leakage current densities below 10^{-6} A cm^{-2} (with an electric field of about 3 MV cm^{-1} applied across the film), and excellent low-voltage TFT characteristics (with supply voltages of about 2 to 3 V).

An interesting approach for TFTs with the bottom-gate structure (**A**, **B**) is the use of a thin oxide layer (SiO_2 or AlO_x) obtained by oxidation of the gate electrode surface in combination with a high-quality insulating organic self-assembled monolayer (SAM) or multilayer.[155–166] These hybrid dielectrics usually have a total thickness between 5 and 10 nm, provide a capacitance between 0.3 and 1 $\mu F/cm^2$, and allow the TFTs to operate with gate-source and drain-source voltages between 2 and 3 V. The thin oxide layer can be obtained either by anodization,[155,156] by UV/ozone treatment,[157] or by plasma oxidation.[158–166] The organic monolayer can be prepared from solution,[155,157–162,164] from the vapor phase,[163,165] or by

microcontact printing.[166] Despite the small dielectric thickness and the low process temperatures (usually below 100 °C, compatible with flexible polymeric substrates), the leakage current densities are usually below 10^{-6} A cm^{-2}. Due to their robustness and versatility, these thin hybrid dielectrics are also useful for a variety of electronic devices other than organic transistors.[167–170]

Organic TFTs with gate capacitance approaching or even exceeding 10 μF/cm^2 have been realized using polymer electrolytes or ion gels.[171–175] In this case, the gate capacitance is not determined by the dielectric thickness, but by the capacitance of the electric double layer.

5. Operation

A field-effect transistor operates as a voltage-controlled current source. By applying a voltage (the gate-source voltage V_{GS}) across the gate dielectric, a sheet of mobile charge carriers is induced in the semiconductor that allows a current (the drain current I_D) to flow through the semiconductor when another voltage (the drain-source voltage V_{DS}) is applied between drain and source (see Fig. 27).

Because the charge carrier density in the semiconductor is a function of the gate-source voltage, the drain current can be modulated by adjusting the gate-source voltage. This modulation of the drain current (output current) with the gate-source voltage (input voltage) is quantitatively described by the most fundamental field-effect transistor parameter, the transconductance g_m:

$$i_D = g_m V_{GS} \quad (1)$$

$$g_m = \frac{i_D}{v_{GS}} = \frac{\partial I_D}{\partial V_{GS}}\bigg|_{V_{DS}=\text{const.}} \quad (2)$$

v_{GS}, i_G, v_{DS}, i_D—small-signal parameters (derivatives about the bias point)
V_{GS}, I_G, V_{DS}, I_D—large-signal parameters

Silicon MOSFETs normally operate in inversion mode, *i.e.* the drain current is due to minority carriers generated by inverting the conductivity at the semiconductor/dielectric interface from *p*-type to *n*-type (for *n*-channel MOSFETs) or from *n*-type to *p*-type (for *p*-channel MOSFETs). In the regions near the source and drain contacts, the silicon is heavily doped (*n*-type for *n*-channel MOSFETs, *p*-type for *p*-channel MOSFETs), so that minority carriers are easily exchanged between the contacts and the channel, while the undesirable flow of majority carriers from drain to source is efficiently blocked by a space charge region. For a thorough discussion of the device structure and the operating principles

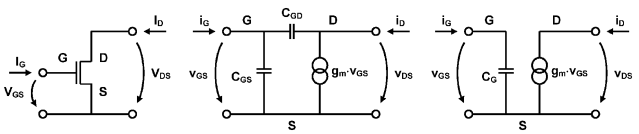

Fig. 27 Schematic (left) and two small-signal equivalent circuits (center and right) of a field-effect transistor, showing the gate-source capacitance C_{GS}, the gate-drain capacitance C_{GD}, the equivalent gate capacitance C_G, and the current source $g_m \cdot v_{GS}$.

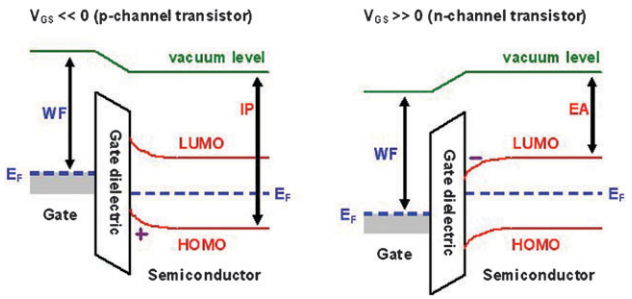

Fig. 28 Energy-level diagrams across the semiconductor/dielectric interface of organic transistors, showing the accumulation of positive charge carriers for negative gate-source voltages (*p*-channel transistor) and the accumulation of negative carriers for positive gate-source voltages (*n*-channel transistor). Abbreviations: WF: work function; EA: electron affinity; IP: ionization potential; LUMO: lowest unoccupied molecular orbital; HOMO: highest occupied molecular orbital; E_F: Fermi energy level.

of silicon MOSFETs, the reader is referred to the authoritative text by Simon Sze and Kwok Ng.[176]

Unlike silicon MOSFETs, organic TFTs typically utilize intrinsic semiconductors. Therefore, organic TFTs usually do not operate in inversion mode, but in accumulation mode. Positively charged carriers are accumulated in the semiconductor near the dielectric interface when a negative gate-source voltage is applied (*p*-channel transistor), or negative charges are accumulated when a positive gate-source voltage is applied (*n*-channel transistor), as shown schematically in Fig. 28.

In organic TFTs, source and drain are usually implemented by directly contacting the intrinsic semiconductor with a metal (*i.e.*, without doped contact regions). Depending on the choice of the materials for the semiconductor and the contacts, the charge transfer of one carrier type is usually more efficient than that of the other, and this determines whether the device operates as a *p*-channel TFT or as an *n*-channel TFT (see Fig. 29).

Despite the fact that the transport physics in organic TFTs is different from that in silicon MOSFETs, the current–voltage

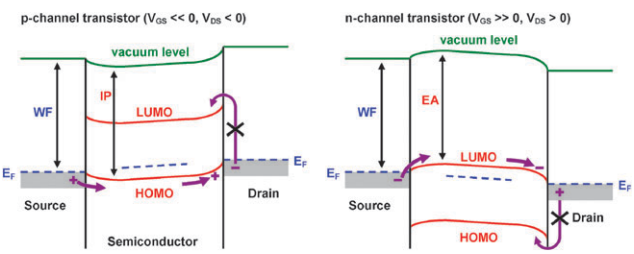

Fig. 29 Energy-level diagrams along the carrier channel of organic transistors, showing the transport of positive carriers from the source through the semiconductor to the drain in the case of a *p*-channel transistor (left), and the transport of negative carriers from the source through the semiconductor to the drain in the case of a *n*-channel transistor (right). In *p*-channel transistors the transfer of negative charges into the semiconductor is blocked due to the large energy difference between the Fermi level of the contact and the LUMO of the semiconductor, and in *n*-channel transistors the transfer of positive charges is blocked by the energy barrier between the contact and the HOMO of the semiconductor.

characteristics can to first order be described with the same formalism:

$$I_D = \frac{\mu C_{diel} W}{L}\left((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right) \quad \text{for} |V_{GS} - V_{th}| > |V_{DS}| \text{ (linear regime)} \tag{3}$$

$$I_D = \frac{\mu C_{diel} W}{2L}(V_{GS} - V_{th})^2 \quad \text{for } |V_{DS}| > |V_{GS} - V_{th}| > 0 \text{ (saturation regime)} \tag{4}$$

Eqn (3) describes the relationship between the drain current I_D, the gate-source voltage V_{GS} and the drain-source voltage V_{DS} in the linear regime, while eqn (4) relates I_D, V_{GS} and V_{DS} in the saturation regime. C_{diel} is the gate dielectric capacitance per unit area, μ is the carrier mobility in the semiconductor, W is the channel width, and L is the channel length of the transistor. For silicon MOSFETs, the threshold voltage V_{th} is defined as the minimum gate-source voltage required to induce strong inversion.[176] Organic TFTs do not operate in inversion mode, so strictly speaking the threshold voltage cannot be defined for organic TFTs. The threshold voltage concept is nonetheless useful for organic TFTs, since the threshold voltage is the minimum gate-source voltage required to obtain appreciable drain current, and because the threshold voltage marks the transition between the different regions of operation.

By combining eqn (2)–(4), the following expressions for the transconductance in the linear and saturation regimes can be derived:

$$g_{m,lin} = \frac{\mu C_{diel} W}{L} V_{DS} \quad \text{for} |V_{GS} - V_{th}| > |V_{DS}| \text{ (linear regime)} \tag{5}$$

$$g_{m,sat} = \frac{\mu C_{diel} W}{L}(V_{GS} - V_{th}) \quad \text{for } |V_{DS}| > |V_{GS} - V_{th}| > 0 \text{ (saturation regime)} \tag{6}$$

By rearranging eqn (3) and (4), expressions for the carrier field-effect mobility in the linear and saturation regimes can be derived:

$$\mu_{lin} = \frac{L}{C_{diel} W V_{DS}} \frac{\partial I_D}{\partial V_{GS}} \quad \text{for } |V_{GS} - V_{th}| > |V_{DS}| \text{ (linear regime)} \tag{7}$$

$$\mu_{sat} = \frac{2L}{C_{diel} W}\left(\frac{\partial \sqrt{I_D}}{\partial V_{GS}}\right)^2 \quad \text{for } |V_{DS}| > |V_{GS} - V_{th}| > 0 \text{ (saturation regime)} \tag{8}$$

Fig. 30 shows the current–voltage characteristics of an organic TFT fabricated on a glass substrate using the bottom-gate (inverted) staggered device structure (shown schematically in Fig. 22a), with a thin layer of vacuum-deposited aluminium as the gate electrode, a hybrid gate dielectric based on an oxygen-plasma-grown AlO_x layer (3.6 nm thick) and an alkylphosphonic acid-based self-assembled monolayer prepared from solution (1.7 nm thick), a thin layer of vacuum-evaporated dinaphtho-[2,3-*b*:2′,3′-f]thieno[3,2-*b*]thiophene (DNTT) as the semiconductor, and source/drain contacts prepared by evaporating gold through a polyimide shadow mask. Compared with pentacene, DNTT provides similar carrier mobility, but better air stability (see Fig. 13). The gate dielectric has a capacitance per unit area (C_{diel}) of 0.8 μF/cm^2, and the TFT has a channel width (W) of 100 μm and a channel length (L) of 10 μm. The device operates as a *p*-channel transistor with a threshold voltage of −1.4 V. Using eqn (2), (7) and (8), the transconductance as well as the mobility in the linear regime (V_{DS} = −0.1 V) and in the saturation regime (V_{DS} = −1.5 V) were calculated and plotted as a function of the gate-source voltage.

In Fig. 30b it can be seen that depending on the gate-source voltage, the drain current varies between 10^{-13} and 10^{-6} A (for V_{DS} = −0.1 V) or between 10^{-12} and 10^{-5} A (for V_{DS} = −1.5 V). The ratio between the maximum drain current (in the on-state of the transistor) and the minimum drain current (in the off-state of the transistor) is about 10^7; this ratio is called the on/off drain current ratio, or simply the on/off ratio of the transistor.

Eqn (3) and (4) describe the drain current for gate-source voltages above the threshold voltage. Below the threshold voltage there is a region in which the drain current depends exponentially on the gate-source voltage. This is the subthreshold region. For the transistor in Fig. 30 the subthreshold region extends between $V_{GS} \sim -1$ V (the switch-on voltage V_{so}) and $V_{GS} \sim -1.4$ V (the threshold voltage V_{th}). The switch-on voltage V_{so} marks the gate-source voltage at which the drain current reaches a minimum.[177] In the subthreshold region the drain current is due to carriers that have sufficient thermal energy to overcome the gate-voltage-controlled energy barrier near the source contact and mainly diffuse, rather than drift, through the semiconductor to the drain contact:

$$I_D = I_0 \exp\left(\frac{q|V_{GS} - V_{FB}|}{nkT}\right) \text{ for } V_{GS} \text{ between } V_{th} \text{ and } V_{so} \tag{9}$$

The slope of the log(I_D) *versus* V_{GS} curve in the subthreshold region is determined by the ideality factor n and the temperature T (q is the electronic charge and k is Boltzmann's constant). It is usually quantified as the inverse subthreshold slope S (also called subthreshold swing):

$$S = \frac{\partial V_{GS}}{\partial(\log_{10} I_D)} = \frac{nkT}{q}\ln 10 \tag{10}$$

The ideality factor n is determined by the density of trap states at the semiconductor/dielectric interface, N_{it}, and the gate dielectric capacitance, C_{diel}:

$$n = 1 + \frac{qN_{it}}{C_{diel}} \tag{11}$$

$$S = \frac{kT}{q}\ln 10\left(1 + \frac{qN_{it}}{C_{diel}}\right) \tag{12}$$

When N_{it}/C_{diel} is small, the ideality factor n approaches unity. Silicon MOSFETs usually have very small interface trap

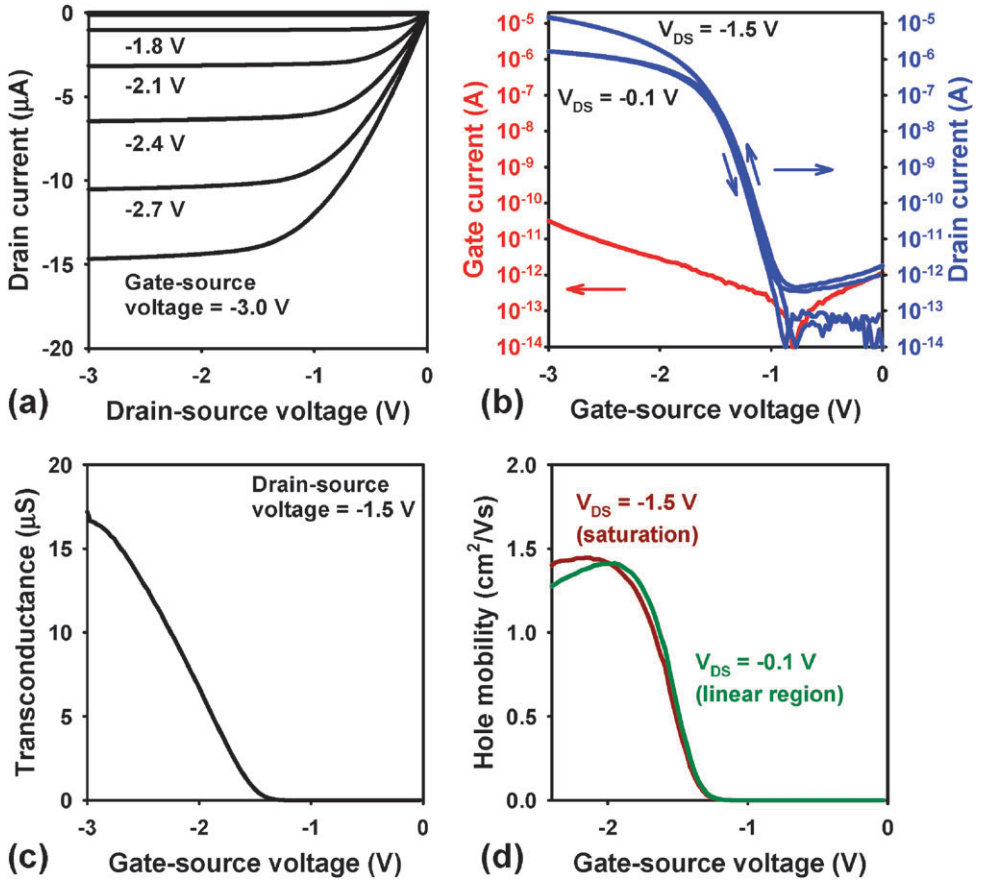

Fig. 30 Electrical characteristics of an organic *p*-channel TFT on a glass substrate using dinaphtho-[2,3-*b*:2′,3′-f]thieno[3,2-*b*]thiophene (DNTT; see Fig. 13b) as the semiconductor. The TFT has a channel length of 10 μm and a channel width of 100 μm. (a) Output characteristics (I_D *versus* V_{DS}). (b) Input characteristics (I_G *versus* V_{GS}) and transfer characteristics (I_D *versus* V_{GS}). (c) Transconductance g_m *versus* V_{GS}, calculated using eqn (2). The maximum transconductance is approximately 15 μS. (d) Carrier field-effect mobility in the linear and saturation regime, calculated using eqn (7) and (8). The maximum mobility is approximately 1.5 cm^2/Vs.

densities and often come close to the ideal room-temperature subthreshold swing of 60 mV/decade, since the quality of the Si/SiO_2 interface is very high. In organic TFTs the semiconductor/dielectric interface is typically of somewhat lower quality, mainly because the materials are deposited at much lower temperature, and thus the subthreshold swing is usually larger. The TFT in Fig. 30 has a subthreshold swing of 80 mV/decade (extracted from the slope of the $\log(I_D)$ *versus* V_{GS} curve in the region $-1.4\ V < V_{GS} < -1\ V$), from which an interface trap density of $2 \times 10^{12}\ cm^{-2}\ V^{-1}$ is calculated using eqn (12).

The subthreshold region extends between the threshold voltage V_{th} and the switch-on voltage V_{so}. Below the switch-on voltage (−1 V for the TFT in Fig. 30) the drain current is limited by charge leakage through the semiconductor, through the gate dielectric, or across the substrate surface. This off-state drain current should be as small as possible, since it limits the applicability of the transistor as a switch, and because the off-state drain current contributes to the static power consumption. The TFT in Fig. 30 has an off-state current of 0.1 pA for $V_{DS} = -0.1$ V and 1 pA for $V_{DS} = -1.5$ V, which corresponds to a on off-state resistance of approximately 1 TΩ.

In the ideal field-effect transistor, the static gate current is zero, since ideally the gate dielectric blocks any direct charge flow between the gate electrode on one side and the semiconductor and the source and drain contacts on the other side. In reality, a non-zero gate current I_G can usually be measured, especially if the gate dielectric is very thin. The TFT in Fig. 30 has a maximum static gate current of about 30 pA at $V_{GS} = -3$ V and $V_{DS} = -1.5$ V.

When the voltage applied across the gate dielectric changes over time, the amount of electronic charge on the gate electrode and in the semiconductor channel also changes over time:

$$\frac{\partial Q_G}{\partial t} = C_G \frac{\partial v_{GS}}{\partial t} \qquad (13)$$

The more rapidly the gate-source voltages changes, the more electronic charge is transported across the input of the transistor per unit time. This charge flow at the gate of the transistor can be interpreted as a displacement current, *i.e.* as the imaginary part of the complex gate current, i_G:

$$i_G = \frac{\partial q_G}{\partial t} = C_G \frac{\partial v_{GS}}{\partial t} = j\omega C_G v_{GS} = j2\pi f C_G v_{GS} \qquad (14)$$

where q_G is the gate charge, C_G is the equivalent gate capacitance, $j = \sqrt{-1}$ is the imaginary unit, $\omega = 2\pi \cdot f$ is the angular frequency, and f is the frequency at which the gate-source voltage changes.

Eqn (14) indicates that the gate current i_G increases linearly with frequency. In contrast, the drain current i_D is independent of the frequency. As the frequency is increased, the current gain, which is defined as the ratio of the absolute values of the drain current i_D and the gate current i_G, therefore decreases. When the current gain drops below unity, the transistor can no longer be operated in a useful manner. The frequency at which the current gain is unity is therefore defined as the cutoff frequency f_T:

$$\frac{|i_D|}{|i_G|} = \frac{g_m v_{GS}}{2\pi f C_G v_{GS}} = \frac{g_m}{2\pi f C_G} \quad (15)$$

$$f_T = f\left(\frac{|i_D|}{|i_G|} = 1\right) \quad (16)$$

$$f_T = \frac{g_m}{2\pi C_G} \quad (17)$$

According to eqn (17), the cutoff frequency is determined only by the transconductance g_m and the equivalent gate capacitance C_G. From the perspective of dynamic performance, g_m and C_G are therefore the two most important transistor parameters. The transconductance g_m can be determined from the current–voltage characteristics of the transistor, as shown in Fig. 30c, or it can be approximately predicted based on the charge carrier mobility μ, the lateral dimensions L and W, and the voltages V_{DS}, V_{GS} and V_{th} using eqn (5) and (6).

Estimating the equivalent gate capacitance C_G is more difficult, due to the so-called Miller effect. According to Fig. 27, the equivalent gate capacitance C_G is the capacitance between the gate electrode and the source contact that results from the combined contributions of the gate-source capacitance C_{GS} and the gate-drain capacitance C_{GD}. Both C_{GS} and C_{GD} have an intrinsic component (given by the interaction between the gate and the channel charge) and a parasitic component (given by the geometric overlap between the gate electrode and the source and drain contacts). Because C_{GD} is located between the input and the output of the transistor, its contribution to the equivalent gate capacitance is a function of the transconductance g_m and the load resistance R_L of the transistor, as described by the Miller effect:

$$C_G = C_{GS} + C_M = C_{GS} + C_{GD}(1 + g_m R_L) \quad (18)$$

where C_M is the Miller capacitance and R_L is the load resistance (*i.e.*, the external resistance connected between the drain and the source). The product $g_m \cdot R_L$ is the voltage gain ($\partial V_{DS}/\partial V_{GS}$) of the transistor, so the Miller effect accounts for the increase in the input capacitance (C_G) due to the amplification of the capacitance between the input and the output (C_{GD}).

For $g_m \cdot R_L \sim 0$, a lower limit for the equivalent gate capacitance ($C_G \sim C_{GS} + C_{GD}$) and hence an upper limit for the cutoff frequency f_T can be estimated:

$$C_G(g_m R_L \sim 0) = C_{GS} + C_{GD} \sim C_{diel} W(L + 2 \cdot \Delta L) \quad (19)$$

$$f_T = \frac{g_m}{2\pi C_G} \sim \frac{g_m}{2\pi C_{diel} W(L + 2 \cdot \Delta L)} \quad (20)$$

where C_{diel} is the gate dielectric capacitance per unit area, W is the channel width, L is the channel length, and ΔL is the overlap between the gate electrode and the source and drain contacts (see Fig. 31).

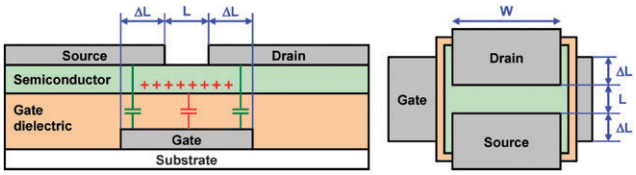

Fig. 31 Intrinsic gate capacitance due to the interaction between the gate and the channel charge (shown in red) and parasitic gate capacitances due to the geometric gate/source and gate/drain overlaps (shown in green) in a field-effect transistor (left: cross-section; right: top view).

For the TFT in Fig. 30, C_{diel} = 0.8 μF/cm^2, W = 100 μm, $L = \Delta L$ = 10 μm, so $C_G \sim$ 25 pF according to eqn (19). At a gate-source voltage of −3 V, the TFT has a transconductance of about 15 μS (see Fig. 30c), so using eqn (20) the cutoff frequency at V_{GS} = −3 V is estimated to be approximately 100 kHz.

One way to experimentally determine the maximum switching frequency of a transistor is to manufacture and characterize a ring oscillator. A ring oscillator is a circuit that consists of an odd number of inverters connected in series, with the output of the last inverter connected to the input of the first inverter. When the input of the first inverter changes from "low" to "high", its output switches from "high" to "low". Since the transistors that make up the inverters contain capacitive elements, the output signal does not switch instantaneously; the time that passes between the change in input signal and the resulting change in output signal is the signal delay per stage (or stage delay). The change in signal propagates through the inverter chain until (after a time that is the product of the stage delay and the number of inverters) it reaches the end of the ring oscillator. Due to the feedback loop (and because the number of inverters is odd), this causes the input of the first inverter to flip again, this time from "high" to "low". The result is that the output of the ring oscillator continuously oscillates between "low" and "high" with a period that is identical to the stage delay multiplied by twice the number of inverter stages.

Fig. 32 shows the schematic and the electrical characteristics of a unipolar inverter that was manufactured on a glass substrate using DNTT TFTs similar to that in Fig. 30. The term "unipolar" describes a circuit that utilizes either *p*-channel or *n*-channel transistors, but not both. In a unipolar inverter, one of the two transistors acts as a drive transistor (having its gate connected to the input and its drain to the output of the inverter), while the other transistor acts as a load device (having its drain connected to the supply voltage node and its source to the output). The inverter in Fig. 32 utilizes a saturated-load design where the gate of the load transistor is connected to the supply voltage (V_{DD}) node. (In an alternative design, the load transistor has its gate connected to the inverter output.) In the case of the saturated-load inverter, the gate-source and drain-source voltages of the load transistor are identical ($V_{GS} = V_{DS}$), so that the load transistor is always biased in saturation. When the input of the inverter is "low" (∼0 V), the drive TFT is in the off-state (has a very

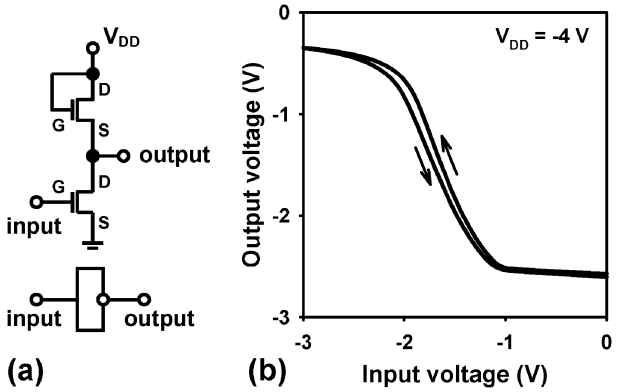

Fig. 32 (a) Schematic of a unipolar inverter based on a saturated-load design. (b) Transfer characteristics of a saturated-load inverter with DNTT *p*-channel TFTs.

large resistance), so the output node is "pulled up" through the load transistor and the output potential is approximately the difference between the supply voltage V_{DD} and the threshold voltage of the load transistor. When the input of the inverter is "high" (~ -3 V), the drive TFT is in the linear regime (has a small resistance), so the output node is "pulled down" through the drive transistor and the output potential is close to the ground potential. As a result, the output of the inverter is "high" when the input is "low" and "low" when the input is "high"; hence the name "inverter". The stage delay of the inverter is determined by the transconductance and the equivalent gate capacitance of the transistors and by the output load of the inverter.

The 5-stage ring oscillator in Fig. 33 oscillates with a period of 200 μsec (at $V_{DD} = -3$ V), *i.e.* the signal delay per stage is 20 μsec. This indicates that the maximum frequency at which the transistors can be operated is about 1/(40 μsec) = 25 kHz (at $V_{DD} = -3$ V). This value is smaller by a factor of 4 than the cutoff frequency calculated using eqn (20), which ignores the Miller effect, as discussed above. Therefore, eqn (20) provides a simple way to estimate an upper limit of the maximum frequency of operation of a field-effect transistor.

The smallest signal delay per stage reported for a ring oscillator based on organic TFTs is 0.7 μsec,[178,179] with a few additional reports of signal delays between 1 and 3 μsec.[61,180–182]

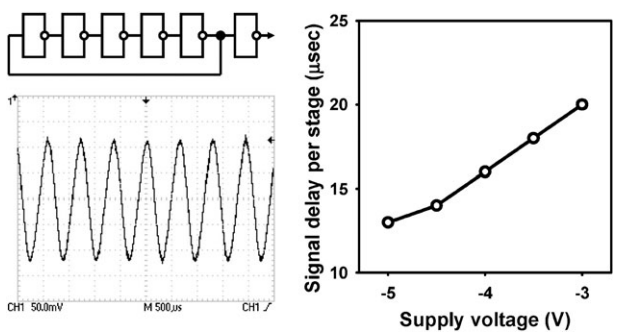

Fig. 33 Schematic, output signal, and signal propagation delay as a function of supply voltage of a unipolar 5 stage ring oscillator based on DNTT saturated load inverters. (The purpose of the sixth inverter at the output of the ring oscillator is to reduce the capacitive load exerted on the ring oscillator by the measurement setup).

Organic ring oscillators with such small signal delays have so far been obtained only by employing fairly thick gate dielectrics (to keep the gate capacitance small) and by applying fairly high supply voltages, usually above 50 V (to maximize the transconductance). By combining a thin gate dielectric with a capacitance of about 1 μF/cm^2,[160] a conjugated semiconductor with a mobility of about 1 cm^2/Vs,[49] and a high-resolution printing process to realize lateral dimensions (L and ΔL) of about 2 μm,[143–147] organic inverters with a stage delay below 1 μsec at a supply voltage of 3 V or less appear feasible. (For comparison, the signal delay per stage of ring oscillators based on silicon MOSFETs at the 45 nm technology node is about 5 psec at $V_{DD} \sim 1$ V,[183] *i.e.* the maximum frequency of operation of these transistors is on the order of 10^{10} Hz.)

In principle, fully functional organic large-scale-integrated circuits can be realized using a unipolar circuit design.[184,185] However, an important limitation of unipolar circuits is that whenever the input voltage is "high" (so that the drive transistor is in the linear regime), a large current flows between the supply voltage node and the ground node. The reason is that the load transistor of a unipolar circuit is permanently conducting. For example, the load transistor of the inverter in Fig. 32 has a constant resistance of about 4 MΩ, so whenever the inverter input is "high", a current of about 1 μA flows through the inverter. This corresponds to a static power dissipation of 4 μW per stage. For a system with 10 000 circuit elements, the static power consumption would be about 20 mW, assuming that at any given time about half of the circuit elements are in the "high" state. Such a large static power consumption is prohibitive for portable applications. In principle, the static power consumption of unipolar circuits can be reduced by increasing the resistance of the load device, but this will substantially increase the signal delay associated with the transition when the input switches from "high" to "low".

In silicon microprocessor technology, the unipolar circuit design was in use for less than a decade (from the Intel 4004 released in 1971 to the Intel 8086 released in 1978) before being replaced by the complementary circuit design (beginning with the Intel 80 286 released in 1982). Complementary circuits utilize both *p*-channel and *n*-channel transistors, so that one of the transistors always blocks the current path between the supply voltage node and the ground node (except during switching). As a result, the static power consumption of complementary circuits is several orders of magnitude smaller than that of unipolar circuits. In addition, complementary circuits have substantially greater immunity against electronic noise.[186] In silicon technology, the move from unipolar to complementary circuits was an important prerequisite for the realization of very-large-scale (VLSI) and ultra-large-scale (ULSI) integrated circuits.

In silicon CMOS technology, both the *p*-channel and *n*-channel FETs are realized with the same semiconductor (silicon). This is possible, because silicon can be chemically doped *p*-type or n-type by incorporating elements from the third or fifth column of the Periodic Table into the silicon lattice. To create a *p*-channel FET, the contact regions are doped heavily *p*-type and the channel region is doped lightly *n*-type (for *n*-channel FETs: contacts heavily *n*-type, channel

region lightly *p*-type). As a result, at $V_{GS} = 0$ neither holes nor electrons are able to flow through the transistor, regardless of the applied drain-source voltage, because one carrier type is blocked by the space-charge regions at the contacts, and the density of the other carrier type in the channel is greatly reduced by the channel doping. When the gate-source voltage exceeds the threshold voltage, an inversion layer is created that allows holes (in a *p*-channel FET) or electrons (in an *n*-channel FET), but not both, to pass through the channel. A large drain current therefore flows only when the transistor is turned "on", while the off-state current is very small.

Because stable *p*-type and *n*-type doping has so far not been demonstrated for organic TFTs, it is difficult to prepare air-stable organic *p*-channel and *n*-channel TFTs with small off-state currents using the same conjugated semiconductor. For example, if the semiconductor has a large HOMO–LUMO gap, the undesirable injection of the "wrong" carrier type is greatly suppressed, so that the off-state currents are very small, but finding two air-stable metals that match the HOMO and LUMO of such a semiconductor is challenging. Ahles and co-workers have prepared *p*-channel and *n*-channel pentacene TFTs by using gold as the contact metal for the *p*-channel TFTs (gold has a workfunction of ~5 eV, so the energy barrier to the HOMO is only a few hundred meV) and calcium as the contact metal for the *n*-channel TFTs (calcium has a workfunction of ~2.8 eV, so the energy barrier to the LUMO is also very small).[187] In this case, the undesirable injection of electrons in the *p*-channel TFTs is suppressed by the large energy barrier between the Fermi level of the gold and the LUMO of the pentacene (and the injection of holes in the *n*-channel TFTs is suppressed by the large barrier between the Fermi level of the calcium and the HOMO of the pentacene), so the off-state leakage currents are indeed very small. However, the use of low-workfunction metals such as calcium means that the *n*-channel TFTs cannot be operated in air.[187] Alternatively, if the semiconductor has a small HOMO–LUMO gap, or if a blend or bilayer of two different semiconductors is employed, so that both the HOMO energy and the LUMO energy are similar to the workfunction of an air-stable metal, then the TFTs may operate in air, but the off-state leakage currents will be unacceptably large.[116–118]

Consequently, air-stable organic complementary circuits with low static power consumption are best realized using dedicated conjugated semiconductors for the *p*-channel and *n*-channel TFTs. Fig. 34 shows the current–voltage characteristics of an organic *n*-channel TFT prepared on a glass substrate using vacuum-evaporated hexadecafluorocopperphthalocyanine (F_{16}CuPc) as the semiconductor. The electron

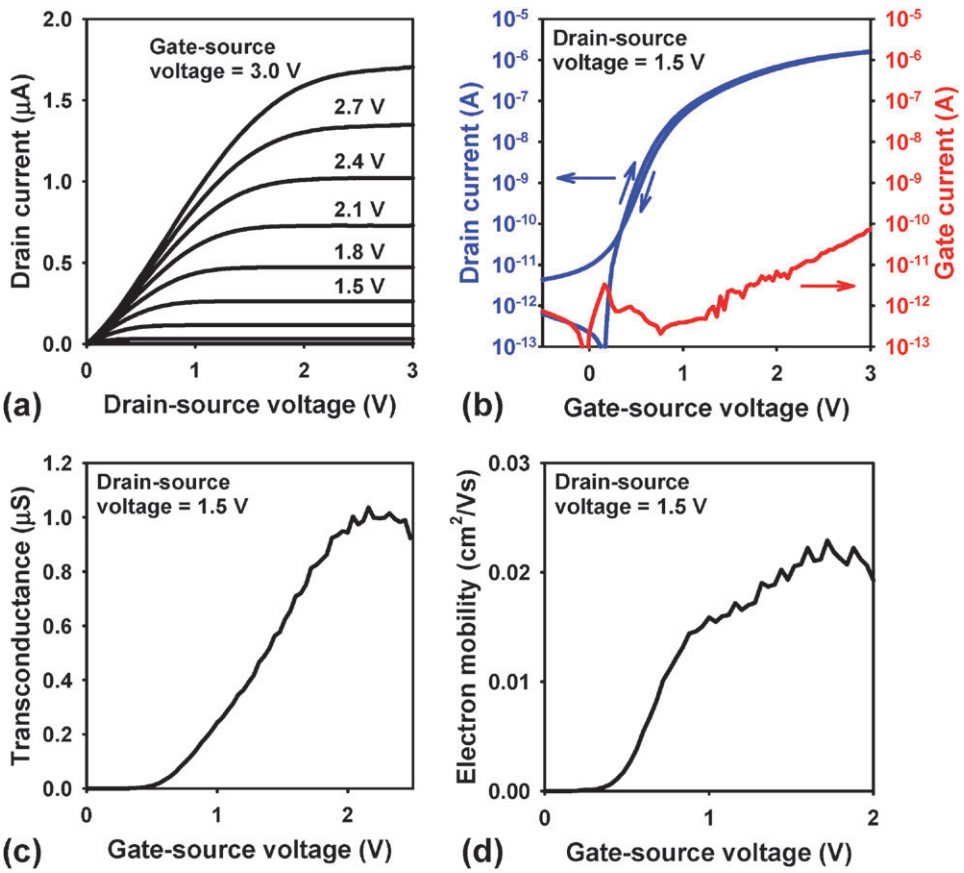

Fig. 34 Electrical characteristics of an organic *n*-channel TFT on a glass substrate using hexadecafluorocopperphthalocyanine (F_{16}CuPc; see Fig. 16c) as the semiconductor. The TFT has a channel length (L) of 20 μm and a channel width (W) of 1000 μm. The current–voltage curves were recorded in ambient air. (a) Output characteristics (I_D *versus* V_{DS}). (b) Input characteristics (I_G *versus* V_{GS}) and transfer characteristics (I_D *versus* V_{GS}). (c) Transconductance g_m *versus* V_{GS}, calculated using eqn (2). The maximum transconductance is approximately 1 μS. (d) Charge carrier field-effect mobility in the saturation regime, calculated using eqn (8). The maximum mobility is approximately 0.02 cm^2/Vs.

affinity of F_{16}CuPc is sufficiently large (4.5 eV) that gold source and drain contacts provide acceptable performance. At the same time, the HOMO–LUMO gap is sufficiently large so that the undesirable injection of holes at negative gate-source voltages is suppressed. The TFT in Fig. 34 has a channel width (W) of 1000 μm and a channel length (L) of 20 μm. The electron mobility is 0.02 cm^2/Vs, the on/off ratio is 10^6, the subthreshold swing is 170 mV/decade, and the cutoff frequency calculated using eqn (20) is 400 Hz. Aside from the semiconductor, the functional materials and the manufacturing process are identical to those employed for the DNTT p-channel TFT in Fig. 30.

By integrating organic p-channel and organic n-channel TFTs on the same substrate, organic complementary circuits can be prepared.[105,143,160,166,188–196] Fig. 35 shows the schematic, a photograph, and the transfer characteristics of a complementary inverter with a pentacene p-channel TFT and a F_{16}CuPc n-channel TFT manufactured on a glass substrate using the same technology as for the TFTs in Fig. 30 and 34. For balanced switching characteristics, the two transistors should have approximately the same transconductance. Since the electron mobility of the F_{16}CuPc n-channel TFT is about an order of magnitude smaller than the hole mobility of the pentacene p-channel TFT (0.02 cm^2/Vs *versus* 0.5 cm^2/Vs), the n-channel TFT was designed to have a channel width that is 10 times greater than that of the p-channel TFT.

When the input of the complementary inverter is "low" (0 V), the p-channel TFT is biased in the linear regime ($V_{GS} = -2$ V, since $V_{DD} = 2$ V) and the n-channel TFT is in the off-state ($V_{GS} = 0$ V), so the output node is "pulled up" to V_{DD} through the p-channel TFT. When the input is "high" (2 V), the n-channel TFT is in the linear regime ($V_{GS} = 2$ V) and the p-channel TFT is in the off-state ($V_{GS} = 0$ V), so the output node is "pulled down" to ground potential through the n-channel TFT. Since in both of the two static states the current path between the supply voltage node and the ground node is blocked by one of the two TFTs, the static inverter current is extremely small (~10 pA in Fig. 35). During switching there is a brief period when both transistors are simultaneously in the low-resistance on-state and a significant current flows between the supply voltage node and the ground node (~1 μA in Fig. 35). Thus, most of the power consumption of a complementary circuit is due to switching, while the static power dissipation is very small.

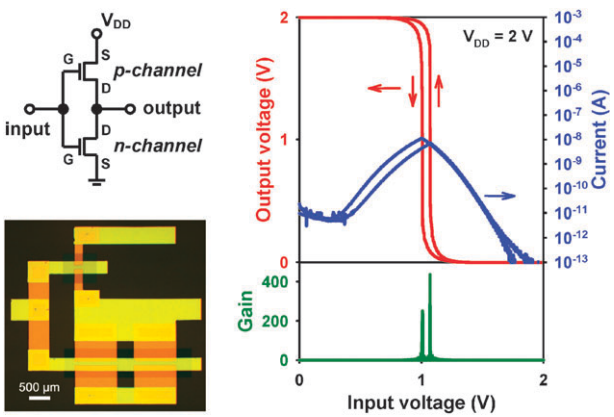

Fig. 35 Schematic, photograph, and transfer characteristics of an organic complementary inverter based on a pentacene p-channel TFT and a F_{16}CuPc n-channel TFT.

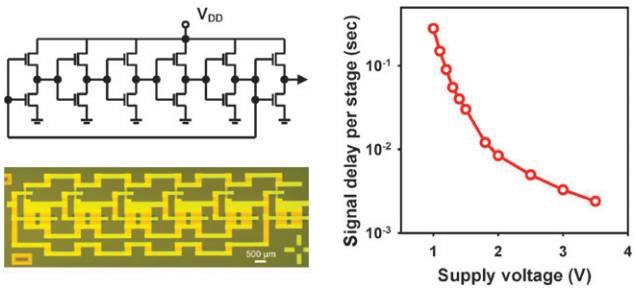

Fig. 36 Schematic, photograph, and signal propagation delay as a function of supply voltage of a 5-stage complementary ring oscillator with pentacene p-channel and F_{16}CuPc n-channel TFTs.

Assuming both transistors of the complementary inverter have the same L, ΔL and C_{diel}, the signal delay will be limited by the cutoff frequency of the transistor with the smaller mobility, in the case of the inverter in Fig. 35 by the F_{16}CuPc n-channel TFT. Fig. 36 shows the schematic, a photograph, and the stage delay as a function of supply voltage of a 5-stage complementary ring oscillator with pentacene p-channel and F_{16}CuPc n-channel TFTs. The stage delay at $V_{DD} = 3$ V is 3.3 msec, which corresponds to a maximum frequency of operation of about 150 Hz. As in the case of the unipolar ring oscillator in Fig. 33, the actual frequency determined experimentally is within a factor of 3 to 4 of the cutoff frequency calculated using eqn (20).

For many practical applications, a frequency of ~100 Hz may not be sufficient. The simplest way to increase the maximum switching frequency is to employ a thicker gate dielectric, so that the gate dielectric capacitance per unit area (C_{diel}) is reduced and the circuits can be operated with a larger supply voltage. Eqn (5) and (6) show that the transconductance g_m does not change when C_{diel} is reduced, as long as the operating voltages (V_{GS}, V_{DS}) are simultaneously increased, but according to eqn (19) a smaller C_{diel} leads to a smaller gate

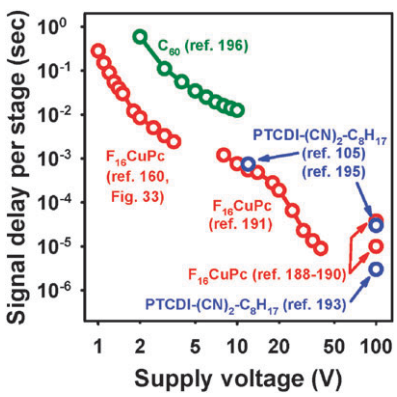

Fig. 37 Signal delay per stage as a function of supply voltage for organic complementary ring oscillators. The organic semiconductor employed for the n-channel TFTs is given for each data set. The semiconductor employed for the p-channel TFTs is either pentacene,[160,191,193,196] an oligothiophene,[188–190] or a polythiophene derivative.[105,195]

capacitance C_G, and this provides a higher frequency of operation, as eqn (20) indicates. Indeed, organic complementary ring oscillators with a stage delay as small as 3 μsec have been reported at V_{DD} = 100 V[193] (see Fig. 37). However, such large supply voltages are difficult to provide, especially in battery-powered portable electronic systems. To allow air-stable organic complementary circuits to operate at frequencies in the range of 10 to 100 kHz with supply voltages below about 5 V, it will be necessary to develop air-stable low-voltage *n*-channel TFTs with electron mobilities similar to the best organic *p*-channel TFT mobilities ($\sim$1 cm^2/Vs), and to reduce the critical dimensions L and ΔL to about 1 μm (ideally using high-resolution printing techniques, rather than photolithography).

6. Outlook

Organic transistors are potentially useful for applications that require electronic functionality with low or medium complexity distributed over large areas on unconventional substrates, such as glass or flexible plastic film. Generally these are applications in which the use of single-crystal silicon devices and circuits is technically or economically not feasible. Examples include flexible displays and large-area sensors. However, organic transistors are unlikely to replace silicon in applications characterized by large transistor counts, small chip size, large integration densities, or high-frequency operation. The reason is that in these applications the use of silicon MOSFETs is very economical.

The static and dynamic performance of state-of-the-art organic *p*-channel TFTs is already sufficient for certain applications, most notably small or medium-size flexible displays[197–199] and simple radio-frequency identification (RFID) tags[185] in which the TFTs operate with critical frequencies in the range of a few tens of kilohertz. Strategies for increasing the performance of organic TFTs include further improvements in the carrier mobility of the organic semiconductor (either through the synthesis of new materials, through improved purification, or by enhancing the molecular order in the semiconductor layer) and more aggressive scaling of the lateral transistor dimensions (channel length and contact overlap). For example, an increase in cutoff frequency from 100 kHz to 1 MHz can be achieved either by improving the mobility from 1 cm^2/Vs to 10 cm^2/Vs (assuming critical dimensions of 10 μm and an operating voltage of 3 V), or by reducing the critical dimensions from 10 μm to 3 μm (assuming a mobility of 1 cm^2/Vs and an operating voltage of 3 V). A cutoff frequency above 20 MHz is projected for TFTs with a mobility of 2 cm^2/Vs and critical dimensions of 1 μm (again assuming an operating voltage of 3 V).

However, these improvements in performance must be implemented without sacrificing the general manufacturability of the devices, circuits, and systems. This important requirement has fueled the development of a whole range of large-area, high-resolution printing methods,[143–147] as well as the development of three-terminal vertical organic devices in which the critical dimension is a film thickness, rather than a lateral distance.[200]

References

1 R. A. Street, *Adv. Mater.*, 2009, **21**, 2007.
2 N. F. Mott and E. A. Davis, *Electronic Processes in Non-Crystalline Materials*, Clarendon Press, Oxford, 2nd edn, 1979.
3 I. McCulloch, M. Heeney, M. L. Chabinyc, D. DeLongchamp, R. J. Kline, M. Cölle, W. Duffy, D. Fischer, D. Gundlach, B. Hamadani, R. Hamilton, L. Richter, A. Salleo, M. Shkunov, D. Sparrowe, S. Tierney and W. Zhang, *Adv. Mater.*, 2009, **21**, 1091.
4 C. G. Choi and B. S. Bae, *Electrochem. Solid-State Lett.*, 2007, **10**, H347.
5 O. D. Jurchescu, J. Baas and T. T. M. Palstra, *Appl. Phys. Lett.*, 2004, **84**, 3061.
6 W. Warta and N. Karl, *Phys. Rev. B: Condens. Matter*, 1985, **32**, 1172.
7 M. C. J. M. Vissenberg and M. Matters, *Phys. Rev. B: Condens. Matter Mater. Phys.*, 1998, **57**, 12964.
8 S. Schiefer, M. Huth, A. Dobrinevski and B. Nickel, *J. Am. Chem. Soc.*, 2007, **129**, 10316.
9 A. Troisi and G. Orlandi, *J. Phys. Chem. B*, 2005, **109**, 1849.
10 G. Horowitz, R. Hajlaoui and P. Delannoy, *J. Phys. III*, 1995, **5**, 355.
11 M. Hultell and S. Stafström, *Chem. Phys. Lett.*, 2006, **428**, 446.
12 A. Tsumura, H. Koezuka and T. Ando, *Appl. Phys. Lett.*, 1986, **49**, 1210.
13 A. Assadi, C. Svensson, M. Willander and O. Inganas, *Appl. Phys. Lett.*, 1988, **53**, 195.
14 R. D. McCullough, R. D. Lowe, M. Jayaraman and D. L. Anderson, *J. Org. Chem.*, 1993, **58**, 904.
15 Z. Bao, A. Dodabalapur and A. Lovinger, *Appl. Phys. Lett.*, 1996, **69**, 4108.
16 H. Sirringhaus, P. J. Brown, R. H. Friend, M. M. Nielsen, K. Bechgaard, B. M. W. Langeveld-Voss, A. J. H. Spiering, R. A. J. Janssen, E. W. Meijer, P. Herwig and D. M. de Leeuw, *Nature*, 1999, **401**, 685.
17 R. J. Kline, M. D. McGehee, E. N. Kadnikova, J. Liu, J. M. J. Frechet and M. F. Toney, *Macromolecules*, 2005, **38**, 3312.
18 L. H. Jimison, M. F. Toney, I. McCulloch, M. Heeney and A. Salleo, *Adv. Mater.*, 2009, **21**, 1568.
19 B. S. Ong, Y. Wu, P. Liu and S. Gardner, *J. Am. Chem. Soc.*, 2004, **126**, 3378.
20 I. McCulloch, M. Heeney, C. Bailey, K. Genevicius, I. MacDonald, M. Shkunov, D. Sparrowe, S. Tierney, R. Wagner, W. Zhang, M. L. Chabinyc, R. J. Kline, M. D. McGehee and M. F. Toney, *Nat. Mater.*, 2006, **5**, 328.
21 M. Shtein, J. Mapel, J. B. Benziger and S. R. Forrest, *Appl. Phys. Lett.*, 2002, **81**, 268.
22 M. Shtein, P. Peumans, J. B. Benziger and S. R. Forrest, *Adv. Mater.*, 2004, **16**, 1615.
23 R. R. Lunt, B. E. Lassiter, J. B. Benziger and S. R. Forrest, *Appl. Phys. Lett.*, 2009, **95**, 233305.
24 K. Kudo, M. Yamashina and T. Moriizumi, *Jpn. J. Appl. Phys.*, 1984, **23**, 130.
25 M. Madru, G. Guillaud, M. Al Sadoun, M. Maitrot, C. Clarisse, M. Le Contellec, J. J. Andre and J. Simon, *Chem. Phys. Lett.*, 1987, **142**, 103.
26 C. Clarisse, M. T. Riou, M. Gauneau and M. Le Contellec, *Electron. Lett.*, 1988, **24**, 674.
27 G. Horowitz, D. Fichou, X. Peng, Z. Xu and F. Garnier, *Solid State Commun.*, 1989, **72**, 381.
28 F. Garnier, G. Horowitz, X. Z. Peng and D. Fichou, *Adv. Mater.*, 1990, **2**, 592.
29 Y. Y. Lin, D. J. Gundlach, S. F. Nelson and T. N. Jackson, *IEEE Trans. Electron Devices*, 1997, **44**, 1325.
30 Y. Y. Lin, D. J. Gundlach, S. F. Nelson and T. N. Jackson, *IEEE Electron Device Lett.*, 1997, **18**, 606.
31 W. Kalb, P. Lang, M. Mottaghi, H. Aubin, G. Horowitz and M. Wuttig, *Synth. Met.*, 2004, **146**, 279.
32 S. Y. Yang, K. Shin and C. E. Park, *Adv. Funct. Mater.*, 2005, **15**, 1806.
33 M. Halik, H. Klauk, U. Zschieschang, G. Schmid, S. Ponomarenko, S. Kirchmeyer and W. Weber, *Adv. Mater.*, 2003, **15**, 917.

34 T. W. Kelley, P. F. Baude, C. Gerlach, D. E. Ender, D. V. Muyres, M. A. Haase, D. E. Vogel and S. D. Theiss, *Chem. Mater.*, 2004, **16**, 4413.
35 S. Lee, B. Koo, J. Shin, E. Lee, H. Park and H. Kim, *Appl. Phys. Lett.*, 2006, **88**, 162109.
36 H. S. Tan, N. Mathews, T. Cahyadi, F. R. Zhu and S. G. Mhaisalkar, *Appl. Phys. Lett.*, 2009, **94**, 263303.
37 A. Virkar, S. Mannsfeld, J. H. Oh, M. F. Toney, Y. H. Tan, G. Y. Liu, J. C. Scott, R. Miller and Z. Bao, *Adv. Funct. Mater.*, 2009, **19**, 1962.
38 Y. Ito, A. Virkar, S. Mannsfeld, J. H. Oh, M. Toney, J. Locklin and Z. Bao, *J. Am. Chem. Soc.*, 2009, **131**, 9396.
39 A. Salleo, M. L. Chabinyc, M. S. Yang and R. A. Street, *Appl. Phys. Lett.*, 2002, **81**, 4383.
40 J. H. Lee, G. H. Kim, S. H. Kim, S. C. Lim, Y. S. Yang, J. H. Youk, J. Jang and T. Zyung, *Synth. Met.*, 2004, **143**, 21.
41 W. J. Kim, W. H. Koo, S. J. Jo, C. S. Kim, H. K. Baik, J. Lee and S. Im, *J. Vac. Sci. Technol., B*, 2005, **23**, 2357.
42 H. Jung, T. Lim, Y. Choi, M. Yi, J. Won and S. Pyo, *Appl. Phys. Lett.*, 2008, **92**, 163504.
43 H. Meng, Z. Bao, A. J. Lovinger, B. C. Wang and A. M. Mujsce, *J. Am. Chem. Soc.*, 2001, **123**, 9214.
44 J. A. Merlo, C. R. Newman, C. P. Gerlach, T. W. Kelley, D. V. Muyres, S. E. Fritz, M. F. Toney and C. D. Frisbie, *J. Am. Chem. Soc.*, 2005, **127**, 3997.
45 S. A. Ponomarenko, S. Kirchmeyer, A. Elschner, N. M. Alpatova, M. Halik, H. Klauk, U. Zschieschang and G. Schmid, *Chem. Mater.*, 2006, **18**, 579.
46 J. Locklin, M. M. Ling, A. Sung, M. E. Roberts and Z. Bao, *Adv. Mater.*, 2006, **18**, 2989.
47 H. Meng, F. Sun, M. B. Goldfinger, F. Gao, D. J. Londono, W. J. Marshal, G. S. Blackman, K. D. Dobbs and D. E. Keys, *J. Am. Chem. Soc.*, 2006, **128**, 9304.
48 H. Klauk, U. Zschieschang, R. T. Weitz, H. Meng, F. Sun, G. Nunes, D. E. Keys, C. R. Fincher and Z. Xiang, *Adv. Mater.*, 2007, **19**, 3882.
49 T. Yamamoto and K. Takimiya, *J. Am. Chem. Soc.*, 2007, **129**, 2224.
50 U. Zschieschang, F. Ante, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Someya, K. Kern and H. Klauk, *Adv. Mater.*, 2010, **22**, 982.
51 P. Herwig and K. Müllen, *Adv. Mater.*, 1999, **11**, 480.
52 A. Afzali, C. D. Dimitrakopoulos and T. L. Breen, *J. Am. Chem. Soc.*, 2002, **124**, 8812.
53 J. E. Anthony, J. S. Brooks, D. L. Eaton and S. R. Parkin, *J. Am. Chem. Soc.*, 2001, **123**, 9482.
54 C. D. Sheraw, T. N. Jackson, D. L. Eaton and J. E. Anthony, *Adv. Mater.*, 2003, **15**, 2009.
55 S. K. Park, T. N. Jackson, J. E. Anthony and D. A. Mourey, *Appl. Phys. Lett.*, 2007, **91**, 063514.
56 M. M. Payne, S. A. Odom, S. R. Parkin and J. E. Anthony, *Org. Lett.*, 2004, **6**, 3325.
57 M. M. Payne, S. R. Parkin, J. E. Anthony, C. C. Kuo and T. N. Jackson, *J. Am. Chem. Soc.*, 2005, **127**, 4986.
58 K. C. Dickey, J. E. Anthony and Y. L. Loo, *Adv. Mater.*, 2006, **18**, 1721.
59 S. Subramanian, S. K. Park, S. R. Parkin, V. Podzorov, T. N. Jackson and J. E. Anthony, *J. Am. Chem. Soc.*, 2008, **130**, 2706.
60 S. K. Park, D. A. Mourey, S. Subramanian, J. E. Anthony and T. N. Jackson, *Appl. Phys. Lett.*, 2008, **93**, 043301.
61 D. J. Gundlach, J. E. Royer, S. K. Park, S. Subramanian, O. D. Jurchescu, B. H. Hamadani, A. J. Moad, R. J. Kline, L. C. Teague, O. Kirillov, C. A. Richter, J. G. Kushmerick, L. J. Richter, S. R. Parkin, T. N. Jackson and J. E. Anthony, *Nat. Mater.*, 2008, **7**, 216.
62 R. Hamilton, J. Smith, S. Ogier, M. Heeney, J. E. Anthony, I. McCulloch, J. Veres, D. D. C. Bradley and T. D. Anthopoulos, *Adv. Mater.*, 2009, **21**, 1166.
63 G. R. Llorente, M. B. Dufourg-Madec, D. J. Crouch, R. G. Pritchard, S. Ogier and S. G. Yeates, *Chem. Commun.*, 2009, 3059.
64 C. Siol, C. Melzer and H. von Seggern, *Appl. Phys. Lett.*, 2008, **93**, 133303.
65 M. Ahles, R. Schmechel and H. von Seggern, *Appl. Phys. Lett.*, 2004, **85**, 4499.
66 L. L. Chua, J. Zaumseil, J. F. Chang, E. C. W. Ou, P. K. H. Ho, H. Sirringhaus and R. H. Friend, *Nature*, 2005, **434**, 194.
67 R. C. Haddon, A. S. Perel, R. C. Morris, T. T. M. Palstra, A. F. Hebard and R. M. Fleming, *Appl. Phys. Lett.*, 1995, **67**, 121.
68 K. Horiuchi, K. Nakada, S. Uchino, S. Hashii, A. Hashimoto, N. Aoki and Y. Ochiai, *Appl. Phys. Lett.*, 2002, **81**, 1911.
69 M. Kitamura, S. Aomori, J. H. Na and Y. Arakawa, *Appl. Phys. Lett.*, 2008, **93**, 033313.
70 T. D. Anthopoulos, B. Singh, N. Marjanovic, N. S. Sariciftci, A. Montaigne Ramil, H. Sitter, M. Cölle and D. M. deLeeuw, *Appl. Phys. Lett.*, 2006, **89**, 213504.
71 X. H. Zhang, B. Domercq and B. Kippelen, *Appl. Phys. Lett.*, 2007, **91**, 092114.
72 X. H. Zhang and B. Kippelen, *J. Appl. Phys.*, 2008, **104**, 104504.
73 J. Hwang, A. Wan and A. Kahn, *Mater. Sci. Eng., R*, 2009, **64**, 1.
74 J. Jang, J. W. Kim, N. Park and J. J. Kim, *Org. Electron.*, 2008, **9**, 481.
75 R. J. Chesterfield, J. C. McKeen, C. R. Newman, P. C. Ewbank, D. A. da Silva Filho, J. L. Bredas, L. L. Miller, K. R. Mann and C. D. Frisbie, *J. Phys. Chem. B*, 2004, **108**, 19281.
76 S. Tatemichi, M. Ichikawa, T. Koyama and Y. Taniguchi, *Appl. Phys. Lett.*, 2006, **89**, 112108.
77 M. Hiramoto, K. Ihara, H. Fukusumi and M. Yokoyama, *J. Appl. Phys.*, 1995, **78**, 7153.
78 D. J. Gundlach, K. P. Pernstich, G. Wilckens, M. Grüter, S. Haas and B. Batlogg, *J. Appl. Phys.*, 2005, **98**, 064502.
79 D. Shukla, S. F. Nelson, D. C. Freeman, M. Rajeswaran, W. G. Ahearn, D. M. Meyer and J. T. Carey, *Chem. Mater.*, 2008, **20**, 7486.
80 Z. Bao, A. Lovinger and J. Brown, *J. Am. Chem. Soc.*, 1998, **120**, 207.
81 M. Gorgoi, *Electronic Properties of Phthalocyanines Deposited on H-Si(111)*, PhD thesis, Technical University Chemnitz, 2005.
82 M. M. Ling and Z. Bao, *Org. Electron.*, 2006, **7**, 568.
83 D. G. de Oteyza, E. Barrena, S. Sellner, J. O. Osso and H. Dosch, *J. Phys. Chem. B*, 2006, **110**, 16618.
84 D. G. de Oteyza, E. Barrena, J. O. Osso, S. Sellner and H. Dosch, *J. Am. Chem. Soc.*, 2006, **128**, 15052.
85 H. E. Katz, A. J. Lovinger, J. Johnson, C. Kloc, T. Siegrist, W. Li, Y. Y. Lin and A. Dodabalapur, *Nature*, 2000, **404**, 478.
86 H. E. Katz, J. Johnson, A. J. Lovinger and W. Li, *J. Am. Chem. Soc.*, 2000, **122**, 7787.
87 A. Facchetti, Y. Deng, A. Wang, Y. Koide, H. Sirringhaus, T. J. Marks and R. H. Friend, *Angew. Chem., Int. Ed.*, 2000, **39**, 4547.
88 A. Facchetti, M. Mushrush, H. E. Katz and T. J. Marks, *Adv. Mater.*, 2003, **15**, 33.
89 A. Facchetti, M. H. Yoon, C. L. Stern, H. E. Katz and T. J. Marks, *Angew. Chem., Int. Ed.*, 2003, **42**, 3900.
90 A. Facchetti, M. Mushrush, M. H. Yoon, G. R. Hutchison, M. A. Ratner and T. J. Marks, *J. Am. Chem. Soc.*, 2004, **126**, 13859.
91 J. A. Letizia, A. Facchetti, C. L. Stern, M. A. Ratner and T. J. Marks, *J. Am. Chem. Soc.*, 2005, **127**, 13476.
92 A. Facchetti, M. H. Yoon and T. J. Marks, *J. Am. Chem. Soc.*, 2006, **128**, 4928.
93 M. H. Yoon, A. Facchetti, C. E. Stern and T. J. Marks, *J. Am. Chem. Soc.*, 2006, **128**, 5792.
94 M. H. Yoon, C. Kim, A. Facchetti and T. J. Marks, *J. Am. Chem. Soc.*, 2006, **128**, 12851.
95 Y. Sakamoto, T. Suzuki, M. Kobayashi, Y. Gao, Y. Fukai, Y. Inoue, F. Sato and S. Tokito, *J. Am. Chem. Soc.*, 2004, **126**, 8138.
96 Y. Inoue, Y. Sakamoto, T. Suzuki, M. Kobayashi, Y. Gao and S. Tokito, *Jpn. J. Appl. Phys.*, 2005, **44**, 3663.
97 B. A. Jones, M. J. Ahrens, M. H. Yoon, A. Facchetti, T. J. Marks and M. R. Wasielewski, *Angew. Chem., Int. Ed.*, 2004, **43**, 6363.
98 R. T. Weitz, K. Amsharov, U. Zschieschang, E. Barrena Villas, D. K. Goswami, M. Burghard, H. Dosch, M. Jansen, K. Kern and H. Klauk, *J. Am. Chem. Soc.*, 2008, **130**, 4637.
99 R. T. Weitz, K. Amsharov, U. Zschieschang, M. Burghard, M. Jansen, M. Kelsch, B. Rhamati, P. A. van Aken, K. Kern and H. Klauk, *Chem. Mater.*, 2009, **21**, 4949.

100 R. Schmidt, J. H. Oh, Y. S. Sun, M. Deppisch, A. M. Krause, K. Radacki, H. Braunschweig, M. Könemann, P. Erk, Z. Bao and F. Würthner, *J. Am. Chem. Soc.*, 2009, **131**, 6215.
101 C. Kim, A. Facchetti and T. J. Marks, *J. Am. Chem. Soc.*, 2009, **131**, 9122.
102 Y. Ishii, R. Ye, M. Baba and K. Ohta, *Jpn. J. Appl. Phys.*, 2008, **47**, 1256.
103 Y. Hosoi, D. Tsunami, H. Ishii and Y. Furukawa, *Chem. Phys. Lett.*, 2007, **436**, 139.
104 S. Handa, E. Miyazaki, K. Takimiya and Y. Kunugi, *J. Am. Chem. Soc.*, 2007, **129**, 11684.
105 H. Yan, Y. Zheng, R. Blache, C. Newman, S. Lu, J. Woerle and A. Facchetti, *Adv. Mater.*, 2008, **20**, 3393.
106 H. Usta, A. Facchetti and T. J. Marks, *J. Am. Chem. Soc.*, 2008, **130**, 8580.
107 C. Piliego, D. Jarzab, G. Gigli, Z. Chen, A. Facchetti and M. A. Loi, *Adv. Mater.*, 2009, **21**, 1573.
108 M. Chikamatsu, A. Itakura, Y. Yoshida, R. Azumi and K. Yase, *Chem. Mater.*, 2008, **20**, 7365.
109 P. H. Wöbkenberg, D. D. C. Bradley, D. Kronholm, J. C. Hummelen, D. M. deLeeuw, M. Cölle and T. D. Anthopoulos, *Synth. Met.*, 2008, **158**, 468.
110 A. Babel and S. A. Jenekhe, *Adv. Mater.*, 2002, **14**, 371.
111 A. Babel and S. A. Jenekhe, *J. Am. Chem. Soc.*, 2003, **125**, 13656.
112 S. Hüttner, M. Sommer and M. Thelakkat, *Appl. Phys. Lett.*, 2008, **92**, 093302.
113 X. Zhan, Z. Tan, B. Domercq, Z. An, X. Zhang, S. Barlow, Y. Li, D. Zhu, B. Kippelen and S. R. Marder, *J. Am. Chem. Soc.*, 2007, **129**, 7246.
114 Z. Chen, Y. Zheng, H. Yan and A. Facchetti, *J. Am. Chem. Soc.*, 2009, **131**, 8.
115 H. Yan, Z. Chen, Y. Zheng, C. Newman, J. R. Quinn, F. Dötz, M. Kastler and A. Facchetti, *Nature*, 2009, **457**, 679.
116 T. D. Anthopoulos, S. Setayesh, E. Smits, M. Cölle, E. Cantatore, B. de Boer, P. W. M. Blom and D. M. deLeeuw, *Adv. Mater.*, 2006, **18**, 1900.
117 E. J. Meijer, D. M. de Leeuw, S. Setayesh, E. van Veenendaal, B. H. Huisman, P. W. M. Blom, J. C. Hummelen, U. Scherf and T. M. Klapwijk, *Nat. Mater.*, 2003, **2**, 678.
118 A. Dodabalapur, H. E. Katz, L. Torsi and R. C. Haddon, *Science*, 1995, **269**, 1560.
119 J. Zaumseil and H. Sirringhaus, *Chem. Rev.*, 2007, **107**, 1296.
120 P. K. Weimer, *Proc. IRE*, 1962, **50**, 1462.
121 P. G. LeComber, W. E. Spear and A. Ghaith, *Electron. Lett.*, 1979, **15**, 179.
122 F. Ebisawa, T. Kurokawa and S. Nara, *J. Appl. Phys.*, 1983, **54**, 3255.
123 P. V. Necliudov, M. S. Shur, D. J. Gundlach and T. N. Jackson, *J. Appl. Phys.*, 2000, **88**, 6594.
124 I. G. Hill, *Appl. Phys. Lett.*, 2005, **87**, 163505.
125 D. J. Gundlach, L. Zhou, J. A. Nichols, T. N. Jackson, P. V. Necliudov and M. S. Shur, *J. Appl. Phys.*, 2006, **100**, 024509.
126 D. Gupta, M. Katiyar and D. Gupta, *Org. Electron.*, 2009, **10**, 775.
127 C. H. Shim, F. Maruoka and R. Hattori, *IEEE Trans. Electron Devices*, 2010, **57**, 195.
128 D. J. Gundlach, L. Jia and T. N. Jackson, *IEEE Electron Device Lett.*, 2001, **22**, 571.
129 Q. J. Cai, M. B. Chan-Park, Q. Zhou, Z. S. Lu, C. M. Li and B. S. Ong, *Org. Electron.*, 2008, **9**, 936.
130 F. C. Chen, Y. S. Lin, T. H. Chen and L. J. Kung, *Electrochem. Solid-State Lett.*, 2007, **10**, H186.
131 B. Stadlober, U. Haas, H. Gold, A. Haase, G. Jakopic, G. Leising, N. Koch, S. Rentenberger and E. Zojer, *Adv. Funct. Mater.*, 2007, **17**, 2687.
132 D. Kumaki, T. Umeda and S. Tokito, *Appl. Phys. Lett.*, 2008, **92**, 013301.
133 M. Kano, T. Minari and K. Tsukagoshi, *Appl. Phys. Lett.*, 2009, **94**, 143304.
134 D. J. Gundlach, T. N. Jackson, D. G. Schlom and S. F. Nelson, *Appl. Phys. Lett.*, 1999, **74**, 3302.
135 H. Klauk, D. J. Gundlach, J. A. Nichols and T. N. Jackson, *IEEE Trans. Electron Devices*, 1999, **46**, 1258.
136 H. Klauk, M. Halik, U. Zschieschang, F. Eder, G. Schmid and C. Dehm, *Appl. Phys. Lett.*, 2003, **82**, 4175.
137 D. V. Muyres, P. F. Baude, S. Theiss, M. Haase, T. W. Kelley and P. Fleming, *J. Vac. Sci. Technol., A*, 2004, **22**, 1892.
138 A. C. Arias, S. E. Ready, R. Lujan, W. S. Wong, K. E. Paul, A. Salleo, M. L. Chabinyc, R. Apte, R. A. Street, Y. Wu, P. Liu and B. Ong, *Appl. Phys. Lett.*, 2004, **85**, 3304.
139 Y. Li, Y. Wu and B. Ong, *J. Am. Chem. Soc.*, 2005, **127**, 3266.
140 O. Vazquez-Mena, G. Villanueva, V. Savu, K. Sidler, M. A. F. van den Boogaart and J. Brugger, *Nano Lett.*, 2008, **8**, 3675.
141 H. Klauk, U. Zschieschang and M. Halik, *J. Appl. Phys.*, 2007, **102**, 074514.
142 G. H. Gelinck, T. C. T. Geuns and D. M. de Leeuw, *Appl. Phys. Lett.*, 2000, **77**, 1487.
143 T. Sekitani, Y. Noguchi, U. Zschieschang, H. Klauk and T. Someya, *Proc. Natl. Acad. Sci. U. S. A.*, 2008, **105**, 4976.
144 J.-U. Park, M. Hardy, S. J. Kang, K. Barton, K. Adair, D. k. Mukhopadhyay, C. Y. Lee, M. S. Strano, A. G. Alleyne, J. G. Georgiadis, P. M. Ferreira and J. A. Rogers, *Nat. Mater.*, 2007, **6**, 782.
145 C. W. Sele, T. von Werne, R. H. Friend and H. Sirringhaus, *Adv. Mater.*, 2005, **17**, 997.
146 Y. Y. Noh, N. Zhao, M. Caironi and H. Sirringhaus, *Nat. Nanotechnol.*, 2007, **2**, 784.
147 N. Zhao, M. Chiesa, H. Sirringhaus, Y. Li, Y. Wu and B. Ong, *J. Appl. Phys.*, 2007, **101**, 064513.
148 M. Halik, H. Klauk, U. Zschieschang, G. Schmid, W. Radlik and W. Weber, *Adv. Mater.*, 2002, **14**, 1717.
149 J. Veres, S. D. Ogier, S. W. Leeming, D. C. Cupertino and S. M. Khaffaf, *Adv. Funct. Mater.*, 2003, **13**, 199.
150 A. F. Stassen, R. W. I. de Boer, N. N. Iosad and A. F. Morpurgo, *Appl. Phys. Lett.*, 2004, **85**, 3899.
151 I. N. Hulea, S. Fratini, H. Xie, C. L. Mulder, N. N. Iossad, G. Rastelli, S. Ciuchi and A. F. Morpurgo, *Nat. Mater.*, 2006, **5**, 982.
152 M. H. Yoon, H. Yan, A. Facchetti and T. J. Marks, *J. Am. Chem. Soc.*, 2005, **127**, 10388.
153 S. Y. Yang, S. H. Kim, K. Shin, H. Jeon and C. E. Park, *Appl. Phys. Lett.*, 2006, **88**, 173507.
154 M. P. Walser, W. L. Kalb, T. Mathis and B. Batlogg, *Appl. Phys. Lett.*, 2009, **95**, 233301.
155 L. A. Majewski, R. Schroeder, M. Voigt and M. Grell, *J. Phys. D: Appl. Phys.*, 2004, **37**, 3367.
156 S. Goettling, B. Diehm and N. Fruehauf, *J. Disp. Technol.*, 2008, **4**, 300.
157 J. Collet, O. Tharaud, A. Chapoton and D. Vuillaume, *Appl. Phys. Lett.*, 2000, **76**, 1941.
158 M. Halik, H. Klauk, U. Zschieschang, G. Schmid, C. Dehm, M. Schütz, S. Maisch, F. Effenberger, M. Brunnbauer and F. Stellacci, *Nature*, 2004, **431**, 963.
159 M. H. Yoon, A. Facchetti and T. J. Marks, *Proc. Natl. Acad. Sci. U. S. A.*, 2005, **102**, 4678.
160 H. Klauk, U. Zschieschang, J. Pflaum and M. Halik, *Nature*, 2007, **445**, 745.
161 P. H. Wöbkenberg, J. Ball, F. B. Kooistra, J. C. Hummelen, D. M. deLeeuw, D. D. C. Bradley and T. D. Anthopoulos, *Appl. Phys. Lett.*, 2008, **93**, 013303.
162 H. Ma, O. Acton, G. Ting, J. W. Ka, H. L. Yip, N. Tucker, R. Schofield and A. K. Y. Jen, *Appl. Phys. Lett.*, 2008, **92**, 113303.
163 S. A. DiBenedetto, D. Frattarelli, M. A. Ratner, A. Facchetti and T. J. Marks, *J. Am. Chem. Soc.*, 2008, **130**, 7528.
164 Y. G. Ha, A. Facchetti and T. J. Marks, *Chem. Mater.*, 2009, **21**, 1173.
165 S. A. DiBenedetto, D. Frattarelli, A. Facchetti, M. A. Ratner and T. J. Marks, *J. Am. Chem. Soc.*, 2009, **131**, 11080.
166 U. Zschieschang, M. Halik and H. Klauk, *Langmuir*, 2008, **24**, 1665.
167 R. T. Weitz, U. Zschieschang, F. Effenberger, H. Klauk, M. Burghard and K. Kern, *Nano Lett.*, 2007, **7**, 22.
168 S. Ju, J. Li, J. Liu, P. C. Chen, Y. G. Ha, F. Ishikawa, H. Chang, C. Zhou, A. Facchetti, D. B. Janes and T. J. Marks, *Nano Lett.*, 2008, **8**, 997.
169 R. T. Weitz, U. Zschieschang, A. Forment-Aliaga, D. Kälblein, M. Burghard, K. Kern and H. Klauk, *Nano Lett.*, 2009, **9**, 1335.

170 T. Sekitani, T. Yokota, U. Zschieschang, H. Klauk, S. Bauer, K. Takeuchi, M. Takamiya, T. Sakurai and T. Someya, *Science*, 2009, **326**, 1516.
171 M. J. Panzer, C. R. Newman and C. D. Frisbie, *Appl. Phys. Lett.*, 2005, **86**, 103503.
172 A. S. Dhoot, J. D. Yuen, M. Heeney, I. McCulloch, D. Moses and A. J. Heeger, *Proc. Natl. Acad. Sci. U. S. A.*, 2006, **103**, 11834.
173 J. Lee, M. J. Panzer, Y. He, T. P. Lodge and C. D. Frisbie, *J. Am. Chem. Soc.*, 2007, **129**, 4532.
174 J. H. Cho, J. Lee, Y. Xia, B. Kim., Y. He, M. J. Renn, T. P. Lodge and C. D. Frisbie, *Nat. Mater.*, 2008, **7**, 900.
175 L. Herlogsson, M. Cölle, S. Tiemey, X. Crispin and M. Berggren, *Adv. Mater.*, 2010, **22**, 72.
176 S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, Wiley, New York, 3rd edn, 2007.
177 E. J. Meijer, C. Tanase, P. W. M. Blom, E. van Veenendaal, B. H. Huisman, D. M. de Leeuw and T. M. Klapwijk, *Appl. Phys. Lett.*, 2002, **80**, 3838.
178 W. Fix, A. Ullmann, J. Ficker and W. Clemens, *Appl. Phys. Lett.*, 2002, **81**, 1735.
179 J. Smith, R. Hamilton, M. Heeney, D. M. de Leeuw, E. Cantatore, J. E. Anthony, I. McCulloch, D. D. C. Bradley and T. D. Anthopoulos, *Appl. Phys. Lett.*, 2008, **93**, 253301.
180 P. Baude, D. A. Ender, M. A. Haase, T. W. Kelley, D. V. Muyres and S. D. Theiss, *Appl. Phys. Lett.*, 2003, **82**, 3964.
181 C. Rolin, S. Steudel, K. Myny, D. Cheyns, S. Verlaak, J. Genoe and P. Heremans, *Appl. Phys. Lett.*, 2006, **89**, 203502.
182 S. K. Park, D. A. Mourey, S. Subramanian, J. E. Anthony and T. N. Jackson, *IEEE Electron Device Lett.*, 2008, **29**, 1004.
183 K. Mistry, *et al.*, *Technical Digest of the 2007 International Electron Device Meeting (Washington DC)*, December 2007.
184 G. H. Gelinck, H. E. A. Huitema, E. van Veenendaal, E. Cantatore, L. Schrijnemakers, J. B. P. H. van der Putten, T. C. T. Geuns, M. Beenhakkers, J. B. Giesbers, B. H. Huisman, E. J. Meijer, E. M. Benito, F. J. Touwslager, A. W. Marsman, B. J. E. van Rens and D. M. de Leeuw, *Nat. Mater.*, 2004, **3**, 106.
185 K. Myny, S. Steudel, P. Vicca, M. J. Beenhakkers, N. A. J. M. van Aerle, G. H. Gelinck, J. Genoe, W. Dehaene and P. Heremans, *Solid-State Electron.*, 2009, **53**, 1220.
186 D. Bode, C. Rolin, S. Schols, M. Debucquoy, S. Steudel, G. H. Gelinck, J. Genoe and P. Heremans, *IEEE Trans. Electron Devices*, 2010, **57**, 201.
187 M. Ahles, R. Schmechel and H. von Seggern, *Appl. Phys. Lett.*, 2005, **87**, 113505.
188 Y. Y. Lin, A. Dodabalapur, R. Sarpeshkar, Z. Bao, W. Li, K. Baldwin, V. R. Raju and H. E. Katz, *Appl. Phys. Lett.*, 1999, **74**, 2714.
189 B. Crone, A. Dodabalapur, Y. Y. Lin, R. W. Filas, Z. Bao, A. LaDuca, R. Sarpeshkar, H. E. Katz and W. Li, *Nature*, 2000, **403**, 521.
190 B. K. Crone, A. Dodabalapur, R. Sarpeshkar, R. W. Filas, Y. Y. Lin, Z. Bao, J. H. O'Neill, W. Li and H. E. Katz, *J. Appl. Phys.*, 2001, **89**, 5125.
191 H. Klauk, M. Halik, U. Zschieschang, F. Eder, D. Rohde, G. Schmid and C. Dehm, *IEEE Trans. Electron Devices*, 2005, **52**, 618.
192 S. De Vusser, S. Steudel, K. Myny, J. Genoe and P. Heremans, *Appl. Phys. Lett.*, 2006, **88**, 162116.
193 B. Yoo, T. Jung, D. Basu, A. Dodabalapur, B. A. Jones, A. Facchetti, M. R. Wasielewski and T. J. Marks, *Appl. Phys. Lett.*, 2006, **88**, 082104.
194 B. Yoo, A. Madgavkar, B. A. Jones, S. Nadkarni, A. Facchetti, K. Dimmler, M. R. Wasielewski, T. J. Marks and A. Dodabalapur, *IEEE Electron Device Lett.*, 2006, **27**, 737.
195 B. Yoo, B. A. Jones, D. Basu, D. Fine, T. Jung, S. Mohapatra, A. Facchetti, K. Dimmler, M. R. Wasielewski, T. J. Marks and A. Dodabalapur, *Adv. Mater.*, 2007, **19**, 4028.
196 J. H. Na, M. Kitamura and Y. Arakawa, *Thin Solid Films*, 2009, **517**, 2079.
197 H. E. A. Huitema, G. H. Gelinck, P. J. G. van Lieshout, E. van Veenendaal and F. J. Touwslager, *J. Soc. Inf. Disp.*, 2006, **14**, 729.
198 I. Yagi, N. Hirai, Y. Miyamoto, M. Noda, A. Imaoka, N. Yoneya, K. Nomoto, J. Kasahara, A. Yumoto and T Urabe, *J. Soc. Inf. Disp.*, 2008, **16**, 15.
199 Y. Nakajima, T. Takei, T. Tsuzuki, M. Suzuki, H. Fukagawa, T. Yamamoto and S. Tokito, *J. Soc. Inf. Disp.*, 2009, **17**, 629.
200 Y. Yang and A. J. Heeger, *Nature*, 1994, **372**, 344.

