

Fermi Level Pinning by Gap States in Organic Semiconductors

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We measure the gap density of states and the Fermi level position in thin-film transistors based on pentacene and dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) films grown on various surfaces using Kelvin probe force microscopy. It is found that the density of states in the gap of pentacene is extremely sensitive to the underlying interface and governs the Fermi level energy in the gap. The density of gap states in pentacene films grown on bare silicon dioxide (SiO₂) was found to be larger by 1 order of magnitude compared to that in pentacene grown on SiO₂ treated with hexamethyldisilazane and larger by 2 orders of magnitude compared to that of pentacene grown on aluminum oxide (AlO_x) treated with a self-assembled monolayer (SAM) of *n*-tetradecylphosphonic acid (HC₁₄-PA). When DNTT was grown on HC₁₄-PA-SAM-treated AlO_x, the gap density of states was even smaller, so that the Fermi level pinning was significantly reduced. The correlation between the measured gap density of states and the transistor performance is demonstrated and discussed.

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The density of states (DOS) in organic molecular layers is of fundamental importance for charge transport in organic materials and devices. In addition, gap states in any (organic and inorganic alike) semiconductor severely affect its electronic transport properties and the performance of devices. The effect of such states in thin films of polycrystalline small-molecule semiconductors may be even more detrimental, since in most cases the crystallinity of organic materials is not perfect and they are expected to have a higher density of structural defects than single crystals. In addition, most organic devices are not fabricated under ultraclean conditions; therefore, the impurity concentration is generally larger than in single crystal inorganic semiconductors. For example, the charge carrier mobility in thin films of pentacene (one of the most commonly used organic device materials) is presumed to be severely affected by defects and trap sites at grain boundaries located near the semiconductor-dielectric interface [1,2]. Furthermore, defect states might be caused by environmental conditions, such as exposure to oxygen and moisture. Therefore, it is essential to gain a fundamental understanding of such effects and their underlying microscopic processes.

Even though some progress has been reported in recent years, the study of gap states in organic semiconductors and devices is very limited. First, reliable, sensitive, and quantitative methods to measure the concentration and energy distribution of such states have to be developed. Second, fundamental issues surrounding the origin of gap states in organic materials are not resolved, and relatively little is known about the influence of these states on the electronic properties and the electrical stability of organics [3–12]. In organic thin-film transistors (TFTs), key parameters such as charge mobility, threshold voltage, subthreshold swing,

and electrical and environmental stability are considerably affected by gap states that act as charge traps both at the interface between the gate dielectric and the organic semiconductor and in the semiconductor volume [13,14].

Gap states can also pin the Fermi level (FL), and even though several reports in recent years emphasized the importance of the FL pinning induced by gap states in organic materials and devices, their role in determining the FL position is still an open question [15,16]. For example, one hypothesis is that the FL pinning (see a comprehensive review by Braun *et al.* [17]) is governed by the work function difference between the organic material and the underlying substrate, and pinning occurs above or below a certain substrate work function. Another model is the induced density of interfacial states [18], which proposes that the FL alignment at metal or organic interfaces is governed by a charge neutrality level that is naturally controlled by the energy and concentration of the interface gap states. Since the FL energy determines the doping concentration, doping efficiency, junction built-in potentials, and bands alignment, the role of gap states in determining the FL position becomes even more important.

Ultraviolet photoelectron spectroscopy is probably the most commonly used method to measure DOS in both inorganic and organic materials and has already been used for organic small molecules such as pentacene [19]. Current-voltage, capacitance-voltage, and deep-level transient spectroscopy measurements were also performed on pentacene TFTs [20]. Hole traps at 0.24, 0.31, and 1.08 eV above the valence band maximum and electron traps at 0.69 eV below the conduction band minimum were observed. Other methods, such as photoconductivity, space-charge-limited current measurements and electron

spin resonance, were also used to extract the DOS in organic materials [8,21,22].

We use Kelvin probe force microscopy (KPFM) to measure the gap density of states and the Fermi level position in pentacene and in dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) thin films grown on bare and on functionalized SiO_2 and AlO_x surfaces. We show that the density of states in the gap of pentacene is extremely sensitive to the properties of the underlying surface. The density of gap states in pentacene grown on bare SiO_2 was found to be larger by 1 order of magnitude compared to that in pentacene grown on SiO_2 treated with hexamethyldisilazane (HMDS) and larger by 2 orders of magnitude compared to that in pentacene grown on AlO_x treated with a self-assembled monolayer (SAM) of *n*-tetradecylphosphonic acid (HC_{14} -PA). DNTT films grown on AlO_x treated with a HC_{14} -PA SAM were found to have an even smaller gap DOS, so small in fact that the FL pinning was significantly reduced, which to our knowledge has not been previously reported for organic TFTs. Moreover, we show that the gap states determine the FL position in the gap and how they affect the transistor performance.

All KPFM and current-voltage measurements were performed on TFTs fabricated in the bottom-gate, top-contact (inverted staggered) device structure. The TFTs with AlO_x /SAM gate dielectrics were fabricated (see Fig. 1) on glass substrates with 20-nm-thick Al gate electrodes, a gate dielectric consisting of a 3.6-nm-thick AlO_x layer and a 1.7-nm-thick HC_{14} -PA monolayer, onto which a 25-nm-thick pentacene or DNTT film was deposited by thermal

sublimation at a base pressure of 10^{-6} mbar, at a substrate temperature of 60°C and with a growth rate of 1 nm/min [23,24]. The TFTs with SiO_2 or SiO_2 /HMDS gate dielectrics (see Fig. 2) were prepared on silicon substrates with a 300-nm-thick layer of SiO_2 grown by thermal oxidation (and either left untreated or treated with a thin layer of HMDS), onto which a 10-nm-thick pentacene film was grown by the molecular-beam deposition method [25] at a base pressure of 4×10^{-10} Torr, at a substrate temperature of 60°C , and with a growth rate of 0.3 nm/min. The TFTs with AlO_x /SAM gate dielectrics have a channel length of 30 μm and a channel width of 100 μm , while the TFTs with SiO_2 or SiO_2 /HMDS gate dielectrics have a channel length of 20 μm and a channel width of 5 mm. All the KPFM and current-voltage measurements were carried out in a nitrogen-filled glove box (less than ~ 5 ppm H_2O) at room temperature using a Dimension 3100 atomic force microscopy system and an Agilent B1500A semiconductor parameter analyzer.

Figure 1(c) shows the current-voltage characteristics of pentacene (black lower line) and DNTT (red upper line) on HC_{14} -PA-SAM-treated AlO_x . The carrier mobilities extracted from the transfer characteristics were $0.09 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for pentacene and $0.62 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for DNTT. The subthreshold swings were found to be 141 mV/decade for pentacene and 95 mV/decade for DNTT. Thus, the DNTT TFT has a steeper subthreshold swing and a larger mobility than the pentacene TFT. It has already been reported that DNTT TFTs show better air stability in comparison to pentacene, due to the larger ionization potential of DNTT (5.4 eV) compared with

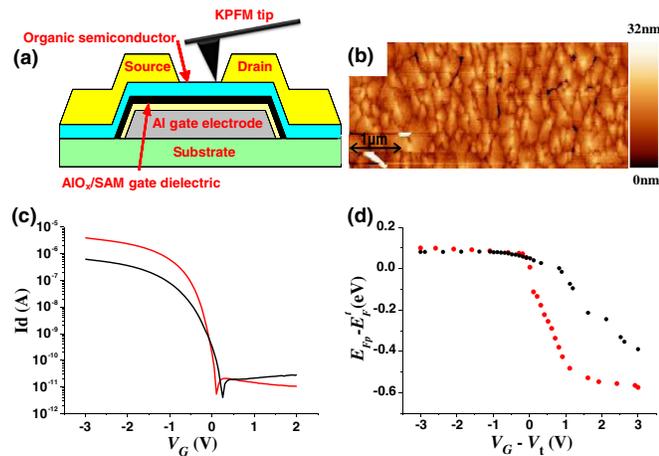


FIG. 1 (color online). (a) Schematic of the organic TFT structure with the KPFM tip above the semiconductor and (b) Atomic force microscopy topography of pentacene grown on HC_{14} -PA-SAM-treated AlO_x . (c) Measured drain current as a function of the gate-source voltage at a drain-source voltage of -1 V of a pentacene TFT (black lower line) and of a DNTT TFT (red upper line) with an AlO_x / HC_{14} -PA-SAM gate dielectric. (d) CPD as a function of V_G measured on pentacene (black upper line) and on DNTT (red lower line) deposited onto HC_{14} -PA-SAM treated AlO_x .

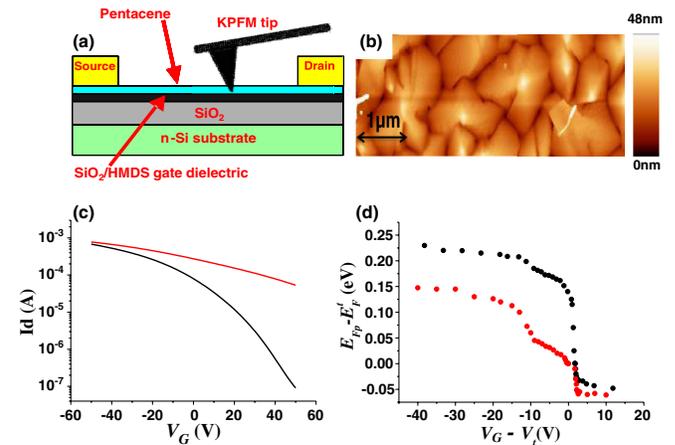


FIG. 2 (color online). (a) Schematic of the organic TFT structure with the KPFM tip above the semiconductor and (b) Atomic force microscopy topography of pentacene grown on HMDS-treated SiO_2 . (c) Measured drain current as a function of the gate-source voltage at a drain-source voltage of -1 V of a pentacene TFT with an SiO_2 /HMDS gate dielectric (black lower line) and with a bare SiO_2 gate dielectric (red upper line). (d) CPD as a function of V_G measured on pentacene grown on HMDS-treated SiO_2 (black upper line) and on pentacene grown on bare SiO_2 (red lower line).

that of pentacene (5.0 eV) [24]. Structural defects induced by oxidation can lead to a degradation of the device performance as measured here.

Figure 1(d) shows the surface potential [defined as $V(x) \equiv \text{CPD}(x) - \text{CPD}_t(x) = 0$] measured by KPFM on pentacene and on DNNT deposited onto AlO_x treated with an HC_{14} -PA SAM far away from the drain and source contacts as a function of the gate-source voltage (V_G). The contact potential difference (CPD) is proportional to the quasi-FL position [26]; therefore, the large CPD change around $V_G = 0$ V is due to the relatively large change in the FL position as holes are injected from the contacts into the channel. The CPD saturates at large negative gate bias due to the larger density of states as the quasi-FL moves into the highest occupied molecular orbital (HOMO) band, which indicates FL level pinning. The measured change in CPD around the threshold voltage is greater in DNNT (red lower line) than in pentacene (black upper line), which is consistent with the steeper subthreshold swing of the DNNT TFT. In the TFTs with the AlO_x /SAM gate dielectrics, the measurements cannot be extended beyond $V_G = -3$ V, which corresponds to a gate field of 5.5 MV/cm, due to dielectric breakdown.

Figure 2(c) shows the current-voltage characteristics of pentacene on HMDS-treated SiO_2 (black lower line) and of pentacene on bare SiO_2 (red upper line). The carrier mobilities extracted from the transfer characteristics were $0.03 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $0.001 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and the subthreshold swings were 12 V/decade and 15 V/decade, respectively. Although in these devices the pentacene was grown by molecular beam deposition, the subthreshold swings are larger by 2 orders of magnitude compared to the pentacene deposited by thermal sublimation onto AlO_x treated with an HC_{14} -PA SAM. In general, alkylphosphonic acid SAMs on AlO_x are more hydrophobic (contact angle 108°) [27] compared to HMDS-treated SiO_2 (contact angle 66°) [28]. In the case of bare SiO_2 the large density of hydroxyl groups will make the surface much more hydrophilic. The smaller the surface energy (i.e., the larger the contact angle) of the gate dielectric is, the smaller is the expected degree of interaction between the pentacene molecules and the gate dielectric surface. Therefore, the larger is the expected degree of interaction between adjacent pentacene molecules, and this better interaction among neighboring pentacene molecules is expected to lead to a more uniform thin-film morphology and hence to a smaller density of gap defects, which is consistent with the measurement results.

Figure 2(d) shows the surface potential measured on pentacene deposited onto HMDS-treated SiO_2 (black upper line) and on pentacene deposited onto bare SiO_2 (red lower line). The CPD change is saturated at a negative gate bias due to a large DOS close to the HOMO band. In addition, the CPD saturates when $V_G > V_t$ due to a large DOS located deeper in the pentacene gap. We believe that this observation is evidence of FL pinning induced by the gap states. On the

contrary, the measured CPD on pentacene grown on HC_{14} -PA-treated AlO_x [Fig. 1(d)] does not show such strong FL pinning in the gap, due to a much smaller concentration of gap states.

The device performance of pentacene-based organic TFTs is highly correlated with the pentacene layer morphology, which is affected by the surface properties of the dielectric, the substrate temperature during the semiconductor deposition, the deposition rate, and the pressure in the deposition chamber [29]. The role of hydrophobic interfacial layers such as HMDS that changes the OH-terminated SiO_2 to a (CH_3) -terminated one in improving the organic field-effect transistor performance is attributed mainly to the reduction of electron trapping at the SiO_2 -pentacene interface [30] compared to an untreated sample. The electron trapping originates mainly from hydroxyl groups, present in the form of silanols at the SiO_2 -pentacene interface [31]. Figures 1(b) and 2(b) show atomic force microscopy topography images of pentacene grown on HMDS-treated SiO_2 [Fig. 1(b)] and pentacene grown on HC_{14} -PA-SAM-treated AlO_x [Fig. 2(b)]. As shown in the figures, the pentacene grain size on HMDS-treated SiO_2 is larger than that on HC_{14} -PA-SAM-treated AlO_x . Different grain size implies that the molecular order and structural defects in the pentacene may be very different, depending on the surface properties. Moreover, the results here suggest that a larger grain size does not necessarily lead to larger charge mobility or smaller density of states.

The DOS were extracted from the CPD measurements as described in our previous work [32] to give

$$g(E) = \frac{d(C_{\text{TFT}}[V_G - V_t - V(x)] \frac{dV(x)}{dV_L})}{qd_{\text{eff}}dV(x)}, \quad (1)$$

where $g(E)$ is the DOS energy distribution, q is the elementary charge, V_G is the gate-source voltage, $V(x)$ is the measured CPD relative to the CPD at the threshold voltage V_t , V_L is the interface potential relative to the potential at V_t , d_{eff} is the effective accumulation layer thickness defined as the channel width that contains 90% of the injected charge concentration and C_{TFT} is the TFT capacitance per unit area that is a serial combination of the gate-dielectric capacitance and the semiconductor layer capacitance. The DOS was obtained by using the data of Figs. 1(d) and 2(d) in Eq. (1).

Figure 3 shows the DOS for pentacene (black, curve 3) and DNNT (red, curve 4) grown on HC_{14} -PA-SAM-treated AlO_x , and for pentacene grown on HMDS-treated SiO_2 (green, curve 2) and on bare SiO_2 (blue, curve 1). The energy scale is derived from the CPD changes in Figs. 1(d) and 2(d) and from the FL position measured by the KPFM as explained below. It is observed that pentacene grown on HC_{14} -PA-SAM-treated AlO_x has a larger gap DOS compared to DNNT grown on the same surface. This is consistent with the differences in the subthreshold swing found

between the two transistors [see Fig. 1(c)] and with the better air stability of DNTT. In addition, it is shown that the gap DOS in pentacene grown on HC₁₄-PA-SAM-treated AlO_x is smaller by 1 order of magnitude compared with the gap DOS in pentacene grown on HMDS-treated SiO₂. The large difference between the DOS distribution is probably due to the larger defect density in the pentacene when deposited onto HMDS-treated SiO₂, as opposed to AlO_x functionalized with a more ordered and more hydrophobic alkylphosphonic acid SAM. Also, the measured energy range for the DOS was much smaller when the pentacene was deposited onto bare or HMDS-treated SiO₂, which is consistent with FL pinning demonstrated in Fig. 2(d). We note that Eq. (1) is a good approximation only if $g(E)$ is much wider compared to the derivative of the Fermi-Dirac distribution with respect to the level shift ($\frac{df_{FD}}{dV_L}$); therefore, any features which are kT wide we consider as a measurement artifact. The measurements were reproducible within the same transistor and for several transistors (see Fig. S1 and S2 in the Supplemental Material [33]).

The dotted vertical lines in Fig. 3 represent the FL position measured for each sample under flat band conditions. The FL energy was measured by the KPFM using reported values of electron affinity ($\chi_p = 3.2$ eV and $\chi_{DNTT} = 2.4$ eV) [34,35] and band gap ($E_g^p = 1.8$ eV and $E_g^{DNTT} = 3.2$ eV) [34,35] for pentacene and DNTT, respectively. The tip work function is determined by measuring an *in situ* peeled, highly ordered pyrolytic graphite with a known work function of 4.6 eV. From the measured work function we find that the FL position in DNTT and pentacene grown on HC₁₄-PA-SAM-treated AlO_x is 0.2 ± 0.1 eV and 0.23 ± 0.1 eV above the HOMO band,

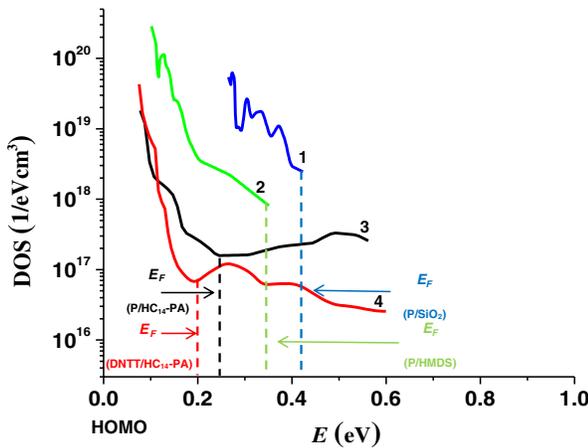


FIG. 3 (color online). DOS in pentacene grown on bare SiO₂ (blue line, curve 1), in pentacene grown on HMDS-treated SiO₂ (green line, curve 2), in pentacene grown on HC₁₄-PA-SAM treated AlO_x (black line, curve 3), and in DNTT grown on HC₁₄-PA-SAM-treated AlO_x (red line, curve 4). The dotted vertical lines represent the FL position in a flat band condition.

respectively. In comparison, the FL position for pentacene grown on HMDS-treated and on bare SiO₂ was found to be 0.35 ± 0.1 eV and 0.42 ± 0.1 eV above the HOMO band, respectively. Each value represents an average of 10 measurements for each sample.

We attribute the differences in the FL energy between the four samples to different degrees of FL pinning by the gap DOS as depicted in Fig. 4. The figure shows that for low density of gap states [Fig. 4(a)], the Fermi level is closer to the HOMO band in comparison with the case of large density of gap states in Fig. 4(b). The FL position determines the energy level alignment so that the work function of the pentacene with the larger density of states (b) is smaller, in agreement with the measurements presented in Fig. 3. The level alignment in both Figs. 4(a) and 4(b) is achieved by hole injection from the source and drain electrodes into the organic layer; this is different to the case in Ref. [16] where the energy level alignment is achieved by electron tunneling through the thin gate oxide layer. The difference in FL pinning for the four samples can also be inferred from the CPD measurements as a function of the back gate bias, dE_f/dV_G , as explained in the Supplemental Material [33]. We emphasize that the FL energy is measured under equilibrium, i.e., the FL position following the charge transfer from the metal contacts into the organic semiconductor film for energy level alignment. The FL (i.e., quasi-FL) is also pinned during device operation near the HOMO band edge where there is a high density of states. This is also observed in our CPD measurement in negative gate bias [Figs. 1(d) and 2(d)].

In conclusion, the KPFM measurements enabled us to determine the DOS energy distribution in pentacene thin-film transistors. We have found that the gap DOS of pentacene grown on aluminum oxide functionalized with a hydrophobic self-assembled monolayer of an alkylphosphonic acid (HC₁₄-PA) is 1 order of magnitude smaller compared to pentacene grown on HMDS-treated SiO₂. Moreover, we have shown that DNTT has an even smaller gap states concentration compared with pentacene grown

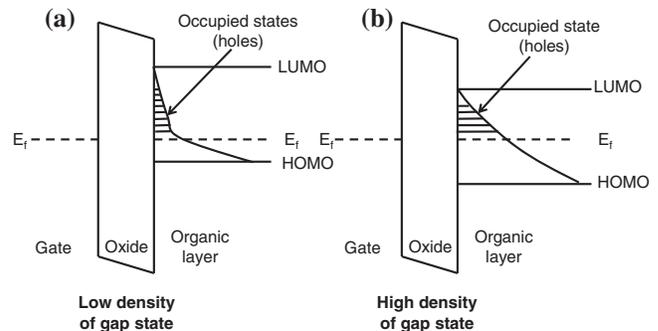


FIG. 4. Schematic energy level of the organic field-effect transistor for low (a) and high (b) density of gap states. The horizontal lines in the gap represent the gap states occupied by holes, below which the Fermi level is pinned.

on the same surface and consequently possesses very weak FL pinning. This observation is consistent with transfer characteristics measurements that show superior performance of DNTT compared with pentacene. Clear evidence of FL pinning induced by gap states was observed in the case of pentacene and correlated with the device performance.

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