Contact Doping and Ultrathin Gate Dielectrics for Nanoscale Organic Thin-Film Transistors

Frederik Ante, Daniel Kälblein, Ute Zschieschang, Tobias W. Canzler, Ansgar Werner, Kazuo Takimiya, Masaaki Ikeda, Tsuyoshi Sekitani, Takao Someya, and Hagen Klauk**

Organic thin-film transistors (TFTs) are of interest for electronic applications on flexible plastic substrates, such as rollable or foldable active-matrix displays,[1] conformable sensor arrays,[2] and flexible identification tags.[3] Due to the relatively small intrinsic field-effect mobility in most conjugated organic semiconductors (<5 cm^2 V^{-1} s^{-1}), the maximum frequency at which organic TFTs can be operated is usually limited to about 1 MHz.[3] For certain applications, such as the integration of the row and column drivers for high-resolution active-matrix displays or sensor arrays directly on the flexible backplane,[4,5] organic TFTs that can be operated at higher frequencies (>10 MHz) are highly desirable. Such high frequencies are indeed feasible, provided the lateral dimensions of the organic TFTs are sufficiently small (about 100 nm). However, TFTs with such small lateral dimensions will suffer from a variety of detrimental short-channel effects, unless a number of important scaling requirements are observed in the design and fabrication of the transistors. Here we report on the successful fabrication and detailed analysis of organic TFTs with channel lengths and gate overlaps of about 100 nm in which the short-channel effects are greatly suppressed by area-selective contact doping (using a strong organic dopant) and by aggressive gate-dielectric scaling (using a 5.7 nm-thick, low-temperature-processed gate insulator based on a molecular self-assembled monolayer). As a result, these nanoscale organic TFTs have off-state drain currents below 1 pA, on/off current ratios near 10^7, as well as clean linear and saturation characteristics. The transconductance of these transistors reaches 0.4 S m^{-1}, which is the largest transconductance reported for organic TFTs with patterned gate electrodes.

The gate electrodes and source/drain contacts of organic TFTs are usually defined by photolithography,[1,3,4] shadow-masking,[2,5] or inkjet printing,[6] and the minimum feature size that can be achieved with these methods is usually above 1 µm. The Cambridge University group has recently developed an innovative self-aligned inkjet-printing process that makes it possible to fabricate organic TFTs with a channel length of less than 200 nm and gate-to-source and gate-to-drain overlaps of less than 700 nm.[7,8] Organic TFTs with such small lateral dimensions can in principle reach frequencies above 10 MHz, despite the modest mobilities in organic semiconductors, and even if the TFTs are operated with low voltages of about 5 V or less (see Supporting Information, SI). The ability to manufacture organic TFTs with nanoscale lateral dimensions using large-area-compatible printing techniques, such as demonstrated by the Cambridge group, creates unique and exciting opportunities for organic TFTs in high-frequency electronic applications.

However, when the channel length of a field-effect transistor is reduced, the thickness of its gate dielectric must also be reduced in order to keep the ratio between the channel length and the gate-dielectric thickness large, ideally at least about 20.[9] Otherwise the electric potential along the carrier channel will be dominated by the lateral electrical field (determined by the drain–source voltage V_{DS} and the channel length L), rather than by the transverse electric field (determined by the gate–source voltage V_{GS} and the gate-dielectric thickness t_{diel}), which has undesirable consequences on the transistor characteristics, including large off-state currents, small on/off current ratios, and poor current saturation. This can be seen in most previous reports on organic TFTs with submicrometer lateral dimensions.[7–17]

A second important requirement for the realization of nanoscale organic TFTs is a substantial reduction

F. Ante, D. Kälblein, Dr. U. Zschieschang, Dr. H. Klauk
Max Planck Institute for Solid State Research
Heisenbergstr. 1, 70569 Stuttgart, Germany
E-mail: F.Ante@fkf.mpg.de; H.Klauk@fkf.mpg.de

Prof. K. Takimiya
Department of Applied Chemistry
Graduate School of Engineering
Institute for Advanced Materials Research
Hiroshima University
Higashi-Hiroshima, Japan

Dr. M. Ikeda
Functional Chemicals R&D Laboratories
Nippon Kayaku Co., Ltd., Kita-ku, Tokyo, Japan

Prof. T. Sekitani, Prof. T. Someya
Department of Electrical Engineering
University of Tokyo
Tokyo, Japan

Dr. T. W. Canzler, Dr. A. Werner
Novaled AG, Dresden, Germany

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of the contact resistance. If the contact resistance is not reduced along with the reduction in channel length, the drain current at small drain–source voltages will be greatly suppressed, which causes the well-documented nonlinearity in the output characteristics of the transistors.[6–17] The contact resistance of organic TFTs can in principle be reduced by area-selective impurity doping. If the energy of the lowest unoccupied molecular orbital (LUMO) of the dopant molecules is near (ideally below) the energy of the highest occupied molecular orbital (HOMO) of the host semiconductor, electrons can move from the host semiconductor to the dopant molecules, thereby creating excess holes in the semiconductor and thus increasing its electrical conductivity.[18–22] This concept has previously been applied to organic p-channel TFTs with channel lengths down to 300 nm.[23–28] In all these reports, however, the gate electrode of the TFTs was not patterned. Instead of a patterned gate electrode, a conducting silicon wafer served not only as the substrate, but also as the gate electrode for all the TFTs on the substrate. As a result, the overlap between the gate electrode and the source and drain contacts of the TFTs was very large (>100 µm). Such a large gate overlap has the distinct advantage that the charge injection from the contact into the semiconductor spreads across a large contact area,[29,30] but it has the distinct disadvantage of producing a large parasitic capacitance that limits the maximum frequency at which the transistors can be operated (see SI). Reducing the gate overlaps helps to reduce the parasitic capacitance, but will also create the problem of a severely reduced contact length and hence possibly much larger contact resistance.[29,30] Thus, a key question that has so far not been addressed is how useful the concept of contact doping is for organic TFTs with submicrometer channel length and with submicrometer gate overlap. To answer this question, electron-beam lithography and a proprietary organic dopant (Novaled NDP-9) have been employed in order to fabricate organic TFTs with submicrometer gate electrodes, precisely aligned, chemically doped source/drain contacts, and submicrometer channel length. Electron-beam lithography is obviously incompatible with large-area electronics, but it is helpful in understanding the material requirements for aggressive gate-dielectric scaling and controlled contact doping, until high-resolution printing techniques[7,8] become more routine.

The organic TFTs developed here are based on the inverted staggered (bottom-gate, top-contact) device architecture. Each TFT has an aluminum gate electrode that is patterned by electron-beam lithography, a 5.7 nm-thick gate dielectric (composed of a thin AlO_x layer created by surface oxidation and an organic self-assembled monolayer grown from solution[31]), a 20 nm-thick layer of the air-stable organic semiconductor dinaphtho-[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT),[32–34] and 25 nm-thick gold source/drain contacts deposited on top of the organic semiconductor layer. To pattern nanoscale source/drain contacts on top of the semiconductor layer without damaging the organic semiconductor by exposure to organic solvents[35] or elevated temperatures,[36] an elegant process was employed that was developed by the RIKEN group, which uses a suspended resist bridge created by electron-beam lithography prior to the deposition of the organic semiconductor layer.[15,23–25] During the deposition of the organic semiconductor, the substrate is tilted, so that the semiconductor forms a continuous layer underneath the suspended resist bridge, while the deposition of the gold source/drain contacts is performed at an angle of 90°, using the resist bridge as a high-resolution shadow mask. Aside from the resist bake, the maximum process temperature is 60 °C, which is fully compatible with flexible polymeric substrates. The fabrication process is described in detail in the SI. **Figure 1** shows a schematic cross-section and three electron microscopy images of the submicrometer organic TFTs.

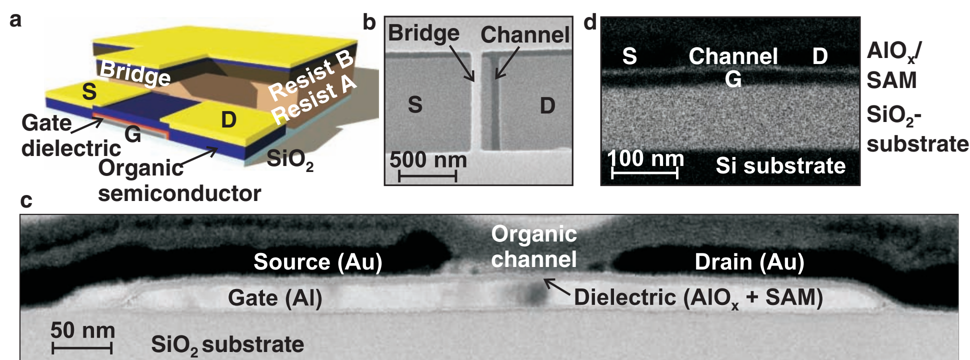

Figure 1. Top-contact organic TFTs with deep-submicrometer channel length and gate overlap and a 5.7 nm-thick low-temperature-processed gate dielectric. a) Schematic cross-section showing the patterned metal gate electrode, the gate dielectric (3.6 nm AlO_x + 2.1 nm self-assembled monolayer), the organic semiconductor layer, the Au source/drain contacts, and the suspended resist bridge created by electron-beam lithography. b) Scanning electron microscope image of the suspended resist bridge and the Au source/drain contacts (sample tilted for imaging). c) Cross-sectional transmission electron microscope image of a TFT with a channel length of 100 nm and a gate overlap of 200 nm. The patterned Al gate electrode, the gate dielectric, and the source/drain contacts are clearly distinguished. The 20 nm-thick organic semiconductor layer, sandwiched between the gate dielectric and the source/drain contacts, is not resolved in this image. d) Oxygen map recorded by electron energy loss spectroscopy in a transmission electron microscope. The oxygen signals from the SiO_2 (top layer of the substrate) and from the AlO_x (part of the gate dielectric) are clearly seen.

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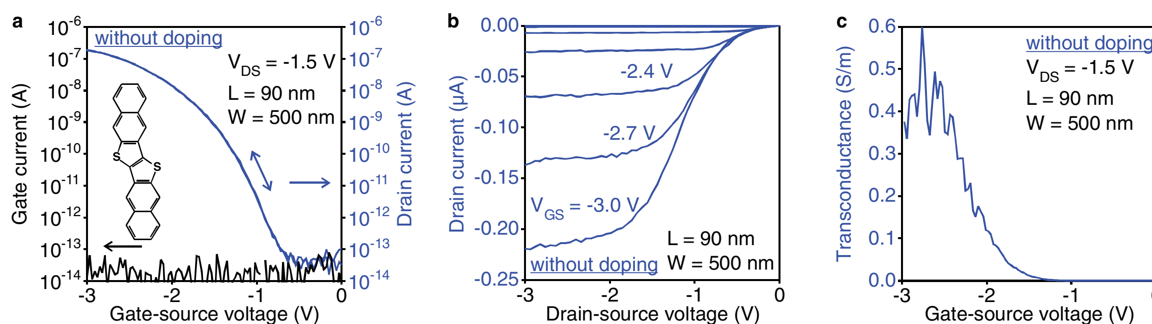

Figure 2. Electrical characteristics of a submicrometer TFT without contact doping (L = 90 nm, ΔL = 200 nm). a) Transfer characteristics. The off-state drain current (at V_{GS} = 0 V) and the gate current are near the detection limit (<10^{-13} A), the on/off current ratio is 10^7, the subthreshold swing is 160 mV dec^{-1}, and the field-effect mobility extracted from the transfer characteristics is 0.05 cm^2 V^{-1} s^{-1}. The hysteresis in the current–voltage curve is negligible. The molecular structure of the organic semiconductor DNTT is shown in the inset. b) Output characteristics of the same device. For large drain–source voltages ($V_{DS} > V_{GS}$-V_{th}) the drain current shows good saturation, despite the small channel length. For small drain–source voltages ($V_{DS} < V_{GS}$-V_{th}), the drain current is greatly suppressed due to the large contribution of the contact resistance to the total device resistance. c) Transconductance ($g_m = \partial I_D/\partial V_{GS}$) per channel width as a function of gate-source voltage for the same device. The width-normalized transconductance reaches a maximum of 0.4 S m^{-1}, which is the largest width-normalized transconductance reported for an organic transistor with a patterned gate electrode.

All electrical measurements were performed in ambient air at room temperature. The electrical characteristics of a TFT with a channel length of 90 nm, a channel width of 500 nm, and a gate overlap of 200 nm are shown in **Figure 2**. The ratio between the channel length (90 nm) and the gate-dielectric thickness (5.7 nm) is sufficiently large to facilitate strong gate coupling, so the off-state drain current is very small (about 10^{-13} A) and the on/off current ratio is very large (10^7), essentially identical to TFTs with a channel length of 30 µm.[32] This on/off current ratio is the largest reported for a submicrometer organic TFT. The field-effect mobility extracted from the current–voltage characteristics is 0.05 cm^2 V^{-1} s^{-1}. The TFT has a maximum transconductance of 0.2 µS (also extracted from the current–voltage characteristics) and a gate capacitance of 1.7 fF (calculated from the device geometry and materials parameters), so the maximum frequency of operation predicted by Equation S1, SI, is 20 MHz. The transconductance normalized to the channel width (500 nm) is 0.4 S m^{-1}, which is the largest width-normalized transconductance that has so far been reported for an organic TFT with a patterned gate electrode. (A transconductance of 0.7 S m^{-1} has recently been obtained for organic TFTs fabricated on a conducting silicon wafer serving both as the substrate and as a global gate electrode.[25])

However, due to the large contribution of the contact resistance in these nanoscale TFTs, the output characteristics in Figure 2 show the familiar non-linearity of the drain current at small drain–source voltages (–1 V ≤ V_{DS} ≤ 0 V). In order to reduce the contact resistance and improve the drain-current linearity, we have also fabricated TFTs with a nominally 1 nm thick, vacuum-deposited layer of the organic molecular dopant NDP-9 inserted between the semiconductor layer and the gold source/drain contacts. Atomic force microscope (AFM) images of DNTT layers without NDP-9 and with various amounts of NDP-9 deposited on top of a DNTT layer are shown in SI, Figure S2. The images indicate that depositing a 1 nm thick NDP-9 layer onto DNTT leads to isolated clusters that coalesce into a continuous layer when more than 1 nm of NDP-9 is deposited.

To confirm that doping with NDP-9 indeed increases the electrical conductivity of DNTT, we first fabricated TFTs with the dopant molecules deposited along the entire channel and in the contact regions. Comparing the transfer characteristics of TFTs without doping (**Figure 3**a) and with contact and channel doping (Figure 3b) shows that the channel doping greatly increases the off-state drain current. To rule out that the observed current increase is due to charge flow through the NDP-9, rather than through the DNTT, devices with 30 nm thick NDP-9 instead of DNTT were also made. SI, Figure S3, shows the current–voltage characteristics of such an NDP-9-only device. As can be seen, the current through the 30 nm-thick NDP-9 layer is below the leakage level, confirming that there is essentially no charge flow through the NDP-9 in this device. This confirms that charge flow in the DNTT TFTs with contact and channel doping (Figure 3b) occurs only through the DNTT and not through the NDP-9.

Figure 3c shows the transfer characteristics (measured within 3 h after fabrication) of TFTs in which the dopant NDP-9 was deposited only in the contact regions, but not in the channel region. In this case the off-state drain current and the subthreshold swing are identical to those of TFTs without doping (Figure 3a), suggesting that the dopants do not drift or diffuse from the contact regions into the channel region during or shortly after transistor fabrication.

Comparing the output characteristics of TFTs without doping (Figure 3a) and with contact doping (Figure 3c) reveals that contact doping with NDP-9 greatly increases the drain current at small drain–source voltages. For example, the drain current at V_{GS} = –3 V and V_{DS} = –0.5 V increases from –5 nA in the TFT without doping to -30 nA in the TFT with contact doping. This 6-fold increase in drain current is not due to a shift in threshold voltage, but due to a reduction in the width of the Schottky barrier at the contact/semiconductor interfaces, which means that a larger portion of the drain–source

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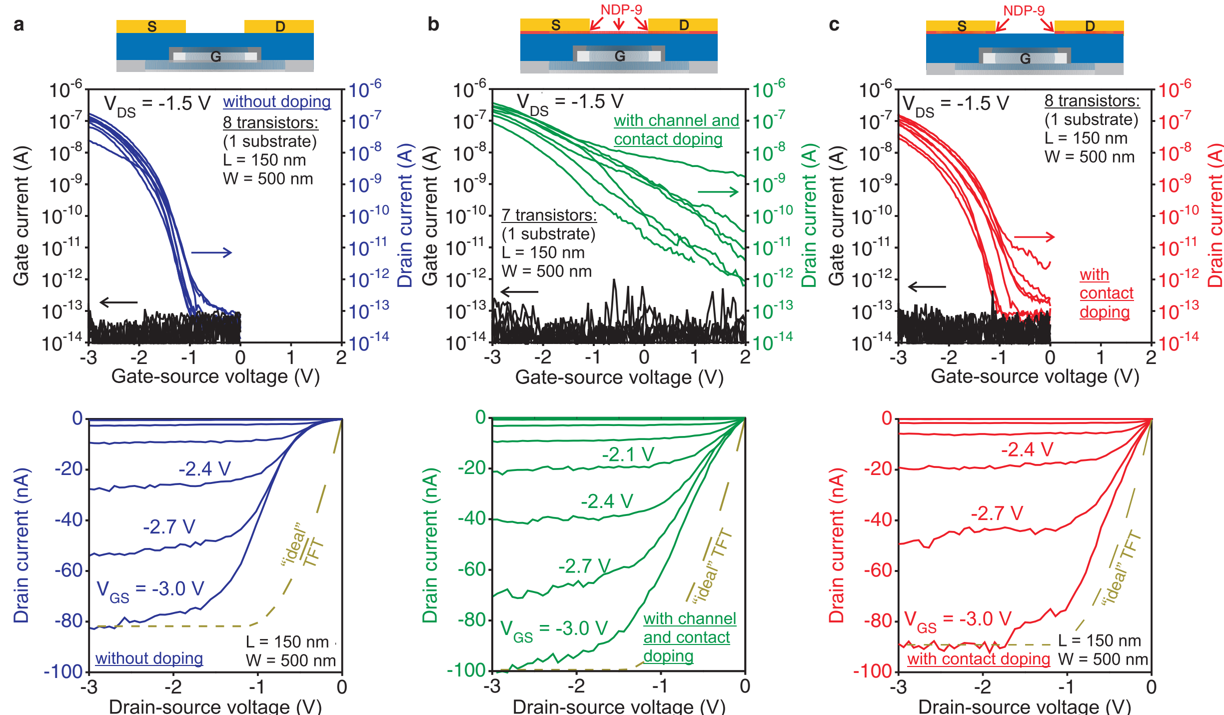

Figure 3. Impact of channel doping and contact doping on the electrical characteristics of submicrometer TFTs (L = 150 nm, ΔL = 200 nm). a) Transfer and output characteristics of submicrometer TFTs without doping. b) Transfer and output characteristics of submicrometer TFTs with contact and channel doping. The transfer characteristics show that the channel doping greatly increases the off-state drain current (from $<10^{-13}$ to about 10^{-9} A at V_{GS} = 0 V), confirming that the dopant is electrically active and increases the excess carrier concentration in the semiconductor. The output characteristics show that the contact doping greatly increases the drain current at small drain–source voltages ($V_{DS} < V_{GS}$-V_{th}), which confirms that the doping reduces the width of the Schottky barrier at the contact/semiconductor interfaces, rendering the contacts essentially Ohmic. c) Transfer and output characteristics of submicrometer TFTs with contact doping (no channel doping). The transfer characteristics show a small off-state drain current and a large on/off ratio (similar to the TFTs without doping), while the output characteristics indicate Ohmic contact characteristics.

voltage drops along the channel, rather than across the contacts. Comparing the output characteristics in Figure 3a,c shows that contact doping also changes the shape of the measured I_D–V_{DS} curves closer to the 'ideal' linear shape.

The above results confirm that NDP-9 acts as a p-type dopant in DNTT, which in turn confirms that electrons are transferred from the HOMO of DNTT to the LUMO of NDP-9, thereby creating excess holes in the DNTT and increasing the conductivity of the semiconductor. This suggests that at the interface between the evaporated DNTT and the evaporated NDP-9, the LUMO energy of NDP-9 is near or below the HOMO energy of DNTT. Since we cannot measure the orbital energies at the DNTT/NDP-9 interface, we have to rely on conclusions from other measurements to elucidate the energy lineup at the DNTT/NDP-9 interface. SI, Figure S4, summarizes the results of several measurements we have carried out to compare the doping strength of NDP-9 to that of an organic dopant that has been previously employed in organic TFTs, 2,3,5,6-tetrafluoro-7,7,8,8-tetracyanoquinodimethane (F_4-TCNQ).[26,27] We found that the sheet resistance of a 30 nm-thick DNTT layer doped with NDP-9 (nominally 1 nm thick) is a factor of 7 smaller than the sheet resistance of a 30 nm-thick DNTT layer doped with F_4-TCNQ (also nominally 1 nm thick; SI, Figure S4a). In addition, our cyclic voltammetry measurements on NDP-9 and F_4-TCNQ indicate that the LUMO energy of NDP-9 is more negative by 0.1 eV than the LUMO energy of F_4-TCNQ (SI, Figure S4d). Since calculations and measurements by several other groups have shown that the LUMO energy of F_4-TCNQ is approximately –5.2 eV,[21,22,37,38] this indicates that the LUMO energy of NDP-9 is about –5.3 eV and thus sufficiently low to allow charge transfer between the LUMO of NDP-9 and the HOMO of DNTT (for which an energy of -5.3 ± 0.1 eV has been determined by cyclic voltammetry and density functional theory;[32] see SI, Figure S3c).

The quantitative analysis of the contact resistance is often performed using the transmission line method (TLM).[29] For TLM analysis it is assumed that the total resistance of a transistor (i.e., the resistance measured at the terminals of the transistor) is the sum of the channel resistance and the contact resistance. Neither the channel resistance nor the contact resistance are directly accessible, but both of them can be extracted by TLM analysis (see SI). However, TLM analysis produces useful results only if the parameter variations among the transistors are negligibly small. Unfortunately, the variations among our submicrometer TFTs are too large to permit TLM analysis (see SI, Figure S5a,b). Nevertheless, since the contact resistance cannot be larger than the total resistance, an upper limit of the contact resistance can be calculated simply by averaging the total resistance

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of a large number of transistors. For our submicrometer TFTs biased in the linear regime (V_{DS} = –0.1 V) we obtain a total resistance of 9.8 kΩ cm for TFTs without doping and 2.7 kΩ cm for TFTs with contact doping (see SI, Figure S5c).

To facilitate a more precise analysis of the contact resistance, we also fabricated long-channel top-contact TFTs with channel lengths ranging from 10 to 60 µm and with gate overlaps ranging from 5 to 200 µm. These TFTs were fabricated using macroscopic shadow masks.[34] In these long-channel TFTs the relative contribution of the contact resistance is much smaller than in the submicrometer TFTs, so the mobility extracted from the current–voltage characteristics of the long-channel TFTs is much larger (≈2.2 cm^2 V^{-1} s^{-1}; SI, Figure S6) than that of the submicrometer TFTs (≈0.05 cm^2 V^{-1} s^{-1}; Figure 2). More importantly, the device-to-device variations in the long-channel TFTs are sufficiently small to allow TLM analysis (see SI, Figure S7). For TFTs without contact doping, we find a contact resistance of 0.66 kΩ cm. Contact doping reduces the contact resistance to 0.39 kΩ cm.

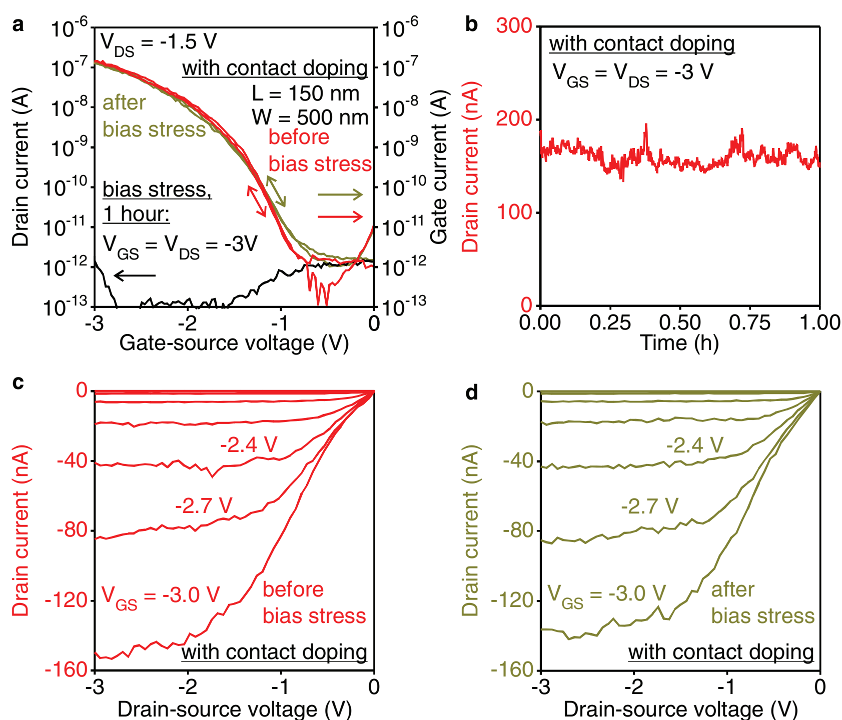

Figure 4. Bias-stress measurement on submicrometer TFTs (L = 150 nm) with contact doping. a) Transfer characteristics of a submicrometer TFT with contact doping before and after bias stress. During bias stress, a gate–source voltage of –3 V (corresponding to a transverse field of 5.2 MV cm^{-1}) and a drain–source voltage of –3 V (corresponding to a lateral field of 0.2 MV cm^{-1}) were continuously applied for 1 h. The results indicate that the dopant molecules incorporated into the contact regions of the TFTs do not drift or diffuse into the transistor channel, as this would lead to an increase in the off-state drain current or a loss of the linearity in the output characteristics. b) Drain current during bias stress over time. c,d) Output characteristics of the same device before (c) and after (d) bias stress.

The observation that the contact resistance of the submicrometer TFTs is significantly larger than that of the long-channel TFTs is explained by the difference in gate overlap. Assuming that charge flow between the source/drain contacts and the channel occurs only in those areas where the gate and the source and drain contacts overlap, the contact length is identical to the gate overlap (L_C = ΔL). The current density across the contact/semiconductor interface is not constant, but has a maximum at the contact edge and decreases asymptotically in the direction away from the edge (see SI, Figure S8a). The transfer length (L_T) is defined as the contact length over which 63% of the charge flow between contact and semiconductor occurs.[29,30] TLM analysis indicates a transfer length of 11 µm for the DNTT TFTs without contact doping (see SI, Figure S7). Calculations and measurements show that when L_C is reduced below L_T, the contact resistance increases dramatically, due to the loss of area available for charge flow (see SI, Figure S8b). This explains why TFTs with $L_C << L_T$ (like our submicrometer TFTs) have larger contact resistance than TFTs with $L_C >> L_T$, (like our shadow-mask-patterned TFTs). It also shows that the choice of the gate overlap is a difficult trade-off between the requirement for a small contact resistance (which requires a large ΔL, so that ideally $L_C > L_T$) and the requirement for a small parasitic capacitance (which calls for the smallest manufacturable ΔL; see SI, Equation S4).

More importantly, the TLM data show that contact doping significantly reduces the transfer length (from 11 to 5 µm; see SI, Figure S7). Contact doping is therefore a powerful tool to break the above-mentioned compromise and allow the simultaneous reduction of contact resistance and overlap capacitance (compare SI, Figure S8b,c). Again, this demonstrates the enormous potential of contact doping for submicrometer TFTs with patterned gate electrodes in high-frequency electronic applications.

A major concern with area-selective doping in organic TFTs is the positional stability of the dopants. If the dopants were to drift or diffuse into the channel, the resulting channel doping would produce large off-state currents.[24,27,28] **Figure 4** shows results from a bias-stress measurement performed on a submicrometer TFT (channel length 150 nm) with contact doping. The TFT was stressed continuously for 1 h in air with the maximum possible gate–source voltage (V_{GS} = –3 V, corresponding to a vertical electric field of 5.2 MV cm^{-1}) and with the maximum possible drain–source voltage (V_{DS} = –3 V; corresponding to a lateral electric field of 0.2 MV cm^{-1}). The results indicate that bias stress does not lead to an increase of the off-state drain current nor to a loss of the linearity in the output characteristics, either one of which might be caused by dopants entering the transistor channel. These results confirm the positional stability of the organic dopant NDP-9 in the contact regions of the DNTT transistors.

In summary, we have successfully employed aggressive gate-dielectric scaling and area-selective contact doping in order to efficiently suppress short-channel effects in nanoscale organic thin-film transistors that have channel lengths

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and gate overlaps of about 100 nm. We have shown that small off-state drain currents (about 10^{-13} A) and large on/off current ratios (10^7) can be achieved in submicrometer organic TFTs, provided that the thickness of the gate dielectric is scaled along with the channel length. A record transconductance of 0.4 S m^{-1} has been obtained for a TFT with a channel length of 90 nm and a gate overlap of 200 nm. We have also shown that contact doping with a strong molecular dopant significantly reduces the transfer length of the TFTs and is thus a powerful tool to simultaneously reduce the contact resistance and the parasitic overlap capacitance in organic TFTs. Contact doping has been found to reduce the contact resistance from 0.66 kΩ cm to 0.39 kΩ cm.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author. Detailed information on the fabrication process of the transistors and additional experimental data are available.

Acknowledgements

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Supporting Information

Contact Doping and Ultrathin Gate Dielectrics for Nanoscale Organic Thin-Film Transistors

**Frederik Ante, Daniel Kälblein, Ute Zschieschang,
Tobias W. Canzler, Ansgar Werner, Kazuo Takimiya, Masaaki Ikeda,
Tsuyoshi Sekitani, Takao Someya, Hagen Klauk**

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1. Maximum frequency of a field-effect transistor

The maximum frequency at which a field-effect transistor can switch or amplify electrical signals (f_T) is determined by the transconductance (g_m) and the gate capacitance (C_{gate}) of the transistor [ref. S1]:

$$f_T = \frac{g_m}{2\pi C_{gate}} \tag{S1}$$

If the transistor is operated in the **saturation regime** (i.e., when $V_{DS} \geq V_{GS}-V_{th} \geq 0$), the transconductance is given by:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\mu W C_{diel}}{L}\left(V_{GS} - V_{th}\right) \tag{S2}$$

where I_D is the drain current, V_{GS} is the gate-source voltage, μ is the charge-carrier field-effect mobility, W is the channel width, C_{diel} is the gate dielectric capacitance per unit area, L is the channel length, and V_{th} is the threshold voltage.

If the transistor is operated in the **linear regime** (i.e., when $V_{GS}-V_{th} \geq V_{DS} \geq 0$), the transconductance is given by:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\mu W C_{diel}}{L} V_{DS} \tag{S3}$$

where V_{DS} is the drain-source voltage.

Neglecting the Miller effect [ref. S1], the gate capacitance is approximately given by:

$$C_{gate} \approx C_{diel}\, W\left(L + 2 \cdot \Delta L\right) \tag{S4}$$

where ΔL is the gate overlap (i.e., the length by which the gate electrode overlaps the source contact and the drain contact; see Figure S1).

Thus, the maximum frequency at which a field-effect transistor can be operated is approximately:

$$f_T \approx \frac{\mu V}{2\pi L\left(L + 2 \cdot \Delta L\right)} \tag{S5}$$

where $V = V_{GS}-V_{th}$ if the transistor operates in the saturation regime or $V = V_{DS}$ if the transistor operates in the linear regime.

For example, operating a transistor that has a channel length L = 2 µm and a gate overlap ΔL = 2 µm with a voltage of 3 V at a frequency of 13.56 MHz (at which radio-frequency identification systems typically operate) would require a field-effect mobility of 3.4 cm^2/Vs. Such large mobilities are indeed possible in organic TFTs [ref. S2-S5], but only if the TFTs have a relatively large channel length ($L \geq 50$ µm). When the channel length is large, the contribution of the contact resistance to the total device resistance is negligible, so the mobility calculated from the current-voltage characteristics of the transistor (the "extrinsic" mobility) is close to the intrinsic mobility (which can indeed be >3 cm^2/Vs in well-ordered organic semiconductor films). However, when the channel length is reduced, the channel resistance decreases ($R_{channel} \sim L$), while the contact resistance remains constant, so the relative contribution of the contact resistance increases and the extrinsic mobility decreases (see

Figure 7 and Figure 13b in ref. [S6]). Therefore, extrinsic mobilities >3 cm^2/Vs are currently not realistic for organic TFTs with $L \leq 2$ µm.

On the other hand, if $L = \Delta L = 200$ nm, a much more realistic extrinsic mobility of 0.04 cm^2/Vs is sufficient for a frequency of 13.56 MHz at 3 V. Therefore, reducing the lateral transistor dimensions into the nanoscale regime is a promising approach for the realization of organic TFTs with operating frequencies >10 MHz.

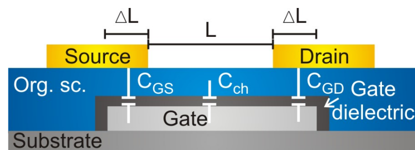

Figure S1: Schematic cross-section of a top-contact organic thin-film transistor.
The schematic indicates the individual parasitic capacitances forming the total gate capacitance C_{gate}. In detail, the image depicts the gate-to-source capacitance (C_{GS}) and the gate-to-drain capacitance (C_{GD}), as well as the channel capacitance $C_{channel}$.

2. Fabrication of submicron TFTs with patterned gate electrodes

Photolithography and electron-beam lithography are processes that require organic solvents and elevated temperatures for resist processing. Since high-mobility small-molecule conjugated semiconductors often undergo phase transitions when exposed to solvents or heat [ref. 35,36], photolithography and electron-beam lithography are in general not suitable to pattern source and drain contacts on top of vacuum-deposited thin films of such semiconductors. Therefore, top-contact small-molecule TFTs are typically fabricated using shadow-masks, which have a resolution that is usually limited to about 10 µm [ref. 34]. To fabricate top-contact small-molecule TFTs with submicron channel length, the RIKEN group recently reported an electron-beam lithography process in which a suspended resist bridge that serves as a high-resolution shadow mask for the top contacts is created prior to the deposition of the organic semiconductor. Using a heavily doped silicon wafer as a global (unpatterned) back gate and a thin layer of thermally grown silicon dioxide as a gate dielectric, the RIKEN group fabricated top-contact pentacene TFTs with a channel length as small as 150 nm [ref. 15,23-25].

We have further developed the RIKEN process to realize small-molecule organic TFTs with a channel length of less than 100 nm on local (patterned) metal gate electrodes using an ultrathin gate dielectric that can be processed at temperatures below 100 °C (to provide compatibility with flexible polymeric substrates).

As a substrate we have employed a silicon wafer covered with a 100 nm thick layer of thermally grown silicon dioxide. The silicon and the silicon dioxide are not part of the final devices, and in principle the TFTs could also be made on glass or plastic substrates. Areas for the local metal gate electrodes are defined on the SiO_2 surface by electron-beam lithography, and 30 nm thick aluminum is deposited by thermal evaporation. The aluminum surface is then exposed to an oxygen plasma to increase the thickness of the native aluminum oxide layer and the density of hydroxyl groups on the aluminum oxide surface. A large density of hydroxyl groups is beneficial for the formation of a dense self-assembled monolayer (SAM), which is prepared in the next step by immersing the substrate into a 2-propanol solution of n-octadecylphosphonic acid. The AlO_x layer (3.6 nm thick) and the SAM (2.1 nm thick) form a hybrid gate dielectric with a total thickness of 5.7 nm. The AlO_x/SAM gate dielectric has a capacitance per unit area (C_{diel}) of 700 nF/cm^2, which allows the TFTs to operate with gate-source voltages of about 3 V. Despite the small dielectric thickness, the gate leakage is relatively small ($< 10^5$ A/cm^2 at 3 V). During the oxygen-plasma treatment and the SAM formation, the areas outside the aluminum gate electrodes remain covered by electron-beam resist, so that the hydrophobic SAM is formed only on the gate electrodes, while the rest of the substrate is left hydrophilic. The latter is useful, since a hydrophobic substrate would be more difficult to coat with resist for the following electron-beam lithography process step. After formation of the AlO_x/SAM gate dielectric, the electron-beam resist is stripped in order to remove the aluminum outside of the gate areas. We have conducted several tests to confirm that the lift-off process does not harm the Al/AlO_x/SAM structure [ref. S7].

To fabricate the suspended resist bridge the substrate is then coated with three layers of electron-beam resist: The first (bottom) layer is a 400 nm thick PMMA/MMA copolymer layer with high electron-beam sensitivity (dose to clear: 25 µC/cm^2), the second (middle) layer is a 120 nm thick PMMA 200K layer, and the third (top) layer is a 140 nm thick PMMA 950K layer with low electron-beam sensitivity (dose to clear: 100 µC/cm^2). If the source/drain spacing is less than about 500 nm, the dose of electrons back-scattered from the substrate surface during the electron-beam process is sufficient to expose the high-sensitivity bottom layer in the (nominally unexposed) regions between the source/drain contacts, while the low-sensitivity middle and top layers are not affected by the back-scattered electrons. As a result, a suspended resist bridge is formed across the channel region of the transistors during development of the resist stack (i.e., the bottom layer is dissolved, while the middle and top layers remain).

In the next step, the organic semiconductor, dinaphtho-[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT), is deposited. In order to form a continuous layer underneath the suspended resist bridge, the substrate is tilted at angles of 45° and 135° while the organic semiconductor is deposited by sublimation in vacuum. During the semiconductor deposition, the substrate is held at a temperature of 60 °C, since this has been found to provide the optimum thin-film morphology and field-effect mobility. The total thickness of the semiconductor film is 20 nm (10 nm deposited at an angle of 45°, plus 10 nm deposited at an angle of 135°, without breaking vacuum).

Finally, the source and drain contacts are deposited with the substrate held at an angle of 90º and with the suspended resist bridge serving as a high-resolution "shadow mask" to define the channel length of the transistors. For the TFTs without contact doping, 30 nm of gold are deposited by thermal evaporation in vacuum. For the TFTs with contact doping, a thin layer of the organic dopant NDP-9 (Novaled, Dresden, Germany) followed by 30 nm of gold are deposited (without breaking vacuum). Figure S2 indicates that depositing a 1 nm thick NDP-9 layer on DNTT leads to isolated clusters that coalesce into a continuous layer when more than 1 nm NDP-9 is deposited.

During the deposition of the gold contacts, it is critically important that the deposited gold layer breaks across the edges of the resist patterns, so that the gold that remains on the electron-beam resist outside the active TFT area is disconnected from the contact pads (source, drain and gate). To confirm this, we carefully measure the electrical resistance between the various probe pads and the gold layer on the resist. This resistance is usually greater than 10^{12} Ω.

The width of the semiconducting layer and the width of the source and drain contacts are identical, since both are defined by the same resist pattern (Figure 1a). Therefore, the channel width of the TFTs is precisely defined and the possibility of fringe currents flowing between source and drain outside of the contact width are effectively eliminated.

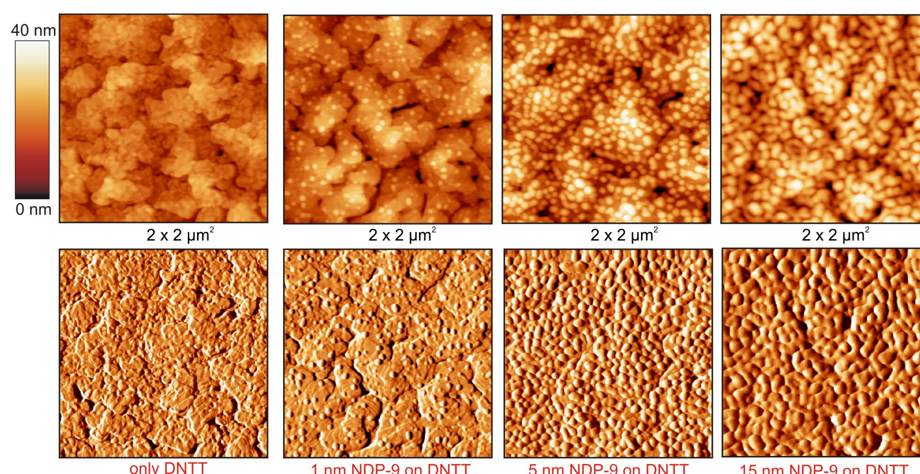

Figure S2: Atomic force microscope (AFM) images of 20 nm thick films of the organic semiconductor DNTT (deposited on 30 nm Al + 3.6 nm AlO_x + 2.1 nm SAM) without dopant and with three different amounts of the organic dopant NDP-9 deposited on top of the DNTT film.
Top row: height images; bottom row: amplitude images.
The AFM images show that a nominally 1 nm thick layer of the dopant NDP-9 (as utilized in the TFTs shown in Figures 3 and 4) forms isolated clusters when deposited on DNTT. When the nominal thickness of the deposited NDP-9 is increased, the clusters eventually begin to coalesce into a continuous film.

3. Electrical properties of the organic dopant NDP-9

After demonstrating that doping the contact regions and the channel region of a DNTT TFT with NDP-9 greatly increases the off-state drain current (as seen in Figure 3b), it was necessary to rule out that the observed increase in off-state drain current is due to charge flow through the dopant NDP-9, rather than through the semiconductor DNTT. Therefore, devices with a 30 nm thick film of NDP-9 instead of DNTT were fabricated and the current-voltage characteristics were measured. Figure S3 shows that the current through the 30 nm thick NDP-9 film is below the leakage level, indicating that there is essentially no charge flow through the NDP-9 in this device, which confirms that charge flow in the DNTT TFTs with contact and channel doping occurs only through the DNTT and not through the NDP-9.

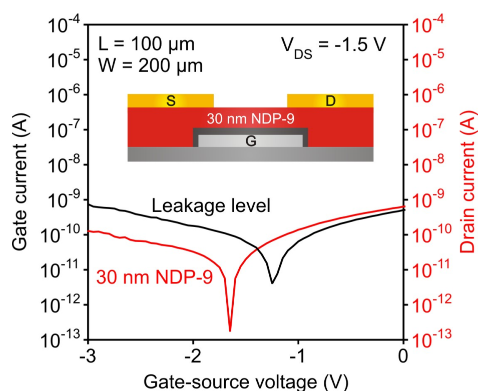

Figure S3: Current-voltage characteristics of a device that uses only a 30 nm thick film of NDP-9 instead of the semiconductor DNTT.
The current through the NDP-9 film is indeed negligible, confirming that there is essentially no charge flow through the NDP-9.

4. Comparison between the organic dopants F_4-TCNQ and NDP-9

An organic dopant that has been previously employed for contact doping in organic TFTs is 2,3,5,6-tetrafluoro-7,7,8,8-tetracyanoquinodimethane (F_4-TCNQ) [ref. 26,27]. We have carried out several measurements to compare the doping strength of NDP-9 and F_4-TCNQ:

- The sheet resistance of a 30 nm thick DNTT film doped with NDP-9 (nominally 1 nm thick) is a factor of 7 smaller than the sheet resistance of a 30 nm thick DNTT film doped with F_4-TCNQ (also nominally 1 nm thick; Figure S4a).
- The electrical conductivity of thin amorphous films of the popular hole-transport materials N,N'-diphenyl-N,N'-bis(1-naphthyl)-(1,1'-biphenyl)-4,4'-diamine/tris-(8-hydroxyquinoline) (**NPB**) and 2,2',7,7'-tetrakis(N,N'-di-p-methylphenylamino)-9,9'-spirobifluorene (**spiro-TTB**) increases more strongly when the films are doped with NDP-9, compared with F_4-TCNQ (Figure S4b).
- The contact resistance of long-channel TFTs doped with NDP-9 is about 10% smaller than the contact resistance of long-channel TFTs doped with F_4-TCNQ (Figure S4c).
- Cyclic voltammetry measurements indicate that NDP-9 is more electronegative by about 0.1 eV than F_4-TCNQ (Figure S4d).

These measurements suggest that NDP-9 is a more suitable dopant for DNTT than F_4-TCNQ.

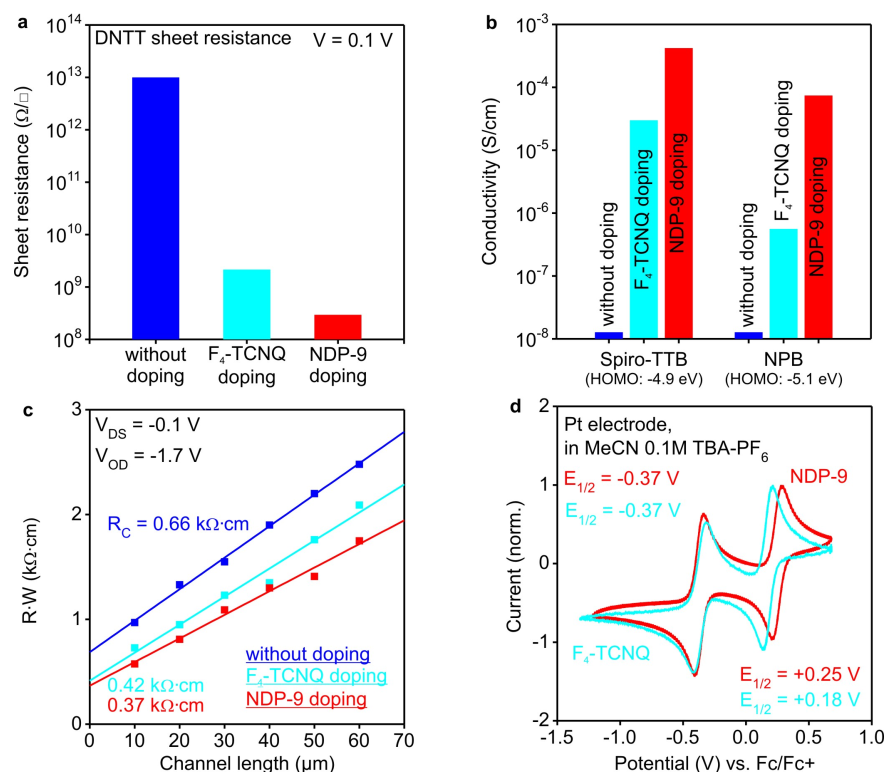

Figure S4: Comparison of the doping strength of the organic dopants NDP-9 and F_4-TCNQ.

a) Effect of doping with F_4-TCNQ and NDP-9 on the sheet resistance of 30 nm thick films of the organic semiconductor DNTT. The DNTT films are polycrystalline. The dopant was vacuum-evaporated as a nominally 1 nm thick layer onto the surface of the DNTT films.

b) Effect of doping with F_4-TCNQ and NDP-9 on the electrical conductivity of NPB and spiro-TTB. The films are amorphous and were prepared by vacuum co-evaporation of the host (NPB or spiro-TTB) and the dopant (10 mol% of F_4-TCNQ or 10 mol% of NDP-9). The energy of the highest occupied molecular orbital (HOMO) of NPB is -5.1 eV, and the HOMO energy of spiro-TTB is -4.9 eV.

c) Effect of doping with F_4-TCNQ and NDP-9 on the contact resistance of DNTT TFTs with contact and channel doping. A nominally 1 nm thick layer of the dopant (F_4-TCNQ or NDP-9) was deposited on top of the DNTT layer in the contact regions and in the channel region of shadow-mask-patterned long-channel TFTs.

d) Cyclic voltammetry measurements on the organic dopant molecules NDP-9 and F_4-TCNQ.

5. Statistical analysis of submicron TFTs without contact doping

Figure S5a shows the distribution of the transconductance per channel width of 27 submicron TFTs without contact doping measured on three substrates. All TFTs have a channel length of 150 nm, a gate overlap of 200 nm, and a channel width of 500 nm. The mean value of the transconductance per channel width is 0.25 S/m. As can be seen, the deviation of the measured values from the mean value is quite large.

Figure S5b shows the transconductance per channel width of 40 submicron TFTs without contact doping measured on four substrates as a function of channel length (90 nm, 150 nm or 300 nm). The TFTs have a gate overlap of 200 nm and a channel width of 500 nm. Again, the variation of the measured values is substantial. As a result, the theoretically predicted relationship between transconductance and channel length ($g_m \sim 1/L$) is not observed, so that an analysis of the data using the transmission line method (TLM) is not possible. Due to the extremely small channel length of these TFTs, the most important parameter limiting the transconductance is the contact resistance, so it is reasonable to assume that the large variation in transconductance is caused by variations in contact resistance. In contrast to long-channel TFTs, where the contribution of the contacts to the device characteristics is small or negligible, the characteristics of nanoscale TFTs are heavily dependent on the efficiency of the contacts. Indeed, scanning photocurrent microscopy experiments on pentacene TFTs have shown that the efficiency of the charge transfer at the contacts can vary significantly, not only from one device to the next, but even along the contact edge within the same device [ref. S8, S9].

To estimate an upper limit of the contact resistance of the submicron TFTs, we have measured the total resistance of a large number of transistors with identical channel length (L = 150 nm) and then calculated the mean value of the total resistance. The total resistance of a field-effect transistor is the sum of the contact resistance and the channel resistance. For submicron TFTs, the contribution of the channel resistance to the total resistance is very small, so that the contact resistance is expected to be only slightly smaller than the total resistance. To obtain the total resistance of each TFT, we have measured the drain current (I_D) at a gate-source voltage (V_{GS}) of -3 V and a drain-source voltage (V_{DS}) of -0.1 V and then used the following equation to obtain the total device resistance (R) normalized to the channel width (W):

$$R\,W = \frac{V_{DS}}{I_D}\,W \qquad \text{(S6)}$$

In Figure S5c the distribution of the total resistance of 19 submicron TFTs without contact doping and 15 submicron TFTs with contact doping is shown. The TFTs have a channel length of 150 nm, a gate overlap of 200 nm, and a channel width of 500 nm. The mean value of the total resistance is 9.8 kΩ·cm for the submicron TFTs without contact doping and 2.7 kΩ·cm for the submicron TFTs with contact doping, which confirms the beneficial effect of the contact doping. Since the contribution of the channel resistance to the total resistance is small for such short channel length, the contact resistance is expected to be only slightly smaller than the calculated total resistance.

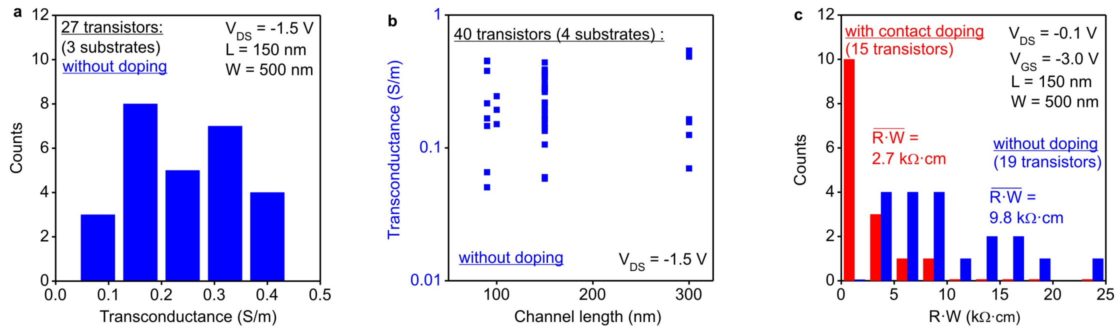

Figure S5: Statistical analysis of submicron TFTs.

a) Distribution of the transconductance ($g_m = \partial I_D/\partial V_{GS}$) per channel width of 27 submicron TFTs without contact doping. The TFTs have a channel length of 150 nm, a gate overlap of 200 nm, and a channel width of 500 nm. The mean value of the transconductance per channel width is 0.25 S/m.

b) Transconductance per channel width of 40 submicron TFTs without contact doping plotted versus the channel length (100 nm, 150 nm or 300 nm). The TFTs have a gate overlap of 200 nm and a channel width of 500 nm. Theory predicts an inversely proportional relationship ($g_m \sim 1/L$), but due to the significant device-to-device variations this relationship is not observed in the submicron TFTs.

c) Distribution of the total resistance of 19 TFTs without contact doping (blue) and 15 TFTs with contact doping (red), normalized to the channel width. The TFTs have a channel length of 150 nm, a gate overlap of 200 nm, and a channel width of 500 nm. The beneficial effect of the contact doping is clearly seen: The average value of the total resistance decreases from 9.8 kΩ·cm to 2.7 kΩ·cm upon contact doping.

6. Fabrication of long-channel TFTs

Since the transfer line method cannot be applied to our submicron TFTs, due to the device-to-device variations, we also fabricated long-channel TFTs with channel length (L) ranging from 10 to 60 µm. Unlike the submicron TFTs, which were fabricated by electron-beam lithography, the long-channel TFTs were fabricated using macroscopic shadow masks [ref. 34]. The gate electrode is a 30 nm thick layer of aluminum deposited by thermal evaporation and patterned with a shadow mask. The gate dielectric is again a combination of a 3.6 nm thick AlO_x layer (created by exposing the Al surface to an oxygen plasma) and a 2.1 nm thick monolayer of n-octadecylphosphonic acid. The semiconductor is again a 30 nm thick layer of DNTT deposited by sublimation in vacuum at a substrate temperature of 60 °C. Finally, the source and drain contacts are deposited and patterned using a shadow mask. For the TFTs without contact doping, 25 nm of gold are deposited by thermal evaporation in vacuum through the shadow mask. For the TFTs with contact doping, a thin layer of the organic dopant NDP-9 followed by 25 nm of gold are deposited (without breaking vacuum and using the same shadow mask for patterning). The shadow-mask-patterned TFTs have a channel width (W) of 200 µm and a gate overlap (ΔL) of 5 µm, 20 µm or 200 µm.

Figures S6a and S6b show the current-voltage characteristics of a long-channel TFT with a channel length of 60 µm. The extrinsic field-effect mobility extracted from these characteristics is 2.2 cm^2/Vs.

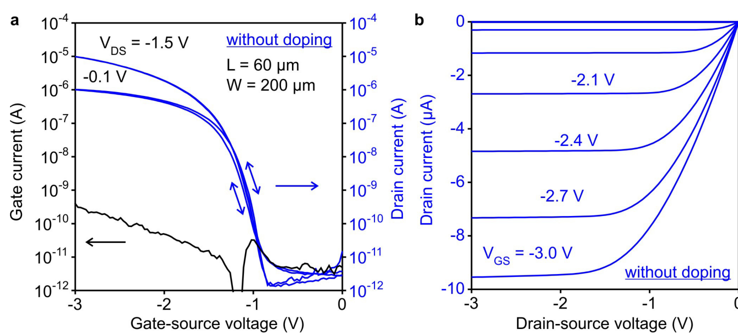

Figure S6: Long-channel TFTs (10 µm ≤ L ≤ 60 µm) and transmission line method.

a) Transfer characteristics of a long-channel TFT with a channel length of 60 µm, a gate overlap of 200 µm, and a channel width of 200 µm. The extrinsic field-effect mobility is 2.2 cm^2/Vs.

b) Output characteristics of the same TFT.

7. Transmission line method (TLM)

For the transmission line method it is assumed that the total resistance (R) of a field-effect transistor is a series connection of the source resistance (R_{source}), the channel resistance ($R_{channel}$), and the drain resistance (R_{drain}):

$$R = R_{source} + R_{channel} + R_{drain} \tag{S7}$$

Since the transmission line method does not distinguish between source and drain resistance, the contact resistance (R_C) is defined as the sum of R_{source} and R_{drain} (which are usually not the same [ref. S10]):

$$R = R_C + R_{channel} \tag{S8}$$

Both, the contact resistance and the channel resistance are inversely proportional to the channel width (W), so that the following normalization is useful:

$$R \cdot W = R_C \cdot W + R_{channel} \cdot W \tag{S9}$$

Unlike the contact resistance, the channel resistance is proportional to the channel length of the transistor (L):

$$R_{channel} \cdot W = R_{sheet} \cdot L \tag{S10}$$

where R_{sheet} is the sheet resistance of the semiconductor layer in the channel region. (Note that the normalization to the channel width is already included in the channel sheet resistance R_{sheet}.) Thus, the following relation between the total resistance, the contact resistance, the channel sheet resistance (which is assumed to be the same for all TFTs), and the channel length is obtained:

$$R \cdot W = R_C \cdot W + R_{sheet} \cdot L \tag{S11}$$

To extract the contact resistance using the transmission line method, we have utilized long-channel TFTs with channel length ranging from 10 to 60 µm. For each TFT, the drain current (I_D) was measured at a fixed overdrive voltage ($V_{GS} - V_{th}$ = -1.7 V) and a fixed drain-source voltage (V_{DS} = -0.1 V), and the total resistance (R) was calculated and normalized to the channel width (W):

$$R \cdot W = \frac{V_{DS}}{I_D} W \tag{S12}$$

The total resistance (R·W) of each TFT was then plotted over the channel length (L), as shown in Figure S7. From this plot, the contact resistance ($R_C \cdot W$) can be extracted by extrapolating the total resistance to the channel length at which the channel resistance disappears:

$$R_C \cdot W = R \cdot W(L = 0) \tag{S13}$$

The contact resistance we have extracted with this method for the long-channel TFTs is 0.66 kΩ·cm without contact doping and 0.39 kΩ·cm with contact doping (gate overlap ΔL = 200 µm). Again, this confirms the beneficial effect of the contact doping in reducing the contact resistance.

The relationship between the total resistance, the channel sheet resistance, and the channel length can also be written in the following way:

$$R \cdot W = R_{sheet} (L + 2 \cdot L_T) \qquad (S14)$$

where L_T is the transfer length. From the R·W *vs.* L plot, the transfer length can be extracted by extrapolating the channel length to a total resistance of zero (R·W = 0):

$$L_T = -\frac{L(R \cdot W = 0)}{2} \qquad (S15)$$

The transfer length we have extracted with this method is 11 µm for the TFTs without contact doping and 5 µm for the TFTs with contact doping.

Note: For this analysis we have assumed that the transmission line method can be applied to transistors with contact doping. We note, however, that TLM can in principle only be applied when the sheet resistance is constant along the device [ref. 29], which is not the case in TFTs with contact doping. Therefore, the TLM results from the TFTs with contact doping have to be taken with caution and serve here only as a rough guidance with an uncertainty of 12% [ref. 29].

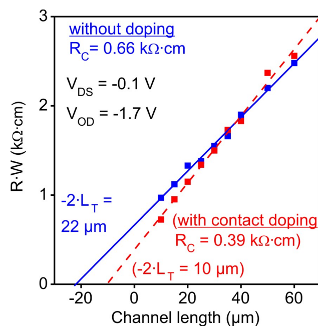

Figure S7: Long-channel TFTs (10 µm ≤ L ≤ 60 µm) and transmission line method. Transmission line method (TLM) analysis of 18 long-channel TFTs with a global (unpatterned) gate electrode (10 µm ≤ L ≤ 60 µm; ΔL = 200 µm). Again, the beneficial effect of the contact doping is clearly seen: The contact resistance decreases from 0.66 kΩ·cm to 0.39 kΩ·cm upon contact doping. In addition to the contact resistance, TLM analysis also yields the transfer length L_T (i.e., the contact length over which 63% of the charge exchange between contact and semiconductor occurs); for the long-channel TFTs the transfer length is 11 µm without contact doping and 5 µm with contact doping.

8. Relationship between gate overlap, contact length, transfer length, and contact resistance

For the following analysis we assume that the flow of charge carriers between the source and drain contacts and the semiconducting channel occurs only in those areas where the gate electrode overlaps the contacts. In reality, charge exchange may also occur in areas outside of the overlap area, but we assume here that this would only be a very small fraction of the total charge and can thus be neglected. With this assumption, it follows that the contact length is identical to the gate overlap ($L_C = \Delta L$).

Figure S8a schematically illustrates the relationship between the gate overlap (ΔL), the contact length (L_C) and the transfer length (L_T). The current density across the contact/semiconductor interface is not constant along the contact length, but has a maximum at the contact edge and decreases asymptotically in the direction away from the contact edge. The transfer length is defined as the contact length over which 63% of the charge exchange between contact and semiconductor occurs [ref. 29,30]. A smaller transfer length means that a smaller contact length (i.e., a smaller contact area) is sufficient to exchange a certain amount of charges across the contact/semiconductor interface at a given voltage. In other words, a smaller transfer length (all else being equal) indicates a better contact.

The contact resistance depends on the ratio between the contact length (L_C) and the transfer length (L_T). If $L_C \ll L_T$, the area available for the exchange of charge carriers between the contact and the channel across the contact/semiconductor interface will be relatively small, and hence the contact resistance ($R_C \cdot W$) will be relatively large. This is the situation in our electron-beam-patterned submicron TFTs, which have a gate overlap of 200 nm (and hence a contact length of 200 nm), which is substantially smaller than the transfer length. In contrast, if $L_C \gg L_T$, the area available for the charge exchange between the contact and the semiconductor channel will be relatively large, and hence the contact resistance will be relatively small. This is the situation in our shadow-mask-patterned long-channel TFTs, which have a gate overlap of 200 µm (and hence a contact length of 200 µm), which is substantially larger than the transfer length. This explains why our submicron TFTs have a larger contact resistance (9.8 kΩ·cm without contact doping, 2.7 kΩ·cm with contact doping; please note that these values represent an upper limit estimated from the total device resistance, as explained in detail on page 5 of the Supporting Information) than our long-channel TFTs (0.66 kΩ·cm without contact doping, 0.39 kΩ·cm with contact doping).

With a number of assumptions and simplifications, the relationship between the contact length, the transfer length, and the contact resistance can be approximately described as follows [ref. 29,30]:

$$R_C \cdot W = 2 \cdot R_{sheet} \, L_T \coth \frac{L_C}{L_T} \qquad \text{(S16)}$$

Using the parameters $R_{sheet} = 330$ kΩ/sq and $L_T = 11$ µm, which we have extracted from the long-channel TFTs without contact doping using the transmission line method (Figure S7), we have plotted the relationship between the contact resistance ($R_C \cdot W$) and the contact length (L_C) for TFTs without contact doping, as shown in Figure S8b. The graph confirms that reducing the contact length below the transfer length leads to a dramatic increase of the contact resistance, which explains the difference in contact resistance between our submicron TFTs ($L = 0.2$ µm; patterned by electron-beam lithography) and our long-channel TFTs (5 µm $\leq L \leq$ 200 µm; patterned using shadow masks). This shows that the choice of the gate overlap ΔL is a trade-off between the requirement for a small contact resistance (which requires a large ΔL, so that ideally $L_C > L_T$) and the requirement for a small parasitic overlap capacitance (which requires a small ΔL; see Equation S4).

This is where the beneficial effect of contact doping comes into play. By doping the contacts, the R_C *vs.* L_T curve is shifted down and to the left, as can be seen by comparing Figure S8b and S8c. This

means that the same (small) contact resistance can be achieved with a smaller contact area and hence with a smaller parasitic capacitance, resulting in a higher maximum frequency.

In principle, the transmission line method can only be applied if the sheet resistance is constant along the entire length of the transistor [ref. 29]. In the TFTs without contact doping, this is indeed the case, so TLM can be safely applied to these devices. Contact doping, however, produces a substantial reduction of the sheet resistance in the regions underneath the source and drain contacts, but not in the channel region, so in the TFTs with contact doping the sheet resistance is not constant along the transistor. Therefore, TLM is strictly not applicable to these devices, so the values extracted for the contact resistance and the transfer length of the TFTs with contact doping should be taken with caution.

	without contact doping	**with contact doping**
contact resistance (R_C·W)	0.66 kΩ·cm	0.39 kΩ·cm
contact resistivity (ρ_C)	0.37 Ω·cm^2	0.10 Ω·cm^2
channel sheet resistance (R_{sheet})	330 kΩ/sq	370 kΩ/sq
transfer length (L_T)	11 µm	5 µm

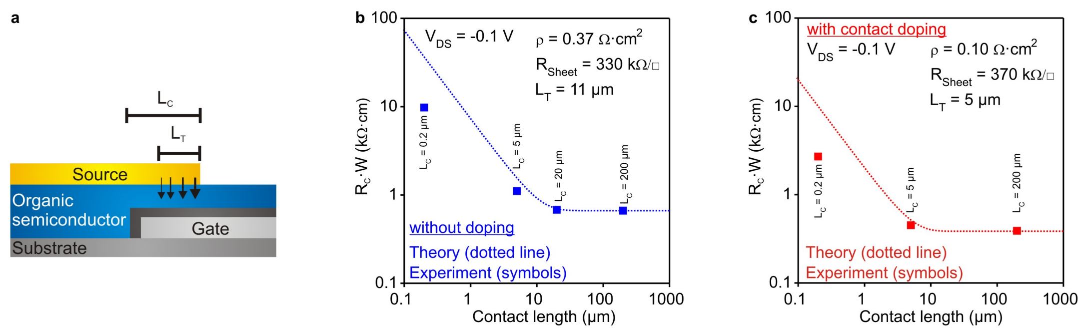

Figure S8: Relationship between gate overlap, contact length, transfer length, and contact resistance.

a) Schematic drawing showing that the current density across the contact/semiconductor interface is not constant over the contact length (L_C), but that the current density has a maximum near the contact edge and decreases asymptotically in the direction away from the contact edge. The transfer length (L_T) is the contact length over which 63% of the charge exchange occurs.

b) Theoretical relationship (black solid line) and measured relationship (blue symbols) between the contact resistance (R_C·W) and the contact length (L_C) for TFTs without doping. The theoretical curve was calculated using R_{sheet} = 330 kΩ/sq and L_T = 11 µm (extracted from Figure S7). The experimental data are from TFTs having contact lengths of 0.2 µm, 5 µm, 20 µm and 200 µm and contact resistances of 9.8 kΩ·cm, 1.1 kΩ·cm, 0.68 kΩ·cm and 0.66 kΩ·cm, respectively. The graph shows that reducing the contact length below the transfer length leads to a significant increase of the contact resistance, since the area available for charge exchange is dramatically reduced. This increase of the contact resistance with decreasing contact length explains why our submicron TFTs have a significantly larger contact resistance than our long-channel TFTs.

c) Theoretical relationship (black solid line) and measured relationship (red symbols) between the contact resistance (R_C·W) and the contact length (L_C) for TFTs with contact doping. The theoretical curve was calculated using R_{sheet} = 370 kΩ/sq and L_T = 5 µm (extracted from Figure S7). The experimental data are from TFTs having contact lengths of 0.2 µm, 5 µm and 200 µm and contact resistances of 2.7 kΩ·cm, 0.45 kΩ·cm and 0.39 kΩ·cm, respectively. Comparing Figures S8b and S8c shows that contact doping makes it possible to simultaneously achieve a small contact resistance and a small parasitic overlap area, and hence a higher maximum frequency.

9. Suppression of short-channel effects

In field-effect transistors in which the ratio between the channel length and the gate dielectric thickness is large (>20), the off-state drain current, the threshold voltage, and the subthreshold slope are independent of the drain-source voltage [ref. 9]. This is the ideal long-channel behavior and can be seen, for example, in the transfer characteristics of the shadow-mask-patterned long-channel TFTs in Figure S6a. When the channel length is reduced without scaling the gate dielectric thickness, the influence of the lateral electric field on the electric potential along the transistor channel increases. As a result, the off-state drain current, the threshold voltage, and the subthreshold slope of the transistor are now influenced by the applied drain-source voltage (see, for example, Figure 9c in [ref. 9]) and the threshold voltage becomes a function of the channel length (see, for example, Figure 10 in [ref. 9]).

On the other hand, if the thickness of the gate dielectric is scaled along with the channel length, so that the ratio between the channel length and the gate dielectric thickness remains large, the ideal long-channel behavior can be preserved in transistors with small channel length. Figure S9a and S9b show the transfer characteristics of submicron TFTs with a channel length of 150 nm. Despite the very small channel length, the ratio between the channel length and the thickness of the gate dielectric is relatively large (~26), owing to the small thickness of the AlO_x/SAM gate dielectric (5.7 nm thick). As a result, the off-state drain current, the threshold voltage, and the subthreshold slope are independent of the drain-source voltage. In addition, the threshold voltage is essentially independent of the channel length (Figure S9c).

The beneficial effect of the contact doping can also be seen: The TFT with contact doping has a significantly larger drain current in the linear regime ($V_{DS} = -0.1$ V, $-3\text{ V} \leq V_{GS} \leq -2$ V) compared with the TFT without doping.

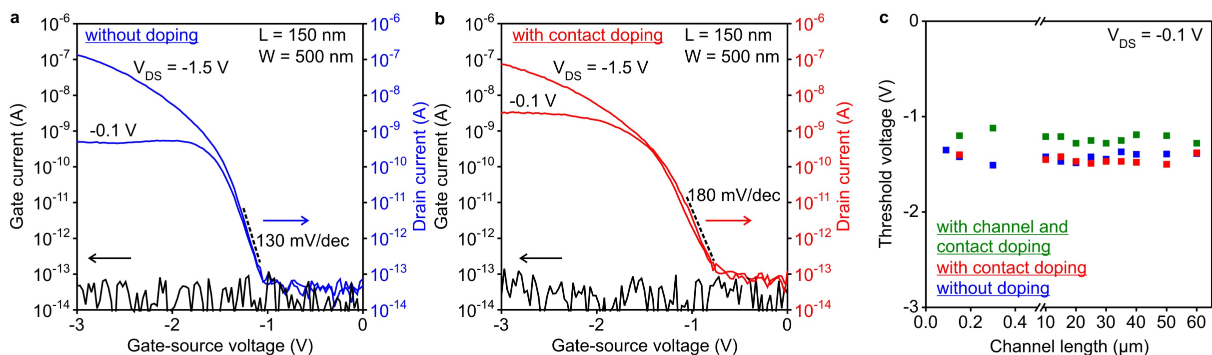

Figure S9: Drain-voltage invariance of the subthreshold behavior and channel-length invariance of the threshold voltage of organic TFTs with ultrathin gate dielectrics.

a) Transfer characteristics of a submicron TFT without doping for two different drain-source voltages ($V_{DS} = -0.1$ V and $V_{DS} = -1.5$ V).
b) Transfer characteristics of a submicron TFT with contact doping for the same drain-source voltages ($V_{DS} = -0.1$ V and $V_{DS} = -1.5$ V). Both TFTs have a channel length of 150 nm, a gate overlap of 200 nm, and a channel width of 500 nm.
c) Threshold voltage extracted from the transfer characteristics of long-channel and submicron TFTs with and without doping plotted versus the channel length. Owing to the small thickness of the AlO_x/SAM gate dielectric (5.7 nm), the threshold voltage is essentially independent of the channel length.

10. Trade-off between the air stability of the organic semiconductor and the contact resistance

In general, the air stability of conjugated organic semiconductors is directly linked to their ionization potential (HOMO energy): A larger ionization potential (lower-lying HOMO level) means that the molecules are less readily oxidized and hence provide better air stability. A popular strategy to increase the air stability of organic transistors is therefore the use of organic semiconductors with larger HOMO energy [ref. 32]. For example, the air stability of DNTT is substantially better than that of pentacene, due to the larger HOMO energy [ref. 34].

Ideally, the work function of the metal employed for the source and drain contacts should match the HOMO energy of the organic semiconductor, since matching energy levels are expected to provide the smallest energy barrier for the charge flow between the contacts and the semiconductor. In reality, however, it is difficult to find a contact material with a work function larger than that of gold, i.e., larger than about 5 eV. (Platinum has a work function of 5.6 eV, but platinum is difficult to deposit by thermal evaporation. Platinum can be deposited by electron-beam evaporation or by RF sputtering, but these methods usually damage the organic semiconductor layer by radiation exposure.)

This creates a difficult compromise between the air stability and the contact resistance of organic TFTs. However, this compromise can be alleviated by area-selective contact doping as shown in this work, because contact doping reduces the contact resistance even in the presence of a large energy barrier between the contacts and the semiconductor.

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