Microcontact-Printed Self-Assembled Monolayers as Ultrathin Gate Dielectrics in Organic Thin-Film Transistors and Complementary Circuits

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Received December 6, 2007. In Final Form: January 2, 2008

We have developed a manufacturing process for organic thin-film transistors and organic complementary circuits in which a microcontact-printed phosphonic acid self-assembled monolayer is employed first as an etch resist to pattern aluminum gate electrodes by wet etching and then as the gate dielectric of the same device. To our knowledge, this is the first report of a printing process for electronic devices that combines the concepts of direct and indirect printing in the same printing step and for the same material by employing a transferred pattern both as an etch resist (indirect printing) and as a functional material as part of the final device (direct printing). Owing to the small thickness and the high quality of the monolayer gate dielectric, the transistors and circuits operate at a low voltage of 3 V.

Introduction

Among the benefits of organic electronics is the fact that the manufacturing of organic devices may be accomplished partially or entirely by printing.[1] For example, a variety of printing techniques have been employed to define the components of organic thin-film transistors (TFTs) (i.e., the gate electrodes, the gate dielectric, the organic semiconductor, and the source/drain contacts).[2−15] In general, printing entails the controlled transfer of a specific material (ink) to the surface of a substrate. The material being transferred can be either a functional material, such as a semiconductor, or a resist intended to serve as a mask during a patterning step.

If the material being transferred is a functional material that constitutes a specific component of the final device, then the method is often called direct printing. Examples are screen-printed or inkjet-printed polymer dielectrics,[3,4,14] contacts based on inkjet-printed conducting polymers[5,13] or metal nanoparticles,[14] and organic semiconductors prepared by thermal transfer,[8] inkjet,[10] or vapor jet printing.[11] Another example is the transfer of patterned metal contacts from an elastomeric conformal relief stamp to the substrate surface.[7]

In contrast, if the printed material serves as a resist for a patterning step such that the transferred material itself is not part of the final device, then the technique may be considered to be indirect. An example is digital lithography,[10] where in the first step the functional material is deposited over the entire substrate, in the second step a resist pattern is created by printing, in the third step the functional material in areas not protected by resist is etched away, and in the final step the resist is stripped. Other examples for indirect printing involve microcontact printing (i.e., the transfer of a patterned organic self-assembled monolayer (SAM) from an elastomeric conformal relief stamp to the substrate surface). The printed SAM pattern then either serves as a resist during a subtractive wet etch process[6] or facilitates an additive patterning process by creating a contrast between hydrophobic and hydrophilic regions on the surface.[9,16] In neither of these cases does the printed SAM serve as a functional material of the final device.

Here we demonstrate a manufacturing process in which a microcontact-printed SAM pattern is employed first as an etch resist to define the metal gate electrode of an organic TFT and then as the gate dielectric of the same device. To our knowledge, this is the first report of a printing process that combines the concepts of direct and indirect printing in the same printing step and for the same material by employing a transferred SAM pattern both as a resist and as a functional material as part of the final device. Whereas SAMs prepared by immersing the substrate in solution are commonly employed in organic transistors to adjust the surface energy of the gate dielectric,[17] to our knowledge this is the first time that a printed SAM serves as a functional layer in a completed electronic device.

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(1) (a) Gamota, D. R., Brazis, P., Kalyanasundaram, K., Zhang, J., Eds.; *Printed Organic and Molecular Electronics*; Kluwer Academic Publishers: Boston, 2004. (b) Klauk, H., Ed.; *Organic Electronics: Materials, Manufacturing and Applications*; Wiley-VCH: Weinheim, Germany, 2006.

(2) Garnier, F.; Hajlaoui, R.; Yassar, A.; Srivastava, P. *Science* **1994**, *265*, 1684.

(3) Bao, Z.; Feng, Y.; Dodabalapur, A.; Raju, V. R.; Lovinger, A. J. *Chem. Mater.* **1997**, *9*, 1299.

(4) Rogers, J. A.; Bao, Z.; Raju, V. R. *Appl. Phys. Lett.* **1998**, *72*, 2716.

(5) Sirringhaus, H.; Kawase, T.; Friend, R. H.; Shimoda, T.; Inbasekaran, M.; Wu, W.; Woo, E. P. *Science* **2000**, *290*, 2123.

(6) Rogers, J. A.; Bao, Z.; Baldwin, K.; Dodabalapur, A.; Crone, B.; Raju, V. R.; Kuck, V.; Katz, H.; Amundson, K.; Ewing, J.; Drzaic, P. *Proc. Natl. Acad. Sci. U.S.A.* **2001**, *98*, 4835.

(7) (a) Loo, Y. L.; Willett, R. L.; Baldwin, K. W.; Rogers, J. A. *Appl. Phys. Lett.* **2002**, *81*, 562. (b) Kim, C.; Shtein, M.; Forrest, S. R. *Appl. Phys. Lett.* **2002**, *80*, 4051.

(8) Blanchet, G. B.; Loo, Y. L.; Rogers, J. A.; Gao, F.; Fincher, C. R. *Appl. Phys. Lett.* **2003**, *82*, 463.

(9) Zschieschang, U.; Klauk, H.; Halik, M.; Schmid, G.; Dehm, C. *Adv. Mater.* **2003**, *15*, 1147.

(10) Arias, A. C.; Ready, S. E.; Lujan, R.; Wong, W. S.; Paul, K. E.; Salleo, A.; Chabinyc, M. L.; Apte, R.; Street, R. A.; Wu, Y.; Liu, P.; Ong, B. *Appl. Phys. Lett.* **2004**, *85*, 3304.

(11) Shtein, M.; Peumans, P.; Benziger, J. B.; Forrest, S. R. *Adv. Mater.* **2004**, *16*, 1615.

(12) Knobloch, A.; Manuelli, A.; Bernds, A.; Clemens, W. *J. Appl. Phys.* **2004**, *96*, 2286.

(13) (a) Wang, J. Z.; Zheng, Z. H.; Li, H. W.; Huck, W. T. S.; Sirringhaus, H. *Nat. Mater.* **2004**, *3*, 171. (b) Sele, C. W.; von Werne, T.; Friend, R. H.; Sirringhaus, H. *Adv. Mater.* **2005**, *17*, 997.

(14) (a) Sekitani, T.; Takamiya, M.; Noguchi, Y.; Nakano, S.; Kato, Y.; Sakurai, T.; Someya, T. *Nat. Mater.* **2007**, *6*, 413. (b) Noh, Y. Y.; Zhao, N.; Caironi, M.; Sirringhaus, H. *Nat. Nanotechnol.* **2007**, *2*, 784.

(15) Bartzsch, M.; Kempa, H.; Otto, M.; Hübler, A.; Zielke, D. *Org. Electron.* **2007**, *8*, 431.

(16) Liu, S.; Wang, W. M.; Mannsfeld, S. C. B.; Locklin, J.; Erk, P.; Gomez, M.; Richter, F.; Bao, Z. *Langmuir* **2007**, *23*, 7428.

(17) Huang, C.; Katz, H. E.; West, J. E. *Langmuir* **2007**, *23*, 13223−13231.

10.1021/la703818d CCC: $40.75 © 2008 American Chemical Society
Published on Web 01/17/2008

Experimental Section

Elastomeric Relief Stamp. Microcontact printing of a self-assembled monolayer is facilitated using an elastomeric polydimethylsiloxane (PDMS) stamp. The stamp is created by pouring a commercially available two-component curable siloxane (Sylguard 184; Dow Corning, Midland, MI) over a relief master, giving a stamp with a thickness of 1 to 2 mm.[18,9] The relief master is prepared by evaporating gold to a thickness of 150 nm through a shadow mask onto the surface of a silicon wafer, followed by evaporating titanium to a thickness of 40 nm over the entire wafer (without any masking). The wafer is then sonicated in 2-propanol to lift off the gold features (exploiting the poor adhesion of gold on silicon); this also removes the titanium located on top of the gold but leaves the titanium behind in those areas of the wafer not covered with gold (taking advantage of the excellent adhesion of titanium on silicon). The result is a negative image of the desired pattern, with the titanium serving as a resist during the subsequent silicon etch. The silicon etch is carried out by immersing the wafer in an aqueous solution of potassium hydroxide (100 g/L KOH, bath heated to 40 °C) for 60 min, etching the silicon to a depth of a few micrometers in those areas not protected by titanium. After the wafer is rinsed and dried, the two-component siloxane is poured over the relief master, followed by curing the stamp in an oven at a temperature of 60 °C for several hours. Finally, the stamp is carefully peeled off of the master, cleaned in 2-propanol and *n*-hexane, and dried at 60 °C.

Microcontact Printing and Gate Stack Formation. The organic transistors and integrated circuits are fabricated on glass substrates and utilize an inverted staggered (bottom-gate, top-contact) device structure. In the first step, the substrate is coated with a uniform 20-nm-thick film of thermally evaporated aluminum. The aluminum surface is briefly exposed to an oxygen plasma to increase the thickness of the (native) aluminum oxide layer and to create a density of hydroxyl groups sufficient for molecular adsorption. The PDMS stamp is briefly immersed (inked) in a 2-propanol solution containing 5 mM *n*-octadecylphosphonic acid, $CH_3(CH_2)_{17}PO(OH)_2$ (PolyCarbon Industries, PCI Synthesis, Devens) and then dried in a stream of nitrogen and placed onto the plasma-treated aluminum-coated substrate to transfer the monolayer pattern. This is done by gradually unbending the stamp over the substrate, without applying mechanical pressure, and leaving the stamp in contact with the substrate for 10 min. The result is a self-assembled monolayer of *n*-octadecylphosphonic acid in those areas of the aluminum surface in contact with the raised regions of the relief stamp.[19] After the stamp is removed, the substrate is briefly heated to 70 °C on a hot plate in order to stabilize the transferred monolayer[20] and then immersed in a dilute mixture of glacial acetic acid, nitric acid, and phosphoric acid (80 vol % H_3PO_4, 10 vol % H_2O, 5 vol % CH_3COOH, 5 vol % HNO_3) in order to etch the aluminum in those areas not protected by the phosphonic acid monolayer resist.

Organic Semiconductors. Prior to use, the organic semiconductors pentacene (Fluka, Germany) and hexadecafluorocopperphthalocyanine (F_{16}CuPc; Sigma-Aldrich, Germany) are purified twice by temperature-gradient sublimation in a quartz tube. Pentacene is used to prepare the p-channel transistors, and F_{16}CuPc is employed for the n-channel TFTs. Both semiconductors are deposited by thermal evaporation from resistively heated molybdenum boats in a vacuum of about 10^{-6} mbar. Patterning of the organic semiconductor layers is accomplished using shadow masks. During the semiconductor depositions, the substrate is held at a temperature of 90 °C for F_{16}CuPc and 60 °C for pentacene because this was found to give the best performance for the respective transistors.

Source and Drain Contacts. Transistors are completed by thermally evaporating gold source and drain contacts to a thickness of 30 nm through another shadow mask. All TFTs (discrete or integrated) have a channel length of 30 μm and a channel width of 100 μm (pentacene p-channel TFTs) or 500 μm (F_{16}CuPc n-channel TFTs). All electrical measurements are carried out in ambient air at room temperature.

Results and Discussion

The manufacturing process for the organic transistors and circuits is shown in Figure 1. A glass substrate is uniformly coated with a thin layer of aluminum and briefly exposed to an oxygen plasma. An elastomeric relief stamp is inked with *n*-octadecylphosphonic acid and brought into contact with the substrate. This creates a patterned SAM on the surface of the aluminum in those regions of the substrate contacted by the raised features of stamp. The SAM pattern then serves as an etch resist to facilitate the high-resolution patterning of the aluminum layer. This concludes the definition of the gate electrodes of the final devices.

Following the aluminum etch, we have explored three options for completing the device process. In the simplest case (option A), we continue immediately with the deposition of the organic semiconductors by evaporating a 30-nm-thick film of pentacene for the p-channel TFTs and a 30-nm-thick film of hexadecafluorocopperphthalocyanine (F_{16}CuPc) for the n-channel TFTs. Both semiconductors are patterned using shadow masks. This is followed by the evaporation of the gold source and drain contacts through another shadow mask.

The gate dielectric of the completed transistors is a stack of oxygen-plasma-enhanced aluminum oxide and the printed phosphonic acid monolayer. Small-angle X-ray reflectivity measurements indicate a thickness of 3.6 nm for the plasma-enhanced aluminum oxide and 2.1 nm for the SAM.[21] The dielectric capacitance is 0.7 $\mu F/cm^2$ (measured by impedance spectroscopy), so the TFTs require operating voltages of about 3 V (Figure 2a,b). The p-channel pentacene TFTs have a carrier mobility of 0.4 cm^2/V s, and the n-channel F_{16}CuPc TFTs have a carrier mobility of 0.01 cm^2/V s. The mobilities are similar to those of pentacene and F_{16}CuPc TFTs with aluminum gate electrodes patterned by shadow masking and with a SAM-based gate dielectric prepared by immersing the substrate in a solution of *n*-octadecylphosphonic acid.[21,22]

The TFTs prepared with option A have a maximum gate current of $\sim 10^{-8}$ A. This is about 2 orders of magnitude smaller than the maximum drain current ($\sim 10^{-6}$ A). For certain organic electronics applications, a gate current of 10^{-8} A may be sufficiently low, and a drain current/gate current ratio of 10^2 may be sufficiently large. For these applications, option A may be the most suitable process option because of its simplicity.

For other applications, in particular applications that require very low stand-by power consumption, it may be desirable to provide TFTs with smaller gate currents and a larger drain current/gate current ratio. This can be accomplished by implementing certain modifications to the gate dielectric process (options B and C, Figure 1).

Option B is intended to eliminate weak spots in the printed SAM after the aluminum etch and prior to the semiconductor deposition, particularly along the periphery of the etched gate patterns. These weak spots in the SAM coverage are eliminated by immersing the substrate in a 2-propanol solution of *n*-octadecylphosphonic acid after the aluminum etch, followed by the semiconductor and source/drain contact depositions (Figure 1). This additional process step increases the overall complexity

(18) Xia, Y.; Mrksich, M.; Kim, E.; Whitesides, G. M. *J. Am. Chem. Soc.* **1995**, *117*, 9576.
(19) (a) Folkers, J. P.; Gorman, C. B.; Laibinis, P. E.; Buchholz, S.; Whitesides, G. M. *Langmuir* **1995**, *11*, 813. (b) Ramsier, R. D.; Henriksen, P. N.; Gent, A. N. *Surf. Sci.* **1988**, *203*, 72. (c) Bram, C.; Jung, C.; Stratmann, M. *Fresenius J. Anal. Chem.* **1997**, *358*, 108.
(20) Goetting, L. B.; Deng, T.; Whitesides, G. M. *Langmuir* **1999**, *15*, 1182.
(21) Klauk, H.; Zschieschang, U.; Pflaum, J.; Halik, M. *Nature* **2007**, *445*, 745.
(22) Klauk, H.; Zschieschang, U.; Halik, M. *J. Appl. Phys* **2007**, *102*, 074514.

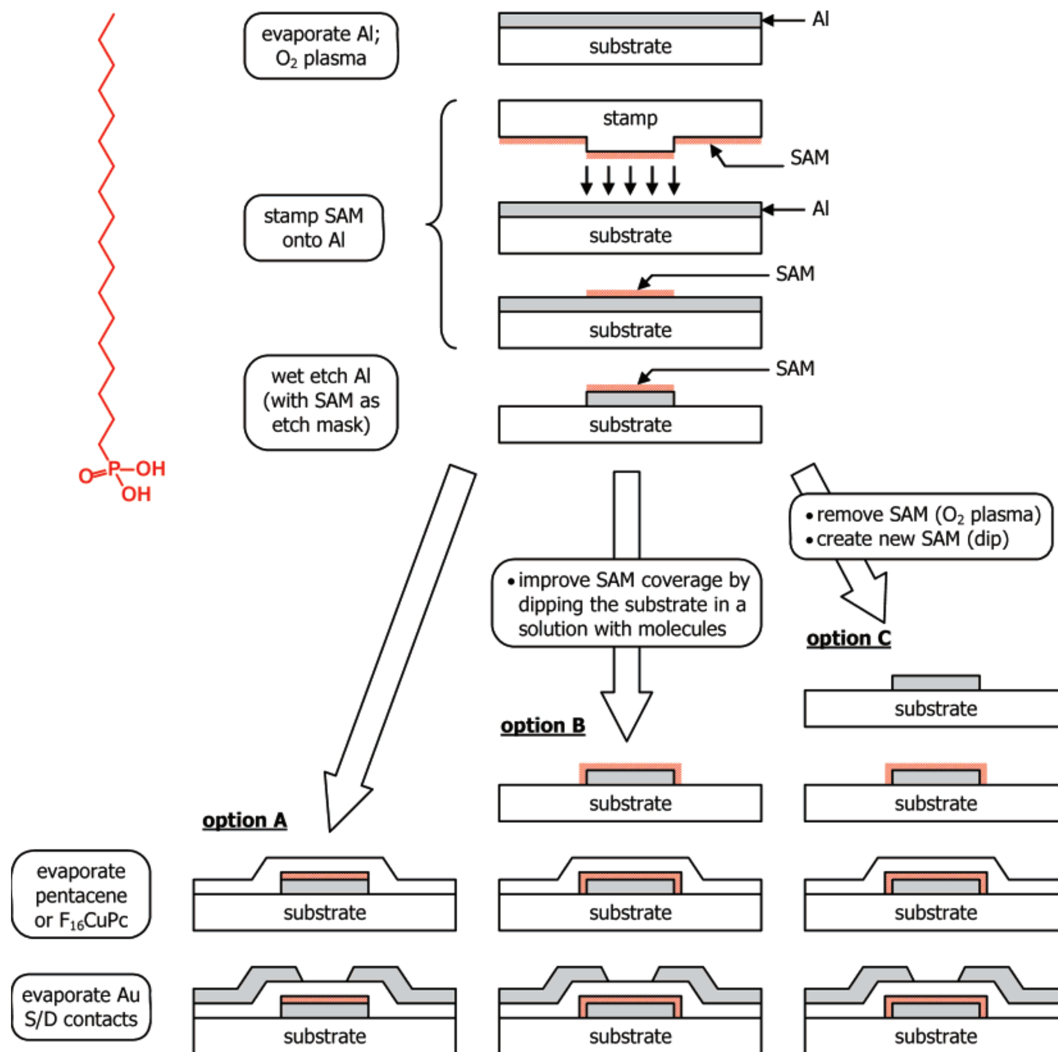


Figure 1. Process flow for organic thin-film transistors with a gate dielectric based on a microcontact-printed *n*-octadecylphosphonic acid self-assembled monolayer.

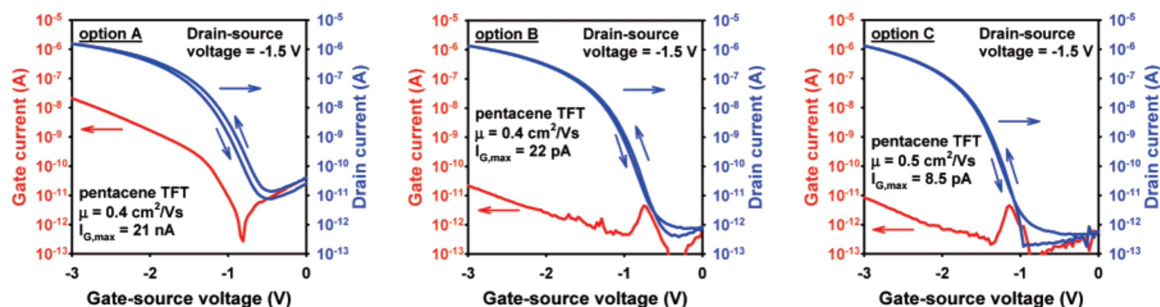
of the manufacturing process by one process step, but it reduces the gate current by 2 to 3 orders of magnitude, from $\sim 10^{-8}$ A (option A) to well below 10^{-10} A (option B; Figure 2a,b). The electrical parameters of the pentacene and $F_{16}CuPc$ TFTs manufactured with option B are essentially identical to those of TFTs with shadow-mask-patterned gates and a SAM-based dielectric prepared from solution.[21]

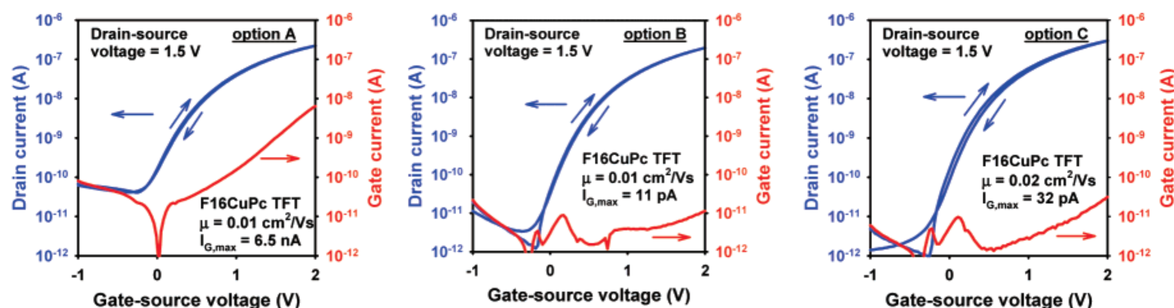
With the intent to reduce the gate current even further, we executed option C by stripping the printed SAM after the aluminum etch and replacing it with a fresh monolayer. This was accomplished by briefly exposing the substrate to an oxygen plasma (to remove the printed SAM) and then immersing the substrate in a 2-propanol solution of *n*-octadecylphosphonic acid (to allow a fresh monolayer to self-assemble). Compared with option B, option C requires one additional processing step (the oxygen plasma etch). In the case of the pentacene TFTs, option C reduces the gate current to below 10^{-11} A for a drain current/gate current ratio of greater than 10^5 (Figure 2a). In the case of the $F_{16}CuPc$ TFTs, there is no significant improvement over option B. (The gate current at $V_{GS} = 2$ V is actually slightly larger compared with option B, whereas the off-state current, the on/off current ratio, and the mobility are slightly improved; see Figure 2b.)

In addition to discrete TFTs, we have also manufactured complementary inverters based on pentacene and $F_{16}CuPc$ TFTs with printed SAM dielectric and wet-etched aluminum gates. The main advantage of complementary circuits over circuits based on a single carrier type is the lower static power consumption because in a complementary logic gate all transistors of one carrier type are always in the nonconducting off state, except during switching.[21,23,24]

Complementary inverters based on all three manufacturing options (options A−C) show sharp switching with rail-to-rail output swings and large small-signal gain (~100) for supply voltages between 1.5 and 3 V (Figure 2c). As expected, the magnitude of the static leakage current (i.e., the undesirable current flowing from the supply rail when $V_{in} = 0$ or $V_{in} = V_{DD}$) in these inverters depends on the manufacturing option. With option A, the leakage current measured at $V_{DD} = 3$ V and $V_{in} = 0$ V is 38 nA. With option B, the leakage current at the same bias is reduced to 110 pA. With option C, the leakage current is even further reduced to 12 pA. This means that the maximum static power dissipation at a supply voltage of 3 V is 114 nW for inverter A, 330 pW for inverter B, and 36 pW for inverter C. Thus, depending on the specific requirements of the intended application, three options are available to strike a useful compromise between manufacturing cost and system performance.

(23) Crone, B. K.; Dodabalapur, A.; Sarpeshkar, R.; Filas, R. W.; Lin, Y. Y.; Bao, Z.; O'Neill, J. H.; Li, W.; Katz, H. E. *J. Appl. Phys.* **2001**, *89*, 5125.
(24) Klauk, H.; Halik, M.; Zschieschang, U.; Eder, F.; Rohde, D.; Schmid, G.; Dehm, C. *IEEE Trans. Electron Devices* **2005**, *52*, 618.





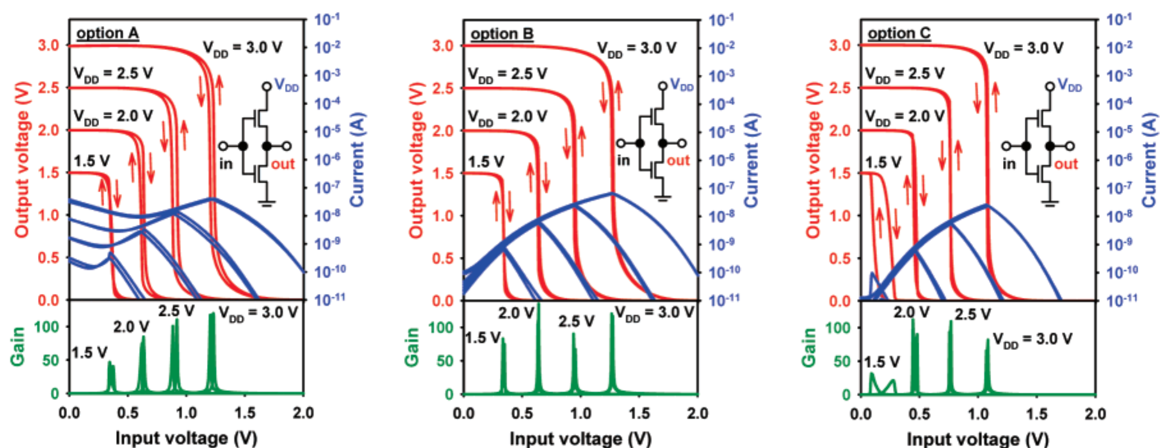


Figure 2. Current−voltage characteristics of p-channel pentacene transistors (a), n-channel $F_{16}CuPc$ TFTs (b), and complementary inverters (c) with printed SAM dielectrics. All TFTs have a channel length of 30 μm.

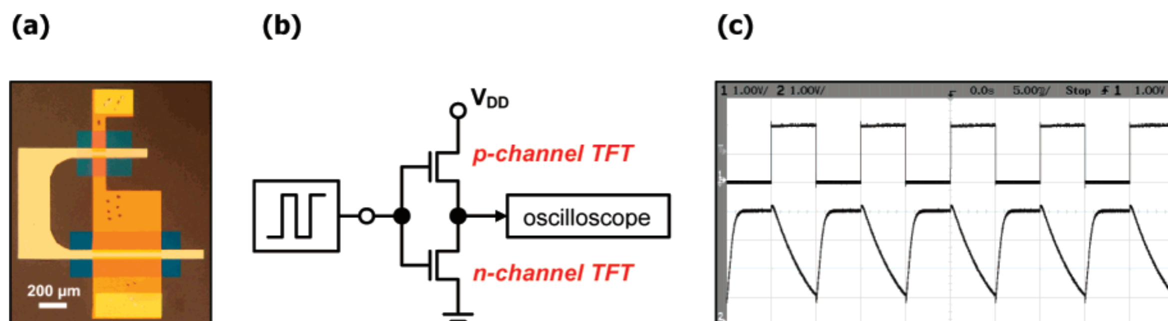


Figure 3. Photograph (a) and dynamic response (b, c) of a complementary inverter manufactured with option C.

The photograph of a complementary inverter manufactured with option C is shown in Figure 3a. To evaluate its dynamic characteristics, we have applied a square-wave signal with an amplitude of 2 V and a period of 10 ms to the input of the inverter while monitoring the output with an oscilloscope, as shown in Figure 3b. Because of the significant difference in carrier mobility between the n-channel TFT and the p-channel TFT, the rise and fall times are different, and the output signal is asymmetric (Figure 3c). The switching speed is limited by the carrier mobility of the n-channel TFT, by the channel length (30 μm), and by the gate-to-contact overlap (30 μm). Faster circuits are feasible by increasing the mobility of the n-channel

transistors[25] and by combining the microcontact-printed monolayer gate stack reported here with high-resolution source/drain contacts. Assuming similar mobilities of 0.5 cm^2/V s for both TFTs and critical dimensions of 5 μm, operating frequencies above 100 kHz at 3 V are projected.

Conclusions

We have utilized a microcontact-printed phosphonic acid self-assembled monolayer to demonstrate a printing technique for electronic devices and circuits that combines the concepts of direct and indirect printing in the same printing step and for the same material. The microcontact-printed SAM serves both as an etch resist for the patterning of the metal gate electrodes of organic thin-film transistors and as an integral part of an ultrathin gate dielectric of the same devices. The small thickness and high quality of the SAM-based dielectric allow the transistors and complementary inverters to operate at a voltage of 3 V.

For the laboratory-scale demonstration reported here, the organic semiconductors and the source/drain contacts were deposited by vacuum evaporation and patterned using manually aligned shadow masks. For future low-cost, high-volume roll-to-roll manufacturing schemes, it may be more useful to deposit the semiconductors and contacts using high-resolution direct printing methods such as thermal transfer,[8] inkjet,[10,14] and vapor jet printing.[11] The realization of more complex circuits or active-matrix displays based on the process described here requires the generation of vertical interconnects between the first metal layer (aluminum) and the second metal layer (gold) through the gate dielectric stack in places where the gate of one TFT must be wired to the source or drain of another TFT. This may be accomplished by a simple mechanical process similar to embossing or punching[26] that results in a local intermixing of the first and second metals.

Acknowledgment. We thank Benjamin Stuhlhofer at the Max Planck Institute for Solid State Research for expert technical assistance and Richard Rook at CADiLAC Laser for providing high-quality shadow masks. M.H. acknowledges financial support by the Deutsche Forschungsgemeinschaft.

LA703818D

(25) Jones, B. A.; Ahrens, M. J.; Yoon, M. H.; Facchetti, A.; Marks, T. J.; Wasielewski, M. R. *Angew. Chem., Int. Ed.* **2004**, *43*, 6363.

(26) Drury, C. J.; Mutsaers, C. M. J.; Hart, C. M.; Matters, M.; de Leeuw, D. M. *Appl. Phys. Lett.* **1998**, *73*, 108.