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# Flexible organic transistors and circuits with extreme bending stability

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**Flexible electronic circuits are an essential prerequisite for the development of rollable displays, conformable sensors, biodegradable electronics and other applications with unconventional form factors. The smallest radius into which a circuit can be bent is typically several millimetres, limited by strain-induced damage to the active circuit elements. Bending-induced damage can be avoided by placing the circuit elements on rigid islands connected by stretchable wires, but the presence of rigid areas within the substrate plane limits the bending radius. Here we demonstrate organic transistors and complementary circuits that continue to operate without degradation while being folded into a radius of 100 μm. This enormous flexibility and bending stability is enabled by a very thin plastic substrate (12.5 μm), an atomically smooth planarization coating and a hybrid encapsulation stack that places the transistors in the neutral strain position. We demonstrate a potential application as a catheter with a sheet of transistors and sensors wrapped around it that enables the spatially resolved measurement of physical or chemical properties inside long, narrow tubes.**

An important trend in large-area electronics for display and sensor applications is mechanical flexibility[1–22]. The ultimate goal is electronic systems that cannot only be flexed (into a bending radius of a few centimetres or perhaps a few millimetres), but can also be tightly rolled, bent around sharp edges or repeatedly creased without degradation of the electronic functionality. This requires the development of devices that can withstand extremely small bending radii without suffering damage. Although there are many reports of flexible organic and inorganic transistors[6–12], in all previous reports the transistors were degraded or destroyed when being bent into a radius smaller than a few millimetres, owing to damage by the bending-induced mechanical strain. There is one report by the Princeton University group[9] of transistors that survive bending to a radius of 500 μm, but these transistors require relatively high operating voltages (15 V), they were not tested during bending (only before and after bending), and integrated circuits were not demonstrated. Although bending radii of 500 μm to a few millimetres are sufficient for displays or sensors that can be wrapped around a macroscopic object[1,2], much smaller bending radii are required if the devices are expected to survive repeated crumpling, creasing or sharp folding. In addition to large bending stability, the transistors and circuits should also have good electrical performance characteristics, such as large carrier field-effect mobility and low operating voltage, and they should not exhibit bending-stress-induced changes or degradation. As Table 1 illustrates, combining extreme bending stability, large field-effect mobility and low operating voltage has been rather challenging. Here we demonstrate organic transistors and circuits with mobilities of 0.5 $cm^2 V^{-1} s^{-1}$ that operate with supply voltages of only 3 V and while being folded into a bending radius as small as 100 μm. To demonstrate a potential electronic application that requires high-performance circuits that operate while being folded into extremely small bending radii, we have manufactured a very thin catheter that measures the spatial distribution of pressure by using a foldable transistor and sensor matrix wrapped around its surface in a helical structure.

The first prerequisite for the fabrication of transistors that can be bent into a small radius is the use of a very thin substrate. Organic thin-film transistors (TFTs) are often fabricated on sheets of polyimide, polyethylene naphthalate or polyethylene terephthalate that are typically around 100 μm thick, with a few reports of organic TFTs on substrates as thin as 25 μm (ref. 1). To allow bending into radii well below 1 mm, we use a polyimide substrate that has a thickness of only 12.5 μm (UPILEX-12.5S, Ube Chemical). These substrates have a surface roughness of about 2.5 nm r.m.s. (see Supplementary Fig. S1b), much rougher than silicon substrates (see Supplementary Fig. S1a) and too rough to permit the formation of well-ordered organic semiconductor films with large field-effect mobility[23]. To reduce the surface roughness, our polyimide substrates are coated with a 500-nm-thick polyimide planarization layer (KEMITITE CT4112, Kyocera Chemical), which is deposited by spin-coating and cured at a temperature of 180 °C. The surface roughness of the planarization layer is 0.3 nm r.m.s., which is similar to the surface roughness of silicon dioxide layers thermally grown on carefully polished single-crystalline silicon wafers (see Supplementary Fig. S1c).

On this very thin, almost atomically smooth surface we have fabricated organic TFTs and organic complementary circuits with excellent static and dynamic performance. As Fig. 1a shows, the thin polyimide foil is indeed extremely flexible. The schematic structure of the organic TFTs is shown in Fig. 1b. Twenty-nanometre-thick aluminium (Al) gate electrodes, a 6-nm-thick hybrid aluminium oxide ($AlO_x$)/organic self-assembled monolayer (SAM) gate dielectric, 30-nm-thick semiconductor layers and 50-nm-thick Au source/drain contacts were sequentially formed on the planarization layer, so the total thickness of the TFTs is only 106 nm. The organic semiconductor is either pentacene (for the p-channel TFTs) or hexadecafluorocopperphthalocyanine ($F_{16}CuPc$, for the n-channel TFTs). Al gates, organic semiconductors and Au source/drain contacts were all patterned using shadow masks, so that no resist baking is required and the maximum process temperature is less than 100 °C. Creating both p-channel and n-channel

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**Table 1 | Comparison with literature data.**

| | Polycrystalline silicon TFTs (ref. 6) | Metal oxide TFTs (ref. 7) | Amorphous silicon TFTs (refs 8,9) | Organic TFTs (ref. 10) | Organic TFTs (ref. 12) | Organic TFTs (this work) |
|---|---|---|---|---|---|---|
| Field-effect mobility | $>10\ cm^2\ V^{-1}\ s^{-1}$ | $7\ cm^2\ V^{-1}\ s^{-1}$ | $0.5\ cm^2\ V^{-1}\ s^{-1}$ | $0.5\ cm^2\ V^{-1}\ s^{-1}$ | $0.1\ cm^2\ V^{-1}\ s^{-1}$ | $0.5\ cm^2\ V^{-1}\ s^{-1}$ |
| Operating voltage | 4 V | 10 V | 15 V | 40 V | 2.5 V | 2 V |
| Minimum bending radius | 10 mm | 30 mm | 0.5 mm | 0.5 mm | 2.5 mm | 0.1 mm |

Carrier field-effect mobility, operating voltage and bending stability reported for inorganic and organic TFTs.

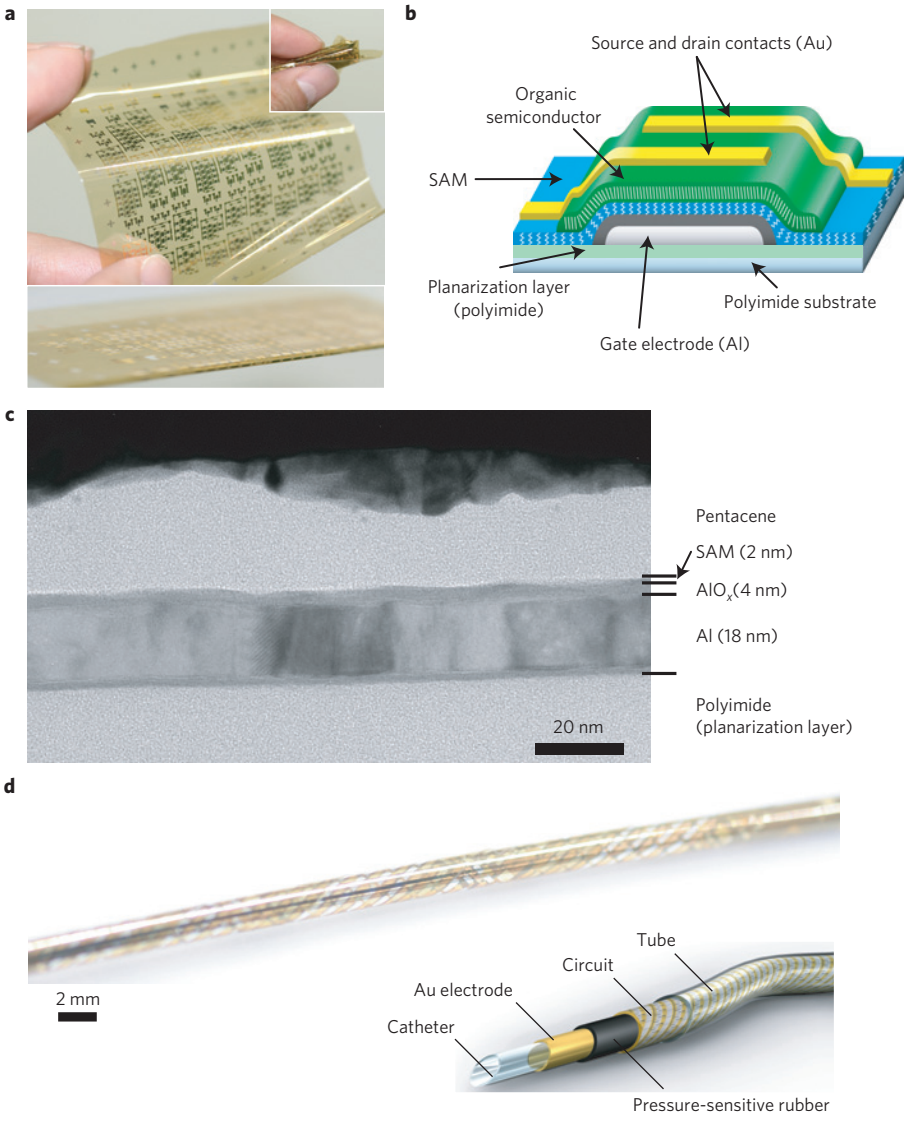


**Figure 1 | Ultraflexible integrated circuits. a**, Photographs of a 12.5-μm-thick polyimide substrate with functional organic TFTs and organic complementary circuits. The array has an area of $75 \times 75\ mm^2$. **b**, Schematic cross-section of the TFTs. **c**, High-resolution cross-sectional electron microscopy image of a flexible TFT. The specimen was prepared using a focused ion beam and imaged by transmission electron microscopy (300 kV). **d**, Photograph of a thin catheter that measures the spatial distribution of pressure along its length and circumference by means of an active-matrix sensor helix. A cross-sectional illustration of the development view is also shown.

TFTs allows for the design of complementary circuits, which have substantially smaller power consumption, larger gain and greater noise immunity than unipolar circuits[24–26].

The final process step is the deposition of a hybrid encapsulation stack that serves two purposes. As the encapsulation stack is composed of a metal layer (Au, 200 nm thick) sandwiched between two polymer layers (parylene, 300 nm and 12.5 μm thick), it is an excellent barrier against the diffusion of oxygen and humidity from the ambient air into the organic semiconductors, and hence greatly increases the air stability of the devices and circuits[27]. Moreover, as the encapsulation stack has the same thickness as the polyimide substrate (that is, 13 μm), the TFTs and circuits are now located in the neutral strain position (where bending-induced compressive and tensile strain cancel each other), which

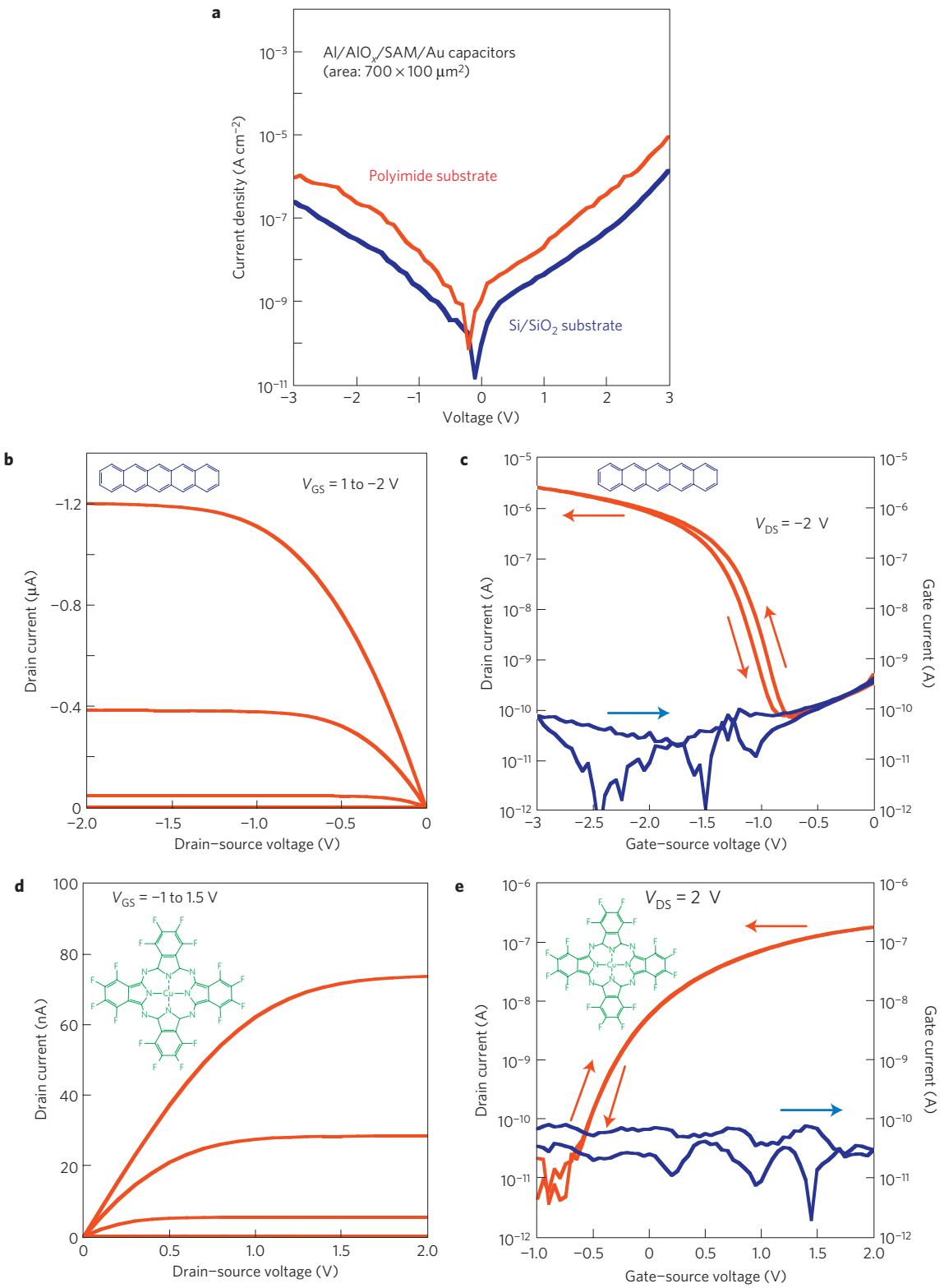


**Figure 2 | Performance of organic TFTs on plastic substrates. a**, Leakage current through the 6-nm-thick $AlO_x$/SAM gate dielectric as a function of applied voltage. Measurements were carried out on Al/$AlO_x$/SAM/Au capacitors on two different substrates: a 12.5-μm-thick polyimide substrate with a 500-nm-thick polyimide planarization layer (red curve), and a thermally oxidized, single-crystalline silicon wafer (blue curve). **b**, Drain current as a function of drain–source voltage for a pentacene p-channel TFT (gate–source voltage ($V_{GS}$) in steps of 0.5 V). **c**, Drain current and gate current as a function of gate–source voltage for a pentacene p-channel TFT (drain–source voltage ($V_{DS}$): −2 V). Owing to the small thickness of the gate dielectric (6 nm), the operation voltage is about 2 V. The field-effect mobility extracted from the transfer characteristics is 0.5 cm$^2$ V$^{-1}$ s$^{-1}$. **d**, Drain current as a function of drain–source voltage for a $F_{16}$CuPc n-channel TFT (gate–source voltage in steps of 0.5 V). **e**, Drain current and gate current as a function of gate–source voltage for a $F_{16}$CuPc n-channel TFT (drain–source voltage: 2 V). The mobility is 0.01 cm$^2$ V$^{-1}$ s$^{-1}$. Hysteresis and gate leakage are very small for both types of TFT.

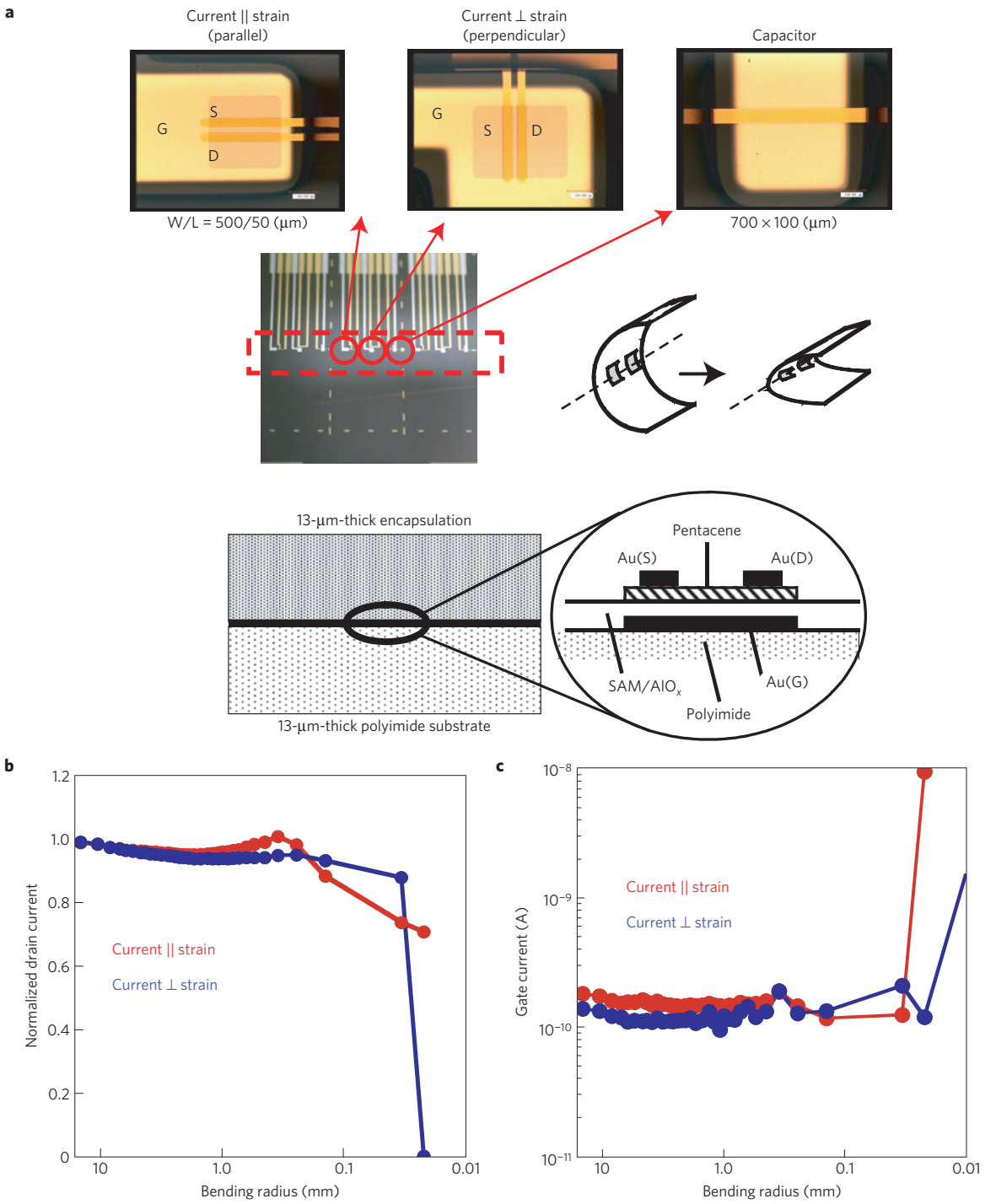


**Figure 3 | Bending tests on ultraflexible organic TFTs. a**, Photographs of a TFT in which the drain current flows parallel to the bending-induced strain, of a TFT in which the current flows perpendicularly to the strain and of an Al/AlO$_x$/SAM/Au capacitor that allows measurement of the gate dielectric capacitance during bending. The TFTs have a channel length of 50 μm and a channel width of 500 μm. The capacitor has an area of 700 × 100 μm$^2$. Bending was carried out using a custom-built precision bending apparatus. **b**, Measured drain currents of two pentacene TFTs (red: strain parallel to the drain current; blue: strain perpendicular to the drain current) as a function of bending radius during inward bending, normalized to the initial drain current measured in the flat state. **c**, Gate currents of the same TFTs measured during inward bending. Drain–source voltage: −2 V; gate–source voltage: −2.5 V.

means they are not subjected to strain and thus are highly stable during sharp bending[9,10].

Figure 1c shows a high-resolution cross-sectional electron microscopy image of a completed transistor. The specimen was prepared using a focused ion beam (FB-2100, Hitachi High-Technologies) and imaged by transmission electron microscopy (HF-3300 Cold-FE TEM, 300 kV, Hitachi High-Technologies). The Al gate as well as the 4-nm-thick AlO$_x$ layer and the 2-nm-thick SAM of the hybrid gate dielectric is clearly resolved in the transmission electron micrograph. Owing to the small surface roughness provided by the 500-nm-thick polyimide planarization layer, the individual TFT layers are very smooth. When the planarization layer is omitted, the TFT layers are much rougher (see Supplementary Fig. S2b).

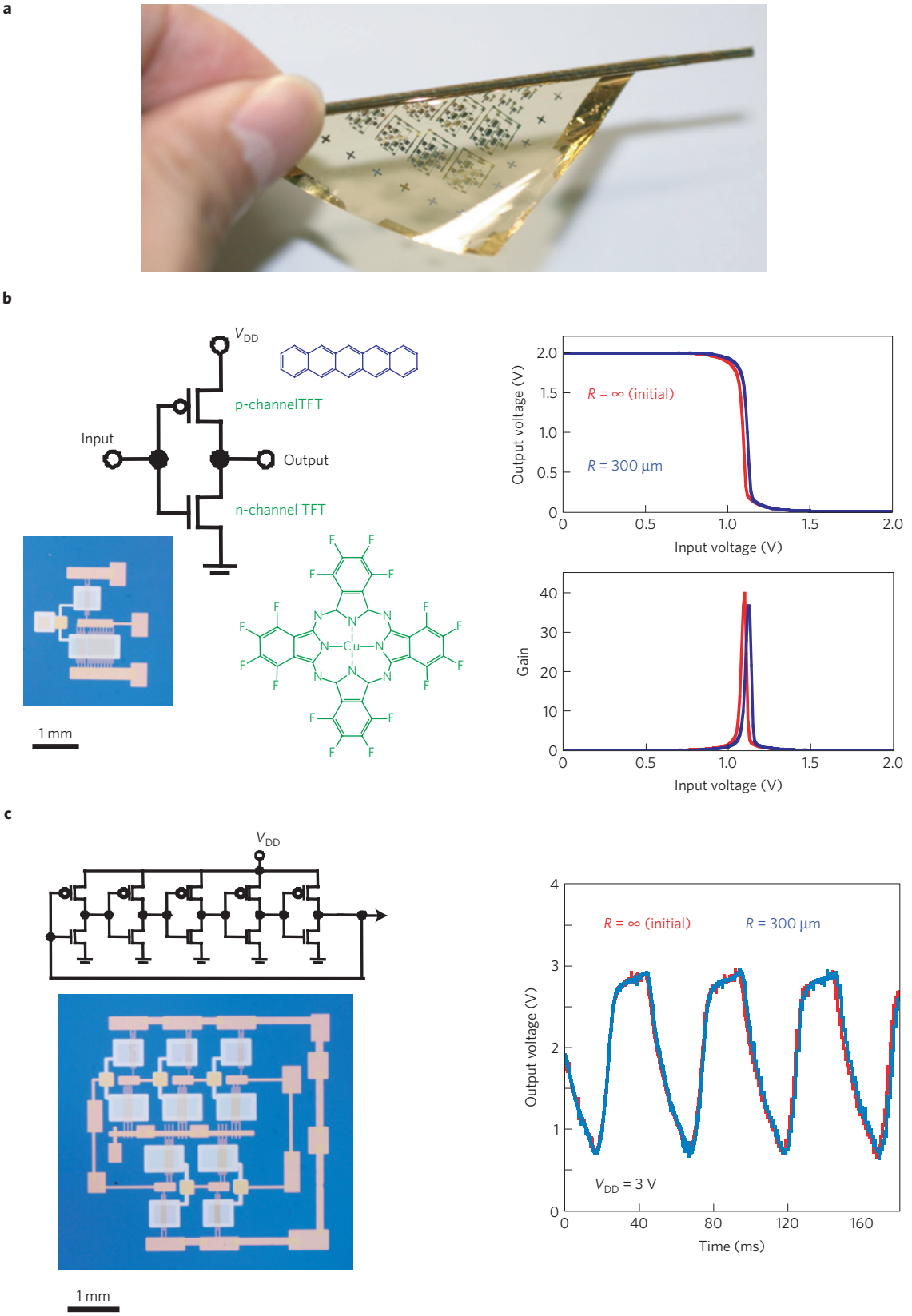


**Figure 4 | Ultraflexible organic circuits. a**, Photograph of a polyimide substrate with functional organic TFTs and circuits wrapped around a cylinder with a radius of 300 μm. **b**, Circuit diagram, photograph and electrical transfer characteristics of a complementary inverter (composed of a pentacene p-channel TFT and a $F_{16}$CuPc n-channel TFT) operated with a supply voltage ($V_{DD}$) of 2 V. The TFTs have a channel length of 20 μm. The transfer characteristics were measured in the flat state and while the inverter was bent into a radius of 300 μm. There is no discernible change in characteristics during bending. **c**, Circuit diagram, photograph and output signals of a five-stage complementary ring oscillator operated with a supply voltage ($V_{DD}$) of 3 V in the flat state and while bent into a radius of 300 μm. The circuit oscillates with a signal delay per stage of 4.5 ms, both in the flat state and during tight bending.

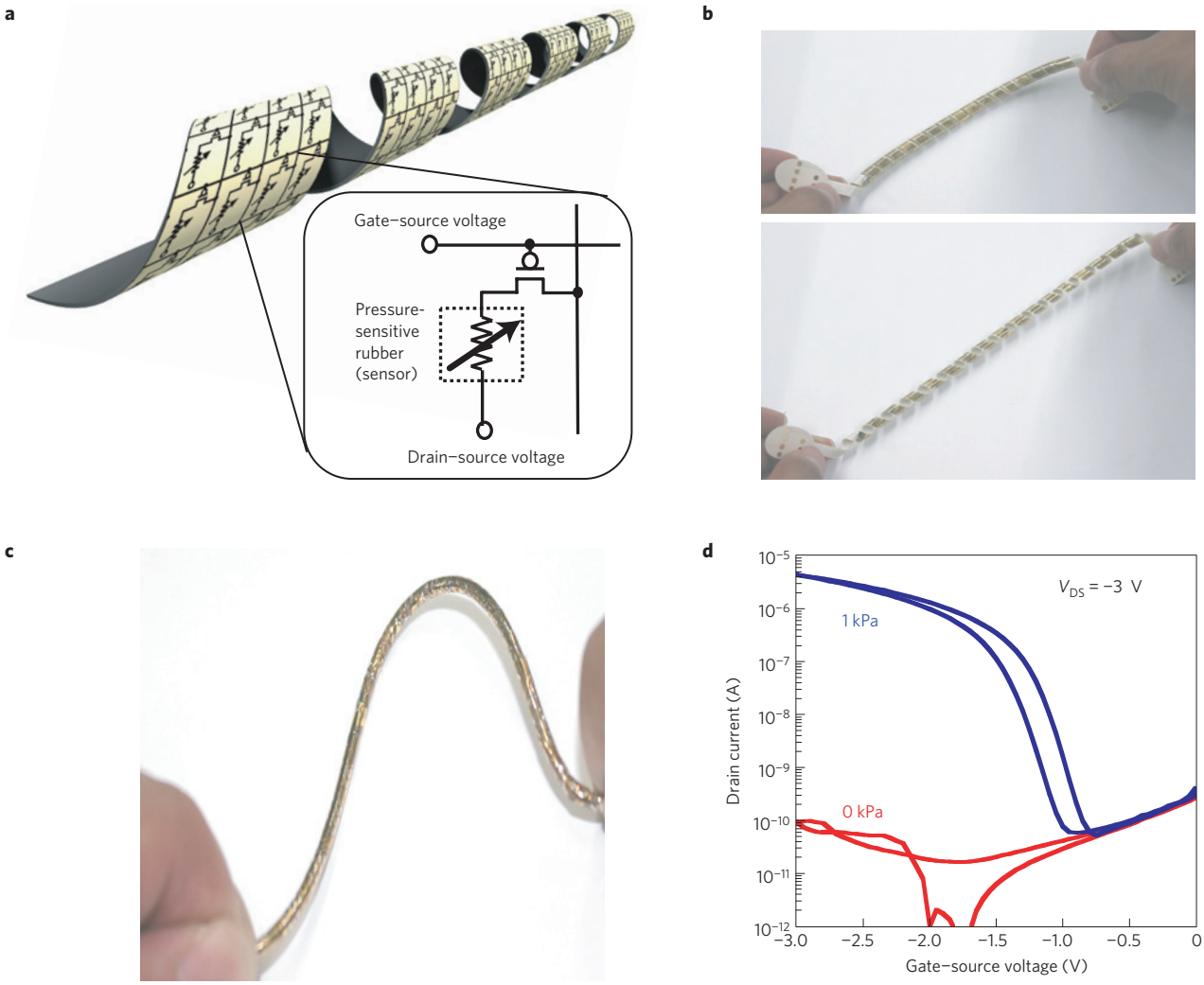


**Figure 5 | Tightly wound pressure-sensor helix. a**, Circuit diagram of an ultraflexible active-matrix pressure-sensor array in the shape of a tightly wound helix. **b**, Photographs of a TFT array fabricated on a shape-memory polymer film (NIPPON MEKTRON, Japan) and permanently transformed into a helix. Even when the helix is stretched by 50% the TFTs remain functional. **c**, Photograph of a tightly wound active-matrix sensor array for a catheter that measures the spatial distribution of pressure. The array was fabricated by laminating three sheets: (1) a foldable 4 × 36 array of pentacene TFTs, (2) a pressure-sensitive rubber sheet and (3) a 12.5-μm-thick polyimide sheet with a Au counter electrode. **d**, Transfer characteristics of an individual sensor cell measured at two different pressures. (Note that applying pressure to the pressure-sensitive rubber sheet creates a conducting path between the source of the TFT and the counter electrode. Thus, the potential of −3 V is present on the source of the TFT only when pressure is applied, allowing the array to measure the spatial distribution of pressure.)

Despite the small gate dielectric thickness (6 nm), the leakage currents through the dielectric are below $10^{-5}$ A cm$^{-2}$ at an applied voltage of 3 V (which corresponds to an electric field of 5 MV cm$^{-1}$; see Fig. 2a). The current–voltage characteristics of a pentacene p-channel and a $F_{16}$CuPc n-channel TFT fabricated on a substrate with a 500-nm-thick polyimide planarization layer are shown in Fig. 2b–e. The mobilities (0.5 cm$^2$ V$^{-1}$ s$^{-1}$ for pentacene, 0.01 cm$^2$ V$^{-1}$ s$^{-1}$ for $F_{16}$CuPc), subthreshold swings and on/off ratios are essentially identical to those of TFTs on glass[25], and the hysteresis in the transfer curves (Fig. 2c,e) is negligible. The electrical characteristics are stable during exposure to air for six months, which is a direct result of the excellent gas barrier characteristics of the 13-μm-thick parylene/Au/parylene passivation stack[27].

To confirm the critical role of the 500-nm-thick polyimide planarization layer for achieving good device performance, we have also fabricated TFTs on a polyimide substrate without a planarization layer. The lack of a planarization layer leads to a much greater surface roughness of the Al gate electrodes and the $AlO_x$/SAM gate dielectric (see Supplementary Figs S1 and S2b), so the pentacene films in these transistors are characterized by much smaller field-effect mobility (0.01 cm$^2$ V$^{-1}$ s$^{-1}$) and substantial hysteresis (see Supplementary Fig. S3).

The bending stability of the transistors was evaluated by bending the substrate into a radius as small as 100 μm along an axis running exactly through the TFTs, with the direction of the bending-induced strain aligned either parallel or perpendicularly to the direction of the current flow from drain to source (see Fig. 3a). Bending was carried out using a custom-built bending apparatus, and the electrical characteristics were measured while the devices were being bent (see Supplementary Fig. S4). Figure 3b shows the measured drain currents of two pentacene TFTs (one bent in the parallel direction and one bent in the perpendicular direction) as a function of bending radius, normalized to the drain current measured in the flat state. Figure 3c shows the gate currents of the same TFTs for each bending radius. Supplementary Fig. S5 shows the capacitance of an Al/$AlO_x$/SAM/Au capacitor as a function of bending radius. As can be seen, the electrical characteristics of the TFTs are stable for bending radii down to 100 μm, which is by far the smallest bending

radius reported for an organic (or inorganic) field-effect transistor. Comparing Fig. 3b and c suggests that the damage that occurs when the bending radius is decreased below 100 μm originates in the gate dielectric of the transistors.

For comparison, we have also carried out bending tests on pentacene TFTs fabricated on thicker polyimide substrates (thickness 75 μm instead of 12.5 μm) and fabricated without the 13-μm-thick parylene/Au/parylene encapsulation stack. In this case, the TFTs are not located in the neutral strain position and thus are fully exposed to the bending-induced mechanical strain. The measurement results, shown in Supplementary Fig. S6, indicate that in these TFTs damage occurs at a much larger bending radius (~3.5 mm), which confirms the benefit of employing an encapsulation stack that places the TFTs in the neutral strain position.

We have also evaluated the bending stability of organic complementary inverters and ring oscillators fabricated along with the pentacene p-channel and $F_{16}$CuPc n-channel TFTs on the flexible polyimide substrates. There are only very few reports of flexible organic complementary ring oscillators, and in all of them the circuits either required large operating voltages[28,29] or had to be operated in an inert environment owing to the use of semiconductors with air degradation[30]. Figure 4a shows a photograph of a 12.5-μm-thick polyimide substrate (complete with a 500-nm-thick planarization layer, organic devices and circuits, and a 13-μm-thick encapsulation stack) tightly wrapped around a cylinder with a radius of 300 μm. Figure 4b shows the circuit diagram, a photograph and the static transfer characteristics of a complementary inverter (composed of a pentacene p-channel TFT and a $F_{16}$CuPc n-channel TFT) fabricated on this substrate. The transfer characteristics were measured in ambient air in the flat state and while the substrate was bent into a radius of 300 μm. There is no discernible change in the electrical characteristics during bending. The schematic, a photograph and the output signal of a five-stage complementary ring oscillator operated with a supply voltage of 3 V are shown in Fig. 4c. The signal delay at this supply voltage is 4.5 ms per stage, similar to circuits made on glass[25]. The signal delays in the range of a few milliseconds are fast enough for certain sensor applications such as artificial skins[2], as highlighted in Figs 1 and 5. Furthermore, as can be seen, the circuit continues to oscillate in the bent state, and the output signal is unaffected by bending of the ring oscillator into a radius of 300 μm. The circuits shown in Fig. 4 were fabricated on a polyimide substrate and therefore relax back into the flat state when released from the cylinder around which they had been wrapped.

An interesting option we have also explored is the fabrication of circuits on a shape-memory polymer film[31]. The substrate is initially in its flat state to facilitate fabrication of high-performance organic devices. After wrapping the substrate around a cylinder into a helix, it is heated to a temperature of about 150 °C and then allowed to cool, which causes the substrate to permanently adapt the helical structure, as shown in Fig. 5b.

To demonstrate a possible application for organic TFTs that operate in the bent state, we have manufactured a thin catheter that measures the spatial distribution of mechanical pressure. The sensor was fabricated by laminating three sheets: a foldable 4 × 36 array of pentacene TFTs, a pressure-sensitive rubber sheet and a 12.5-μm-thick polyimide sheet with a gold counter electrode. The picture is shown in Fig. 1d and demonstrated in Fig. 5 and Supplementary Fig. S9. The source contacts of all 144 transistors are connected to the rubber sheet, and the counter electrode is in contact with the opposite surface of the rubber sheet. When mechanical pressure is exerted on the catheter, the electrical resistance between the rubber's top and bottom surfaces decreases (see Supplementary Fig. S9). A potential of −3 V applied to the counter electrode is supplied to the TFTs in those positions where pressure is applied, and thus the spatial distribution of pressure can be obtained by interrogating the TFTs in the active-matrix array.

We have demonstrated that low-voltage organic transistors that are fabricated on planarized polymeric substrate and covered with an encapsulation stack that places the devices into the neutral strain position operate reliably and with excellent performance characteristics while being folded into a bending radius as small as 100 μm. This may open a wide range of opportunities for electronic applications that require a high degree of mechanical flexibility combined with operating voltages accessible by small batteries. As an example we have illustrated a thin catheter that measures the spatial distribution of mechanical pressure using a helical sensor array enabled by ultraflexible organic transistors.

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## Author contributions

T. Sekitani and T. Someya designed the concept. T. Sekitani, U.Z., H.K. and T. Someya carried out experimental work, data analysis and wrote the paper. T. Someya supervised the project.

## Additional information

The authors declare no competing financial interests. Supplementary information accompanies this paper on www.nature.com/naturematerials. Reprints and permissions information is available online at http://npg.nature.com/reprintsandpermissions. Correspondence and requests for materials should be addressed to T. Someya.

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SUPPLEMENTARY INFORMATION

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SUPPLEMENTARY INFORMATION

# Flexible organic transistors and circuits with extreme bending stability

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## 1. Device Fabrication and characterization

Organic thin-film transistors (TFTs) and integrated circuits were fabricated on 12.5 μm thick, highly flexible polyimide film (see Figure 1a). The schematic cross-section of the TFTs is shown in Figure 1b.

In the first step of the fabrication process, the substrate was coated with a 500 nm thick polyimide planarization layer, which was deposited by spin-coating and cured for 5 hours at a temperature of 180 ºC in nitrogen. The planarization layer reduces the surface roughness of the flexible substrate from 2.5 nm to 0.32 nm RMS, which is essentially identical to the surface roughness of a polished single-crystalline silicon wafer (see Figures S1 and S2).

The gate electrodes of the transistors were prepared on the surface of the planarization layer by evaporating a nominally 20 nm thick layer of aluminum (Al) through a shadow mask. A 4 nm thick layer of aluminum oxide ($AlO_x$) was then created on the Al surface by an oxygen plasma treatment (10 min at a plasma power of 100 W). The substrate was then immersed in a 2-propanol solution of n-octadecylphosphonic acid to create a densely packed organic self-assembled monolayer (SAM) with a thickness of 2 nm on the oxidized Al surface. The total thickness of the gate dielectric is therefore 6 nm, and it has a capacitance per unit area of 0.6~0.65 μF/cm$^2$.

50 nm thick layers of the organic semiconductors pentacene (for the p-channel TFTs) and $F_{16}CuPc$ (for the n-channel TFTs) were then deposited by vacuum sublimation through shadow masks. The source and drain contacts were prepared on top of the organic semiconductors by evaporating gold (Au) to a thickness of 50 nm through a shadow mask.

Finally, a polymer/metal encapsulation stack (300 nm thick parylene, 200 nm thick gold, and 12.5 μm thick parylene) was deposited in order to protect the transistors from air-induced degradation. Consequently, all measurements reported below were carried out in ambient air. Furthermore, the deposition of the 13 μm thick encapsulation stack places the TFTs and circuits at the neutral strain position.

All measurements were performed in air. TFT characteristics were measured using an Agilent 4155C parameter analyzer with a sweep rate of about 0.1 V/sec. Figures 2b and 2c show the output and transfer characteristics of a pentacene p-channel TFT, and Figures 2d and e show the characteristics of a $F_{16}CuPc$ n-channel TFT. The hysteresis seen in Figures 2c and 2e is very small, indicating that the bias-stress effect and the density of active impurities are negligible.

## 2. Substrate Bending

To evaluate the bending stability of the TFTs, the substrate was bent along an axis running exactly through the transistors. To determine whether the angle between the direction of the bending-induced mechanical strain and the direction of the drain current in the TFTs has any effect, we fabricated TFTs in which the drain current flows parallel to the strain direction as well as TFTs in which the drain current flows perpendicularly to the strain direction (see Figure 3).

The strain S induced in a particular layer having a thickness $t_L$ located on the surface of a substrate having a thickness $t_S$ by bending the substrate into a radius R is given by the following equation:

$$S = \frac{t_L + t_S}{2R} \frac{1 + 2\eta + \chi\eta^2}{(1+\eta)(1+\chi\eta)} \qquad (1)$$

where $\eta = t_L/t_S$, $\chi = Y_L/Y_S$, $Y_L$ is Young's modulus of the layer and $Y_S$ is Young's modulus of the substrate [S1].

Figure S6 shows how the drain currents and gate currents of pentacene TFTs on a 75 μm thick polyimide substrate change upon bending. From Figure S6 it can be seen that the smallest radius into which the substrate can be bent before the TFTs degrade is 3.5 mm. According to Equation (1) this corresponds to a strain S = 1%, assuming $t_L$ = 106 nm (the total thickness of the TFTs), $t_S$ = 75 μm (the polyimide substrate thickness), and $Y_L \approx Y_S$. This suggests that 1% is the maximum compressive strain that pentacene TFTs can withstand.

By reducing the substrate thickness from 75 μm to 13 μm, the bending radius at which the strain reaches 1% is reduced from 3.5 mm to 600 μm. However, Figure 3 shows that pentacene TFTs fabricated on a 13 μm thick polyimide substrate can be bent into a radius of 100 μm before degradation sets in. This is because the TFTs in Figure 3 were encapsulated with a 13 μm thick parylene/Au/parylene stack, so that the TFTs are located at the neutral strain position and the compressive strain from the substrate and the tensile strain from the encapsulation layer cancel each other at the position of the TFTs. Because of the excellent adhesion of the parylene encapsulation layer, this structure is robust during bending to a radius as small as about 100 μm, indicating an excellent robustness of contact between source/drain electrodes and organic semiconductors. However,

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further decrease in bending radii results in damages in the gate dielectric of the transistors (See Figure 3c).

## 3. Operation speed

As summarized in Figure S8, signal delay of the ring oscillator depends, not only on channel length (L), but also on supply voltage, $V_{DD}$. The smallest signal delay on our complementary five stage ring oscillator is 4.5 ms, whose signal delays in the range of a few milliseconds are good enough for certain sensor applications like artificial skins, as highlighted in Figures 1 and 5. For example, the real-time scanning (the frame rate of 2 Hz) for a 100-by-100 sensory array can be achieved by the transistors with frequency response of about 5 ms with line-scanning method. In such sensor applications, mechanical durability and operation voltage are often more important than high operation speed.

When we compare our results with silicon-based circuits [S2], our organic circuits are slower than silicon ones, however, the silicon circuits were bent with a radius of only 4.5 mm. In contrast, our organic ring oscillator continues to operate without any change in electrical performance while being folded into a radius of 300 μm.

We would like to compare our results with previous organic transistor-based circuits. It is very important to compare the results among different structures at the same voltage, since the signal delay depends on the supply voltage: In general, circuits operated with larger voltage have smaller signal delay. Note that the unipolar circuits [S3] were operated with a supply voltage of 50 V, while our complementary circuits operate with much more battery-friendly voltages between 1.5 and 3 V. It is true that the signal delay of our flexible organic complementary ring oscillator (4.5 ms) is larger than that of some previously reported unipolar organic circuits [S3], due to the relatively small mobility of n-channel organic semiconductors. Compared with unipolar circuits, however, complementary circuits have much lower power consumption and are thus much more attractive for practical applications. Nevertheless, the flexible ring oscillator we show in this work is as fast as organic complementary circuits made on rigid glass [S4].

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## SUPPLEMENTARY INFORMATION

### Figure caption of the Supplementary Information

**Figure S1. Surface roughness of the individual layers of organic TFTs fabricated on three different substrates.** Using atomic force microscopy (AFM) we have measured the root-mean-square (RMS) surface roughness of the individual layers of which an organic thin-film transistor (TFT) is composed. Organic TFTs were fabricated on three different substrates: **a,** A thermally oxidized, single-crystalline silicon ($Si/SiO_2$) wafer. **b,** A 12.5 µm thick polyimide substrate without planarization layer. **c,** A 12.5 µm thick polyimide substrate with a 500 nm thick polyimide planarization layer. AFM images were taken (from top to bottom): of the substrate, after the deposition of the Al gate electrodes, after the oxygen-plasma-induced oxidation of the Al gates, after the formation of the phosphonic-acid self-assembled monolayer (SAM), and after the deposition of the pentacene semiconductor layer on the $AlO_x$/SAM gate dielectric.

**Figure S2. Schematic cross-sections and high-resolution transmission electron microscope (TEM) images of organic TFTs fabricated on three different substrates. a,** Pentacene TFT fabricated on a thermally oxidized, single-crystalline silicon ($Si/SiO_2$) wafer. **b**, Pentacene TFT fabricated on a 12.5 µm thick polyimide substrate without planarization layer. **c**, Pentacene TFT fabricated on a 12.5 µm thick polyimide substrate with a 500 nm thick polyimide planarization layer. The surface of the planarized polyimide substrate (and thus the individual TFT layers on this substrate) are almost atomically smooth, similar to the situation on the $Si/SiO_2$ substrate.

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**Figure S3. Current-voltage characteristics of a pentacene TFT fabricated on a polyimide substrate without planarization layer.** When the planarization layer is omitted, the surface on which the TFTs are fabricated is much rougher, so the morphology of the pentacene films does not facilitate a high degree of orbital overlap between the conjugated molecules, resulting in poor TFT performance, including low field-effect mobility (0.01 $cm^2/Vs$), large hysteresis, and small on/off ratio.

**Figure S4. Photographs taken during bending tests. a,** Photograph of the custom-built bending apparatus in action. **b**, The exact bending radius was determined from digital photographs taken along the bending axis. **c**, Photograph of a substrate with organic TFTs and circuits wrapped around a cylinder with a radius of 300 µm. Fine gold wires are used to connect the TFTs and circuits to a semiconductor parameter analyzer to facilitate electrical testing in the bent state.

**Figure S5. Capacitance of Al/$AlO_x$/SAM/Au capacitors fabricated on 12.5 µm thick polyimide substrates with a 500 nm thick polyimide planarization layer as a function of bending radius.** The blue curve shows the capacitance measured on a capacitor *with* a 13 µm thick parylene encapsulation stack (so this capacitor is located in the neutral strain position). The red curve shows the capacitance of a capacitor *without* encapsulation (so this capacitor is *not* located in the neutral strain position). For both curves the capacitance (C) is normalized to the capacitance measured in the flat state ($C_0$ = 0.65 $\mu F/cm^2$).

**Figure S6. Bending stability of pentacene TFTs fabricated on thicker substrates (thickness 75 µm instead of 12.5 µm) without encapsulation stack.** In this case, the TFTs are not located in the neutral strain position of the substrate and thus are stable only to a bending radius of about 3.5 mm (as opposed to 100 µm, as was shown in Figure 3). Drain-source voltage: -2 V, gate-source voltage: -2.5 V.

**Figure S7. Electrical characteristics of a pentacene TFT before, during and after bending to a radius of 200 µm.** The TFT was fabricated on a 12.5 µm thick polyimide substrate with a 500 nm thick polyimide planarization layer and a 13 µm thick parylene encapsulation stack. The TFT characteristics confirm that the devices are not damaged when bent into a radius of 200 µm.

**Figure S8. Signal propagation delay of complementary ring oscillators based on TFTs with a channel length of 50 µm and 20 µm a as a function of supply voltage.**

**Figure S9. Pressure sensor system. a,** Schematic cross-section of a pressure sensor sheet fabricated by laminating three sheets: (1) a foldable 4 × 36 array of pentacene TFTs, (2) a pressure-sensitive rubber sheet (PCR Technical Co. Ltd, Japan), (3) a 12.5-µm-thick polyimide sheet with a gold counter electrode. **b,** Circuit diagram of the array. The gate electrodes are connected to word lines (WL) and the drain contacts to bit lines (BL). **c,** Electrical resistance measured between the top and bottom surfaces of the pressure-sensitive rubber sheet as a function of mechanical pressure. When pressure is applied to the rubber sheet, the resistance decreases from 1 MΩ at 100 Pa to 100 Ω at $10^4$ Pa.

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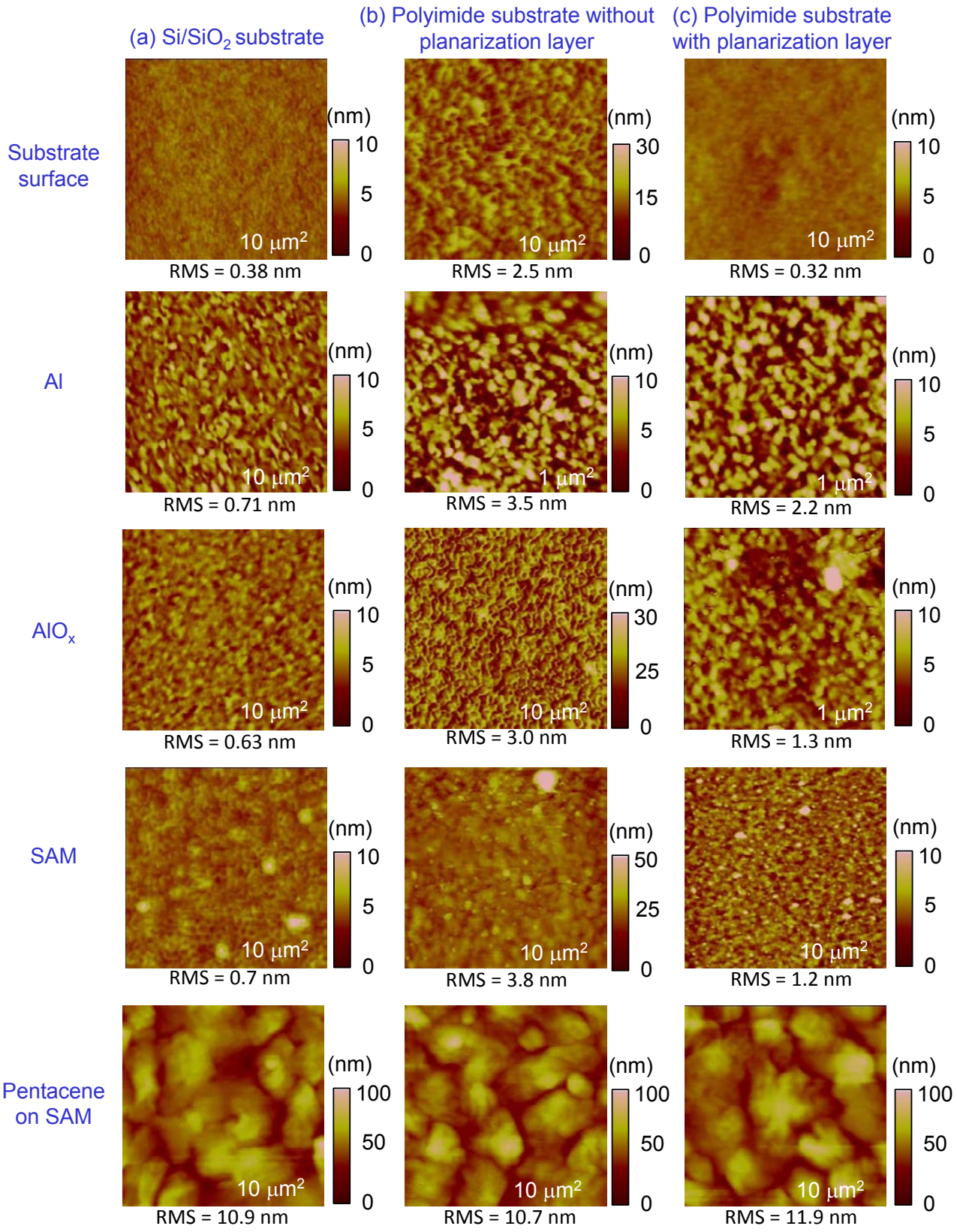


Fig. S1 / T. Sekitani et al.

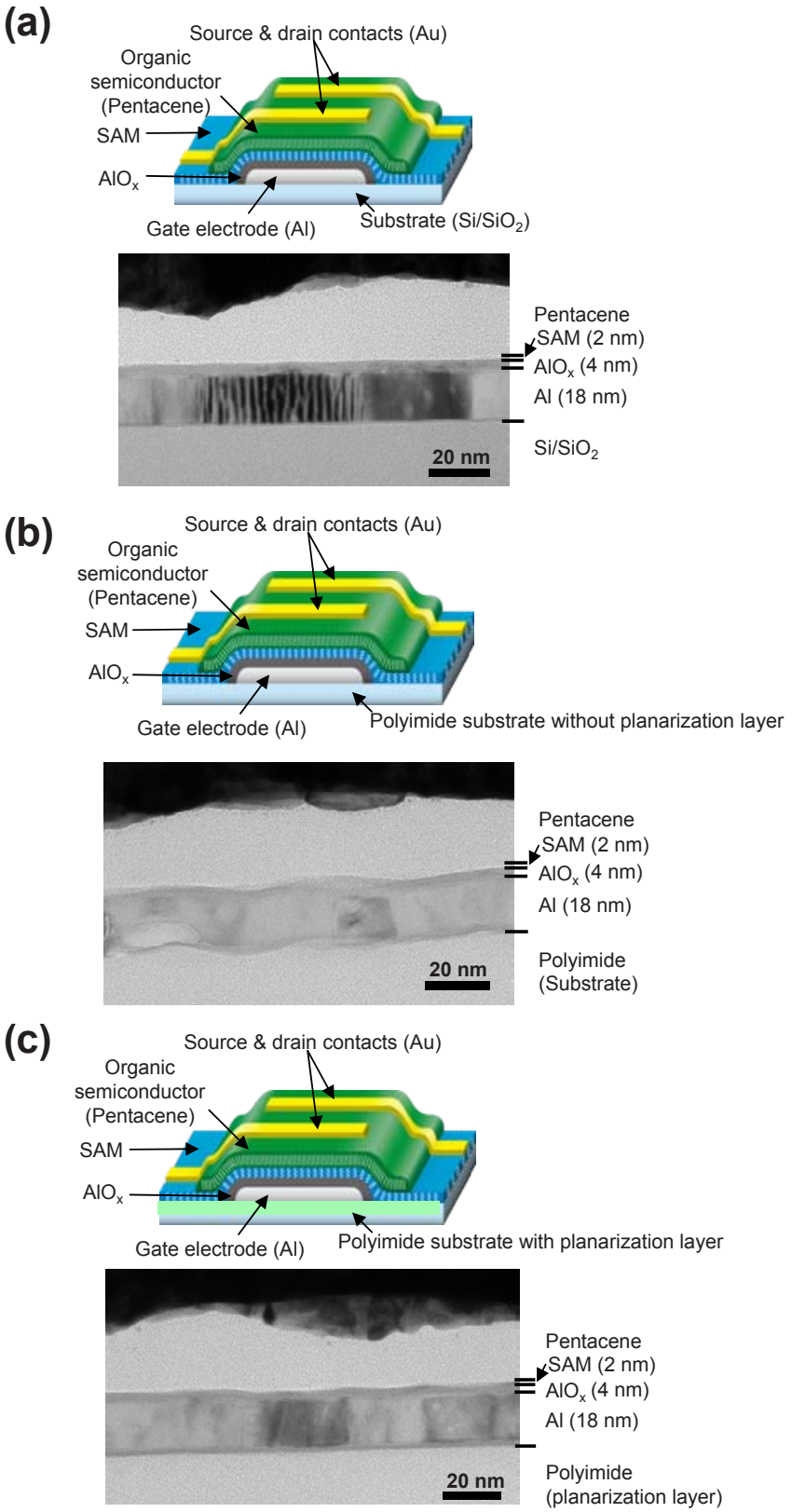


Fig. S2 / T. Sekitani et al.

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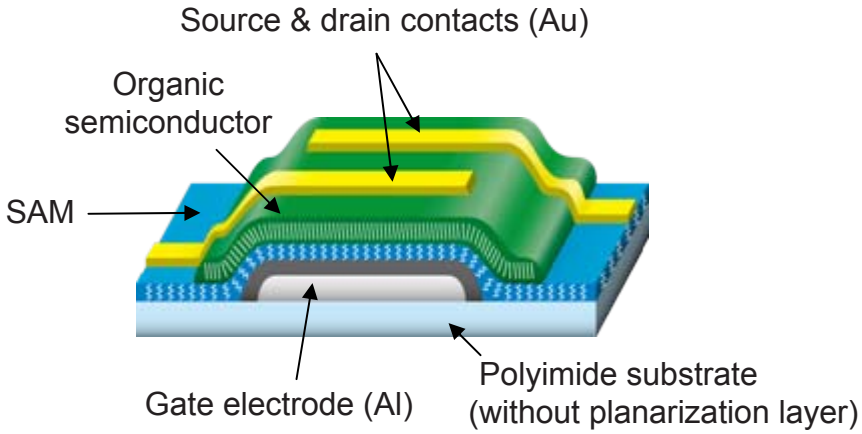


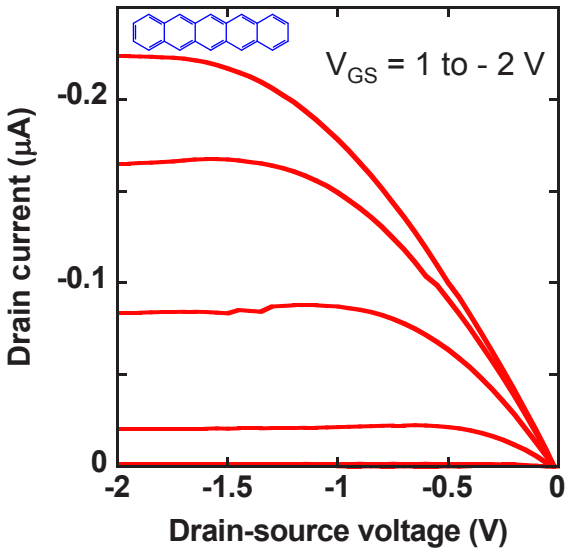


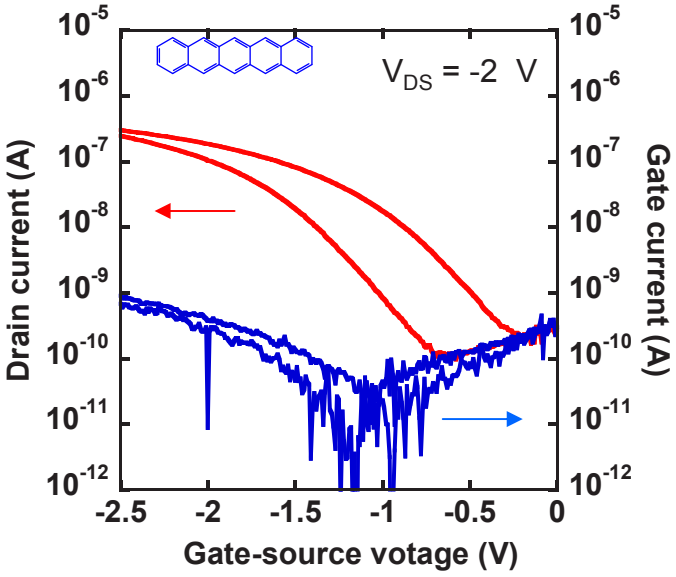


Fig. S3 / T. Sekitani et al.

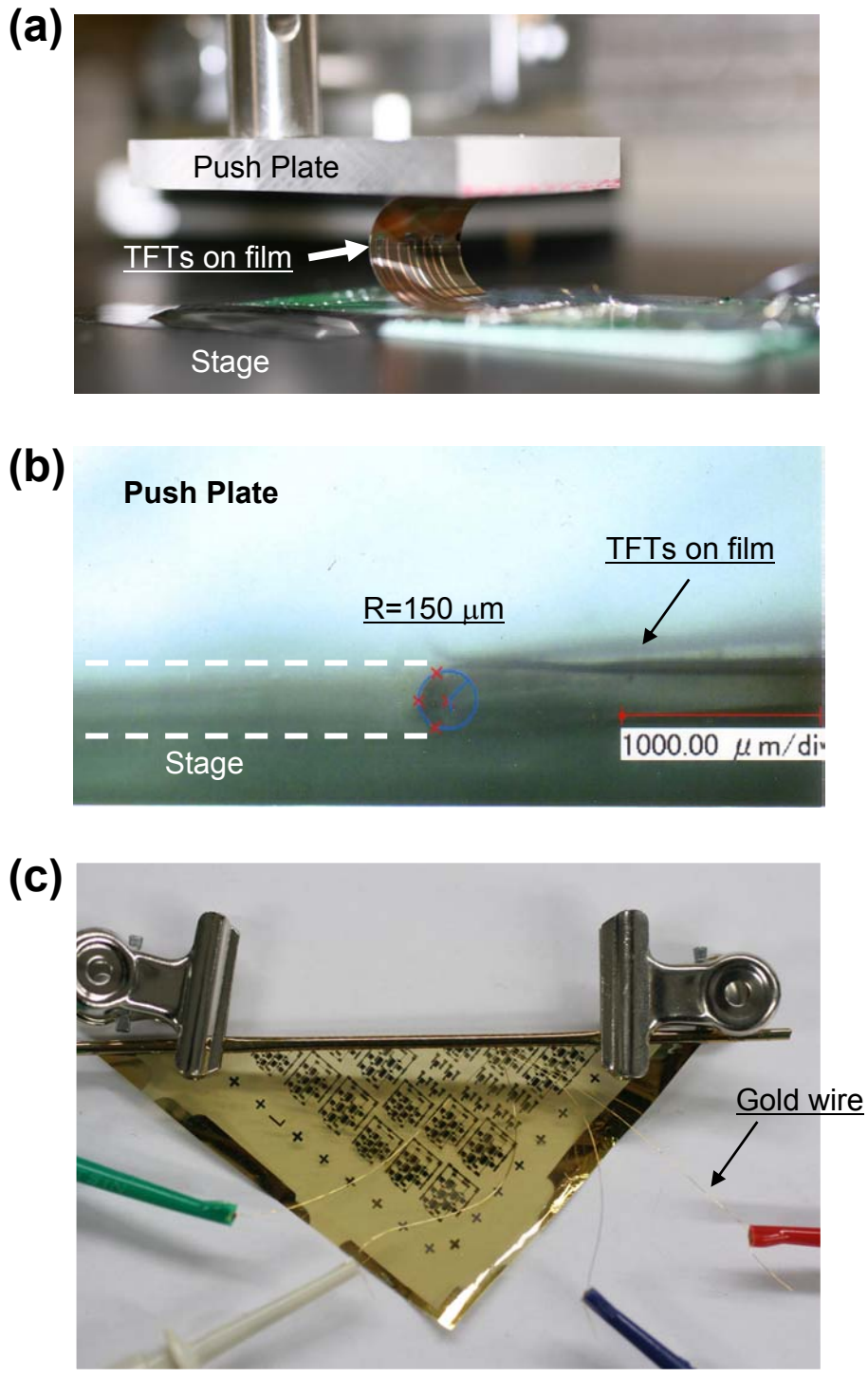


Fig. S4 / T. Sekitani et al.

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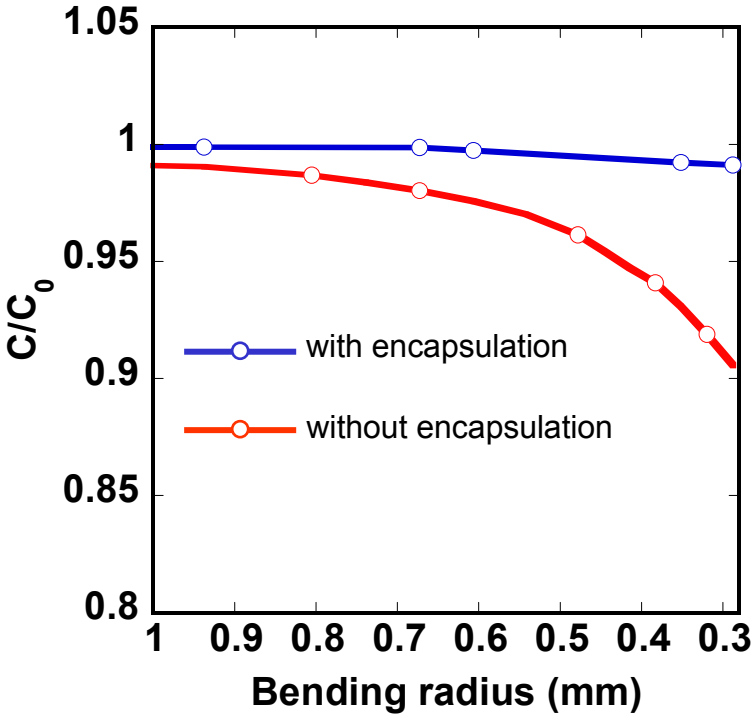
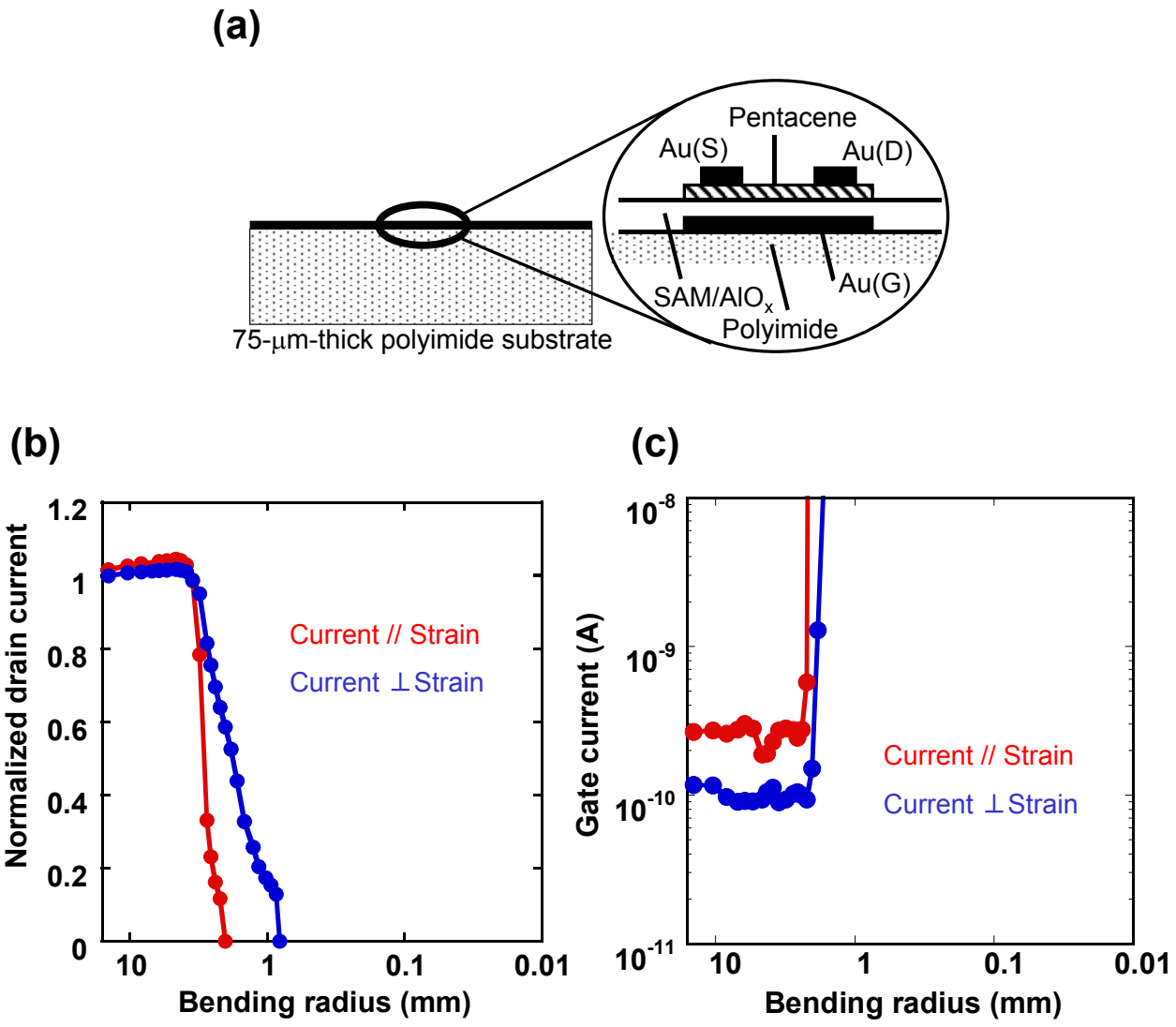



Fig. S5 / T. Sekitani et al.

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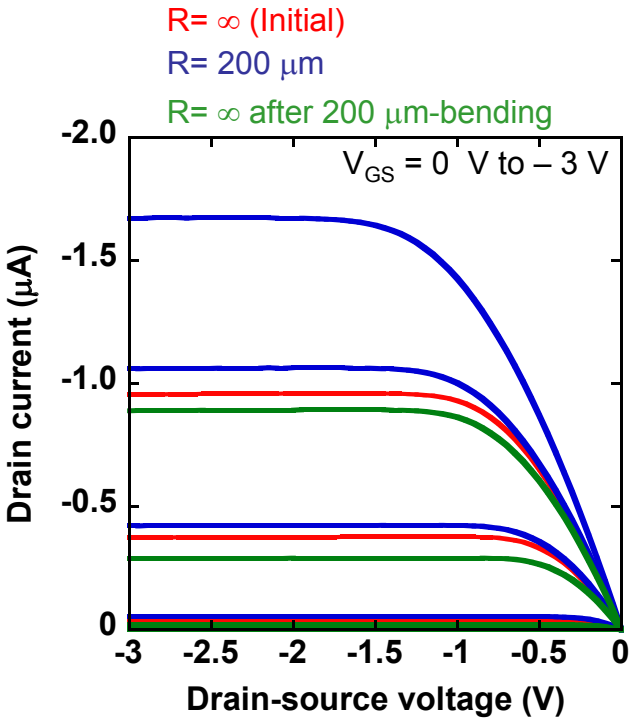


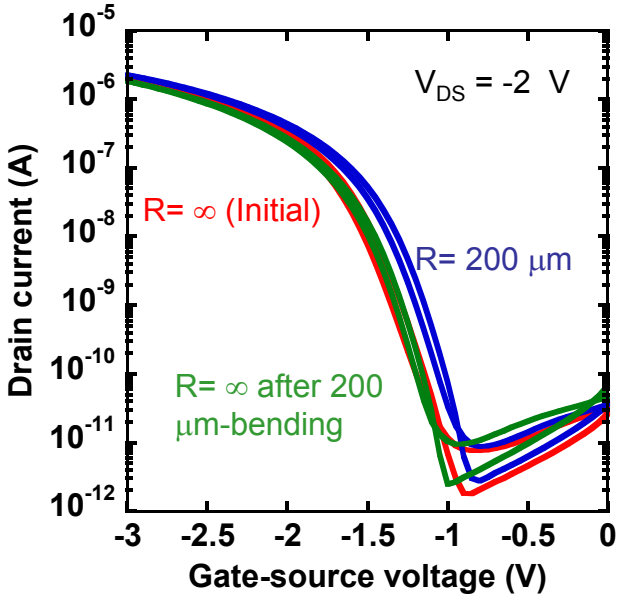


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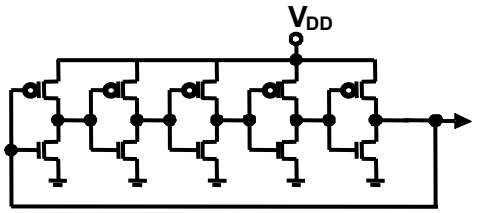
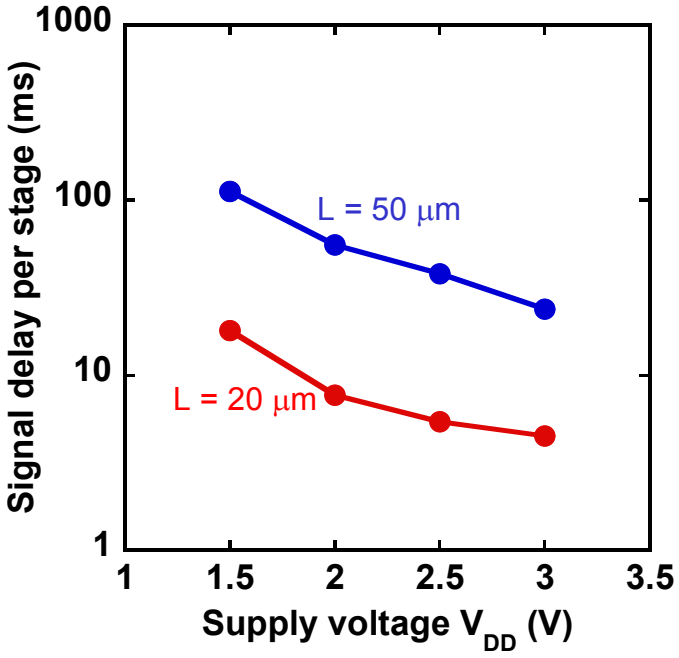
Complementary five stage ring oscillator

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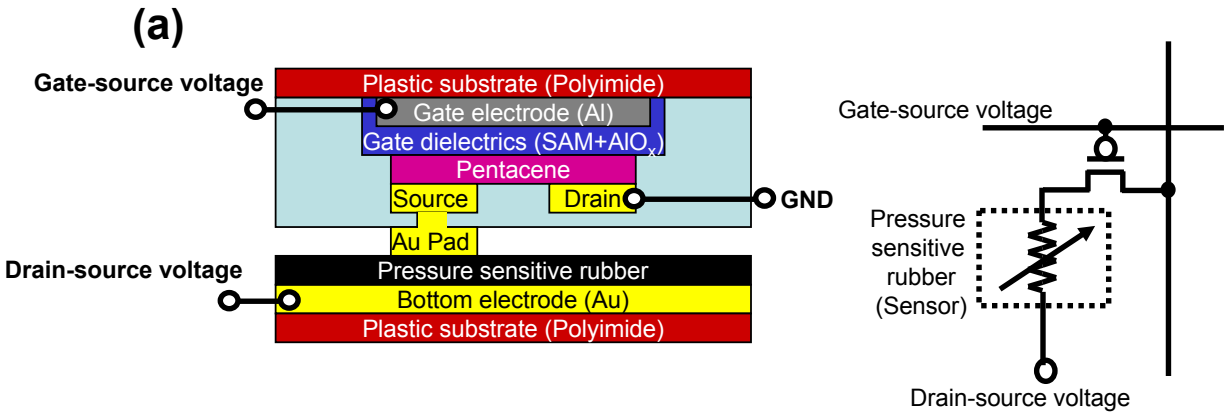


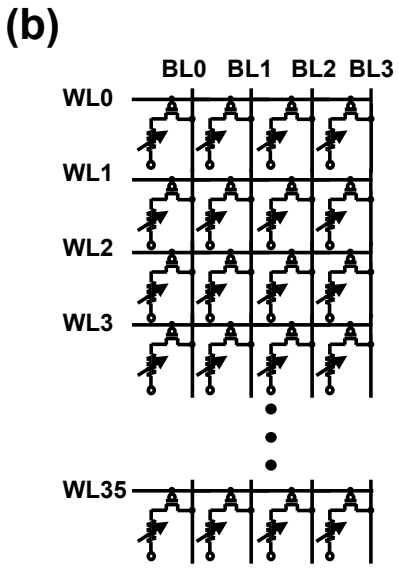


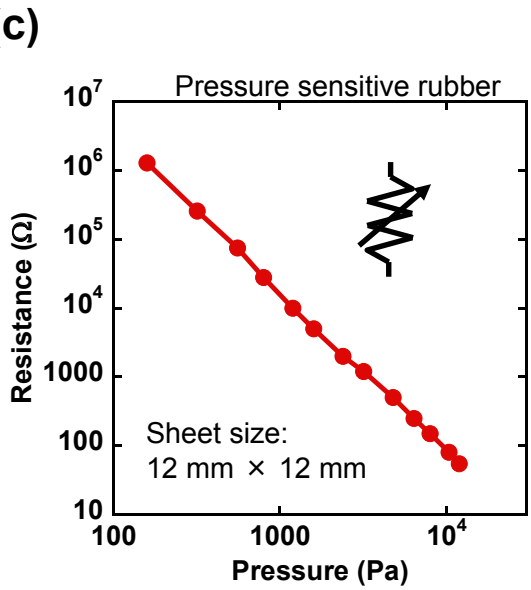


Fig. S9 / T. Sekitani et al.