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COMMUNICATION

Flexible low-voltage organic thin-film transistors and circuits based on C_{10}-DNTT†

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Using the recently developed organic semiconductor, 2,9-didecyldinaphtho[2,3-*b*:2′,3′-*f*]thieno[3,2-*b*]thiophene (C_{10}-DNTT), we have fabricated organic thin-film transistors and ring oscillators on flexible polymeric substrates. By utilizing a gate dielectric with a small thickness (5.3 nm) and a large capacitance (800 nF cm^{-2}), the transistors can be operated with relatively low voltages of about 2 to 3 V. To improve the charge exchange between the organic semiconductor and the gold source and drain contacts, a thin layer of a non-alkylated organic semiconductor (DNTT) sandwiched between two thin layers of a strong organic dopant (NDP-9) was inserted between the C_{10}-DNTT and the gold contacts. The optimized transistors have a field-effect mobility of 4.3 cm^2 V^{-1} s^{-1}, an on/off current ratio of 10^8, and a subthreshold swing of 68 mV per decade. The ring oscillators have a signal propagation delay of 5 μs per stage at a supply voltage of 3 V, making these the fastest organic circuits at supply voltages below 7 V reported to date.

Organic thin-film transistors (TFTs) are of interest for large-area electronics applications, such as flexible active-matrix displays and conformable sensor arrays.[1,2] Among the challenges in the development of high-performance organic TFTs, especially on flexible polymeric substrates, is to simultaneously achieve a large field-effect mobility, a large on/off current ratio, and a steep subthreshold swing.

The largest field-effect mobilities are typically obtained by using organic semiconductors that condense into thin films with a favorable crystal structure and a low defect density, most notably pentacene,[3–6] 2,8-difluoro-5,11-bis(triethylsilylethynyl) anthradithiophene (diF-TESADT),[7] dinaphtho[2,3-*b*:2′,3′-*f*]thieno[3,2-*b*]thiophene (DNTT),[8,9] dialkylbenzothieno[3,2-*b*]benzothiophene (C_8-BTBT, C_{12}-BTBT),[10–12] hexamethylenetetrathiafulvalene (HMTTF),[13] poly[2,6-(4,4-bis-alkyl-4*H*-cyclopenta[2,1-*b*:3,4-*b*′]dithiophene)-*alt*-4,7-(2,1,3-benzothiadiazole)] (CDT-BTZ),[14] dianthra[2,3-*b*:2′,3′-*f*]thieno[3,2-*b*]thiophene (DATT),[15] and 2,9-didecyldinaphtho[2,3-*b*:2′,3′-*f*]thieno[3,2-*b*]thiophene (C_{10}-DNTT),[16,17] all of which have shown field-effect mobilities above 3 cm^2 V^{-1} s^{-1} in thin-film transistors.

A large field-effect mobility will also produce a large on-state drain current, so that achieving a large on/off current ratio then hinges on minimizing the off-state drain current, which requires avoiding charge leakage through the semiconductor, through the gate dielectric, and around the periphery of the TFT. Charge leakage around the periphery of the TFTs can be eliminated by patterning the semiconductor layer[18–20] and by rendering the substrate hydrophobic in order to avoid surface conduction through adsorbed water. Charge leakage through the semiconductor can be minimized by purification of the semiconductor (to eliminate bulk impurities)[21] and by choosing a semiconductor with a large HOMO–LUMO gap (to block the undesired injection of minority carriers from the drain contact).[22]

Avoiding charge leakage through the gate dielectric is straightforward if the gate dielectric is either sufficiently thick (to eliminate direct tunneling and to minimize Fowler–Nordheim tunneling and Ohmic currents) or grown at a sufficiently high temperature (to produce a dense, defect-free insulator). For example, organic TFTs with SiO_2 gate dielectrics grown at temperatures above 800 °C or using spin-coated polymer gate dielectrics with a thickness of several hundred nanometres can have on/off current ratios as large as 10^{10}.[16,19–21,23–25]

However, high process temperatures interfere with the grand goal of manufacturing organic TFTs on commercially available polymeric substrates (which typically have a glass transition temperature below 150 °C), and thick gate dielectrics usually have a rather small capacitance per unit area, which results in a large operating voltage and a poor subthreshold swing. The reason for the latter is that the subthreshold swing is determined by the ratio between the density of trap states at the semiconductor/dielectric interface and the capacitance per unit area of the gate dielectric.[26] Organic TFTs on polymeric substrates that provide low charge leakage, low operating voltages, and a steep subthreshold swing therefore require a gate dielectric that is dense, defect-free, has a large capacitance per unit area, and can be produced at temperatures below about 150 °C. Options include high-permittivity metal oxides, high-permittivity polymers, polyelectrolytes, and ultrathin oxide/monolayer or oxide/multilayer dielectrics.[27]

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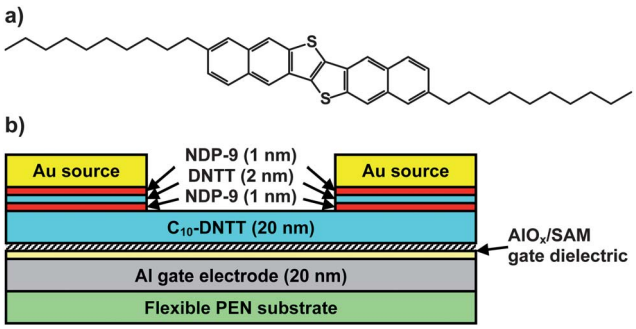

Fig. 1 (a) Chemical structure of the organic semiconductor 2,9-didecyldinaphtho[2,3-*b*:2′,3′-*f*]thieno[3,2-*b*]thiophene (C_{10}-DNTT). (b) Schematic cross-section of the bottom-gate, top-contact (staggered inverted) C_{10}-DNTT transistors with NDP-9/DNTT/NDP-9 contact doping fabricated in this work.

Here we report on bottom-gate, top-contact organic TFTs that have a mobility of 4.3 $cm^2\ V^{-1}\ s^{-1}$, an on/off ratio of 10^8, and a subthreshold swing of 68 mV per decade. The substrate is flexible, transparent polyethylene naphthalate with a thickness of 125 μm (Teonex® Q65 PEN; kindly provided by William A. MacDonald, DuPont Teijin Films, Wilton, UK). Aluminium gate electrodes with a thickness of 20 nm were deposited by thermal evaporation in a vacuum through a polyimide shadow mask (CADiLAC Laser, Hilpoltstein, Germany) and briefly exposed to an oxygen plasma to create a 3.6 nm thick AlO_x film, followed by immersing the substrate in a 2-propanol solution of *n*-tetradecylphosphonic acid to form a 1.7 nm thick self-assembled monolayer (SAM) on the AlO_x surface. The result is a dense AlO_x/SAM gate dielectric with a thickness of 5.3 nm and a capacitance of 800 nF cm^{-2} that allows the TFTs to operate with relatively low voltages of about 2 to 3 V.[28]

A 20 nm thick layer of the organic semiconductor 2,9-didecyldinaphtho[2,3-*b*:2′,3′-*f*]thieno[3,2-*b*]thiophene (C_{10}-DNTT; see Fig. 1a) that was recently developed at Hiroshima University[16,17] and was purified by temperature-gradient sublimation prior to use was then deposited in a vacuum at a substrate temperature of 80 °C and patterned using a shadow mask. Compared with pentacene and DNTT, the decyl substituents in C_{10}-DNTT force the molecules into a tighter packing with enhanced orbital overlap, which creates the possibility for larger carrier mobilities in the plane parallel to the substrate surface.[17] C_{10}-DNTT also has a relatively large HOMO–LUMO gap of almost 3 eV that is beneficial for achieving a small off-state drain current and hence a large on/off ratio.[16,17,28] However, the long aliphatic substituents protruding from the conjugated core of the C_{10}-DNTT molecules also impede the charge transport in the vertical direction and hence the efficient exchange of charge carriers between the C_{10}-DNTT molecules and the Au source and drain contacts located on top of the semiconductor. Strategies to alleviate this effect and provide improved charge exchange, reduced contact resistance and increased effective field-effect mobility include the introduction of area-selective contact doping at the interface between the semiconductor channel and the metal contacts.[29–32] Therefore, a 1 nm thick layer of the strong organic dopant NDP-9 (provided by Novaled, Dresden, Germany),[33] a 2 nm thick layer of the organic semiconductor DNTT,[16,17,28] and another 1 nm thick layer of NDP-9 were sequentially deposited onto the C_{10}-DNTT layer through a shadow mask prior to depositing the Au source and drain contacts through the same shadow mask. By depositing the NDP-9/DNTT/NDP-9 stack and the Au contacts through the same shadow mask, the doping effect is confined to the contact regions of the transistors (see Fig. 1b for a schematic cross-section of the completed TFTs).

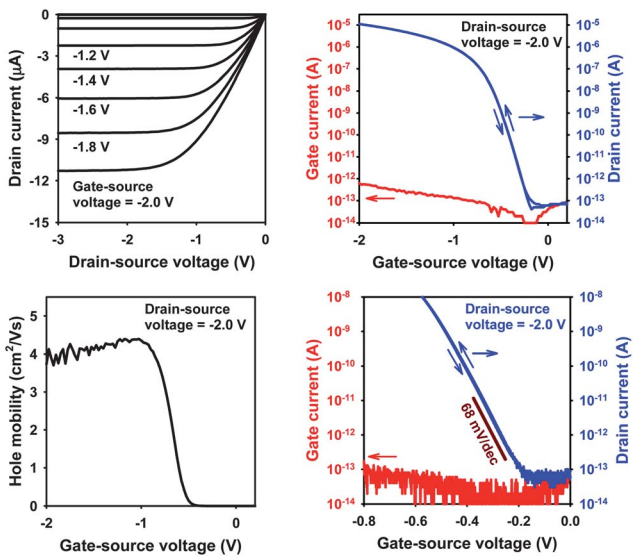

Fig. 2 Electrical characteristics of a flexible C_{10}-DNTT TFT with a channel length of 30 μm and a channel width of 100 μm. The TFT has a field-effect mobility of 4.3 $cm^2\ V^{-1}\ s^{-1}$, a threshold voltage of −0.4 V, an on/off current ratio of 10^8, and a subthreshold swing of 68 mV per decade.

Fig. 2 shows the current–voltage characteristics of a C_{10}-DNTT TFT with NDP-9/DNTT/NDP-9/Au contacts on a flexible PEN substrate. The TFT has a channel length of 30 μm, a channel width of 100 μm, an effective field-effect mobility (measured in the saturation regime) of 4.3 $cm^2\ V^{-1}\ s^{-1}$, a maximum gate current of 0.4 pA, an off-state drain current below 0.1 pA, an on/off current ratio of 10^8, a threshold voltage of −0.4 V, and a subthreshold swing of 68 mV per decade. To our knowledge these are the largest on/off current ratio, the steepest subthreshold swing, and the second-largest field-effect mobility reported for a flexible organic TFT (see Table 1). For organic TFTs fabricated on rigid silicon substrates, Xu *et al.*[40,44] and Li *et al.*[43] have reported even steeper subthreshold swings of 66 and 67 mV per decade, which come even closer to the room-temperature limit of 60 mV per decade. Tan *et al.* have reported a field-effect mobility of 6.4 $cm^2\ V^{-1}\ s^{-1}$ for flexible pentacene TFTs which also operate with low voltages (around 3 V), but which show a somewhat larger off-state drain current (100 pA) that limits the on/off current ratio to 2×10^5.[49]

In addition to C_{10}-DNTT TFTs with NDP-9/DNTT/-NDP-9/Au contacts, we have also fabricated C_{10}-DNTT TFTs without DNTT and without NDP-9, with only DNTT or only NDP-9, and with a double-layer stack of DNTT and NDP-9 inserted between C_{10}-DNTT and Au. The electrical properties of these TFTs are summarized in Table 2. Fig. 3 shows a comparison of the output curves of all five of these TFTs (all having a channel length of 30 μm and a channel width of 100 μm) measured at a single gate-source voltage of −1.8 V. The comparison shows that inserting a triple-layer stack of NDP-9/DNTT/NDP-9 provides the steepest slope in the output curve (*i.e.*, the smallest differential output resistance) in the linear region of operation, indicating that this contact configuration provides the most efficient exchange of charge carriers between the Au contacts and the semiconductor channel.

Table 1 Literature summary of organic TFTs with a subthreshold swing (SS) steeper than 100 mV per decade (ref. 34–44) and of flexible organic TFTs with a field-effect mobility greater than 2 $cm^2\ V^{-1}\ s^{-1}$ (ref. 45–52)

Reference	Substrate	Semiconductor	Gate dielectric	SS/mV dec^{-1}	Mobility/ $cm^2\ V^{-1}\ s^{-1}$	On/off current ratio	Process temp. /°C
34	Silicon	Pentacene	e-Beam-evaporated HfLaO	78	0.7	10^5	350
35	Silicon	Pentacene	Plasma-grown AlO_x/SAM	85	0.3	10^5	60
36	Silicon	DH4T	Thermally grown SiON	77	0.007	2×10^4	n/a
37	Flexible PET	4T-TMS	Polyvinylphenol (PVP)	80	0.2	5×10^4	100
38	Silicon	Pentacene	Cyanoethylated pullulan	89	1.3	10^5	200
39	Silicon	Pentacene	ALD HfLaO/PVP	90	0.3	2×10^5	300
40	Silicon	Pentacene	Cyanoethylated pullulan	66	1.1	3×10^5	200
41	Silicon	Pentacene	Sol–gel HfO_2/SAM	75	0.8	10^7	550
41	Silicon	C_{60}	Sol–gel HfO_2/SAM	95	4.6	10^7	550
42	Flexible PC	TESADT	PEALD AlO_x/polystyrene	85	1.3	10^6	110
43	Silicon	TIPS–pentacene	Thermally grown SiO_2	67	1.5	10^8	800
44	Silicon	Pentacene	Cyanoethylated pullulan	66	5.0	10^5	70
45	Flexible PET	Pentacene	Polyvinyl alcohol (PVA)	400	2.6	2×10^3	70
46	Flexible PET	Pentacene	Sol–gel silica	260	3.0	10^5	100
47	Flexible PET	Pentacene	$BaTiO_2$ nanoparticles	106	3.5	2×10^4	<100
48	Flexible PET	Pentacene	$BaSrTiO_2$ nanoparticles	216	3.4	10^3	<100
49	Flexible PET	Pentacene	Sol–gel silica	160	6.4	2×10^5	100
50	Flexible PEN	C_{60}	ALD AlO_x/polystyrene	300	2.2	10^5	120
51	Flexible PET	Pentacene	PPO–PS blend	2300	3.2	10^8	60
52	Flexible PEN	DNTT	Plasma-grown AlO_x/SAM	100	2.1	10^8	60
This work	Flexible PEN	C_{10}-DNTT	Plasma-grown AlO_x/SAM	68	4.3	10^8	80

Table 2 Summary of the electrical characteristics of flexible C_{10}-DNTT TFTs with five different contact configurations fabricated in this work

Substrate	Semiconductor	Contact structure	SS/mV dec^{-1}	Mobility/ $cm^2\ V^{-1}\ s^{-1}$	On/off current ratio	Threshold voltage/V
Flexible PEN	C_{10}-DNTT	Au	80	2.1	10^8	−0.5
Flexible PEN	C_{10}-DNTT	DNTT/Au	70	3.0	10^8	−0.4
Flexible PEN	C_{10}-DNTT	NDP-9/Au	75	3.7	10^8	−0.4
Flexible PEN	C_{10}-DNTT	DNTT/NDP-9/Au	70	3.7	10^8	−0.4
Flexible PEN	C_{10}-DNTT	NDP-9/DNTT/NDP-9/Au	68	4.3	10^8	−0.4

Fig. 4a illustrates the time-dependent decay of the drain current of a flexible C_{10}-DNTT TFT with NDP-9/DNTT/NDP-9/Au contacts and a channel length of 30 μm during continuous bias stress. The bias-stress test was performed by applying a gate-source voltage and a drain-source voltage of −2 V for a period of 64 hours. Under these bias conditions, the charge-carrier density in the conduction channel is about $8 \times 10^{12}\ cm^{-2}$ and the sheet resistance of the channel is about 600 kΩ sq^{-1}.[52] As can be seen, 64 hours of continuous bias stress under these conditions lead to a decay of the drain current by about 30%, which is similar to the bias-stress stability of hydrogenated amorphous silicon TFTs fabricated with a maximum process temperature of 285 °C,[53,54] despite the fact that our C_{10}-DNTT TFTs were fabricated at a much lower temperature of 80 °C. A 30% decay of the drain current corresponds to a threshold-voltage shift of 50 mV in our TFTs. Fig. 4b documents the shelf-life stability of a flexible C_{10}-DNTT TFT with NDP-9/DNTT/NDP-9/Au contacts and

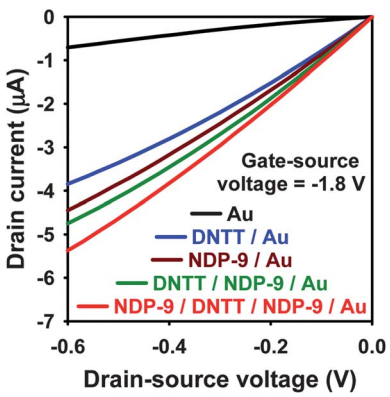

Fig. 3 Output curves measured at a single gate-source voltage of −1.8 V of five C_{10}-DNTT TFTs with different contact configurations (Au; DNTT/Au; NDP-9/Au; DNTT/NDP-9/Au; NDP-9/DNTT/NDP-9/Au). All five TFTs were fabricated on PEN substrates with the same gate dielectric (AlO_x/SAM) and the same channel length (30 μm) and channel width (100 μm).

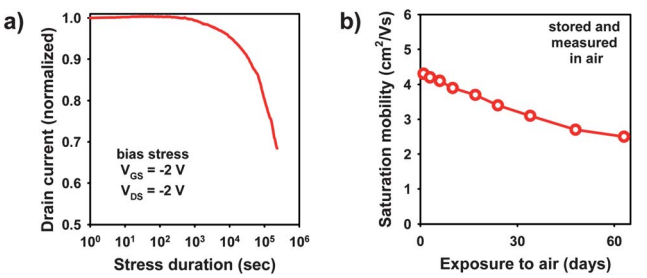

Fig. 4 (a) Bias-stress stability of a C_{10}-DNTT TFT with NDP-9/DNTT/NDP-9/Au contacts (channel length 30 μm and channel width 100 μm). (b) Shelf-life stability of a C_{10}-DNTT TFT with NDP-9/DNTT/NDP-9/Au contacts (channel length 30 μm and channel width 100 μm).

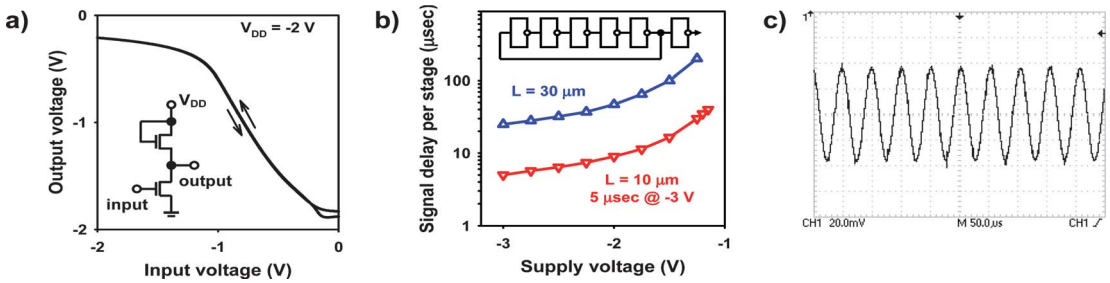

Fig. 5 (a) Static transfer characteristics of an inverter with saturated load based on C_{10}-DNTT TFTs on a flexible PEN substrate. (b) Signal propagation delay as a function of supply voltage of flexible 5-stage ring oscillators based on C_{10}-DNTT TFTs with channel lengths of 30 µm and 10 µm. (c) Output voltage of a flexible 5-stage ring oscillator based on C_{10}-DNTT TFTs with a channel length of 10 µm measured at a supply voltage of −3 V. For the measurements, the output node of the integrated buffer inverter (which has the same dimensions as the five inverters within the ring oscillator) was connected with a BNC cable to a high-input-impedance, unity-gain voltage buffer, the output of which was connected to an oscilloscope.

a channel length of 30 µm. As can be seen, the measured field-effect mobility remains well above 2 $cm^2\ V^{-1}\ s^{-1}$ after two months of continuous exposure to air with a humidity of about 50%.

To evaluate the dynamic performance of the flexible C_{10}-DNTT TFTs we have designed and fabricated 5-stage ring oscillators composed of unipolar inverters based on a saturated-load design. The circuit schematic and the static transfer characteristics of such an inverter are shown in Fig. 5a. Fig. 5b shows the signal propagation delay per stage as a function of the supply voltage measured for flexible ring oscillators with two different design rules. When the TFTs have a channel length of 30 µm and a gate-to-contact overlap of 30 µm, the signal delay measured at a supply voltage of −3 V is 25 µs per stage (blue datapoints in Fig. 5b), whereas when the TFTs have a channel length of 10 µm and a gate-to-contact overlap of 15 µm (which are the smallest lateral dimensions attainable with our polyimide shadow masks), the signal delay measured at a supply voltage of −3 V is 5 µs per stage (red datapoints in Fig. 5b). Although this is more than an order of magnitude slower than the signal delay recently reported by Myny *et al.* for flexible ring oscillators based on pentacene TFTs with a 100 nm thick sputtered Al_2O_3/SAM gate dielectric and a channel length of 2 µm,[55] it is the shortest signal delay reported for an organic ring oscillator at supply voltages below 7 V. Signal delays below 1 µs per stage at a supply voltage of 3 V are projected for a design rule of 5 µm realized by means of high-resolution stencil masks.[56]

In summary, we have fabricated low-voltage organic thin-film transistors and ring oscillators with record static and dynamic performance on flexible polymeric substrates. The devices utilize the recently developed high-mobility organic semiconductor 2,9-didecyldinaphtho[2,3-*b*:2′,3′-*f*]thieno[3,2-*b*]thiophene (C_{10}-DNTT), a high-capacitance gate dielectric based on an alkylphosphonic acid self-assembled monolayer, and area-selective contact doping using a strong organic molecular dopant to improve the exchange of charge carriers between the semiconductor channel and the gold source and drain contacts. The transistors have a carrier mobility of 4.3 $cm^2\ V^{-1}\ s^{-1}$, an on/off current ratio of 10^8, a subthreshold swing of 68 mV per decade, and a signal propagation delay of 5 µs per stage at a supply voltage of 3 V.

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