

Integrated Circuits using Top-Gate ZnO Nanowire Transistors with Ultrathin Organic Gate Dielectric

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Abstract

We report on field-effect transistors based on single-crystalline ZnO nanowires with a diameter of about 50 nm grown by wet-chemical synthesis. The as-grown nanowires have a large conductivity that makes it difficult to control the drain current with the gate field, but the conductivity is greatly reduced by a post-growth anneal at 600 °C. Using a solution-processed organic gate dielectric with a thickness of 2.1 nm and overlapping metal top gate electrodes patterned by electron-beam lithography we have prepared nanowire transistors with good static performance. By patterning more than one transistor on the same nanowire we have also prepared simple logic circuits on a single nanowire.

Introduction

Nanowire field-effect transistors (FETs) hold great promise for high-density circuits and memory arrays (1), and to replace thin-film transistors (TFTs) in active-matrix displays where the larger

carrier mobility and smaller footprint of nanowire FETs compared with a-Si:H and organic TFTs may provide faster pixel charging and larger aperture ratio (2). The synthesis of single-crystalline semiconductor nanowires often requires high temperatures, but the nanowires can usually be synthesized on a temperature-compatible growth substrate and then be transferred to the target substrate for FET assembly. If the temperature during FET manufacturing is below ~150 °C, high-mobility nanoscale FETs can therefore be realized on polymeric substrates for flexible active-matrix displays or integrated circuits.

Nanowire Synthesis and Characterization

The ZnO nanowires were grown by hydrothermal synthesis in an autoclave at a temperature of 150 °C in an aqueous solution of sodium hydroxide and ammonium peroxodisulfate, using zinc foil as the growth substrate (3). Fig. 1a shows a scanning electron microscope image of the nanowires. The crystallinity of the nanowires was confirmed by high-resolution transmission electron microscopy (Fig. 1b). To measure the electrical conductivity of the ZnO nanowires, they were removed from the zinc foil by sonication in 2-propanol and dispersed on a heavily doped, thermally oxidized silicon substrate. Aluminum source/drain contacts were defined by electron-beam lithography. As Fig. 2a shows, the as-grown ZnO nanowires have a large electrical conductivity that makes it difficult to modulate the drain current with the electric field from the silicon back gate. The large conductivity is believed to be due to dopants incorporated into the ZnO nanowires during hydrothermal growth.

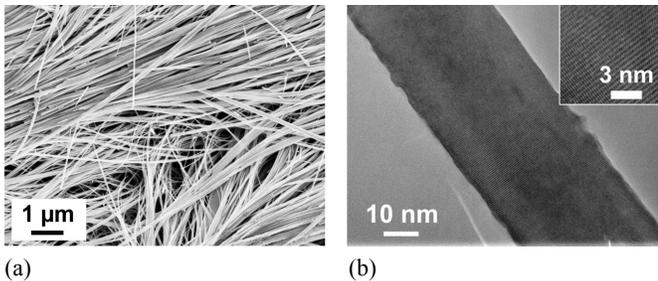


Fig. 1. (a) Scanning electron microscope (SEM) image of hydrothermally grown ZnO nanowires.
(b) High-resolution transmission electron microscope (HRTEM) image of a single ZnO nanowire, showing the high degree of crystallinity of the solution-grown ZnO nanowires.

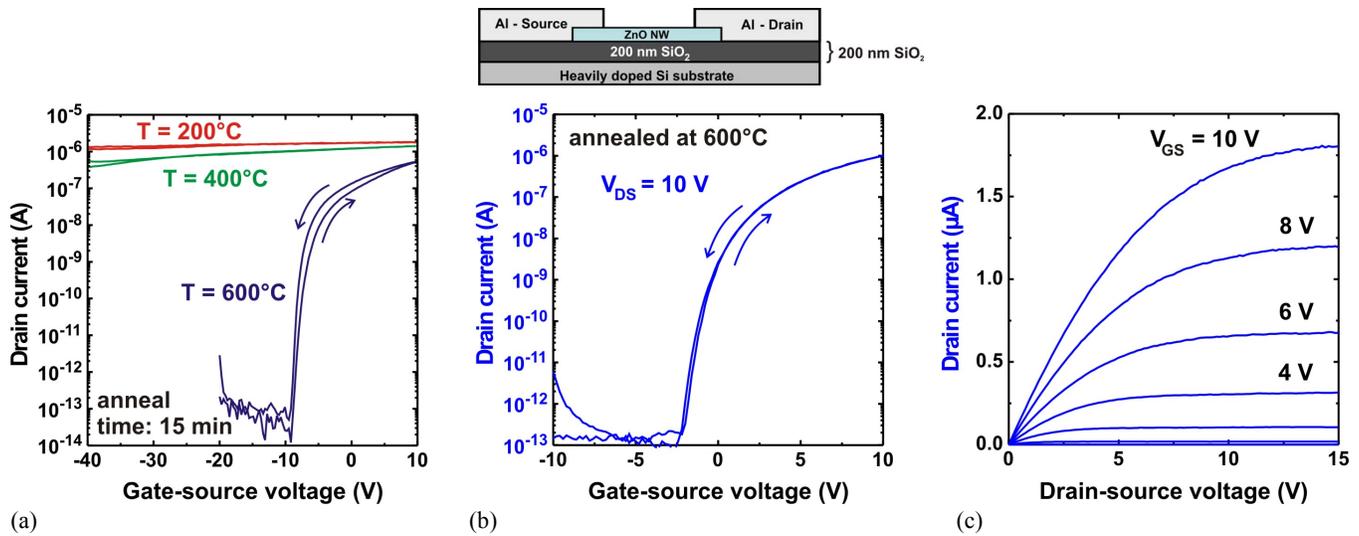


Fig. 2. (a) Transfer characteristics of FETs using ZnO nanowires annealed at different temperatures. (b), (c) Characteristics of an FET on a heavily doped, oxidized Si substrate (back gate) using a ZnO nanowire annealed at 600°C.

Fig. 2a shows that these dopants can be removed by annealing the ZnO nanowires at a temperature of 600 °C in air. Silicon-back-gated FETs based on ZnO nanowires annealed at 600 °C have excellent

electrical characteristics, including negligible off-state drain current (<1 pA), an on/off current ratio of 10^7 , and an electron mobility of about $50 \text{ cm}^2/\text{Vs}$ (see Fig. 2b and 2c).

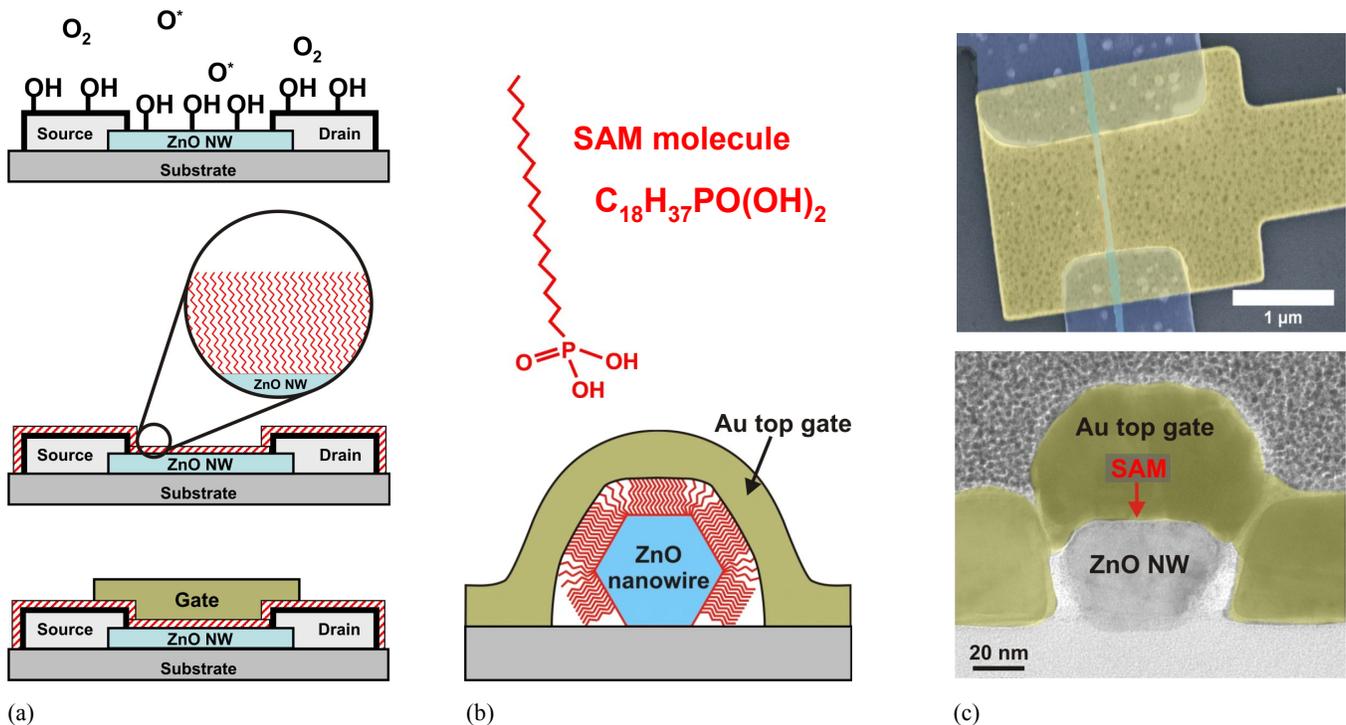


Fig. 3. (a) Fabrication of top-gate FETs. ZnO nanowires with Al S/D contacts are exposed to an O_2 plasma to clean the ZnO and Al surfaces and increase the density of hydroxyl groups necessary for adsorption of the molecules forming the self-assembled monolayer (SAM) gate dielectric. The SAM is prepared from solution. Au top gates are patterned by electron-beam lithography. (b) Schematic cross section of the channel region of a top-gate ZnO nanowire FET, showing the SAM gate dielectric and the gold top gate. The molecular structure of the molecule (octadecylphosphonic acid) is also shown. (c) TEM image of the channel cross-section, and SEM image of a top-gate ZnO nanowire FET.

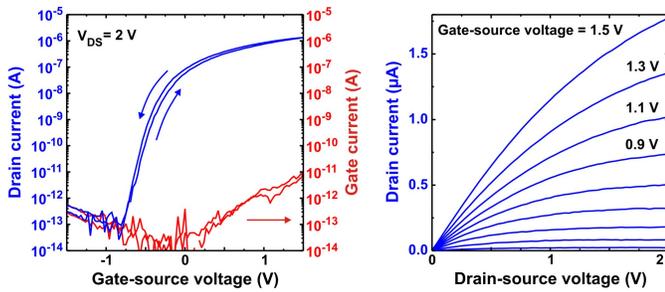


Fig. 4. Transfer and output characteristics of a top-gate FET with a channel length of 2 μm , based on a ZnO nanowire with a diameter of 50 nm. The transistor has an on/off current ratio of about 10^7 , a transconductance of 1 μS , and a steep subthreshold swing of 90 mV/decade.

Top-Gate ZnO Nanowire Transistors

To prepare low-voltage top-gate nanowire FETs and circuits, the substrate is briefly exposed to an oxygen plasma and then immersed in a 2-propanol solution of n-octadecylphosphonic acid, allowing a densely packed monolayer to self-assemble on the surfaces of the ZnO nanowires and of the Al source/drain contacts. This 2.1 nm thick organic self-assembled monolayer (SAM) serves as the gate dielectric. Using electron-beam lithography, Au top gates that overlap the source/drain contacts by a few tens of nanometers are defined (Fig. 3). The maximum process temperature is 160 $^{\circ}\text{C}$ to bake the resist.

Fig. 4 shows the characteristics of a top-gate ZnO nanowire FET with a channel length of 2 μm . The

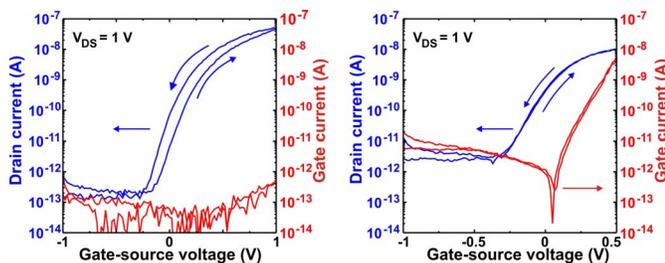


Fig. 5. Comparison between a top-gate FET with SAM gate dielectric (left graph) and without SAM gate dielectric (right graph), confirming the insulating properties of the SAM. The FET with SAM gate dielectric has a very small gate current (MISFET), while the FET without SAM has a large gate current (MESFET).

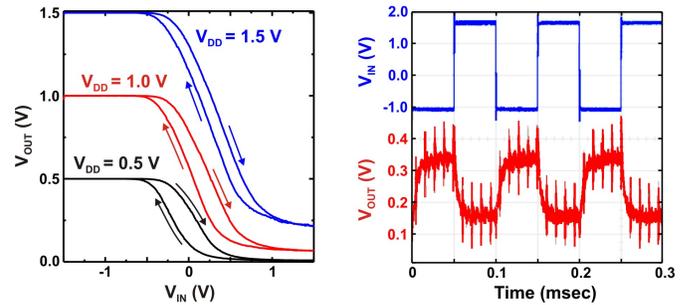
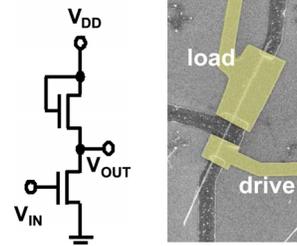


Fig. 6. Circuit schematic, SEM image, and static and dynamic characteristics of a unipolar nMOS inverter with saturated load fabricated on a single ZnO nanowire.

FET operates with gate-source and drain-source voltages of 1 to 2 V and has a transconductance of 1 μS , an on/off ratio of 10^7 , a subthreshold swing of 90 mV/decade, and an off-state drain current of less than 1 pA. Despite the small thickness of the gate dielectric, the maximum gate current is below 10 pA. For comparison, we have also prepared FETs without the SAM dielectric; these devices behave like Schottky-gate MESFETs with much larger gate currents (5 nA at $V_{\text{GS}} = 0.5 \text{ V}$; Fig. 5). This confirms the insulating properties of the low-temperature organic monolayer.

Many of the ZnO nanowires are sufficiently long so that several FETs can be defined on each nanowire, allowing the fabrication of logic circuits on a single nanowire. An example of an nMOS inverter with saturated load on a 10 μm long ZnO nanowire is shown in Fig. 6. The maximum small-signal gain of this inverter is about 2. Due to the fact that the threshold voltage of the FETs is very close to zero, a slightly negative input voltage is required to obtain a clean positive output signal. This means that the input and output levels of the inverter do not match, i.e. these inverters cannot be cascaded.

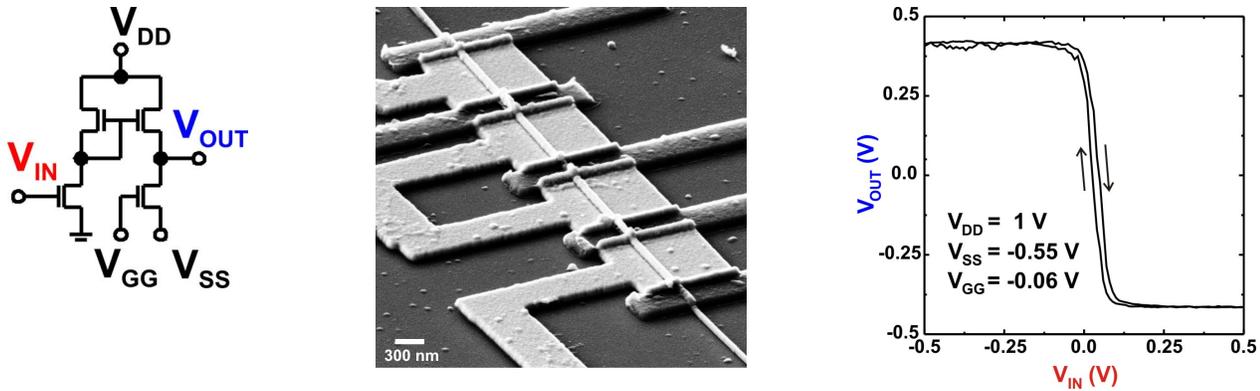


Fig. 7. Circuit schematic, SEM image, and static transfer characteristics of a unipolar nMOS inverter with integrated level-shift stage realized on a single ZnO nanowire. Due to the level-shift stage, the inverter shows matching input and output levels and a large small-signal gain (~ 12).

To obtain better small-signal gain and allow cascading of logic gates, we have designed and manufactured nanowire inverters with an integrated level-shift stage. The level-shift stage adjusts the output levels to make them compatible with the input levels (4). Fig. 7 shows an nMOS inverter with level shifting on a $12\ \mu\text{m}$ long ZnO nanowire. All four FETs of the circuit have a channel length of $1\ \mu\text{m}$ and were prepared on the same nanowire. The small-signal gain of the inverter with level-shifting is about 12. Because the input and output voltages are identical, these inverters can be cascaded. Fig. 8 shows that when two inverters with integrated level-shift stage are cascaded, a small-signal gain of 35 (Fig. 8b) and a large-signal gain of 9 (Fig. 8c) are obtained.

The maximum switching frequency of our ZnO nanowire inverters is about 10 kHz (see Fig. 6). This frequency is limited by the parasitic capacitance that results from the large overlap area between the probe pads and the doped Si substrate. Based on the transconductance ($1\ \mu\text{S}$) and the gate capacitance ($\sim 2\ \text{fF}$) of the top-gate nanowire FETs, a cutoff frequency near 100 MHz is projected for FETs on insulating glass substrates.

- (1) A. Javey et al., *Nano Lett.* **2007**, 7, 773
- (2) S. Ju et al., *Nano Lett.* **2008**, 8, 997
- (3) C. Lu et al., *Chem. Comm.* **2006**, 3551
- (4) H. Klauk et al., *Appl. Phys. Lett.* **2003**, 82, 4175

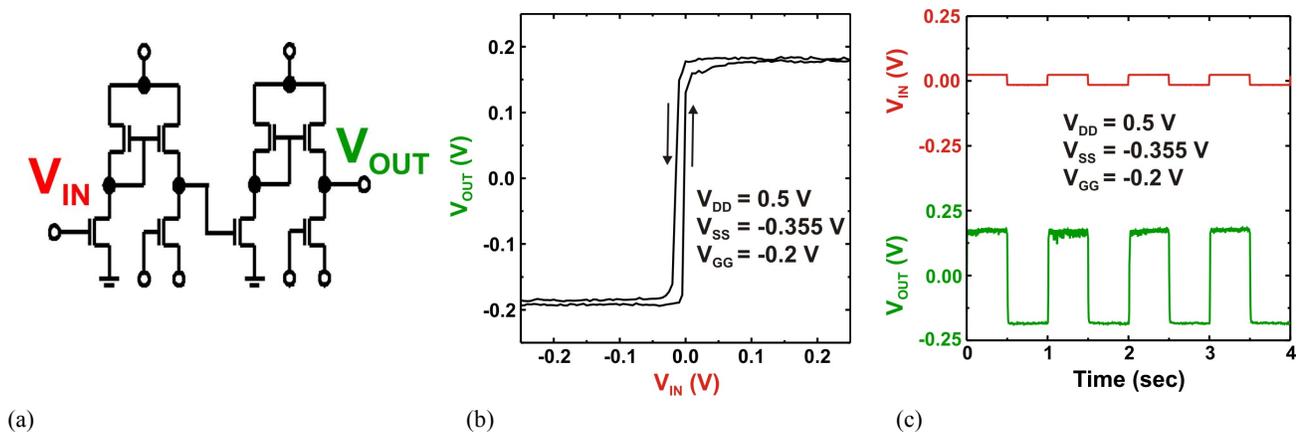


Fig. 8. (a) Circuit schematic of two cascaded inverters with level-shift stage. (b) Static transfer characteristics of the two cascaded inverters, showing a small-signal gain of 35. (c) Dynamic transfer characteristics of the two cascaded inverters, showing that a large-signal gain of 9 is obtained.