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Polymer-electrolyte gated graphene transistors for analog and digital phase detection

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We present an alternating current (ac) circuit based on a misoriented bilayer graphene device for analog and digital phase detection. We exploit the ambipolar nature of the transfer characteristics of a misoriented bilayer graphene transistor. The transistor action here is realized using an electrochemical gate integrated into a solid polymer electrolyte layer. This unique combination provides a voltage gain close to unity under ambient conditions, which is one order of magnitude higher than that attainable in back-gated devices. The achieved gain provides sufficient sensitivity to detect phase differences between pairs of analog or digital signals. © *2011 American Institute of Physics*. [doi:10.1063/1.3615247]

Graphene is emerging as an active element in a number of nanoscale electronic devices. Numerous types of graphene devices in a field-effect transistor (FET) configuration[1,2] have already been demonstrated including graphene logic gates,[3] integrated digital inverters,[4] and digital memories.[5] However, for direct current (dc) circuits, the field effect achievable in monolayer graphene devices is quite low. State-of-the-art graphene FETs suffer from a very low voltage gain of 0.04 when operated at room temperature.[3,4] On the other hand, the high mobility of these devices has motivated the realization of devices deployable in ac circuits and in high frequency applications. Typical examples include binary phase-shift keying modulators[6] and analog frequency doublers.[7] Here, we demonstrate the realization of analog and digital phase shift detectors, which are the basic building blocks of phase-locked loops, one of the most important electronic circuits in communication technologies.[8] For this purpose, we deploy misoriented bilayer graphene as the active material and make use of its ambipolar transport characteristics.[9] The top layer of misoriented bilayers is effectively decoupled from the substrate. Using a solid polymer electrolyte (SPE) as gate dielectric, we can tune the conductivity of the upper layer.[10–13] In this manner, we attain a gain more than 1 using a simple fabrication procedure at room temperature. While a gain of more than unity provides a high sensitivity for phase shift detection, it is a prerequisite for the realization of an amplifier. Gain larger than unity was only recently reported for graphene monolayer[14] and bilayer[15] FETs with an ultra-thin dielectric in a top-gating configuration at cryogenic temperatures.

Figures 1(a) and 1(b) show a schematic representation and an atomic force microscopy (AFM) image of the graphene FET comprised of a misoriented bilayer graphene with Ti/Au electrodes on top. The bilayer was obtained using the mechanical exfoliation technique[16] and then identified using AFM and Raman spectroscopy.[17] The identification of misoriented bilayers is well-documented[10,11,18] and it has been shown previously that the misorientation electronically decouples the two graphene layers. The bottom layer acts as a pseudosubstrate, which electrostatically screens the top layer from the substrate, and thus, imparting enhanced carrier mobility ($\sim 10^4$ cm^2 V^{-1} s^{-1} in our samples at low carrier densities).[11] A SPE is employed as the gate dielectric and a silver wire immersed in the SPE layer is used to efficiently gate[11,19,20] the decoupled upper layer in the bilayer. It consists of polyethylene oxide and lithium hexafluorophosphate ($LiPF_6$) (20:7 weight ratio) in a 4:1 methanol/water mixture and was drop-cast on top of the conducting channel.

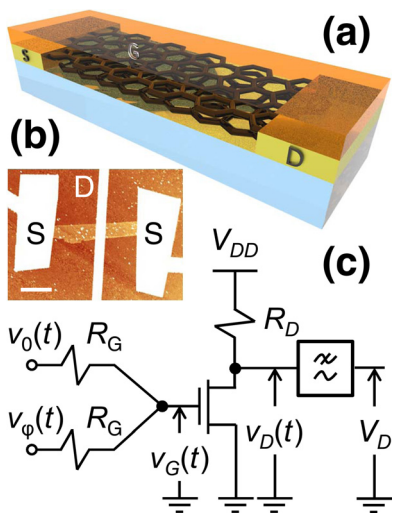

FIG. 1. (Color online) A misoriented bilayer graphene phase detector. (a) A schematic of a misoriented bilayer graphene FET with a polymer electrolyte gate. (b) An AFM image of two misoriented graphene FETs (only one of them is used in phase detection). The scale bar is 2 μm. (c) A circuit diagram of the phase detector comprised of a graphene FET, three off-chip resistors ($R_G = 100\ \Omega$ and $R_D = 2.8$ kΩ), and a low-pass filter. The power supply is $V_{DD} = 1$ V.

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Figure 1(c) shows the electronic equivalent circuit for phase detection. One electrode acts as the drain (D) connected to an external power supply V_{DD} via an off-chip pull-up resistor R_D. The other electrode acts as the source (S) which is grounded; the third electrode in Fig. 1(b) is not used. The input voltages are supplied through two off-chip resistors R_G to the SPE gate (G). The output dc voltage V_D is taken from the output of the low-pass filter which filters the drain voltage v_D. All measurements were performed under ambient conditions.

Figure 2 shows a drain voltage v_D vs. gate voltage v_G transfer curve measured with the circuit shown in Fig. 1(c). Phase detection is based on the symmetry and nonlinearity of the transfer curve in the vicinity of the charge-neutrality point (CNP). Reference v_0 and phase shifted v_φ signals are connected to the two inputs of the detector resulting in the gate voltage $v_G = (v_0 + v_\varphi)/2$. In order to detect the phase difference between the signals, the input signals must be biased at the CNP. For analog phase detection, the input signals are then given by $v_0(t) = V_{GCNP} + V_0 \sin\omega t$ and $v_\varphi(t) = V_{GCNP} + V_0 \sin(\omega t + \varphi)$, where V_{GCNP} is the gate voltage at the CNP, φ is the phase difference between the signals, V_0 their amplitude, and $f = \omega/(2\pi)$ is the signal frequency. This yields a gate voltage $v_G(t) = V_{GCNP} + V_0 \cos(\varphi/2)\sin(\omega t + \varphi/2)$, i.e., the gate voltage is also biased at the CNP with an amplitude of the ac component $\propto \cos(\varphi/2)$. A larger phase φ results in a smaller ac amplitude of the gate voltage. Since the transfer curve decreases on both sides of the CNP, decreasing the ac amplitude of the gate voltage increases the minimum of the drain voltage v_D while the maximum remains constant, and this increases the dc offset V_D of the drain voltage. The dependence of the output dc component V_D on the phase difference φ can be derived by approximating the transfer curve as a second-order Taylor series $v_D - V_{DCNP} = -k(v_G - V_{GCNP})^2$. This is valid for small voltages $|v_G - V_{GCNP}|$ (i.e., small amplitudes V_0), where V_{DCNP} is the drain voltage at the CNP and k is a positive constant. The drain voltage is then $v_D(t) = V_D + (kV_0^2/4)(1 + \cos\varphi)\cos(2\omega t + \varphi)$, which has an ac component at a frequency $2f$ that was recently utilized in frequency doublers.[7] The dc component of the drain voltage is $V_D = V_{DCNP} - (kV_0^2/4)(1 + \cos\varphi) \propto -\cos\varphi$,

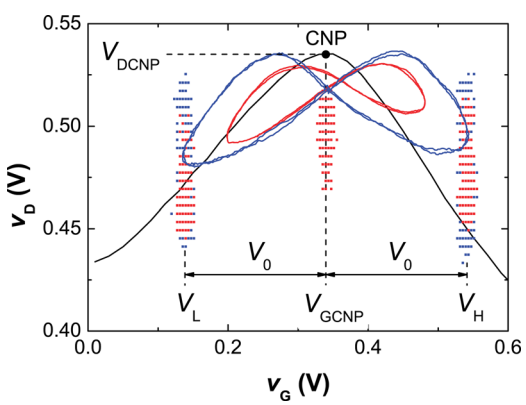

FIG. 2. (Color online) Transfer curves of the circuit shown in Fig. 1(c): static (dc) curve (black line) and dynamic (ac) curves (blue and red lines/scatter). Blue plots correspond to a phase difference of $\varphi = 0°$, while red plots correspond to $\varphi = 90°$. The lines correspond to analog signals (see Fig. 3(a)), while the scatter corresponds to digital signals (see Fig. 3(b)). $V_0 = 200$ mV is the amplitude of the input signals which are offset at the CNP.

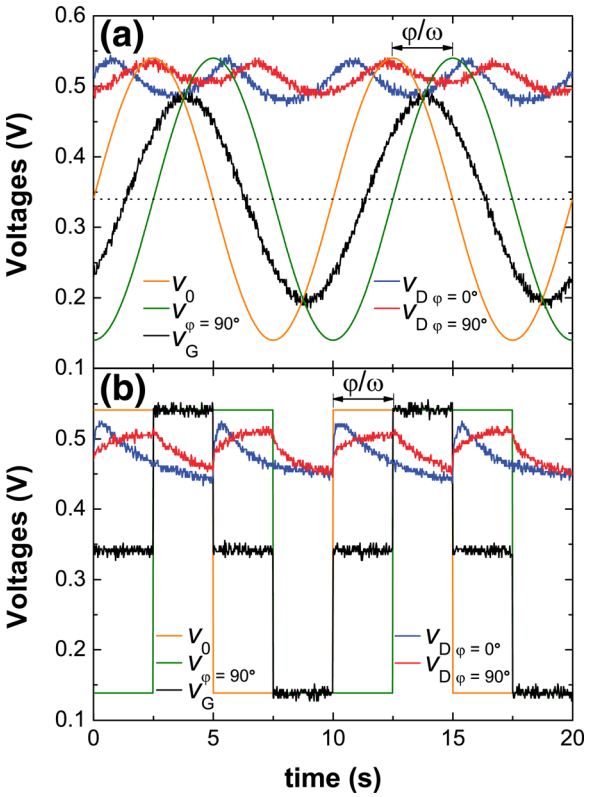

FIG. 3. (Color online) Input and output signals measured with the graphene phase detector at a frequency $f = 100$ mHz. Reference input signal $v_0(t)$ (orange), phase-shifted input signal $v_\varphi(t)$ for the case $\varphi = 90°$ (green), measured gate voltage $v_G(t)$ for the case $\varphi = 90°$ (black), and measured drain voltages $v_D(t)$ for the case of no phase shift ($\varphi = 0°$) between the inputs (blue) and for the case $\varphi = 90°$ (red). (a) Analog and (b) digital phase detection.

and it carries the information about the phase shift between the input signals.

Figure 3(a) shows drain voltage waveforms measured with the analog graphene phase detector in the case of phase shifts of 0° and 90°. It is apparent that the drain voltage has a comparatively larger dc component V_D for the latter case. Both drain voltage waveforms have a pronounced $2f$ component and are lagging by ~25° behind the respective gate voltage waveforms due to gate hysteresis. The lag can be understood from Fig. 2, where both the static (dc) and the dynamic (ac) transfer curves are shown. Parasitic capacitances between the polymer gate and source/drain contacts are so large that they cannot charge/discharge at the same rate at which the input signals are changed. Consequently, the up and the down sweeps of the gate voltage $v_G(t)$ result in different transfer curves leading to a typical hysteretic butterfly-shaped curve as the full cycle is completed.[5] The static CNP splits into two dynamic CNPs (one on either side). The time delay between the static and dynamic CNPs equally shifts both half cycles of the drain voltage without influencing phase detection.

Figure 4 shows that the drain voltage V_D exhibits the predicted $(-\cos\varphi)$ dependence on the phase difference φ. Efficient phase detection requires a high sensitivity of the drain voltage V_D to φ, i.e., a large difference between the maximum and the minimum drain voltage V_D in the phase curve. From the expression for V_D, this difference is $kV_0^2/2$, i.e., the constant k must be as large as possible. This

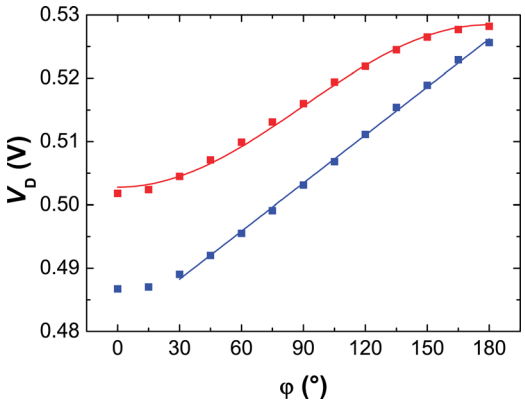

FIG. 4. (Color online) Measured dc component V_D of the drain voltage $v_D(t)$ vs. phase shift φ between the inputs, in the case of analog (red/top) and digital (blue/bottom) detection. Corresponding curve fits in the case of analog ($\propto -\cos\varphi$) and digital ($\propto \varphi$) detection are shown as solid lines.

translates to a need for a large small-signal gain $A = dv_D/dv_G = 2k(V_{GCNP} - V_G)$, where V_G is the gate voltage at the selected operating point. The same is true also for frequency doubling in order to increase signal-to-noise ratio. For the device in Fig. 2, a maximum gain of 0.6 is obtained at $V_G = 0.5$ V. Gain higher than unity was attained in a complementary configuration (see supplementary material).[17] Such gain values cannot be obtained in conventional back-gated devices in which there would be almost no difference between minimum and maximum drain voltages in the phase curve. Back-gated graphene FETs could only be employed in phase detection if input signals with very large amplitude V_0 were used. But this would imply a significant increase in the input power dissipation $(V_0^2/R_G)\sin^2(\varphi/2)$. Moreover, the use of back-gated devices would require a large input bias $V_{GCNP} >$ 20 V, as they are strongly *p*-doped by ambient impurities.

Digital phase detection was realized based on the exclusive-OR functionality of the present circuit.[3] Here, $v_0(t)$ and $v_\varphi(t)$ are digital input signals, which can take either a high $V_H = V_{GCNP} + V_0$ or a low $V_L = V_{GCNP} - V_0$ value. The output drain voltage $v_D(t)$ shows a high value V_{DH} when the two digital inputs $v_0(t)$ and $v_\varphi(t)$ are different and shows a low value V_{DL} when the two inputs are identical. In other words, the duty cycle of the drain voltage is $\varphi/180°$. The dc component of the drain voltage is then $V_D = V_{DL} + 2(V_{DH} - V_{DL})(\varphi/180°) \propto \varphi$. Figure 3(b) shows drain voltage waveforms measured with the digital phase detector for phase shifts of 0° and 90°. As in the case of analog detection, the drain voltage for $\varphi = 90°$ has a larger dc component in comparison to the case for $\varphi = 0°$. The phase curve for the case of digital detection is shown in Fig. 4, which follows the predicted $\propto \varphi$ dependence.

Ideally, the output drain voltage must instantly switch when the gate voltage input changes its level. However, the drain voltage $v_D(t)$ does not instantly reach levels V_{DH} and V_{DL} when the gate voltage is changed [Fig. 3(b)]; instead, parasitic capacitances increase the transition time and, therefore, the drain voltage exponentially tends to these levels. For $\varphi = 0°$, the gate voltage takes only two possible values (V_L or V_H) and the output drain voltage should be constant (V_{DL}). However, the output drain voltage shows a spike when $v_0(t)$ changes its state [Fig. 3(b), blue curve] because the transition time is finite when passing the operating point over the CNP. For very small phase shifts ($\varphi \leq 15°$), the detected voltage is insensitive to phase change (Fig. 4, blue curve) because the mid-state V_{GCNP}, which corresponds to a duty state of the drain voltage $v_D(t)$, is too short. The transition time can also be observed in the transfer curve shown in Fig. 2: for each of the three possible values of the gate voltage (V_L, V_{GCNP}, and V_H), the drain voltage takes a range of values instead of a single value. As for analog detection, large gain is necessary to discriminate between the output voltage levels V_{DH} and V_{DL}. The parasitic capacitances and the ensuing hysteresis in the dynamic transfer curve could be eliminated by passivating the source/drain electrodes, which should also allow for higher clock rates and improved performance.

In summary, we have demonstrated analog and digital phase detectors based on a single misoriented bilayer graphene transistor. Phase detection was enabled by a drop-cast solid polymer electrolyte gate dielectric, which increased the small-signal gain by one order of magnitude over conventional back-gated devices. In order to extend the frequency range of the detectors, passivation of the contacts will be necessary to eliminate parasitic capacitances. In this way, simple phase detectors could be realized representing an important step towards functional graphene electronic ac circuits.

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