Contact Effects in Organic Transistors

THÈSE N^{O} 4989 (2011)

PRÉSENTÉE LE 26 JUILLET 2011

À LA FACULTÉ SCIENCES DE BASE
LABORATOIRE DE SCIENCE À L'ÉCHELLE NANOMÉTRIQUE
PROGRAMME DOCTORAL EN PHYSIQUE

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

POUR L'OBTENTION DU GRADE DE DOCTEUR ÈS SCIENCES

PAR

Frederik Sebastian ANTE

acceptée sur proposition du jury:

Prof. O. Schneider, président du jury
Prof. K. Kern, directeur de thèse
Prof. J. Brugger, rapporteur
Dr H. Klauk, rapporteur
Prof. A. Morpurgo, rapporteur

ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE
Suisse
2011

to my parents

Abstract

Organic thin-film transistors (TFTs) are of interest for applications that require electronic functionality with low or medium complexity distributed over large areas on unconventional substrates, such as flexible polymeric films. Generally these are applications in which the use of silicon devices and circuits is technically or economically not feasible. Examples include flexible displays and large-area sensor arrays. The static and dynamic performance of state-of-the-art organic p-channel transistors is already sufficient for applications in which the transistors operate with frequencies of a few tens of kilohertz.

Strategies to improve the performance of organic TFTs include improvements in the field-effect mobility of the charge carriers in the organic semiconductor layer and more aggressive scaling of the transistor dimensions. Additional advances are also required in the environmental and operational stability of organic TFTs and in the application of controlled contact doping for the reduction of the contact resistance of organic TFTs.

In this thesis, high-resolution silicon stencil masks are introduced to pattern top-contact organic TFTs with lateral dimensions as small as 0.8 µm. Taking advantage of the recently synthesized high-mobility air-stable organic semiconductor dinaphtho[2,3-b:2´3´-f]thieno[3,2-b]thiophene (DNTT), polycrystalline organic p-channel TFTs with excellent air-stability and an intrinsic mobility of 3.4 cm^2/Vs were fabricated. The transistors employ an ultra-thin gate dielectric based on a plasma-grown oxide layer in combination with an organic self-assembled monolayer (gate capacitance ∼1 $\mu F/cm^2$), allowing the TFTs to operate with low voltages of about 3 V. Transistors with dimensions of less than 100 nm were manufactured using polymer resist shadow masks that have been fabricated by electron-beam lithography. Thanks to the 5 nm thick gate dielectric the TFTs show no short-channel effects. The subthreshold swing, the on/off current ratio, and the threshold voltage are comparable to long-channel TFTs with lateral dimensions of ∼100 µm. However, organic transistors with reduced dimensions are often limited by the energy barrier at the interface between the semiconductor and the source/drain contacts. One approach to reduce this energy barrier is the introduction of a strong electron acceptor into the contact area that acts as a dopant. With contact doping, the contact resistance is reduced and the effective mobility of short-channel TFTs increases by more than 200%.

Transistors (without doping) with lateral dimensions of ∼1 µm have a transconductance of about 1 S/m, so that the TFTs operate at frequencies of several megahertz. The influence of strongly reduced lateral dimensions on the contact resistance and the maximum operation frequency is investigated and scaling limitations are discussed.

Keywords:

Organic thin-film transistor, contact doping, contact resistance, transfer length, organic semiconductor, ultra-thin gate dielectric, low-voltage transistor, dynamic performance, dinaphtho[2,3-b:2´3´-f]thieno[3,2-b]thiophene, DNTT

Abstract

Organische Dünnschichttransistoren (englisch: thin-film transistor, TFT) sind für elektronische Anwendungen auf unkonventionellen Substraten, wie zum Beispiel biegsamen Plastikflächen, von Interesse. Typischerweise betrachtet man dabei Einsatzgebiete, bei denen die Verwendung von Silizium-basierten Bauelementen und Schaltkreisen technisch nicht möglich oder ökonomisch nicht sinnvoll ist. Dies wären zum Beispiel flexible Displays oder großflächige Sensorfelder. Die aktuelle statische und dynamische Leistungsfähigkeit von organischen p-Kanal Transistoren ist ausreichend für Anwendungen, die eine Schaltfrequenz von einigen zehn Kilohertz pro Transistor benötigen.

Ansätze, um die Leistungsfähigkeit von organischen Transistoren weiter zu erhöhen, beinhalten Verbesserungen im Bereich der Ladungsträgerbeweglichkeit in der organischen halbleitenden Schicht und die kontinuierliche Reduktion der Strukturabmessungen der einzelnen Transistoren. Zusätzliche Fortschritte sind auch in den Bereichen der Luft- und Betriebsstabilität nötig. Letztlich ist auch die erfolgreiche Einführung von kontrolliertem Kontaktdotieren nötig, um den Kontaktwiderstand in organischen Transistoren mit reduzierten Strukturabmessungen zu verringern.

In dieser Arbeit wurden hochauflösende Silizium-Schattenmasken verwendet, um organische Transistoren bis zu einer minimalen Strukturabmessungen von 0.8 µm herzustellen. In der gewählten Transistorgeometrie werden die Metallkontakte auf den organischen Halbleiter aufgebracht. Es wurde Dinaphtho[2,3-b:2´3´-f]thieno[3,2-b]thiophene (DNTT) als Halbleiter ausgewählt, da sich dieses durch eine ausgezeichnete Luftstabilität und hohe Löcherbeweglichkeit auszeichnet. Polykristalline organische p-Kanal Transistoren mit einer intrinsischen Ladungsträgerbeweglichkeit von 3.4 cm^2/Vs konnten in dieser Arbeit realisiert werden. Die Transistoren basieren auf einem Gatedielektrikum bestehend aus einer dünnen Lage Plasma-gewachsenem Aluminiumoxid und einer organischen selbstorganisierenden Monolage (Gatekapazität $\sim$1 $\mu F/cm^2$). Dies ermöglicht es, die Transistoren mit niedrigen Spannungen von etwa 3 V zu betreiben. Um TFTs mit Strukturabmessungen von weniger als 100 nm herzustellen, wurden Schattenmasken aus einem Poylmerresist mittels Elektronenstrahllithographie gefertigt. Aufgrund des 5 nm dünnen Gatedielektrikums weisen diese Transistoren keine Kurzkanaleffekte auf. Der Unterschwellanstieg, das Verhältnis aus Ein- zu Ausstrom und die Schwellspannung sind vergleichbar zu Langkanaltransistoren mit Strukturabmessungen von 100 µm. Allerdings sind organische Transistoren mit reduzierten Strukturabmessungen häufig durch die Energiebarriere an der Grenzfläche zwischen dem Halbleiter und den Source- /Drainkontakten beeinträchtigt. Durch den gezielten Einbau von starken Elektronenakzeptoren als Dotanden kann diese Energiebarriere erniedrigt werden. Mittels Kontaktdotierung konnte somit der Kontaktwiderstand reduziert und die effektive Ladungsträgerbeweglichkeit in

Kurzkanaltransistoren um mehr als 200% erhöht werden.

Transistoren (ohne Kontaktdotierung) mit Strukturabmessungen von ∼1 µm weisen einen Durchgangsleitwert von ungefähr 1 S/m auf, weshalb diese TFTs mit einer Frequenz von einigen Megahertz betrieben werden können. Außerdem werden in dieser Arbeit der Einfluss von extrem reduzierten Strukturabmessungen auf den Kontaktwiderstand und die maximale Betriebsfrequenz untersucht, sowie potentielle Einschränkungen diskutiert.

Schlagwörter:

Organischer Dünnschichttransistor, Kontaktdotierung, Kontaktwiderstand, Transferlänge, organischer Halbleiter, ultra-dünnes Gatedielektrikum, Niederspannungs-Transistor, dynamischer Betrieb, dinaphtho[2,3-b:2´3´-f]thieno[3,2-b]thiophene, DNTT

Contents

1 Introduction

Transistors are among the most important inventions of the twentieth century [1]. The transistor is the key active component for amplifying or switching electronic signals. Simple logic circuits require only a few transistors, whereas modern high-end microprocessors employ more than a billion transistors [2]. Since state-of-the-art transistors have feature sizes of less than 30 nm, such a large number of transistors can be realized on an area of only a few square centimeters. In the year 2009 alone, approximately 10^{19} transistors were manufactured, most of them for high-performance microprocessors and solid-state memory chips [3].

The first patent dealing with the idea of a transistor dates back to 1925 by Julius E. Lilienfeld, but in this time an experimental realization was not possible due to the lack of technologies for processing thin layers of functional electronic materials. The first experimental realization of a solid-state amplifier (= transistor) was reported by Rudolf Hilsch and Robert W. Pohl in 1938 at the University of Göttingen [4]. They modulated the current in a potassium bromide crystal using an external control electrode and achieved a gain of 20 to 100, but their results were hardly reproducible. Therefore, often the work by William B. Schockley, Walter H. Brattain, and John Bardeen in 1947 at Bell Labs is considered as the first successful realization of a transistor, for which they were awarded with the Nobel Prize in Physics in 1956.

The word "transistor" is a combination of the words "transfer" and "resistor", and describes the situation where the electrical resistance of an active material between two electrodes is controlled by a third electrode. Thus, the magnitude of the electric current flowing through the transistors can be modulated. If this modulation is achieved by accessing this active material directly, the transistor is called a **bipolar transistor**, like the transistor manufactured at Bell Labs. This consisted of germanium as the active material and metal point contacts as electrodes. Today, bipolar transistors account for only a very small portion of the total number of transistors that are manufactured.

By far the most important type of transistor today is the **field-effect transistor** (FET). FETs were first developed in the 1960s and two basic implementations are employed. In one of those implementation the semiconductor has the form of a single-crystalline wafer that serves as the substrate and as the active material of the transistor. Historically, these

FETs are named *metal oxide semiconductor field-effect transistor* (MOSFET). The most common MOSFET utilizes a silicon wafer. It exhibits a superior dynamic performance and accounts for $> 99\%$ of all transistors and is mainly employed for applications that require a high integration density (number of transistors per area), such as microprocessors.

In the second important FET implementation, the substrate and the active material are usually not identical. Instead, the semiconductor and the other components of the FET are deposited onto a rigid or flexible substrate in the form of thin films. Such an FET is called *thin-film transistor* (TFT). The semiconductor is typically amorphous or polycrystalline silicon. TFTs do not achieve the performance and integration density of MOSFETs. However, TFTs can be manufactured on a wide variety of substrates, which allows the utilization of TFTs for large-area applications, such as to control the individual pixels in active-matrix displays.

Today's state-of-the-art single-crystalline, polycrystalline, or amorphous silicon transistors are processed at temperatures > 300°C, so that these are not compatible with flexible plastic substrates which usually have a glass transition temperature of < 200°C. For applications like flexible displays, conformable sensor arrays, and printable electronics one approach is to reduce the process temperature of silicon TFTs [5, 6]. Another strategy is to utilize novel semiconducting materials, such as transparent oxides [7], nanotubes [8], nanowires [9], or organic materials [10]. Among these, organic semiconductors are particularly suited for solution-processing or vacuum-deposition at or near room temperature [11, 12, 13, 14, 15, 16]. The first reports on the electrical conduction of organic materials was already reported by Alfredo Pochettino more than 100 years ago [17]. However, the work by Alan J. Heeger, Alan MacDiarmid, and Hideki Shirakawa in 1977, who were awarded with the Nobel Prize in Chemistry in 2000, is often considered as the breakthrough in the realization of high-performance organic electronics [18].

Semiconducting organic materials are useful to realize the active material in electronic devices, such as light-emitting diodes, solar cells, and thin-film transistors. Organic light-emitting diodes are already commercially available in the form of active-matrix displays of some high-end smartphones (on rigid substrates, driven by silicon TFTs). Organic solar cells can also already be purchased, although the production is still limited to small volumes. Organic transistors, on the other hand, are still mainly the subject of academic research and of small-scale industrial development (Plastic Logic).

The first **organic transistor** was reported in 1987 by Koezuka and co-workers based on a thin film of the semiconducting polymer polythiophene [19]. The charge-carrier mobility, which is a measure of the efficiency of the charge-carrier transport in (organic) semiconductors, has since then improved by several orders of magnitude thanks to novel organic semiconductors and improved process techniques (Figure 1.1). For example, the mobility is now sufficiently large to drive the individual pixels in rollable displays with a

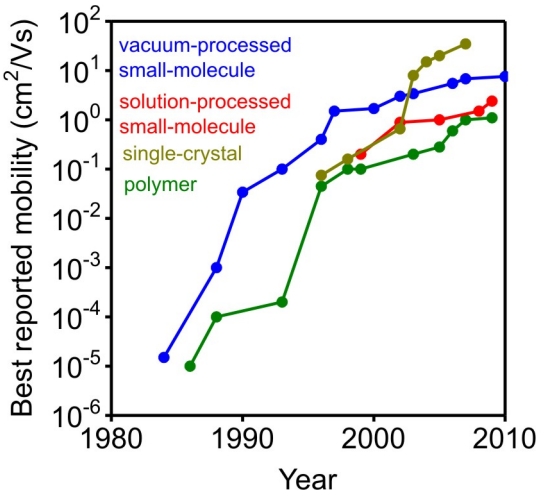

Figure 1.1: Development of the largest reported field-effect mobility of organic transistors for each year. The graph illustrates the largest reported hole mobility for field-effect transistors employing vacuum-processed small molecules, solution-processed small molecules, organic single-crystals, or polymers as organic semiconductor. Mainly adopted from [3]

row access time of a few kilohertz [20] or to realize radio-frequency identification tags [21]. However, for instance high-definition displays require a much faster response frequency for every individual transistor. A common method to increase the maximum operation frequency of transistors are to reduce the lateral dimensions ($f_T \sim 1/L^2$). Unfortunately, this leads to several undesired effects, for instance a significant contribution of the contact resistance to the total transistor resistance, so that the effective mobility of the transistor is reduced.

The aim of this thesis is to investigate and understand the impact of aggressively reduced lateral dimensions on the electrical characteristics of organic TFTs in more detail. Therefore, in chapters 2 and 3 the fundamentals of organic semiconductors and thin-film transistors will be presented, with the focus on organic transistors. In the literature, downscaling of organic transistors was often reported for the bottom-contact geometry, in which the metal contacts are deposited prior to the organic semiconductor. The metal contacts are fabricated by standard photolithography or electron-beam lithography. However, the bottom-contact geometry exhibits a large contact resistance that significantly influences the electrical characteristics. Therefore, aggressive scaling (which is enabled for example by electron-beam lithography) is not very useful, since these bottom-contact transistors are limited by the contact resistance rather than by the resolution of the lithography technique itself.

In the top-contact geometry, in which the metal contacts are processed on top of the organic semiconductor, the contact resistance is typically much smaller. Thus, the top-contact geometry is more suited to study aggressively reduced lateral dimensions. However, exposing a vacuum-deposited organic film to organic solvents (as employed in stan-

dard lithography) significantly degrades the semiconductor performance [22]. Therefore, top-contact organic transistors are often fabricated by shadow masking. So far, there are only studies focusing on either large [23, 24] or small [25] dimensions, depending on the resolution of the employed shadow masking technique. A detailed study on organic top-contact TFTs with a broad range of lateral dimensions manufactured with a comparable process has so far not been reported. In chapter 4 one approach to fabricate top-contact transistors with dimensions between 200 µm and 0.09 µm is presented. As the active material in the organic TFTs, the recently developed organic semiconductor dinaphtho[2,3-b:2´3´-f]thieno[3,2-b]thiophene (DNTT) was utilized, since it exhibits a large charge-carrier mobility and a good air-stability [26, 27]. The morphology and crystal structure of vacuum-deposited thin films of DNTT and their suitability for organic transistors is investigated in chapter 5. Often the organic semiconductor pentacene, whose chemical structure is similar to that of DNTT, is considered as the prototypical active material for organic transistors. Therefore, data obtained for DNTT transistors will be compared to results reported on pentacene transistors.

The electrical characteristics of DNTT TFTs with large lateral dimensions, but also with extremely reduced dimensions (∼90 nm), and the impact of the contact resistance on the electrical characteristics are discussed in chapter 6. Issues related to the air stability are addressed in chapter 7. Area-selective contact doping to control the contact resistance is an extremely successful technique in silicon MOSFET technology. This concept was also adopted for the organic transistors studied in this thesis and the results on organic doping of the contact area are presented in chapter 8. The last chapter of this thesis deals with the dynamic response of DNTT transistors and simple integrated circuits.

2 Organic semiconductors

Solids in the form of single-crystals, polycrystalline films, or amorphous films that are composed of hydrocarbon molecules are considered as organic solids. Organic molecules mainly consist of carbon and hydrogen atoms, although other atoms, such as nitrogen, oxygen, sulfur, or fluorine may also be included [28]. The definition of organic solids is very general and covers many materials, but in the framework of this thesis only the group of intrinsic **organic semiconductors** is of importance. This group includes all organic solids that are insulating (in a highly pure structure) at room temperature or below, but electrically conducting when excess charges are introduced, e.g. by an externally applied electric field [28]. If the structure of these organic semiconductors contains (un)intentionally incorporated defects, impurities, or foreign atoms, the conductivity can be either increased (charge-carrier doping) [29, 30, 31] or decreased (charge-carrier trapping) [32].

There are two groups of molecules forming organic semiconductors, **polymers** and **small-molecules**. Polymers are not subject of this thesis and for further information the interested reader is referred to the literature [13, 33]. Among the most prominent small-molecule compounds are the acenes, e.g. benzene or pentacene (Figure 2.1b,c). Recently heteroarenes based on benzene and thiophene rings have been receiving large attention due to their superior charge transport and air stability compared to acenes [34, 35].

For the charge transport in organic semiconductors the presence of a conjugated $\pi-$ electron system is essential [28]. This important concept of conjugation is discussed in section 2.1. In section 2.2 widely used models explaining the charge transport in organic semiconductors are briefly discussed. An overview of process technologies for organic semiconductors (section 2.3) is followed by a section with details on the organic semiconductor utilized in this work (section 2.4).

2.1 Electronic properties of individual molecules

A free carbon atom has four valence electrons in its electronic ground state ($1s^2 2s^2 2p^2$), so that two different kinds of chemical bonds are expected, depending on whether 2s- or 2p-electrons are included in the chemical bond formation. However, in many organic

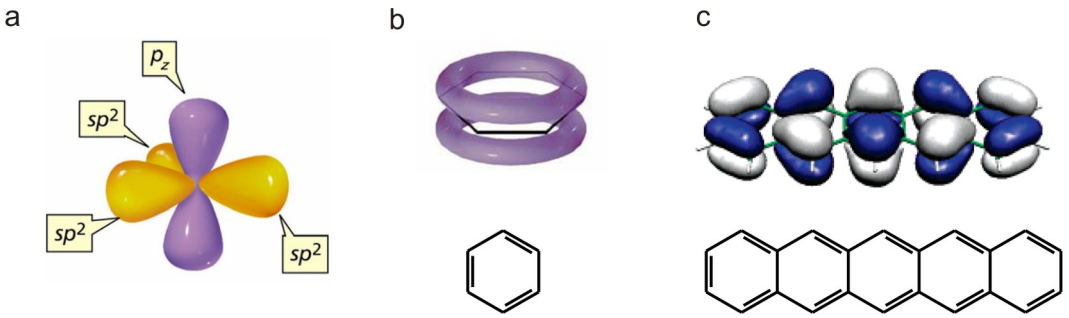

Figure 2.1: Carbon-based compounds with sp^2-hybridization. a) sp^2-atomic hybrid orbitals and p_z orbitals of carbon. b) Chemical structure and delocalized π-electron system of benzene (C_6H_6). c) Chemical structure and delocalized molecular orbitals of pentacene ($C_{22}H_{14}$). Images adapted from [37, 38]

molecules, for example methane (CH_4), the formation of four uniform chemical bonds is observed [36]. This observation is explained by the concept of hybrid orbitals, which assumes a hybridization between the 2s- and the three 2p- (x, y and z direction) atomic orbitals of carbon. This hybridization results in the formation of four uniform sp^3-atomic hybrid orbitals (sp^3-hybridization). The formation of three identical atomic hybrid orbitals is denoted as sp^2-hybridization (2s, $2p_x$ and $2p_y$) and the formation of two identical atomic hybrid orbitals as sp-hybridization (2s and $2p_x$). The two latter hybridization are, for instance, observed in ethylene (C_2H_4) and ethyne (C_2H_2), respectively.

For the electronic properties of organic semiconductors the concept of sp^2-hybridization is essential. Here, the 2s-, $2p_x$- and the $2p_y$-atomic orbitals form three trigonal-planar aligned $2sp^2$-atomic hybrid orbitals, with the $2p_z$-atomic orbital pointing perpendicularly out of this plane (Figure 2.1a). One of the most prominent examples for this configuration is the benzene molecule (C_6H_6, Figure 2.1b), which is the basic unit of many organic semiconductors. Here, the sp^2-atomic hybrid orbitals (in the molecular plane) of the carbon atoms form σ-bonds with the neighboring carbon or hydrogen atoms. The combination of all these σ-bonds is denoted as localized σ-molecular orbitals. The p_z-atomic orbitals (out of the molecular plane) of the carbon atoms form π-bonds with one neighboring carbon atom, and their combinations are called π-molecular orbitals. There is an alternation of single (only σ-bonds) and double bonds (σ- and π-bonds) within the benzene molecule, so that the π-bonds (π-electrons) are not assigned to a certain carbon atom pair, but are delocalized over the whole molecule (Figure 2.1b). In total there are twelve bonding and twelve anti-bonding localized σ-molecular orbitals in the molecule plane and three bonding and three anti-bonding delocalized π-molecular orbitals. The delocalized π-molecular orbitals are responsible for the electronic properties of the molecule. The frontier molecular orbitals, i.e. the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO), are of particular interest. The energetic position of the HOMO corresponds to the ionization energy of the molecule and the LUMO

corresponds to the electron affinity of the molecule. In analogy to inorganic semiconductors, such as silicon, the energy difference between these two energy levels is defined as the energy gap. The HOMO-LUMO gap of benzene is 6.8 eV, which is too large to be useful for electronic applications. However, the HOMO-LUMO gap energy decreases as the number of delocalized π-electrons participating in the π-system is increased [28]. This is seen for the acenes, for instance, so that the HOMO-LUMO gap of pentacene ($C_{22}H_{14}$, five linear fused benzene rings, Figure 2.1c) is only 2.2 eV [28] and allows the utilization of this organic semiconductor in electronic applications [33, 39, 40, 41].

2.2 Charge-carrier transport in organic semiconductors

Organic semiconducting solids are intrinsically insulating and their conductivity must be triggered by external factors, like shifting the Fermi level by an externally applied field to modify the charge-carrier density. The ability of a charge carrier to move in a solid is quantified by the mobility μ (unit: $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$), which is the proportionality factor between the mean drift velocity $\mathrm{v_D}$ of the charge carriers and the applied electric field $\overrightarrow{\mathrm{E}}$: $\mathrm{v_D} = \mu \cdot \overrightarrow{\mathrm{E}}$. The charge-carrier mobility is a material parameter and determines the electrical conductivity σ:

$$\sigma = e \cdot \mu \cdot \mathrm{n} \tag{2.1}$$

with the elementary charge e (negative for electrons and positive for holes) and the charge-carrier density n. In inorganic semiconductors the strong covalent bonds between neighboring atoms form broad energy bands and the charge-transport mechanism is often described by a band-like transport. In contrast, individual molecules in organic semiconductors interact via much weaker van der Waals forces, so that the energy bands are more narrow. Due to the unintentional incorporation of chemical impurities, structural defects or grain boundaries, which introduce a large density of localized states disturbing the periodicity of the crystal lattice, the assumption of a simple band-like transport usually fails in organic semiconductors. In a first approximation, the efficiency of the charge transport through the organic semiconductor depends on the overlap between the π-molecular orbitals of neighboring molecules (= on the value of the transfer integral, which describes the interaction between neighboring HOMOs or LUMOs) and is typically more effective for well-ordered films [28]. However, a main problem originates from the broad range of charge-carrier mobilities reported at room temperature for organic semiconductors ($10^{-6} - 10^{1}\ \frac{\mathrm{cm}^2}{\mathrm{Vs}}$) [3], so that currently no single model fully describes this charge-transport mechanism. From the multitude of proposed models, the **variable-range hopping model** (VRH model) and the **multiple trapping and release model** (MTR model) are often utilized to describe the charge transport in organic semiconductors and will be briefly discussed in the next paragraphs.

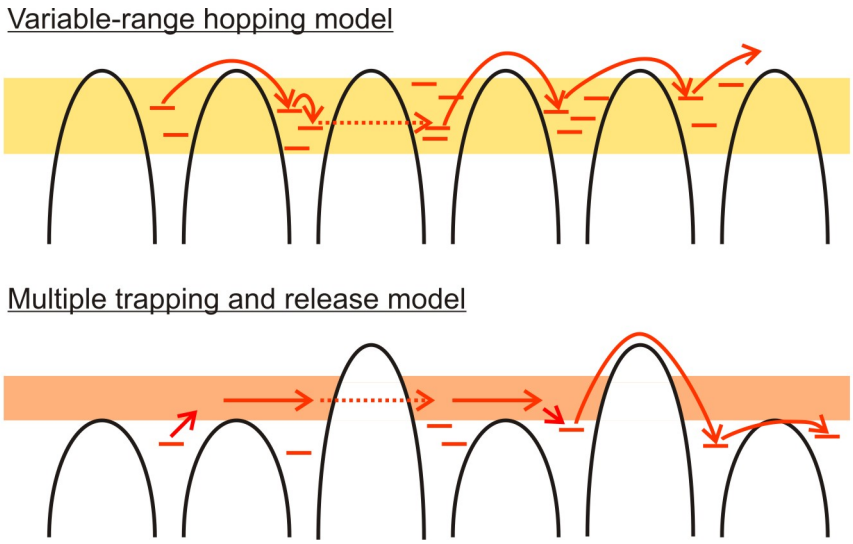

Figure 2.2: Charge-transport mechanisms in organic semiconductors. a) The variable-range hopping model assumes a transport mechanism driven by thermal energy and/or tunneling between discrete states. The model is useful to describe the charge transport in amorphous organic semiconductors with a charge-carrier mobility of $\sim 10^{-3}\ \frac{\mathrm{cm}^2}{\mathrm{Vs}}$. b) The multiple trapping and release model assumes a transport mechanism driven by thermal activation of charge carriers into extended states followed by a trapping in discrete states. This model is useful to describe the charge transport in polycrystalline organic semiconductors with a charge-carrier mobility of $\sim 1\ \frac{\mathrm{cm}^2}{\mathrm{Vs}}$. Schematics adapted from [42].

Variable-range hopping model

The VRH model was introduced to decribed the charge transport in disordered inorganic materials [43], but it is also applicable to organic semiconductors [44]. In this model the charge-carrier transport is considered as a hopping between localized electronic states, which can be considered as charge traps induced by chemical impurities, structural defects or grain boundaries (Figure 2.2). The hopping rate (= mobility) between two localized states is thermally activated and/or tunneling assisted and the relaxation takes place under phonon emission. The necessary activation energy further depends on the molecular order and on the charge-carrier density. If the charge-carrier density is increased, the lower trap levels are filled, the activation energy decreases, and the mobility increases. The mechanism to control the charge-carrier density by an external voltage is discussed in section 3.1.1. The VRH model is useful to describe the charge-transport mechanism in amorphous materials with a maximum mobility of $\sim 10^{-3}\ \frac{\mathrm{cm}^2}{\mathrm{Vs}}$.

Multiple trapping and release model

The MTR model was introduced to describe the charge transport in amorphous silicon [45] and was adapted to organic transistors by Horowitz and co-workers [46]. In the model

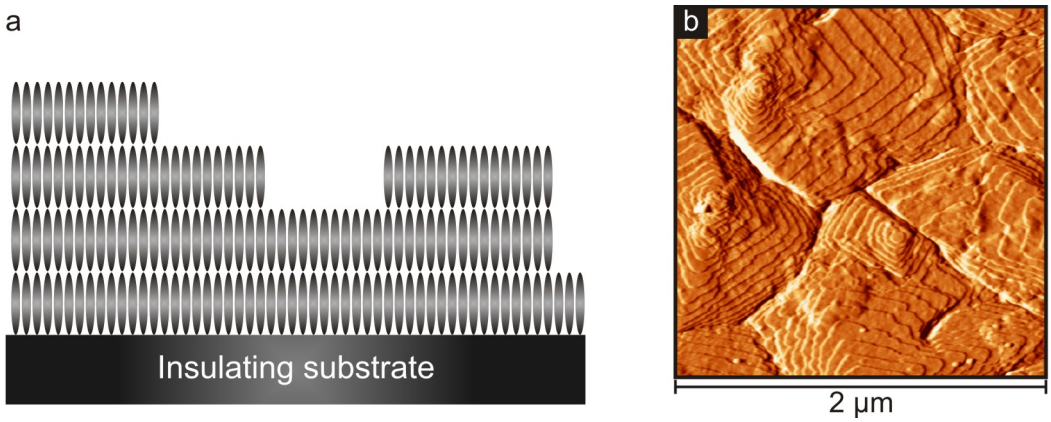

Figure 2.3: Morphology of a polycrystalline organic thin film. a) Schematic of the three-dimensional growth of a small molecule on an insulating substrate. The arrangement of the molecules favors a strong overlap of the delocalized π-electrons perpendicular to the long axis of the molecule (parallel to the surface). b) Atomic force microscope (amplitude) image of a polycrystalline pentacene film grown on an insulating low-energy surface. The crystallites and the terrace steps corresponding to the length of one pentacene molecule are shown.

a charge transport in extended states (transport band) above the localized states (Figure 2.2) is assumed. Similar to the VRH model, the mobility is temperature-activated and further depends on the charge carrier density and the activation energy from localized states into the extended transport states. The transport is explained by a thermal activation of charge carriers into the transport band, in which an efficient charge transport is possible. Impurities, defects, and grain boundaries can scatter charge carriers back into localized states. The typical activation energies in the MTR model are around 10-30 meV. The model is useful to describe the charge transport in organic TFTs with mobilities as large as $\sim$1 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$.

2.3 Processing of organic semiconductors

A variety of methods are available to grow an organic (semiconducting) solid for electronic applications, but not all of these can be discussed here. Soluble molecules can be processed by spin coating [47], dip or drop casting [48], airbrush deposition [49], and printing techniques [11, 14, 50]. Spin coating and printing of molecules often leads to amorphous films with no long-range order [47], whereas dip or drop casting produces small crystals with a higher molecular order, but which are randomly dispersed on the substrate [51].

Other techniqures to process molecules (soluble and non-soluble molecules) include single-crystal growth [52, 53, 54, 55], chemical vapor deposition [56], and sublimation in vacuum [57, 58, 59, 60]. However, the necessity to sublime the semiconductor without decomposition of the molecules limits these techniques to molecules with a low molecular weight (the

deposition of macro molecules is possible, for instance by electrospray ion-beam deposition [61] or matrix-assisted laser desorption/ionization [62]). Single-crystal growth produces organic solids with a high material purity, molecular order, and the most effective charge transport, but this technique is complex and time consuming.

The sublimation of organic semiconductors in vacuum is a simple method to produce films with a long-range molecular order. This technqiue was also used to deposit the organic semiconductors utilized in this work. Vacuum-deposited small molecules often form well-ordered polycrystalline films. The exact morphology and nucleation density on the surface depend mainly on the substrate temperature, substrate surface energy, surface roughness, and deposition rate [63]. It is known that the molecules favor a two-dimensional growth with large grains on inorganic dielectrics with a high surface energy and a three-dimensional growth with smaller grains on low-energy dielectrics. The mobility is typically higher in films grown on the latter surfaces [3]. The exact mechanism responsible for this observation is not yet clarified, but it is likely that voids between disconnected grains hinder the charge transport for two-dimensionally grown organic semiconductors on high-energy surfaces [3]. In addition, an elevated substrate temperature (∼60-100°C) is utilized to provide additional energy to the molecules, so that the diffusion length on the surface is increased and the number of nucleation centers is reduced [63]. However, if the substrate temperature is too high, the sticking coefficient of the molecules is reduced and no nucleation on the substrates occurs. Even though thermally evaporated organic semiconductors often exhibit a three-dimensional film growth, as illustrated in Figure 2.3b, the exact molecular order can vary depending on the molecule itself and the substrate surface. In the case of pentacene the molecules lie flat on conducting surfaces (due to the strong overlap between the delocalized π-electrons of pentacene and the electrons on the surface of the conducting substrate) [64], whereas the molecules stand perpendicular on insulating surfaces (Figure 2.3a) [65, 66]. In contrast, the first two layers of thermally evaporated films of hexafluorocopperphthalocyanine ($F_{16}CuPc$) lie flat on insulating surfaces [67, 68].

The arrangement of pentacene molecules on insulating substrates (Figure 2.3a) results in an efficient charge transport in the plane parallel to the substrate (strong interaction between neighboring molecules) and a less effective transport perpendicular to the substrate (weak interaction between neighboring molecules).

2.4 Dinaphtho[2,3-b:2´3´-f]thieno[3,2-b]thiophene (DNTT)

In this thesis the organic semiconductor dinaphtho[2,3-b:2´3´-f]thieno[3,2-b]thiophene ($C_{22}H_{12}S_2$, DNTT) that was introduced by Yamamoto and Takimiya in 2007 [26, 27] has

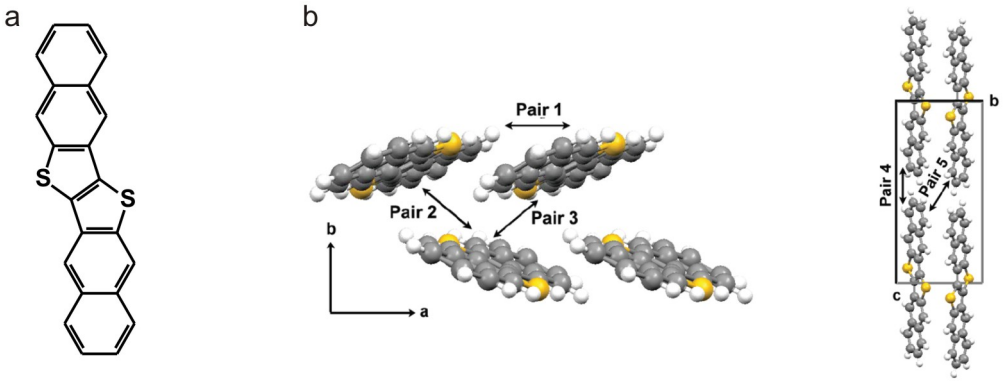

Figure 2.4: Chemical structure and crystal structure of DNTT. a) Chemical structure of dinaphtho[2,3-b:2´3´-f]thieno[3,2-b]thiophene (DNTT, $C_{22}H_{12}S_2$). b) Crystal structure of DNTT. The molecules pack in a herringbone structure in the ab-plane (a = 6.187 Å, b = 7.662 Å) with a layer spacing of 16.21 Å in the c-direction. Values and schematics adapted from [35].

been utilized. The DNTT molecule is a symmetric heteroarene with six fused aromatic rings consisting of two naphthalene and two thiophene units (Figure 2.4a). It currently receives a lot of attention due to its high mobility and its excellent air stability [26]. For single-crystals of DNTT, Haas and co-workers reported a hole mobility of 8.3 $\frac{cm^2}{Vs}$ [69], and in polycrystalline thin-films a reasonably large hole mobility of 3 $\frac{cm^2}{Vs}$ was measured [27]. The HOMO energy in DNTT is -5.4 eV [26] and energetically deeper compared to the prototypical small-molecule pentacene, which has a HOMO energy of -5.0 eV, so that the oxidation potential of DNTT molecules is larger and a better air stability can be expected. The LUMO energy of DNTT is at -3.0 eV [26] introducing a sufficiently large HOMO-LUMO gap of -2.4 eV (pentacene: 2.2 eV [28]) allowing the utilization of DNTT for organic transistors.

As is common for most crystalline organic semiconductors, the molecules pack in a herringbone structure in the ab-plane (a = 6.187 Å, b = 7.662 Å) with a layer spacing of 16.21 Å in the c-direction [26] (Figure 2.4b). The theoretically calculated effective mass of holes at the top of the valence band at the Γ point is 1.9 m_0 along the a-plane and 2.7 m_0 along the b-plane, with m_0 being the free electron mass [35]. Compared to pentacene with an effective mass of 1 to 4 m_0, depending on the film phase, the anisotropy of the effective mass in DNTT films is small [35]. This is in good agreement with the experimentally derived mobilities in the ab-pane of DNTT single-crystals and confirms the isotropic distribution (note: the charge-carrier mobility is inversely proportional to the effective mass) [54].

3 Theory of thin-film transistors

Field-effect transistors are three-terminal devices consisting of a source, a drain, and a gate electrode. The resistance of a semiconductor between the source and the drain contact is controlled by the electric potential applied to the gate electrode that is capacitively separated from the semiconductor by the gate dielectric (Figure 3.1). Thus, by applying a gate-source voltage the resistance of the semiconductor is controlled, so that the current flowing along the channel from the source to the drain contact under the influence of an additional drain-source voltage can be modulated. The distance between the source and the drain contact is called channel length L and the overlap distance between the gate electrode and the source/drain contacts is called contact length L_C. Both these parameters, L and L_C, play important roles in determining the electrical properties of organic transistors.

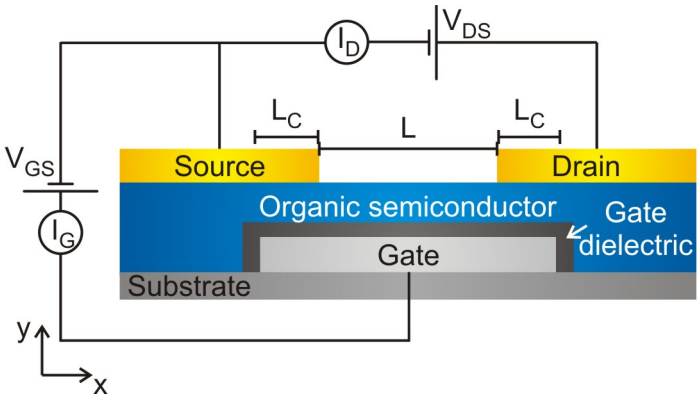

Figure 3.1: Schematic of a thin-film transistor. The schematic illustrates a thin-film transistor. The transistor consists of three terminals, the source, the drain, and the gate electrode. The resistance of the semiconductor between the source and the drain contact is controlled by the electric potential applied to the gate electrode that is capacitively separated from the semiconductor by the gate dielectric. Thus, by applying a gate-source voltage the resistance of the semiconductor is controlled, so that the current flowing along the channel from the source to the drain contact under the influence of an additional drain-source voltage can be modulated.

In section 3.1 the basic transistor equations will be derived, their adaptability to organic transistors will be discussed, and the most important transistor parameters will be defined. Subsequently, the dynamic properties of transistors (section 3.2) and the effects leading to deviations from the ideal electrical characteristics will be discussed (section 3.3).

3.1 Basic transistor equations

In this section a model to derive the basic transistor equations will be discussed. It is mainly related to the model describing the single-crystalline silicon MOSFET and can be followed in [70, 71]. First, the surface charge density of a p-doped (incorporation of electron-deficient dopant species) semiconductor as a function of the surface potential will be calculated. The derived formula will be modified to account for the situation in organic transistors, where the organic semiconductor is typically intrinsic and the transistors are operated in the accumulation mode [72].

3.1.1 Metal-insulator-semiconductor capacitor

For TFTs (Figure 3.1) the drain current I_D along the transistor channel length L from the source to the drain contact is controlled by the gate-source voltage V_{GS}. The gate electrode is electrostatically coupled via the gate dielectric to the organic semiconductor. Following Drude's model, the drain current is proportional to the conductivity σ of the semiconductor and the drain-source voltage V_{DS} along the transistor channel:

$$I_D \propto \sigma \cdot V_{DS} \tag{3.1}$$

with

$$\sigma = e \cdot p \cdot \mu_0. \tag{3.2}$$

Here, e is the elementary charge, p the density of charge carriers in the organic semiconductor, and μ_0 the intrinsic charge-carrier mobility. Since μ_0 is assumed to be independent of the electrostatic potential, the density of charge carriers p must be controlled by the gate-source voltage to modify the conductivity of the channel. In a p-doped semiconductor the density of holes in the valence band is given by

$$p_0 = N_V \cdot \frac{n_A}{n_D} \exp\left(-\frac{E_V - E_F}{k_B T}\right), \tag{3.3}$$

with the valence band energy E_V and the Fermi energy E_F. N_V is the effective density of states in the valence band, n_A and n_D are the densities of acceptors and donors, respectively, k_B the Boltzmann constant, and T the temperature. The density of holes in the semiconductor is influenced by the external electrostatic potential $\phi(y)$ (the gate-source voltage). The potential $\phi(y)$ has its maximum at the gate dielectric/semiconductor interface (surface potential $\phi(y = 0) = \phi_S$) and can be neglected in the bulk ($\phi(y \to \infty) = 0$). Therefore, the density of holes in the bulk is well described by equation 3.3, however, close to the gate dielectric/semiconductor interface the density of holes is strongly influenced

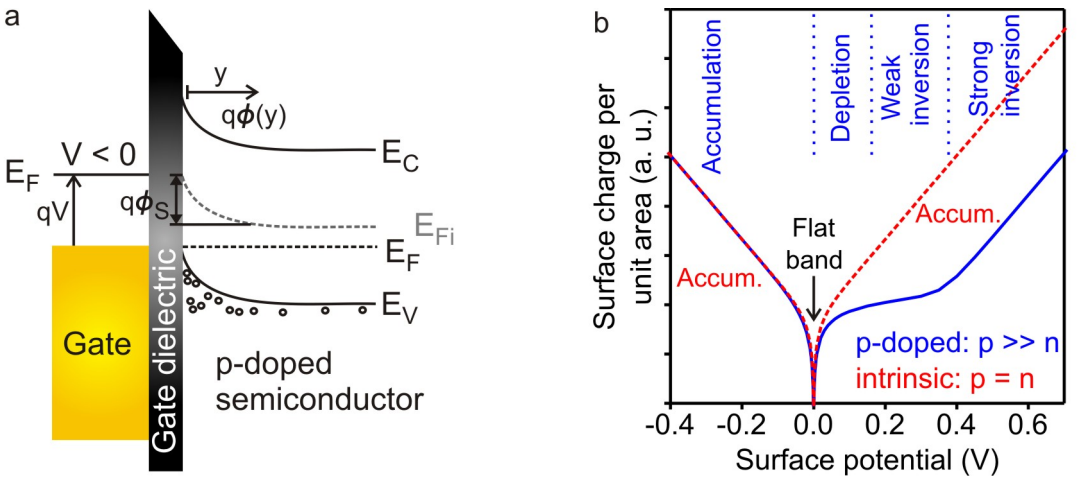

Figure 3.2: Ideal metal/insulator/semiconductor capacitor and surface charge density as a function of the surface potential. a) The schematic shows the energy level alignment across a metal (gate) electrode/(gate) dielectric/p-doped semiconductor capacitor. By applying a negative potential to the gate electrode, the hole density in the semiconductor is increased (accumulation). Applying a positive potential to the gate electrode reduces the hole density (depletion) and strongly increases the electron density for a higher potential (inversion). b) Surface charge per unit area as a function of the surface potential for a p-doped semiconductor indicating the five characteristic regions: hole accumulation, flat band point, hole depletion, weak, and strong inversion.

by the potential ϕ. Depending on the sign of ϕ the energy bands are bent upwards or downwards (at the gate dielectric/semiconductor interface), so that holes or electrons are accumulated (Figure 3.2a). The density of holes as a function of the potential ϕ in the vicinity of the gate dielectric/semiconductor interface is expressed by:

$$\mathrm{p}_\phi(\mathrm{y}) = \mathrm{p}_0 \cdot \exp\left(-\frac{e\phi(\mathrm{y})}{\mathrm{k_B T}}\right) \tag{3.4}$$

and for electrons:

$$\mathrm{n}_\phi(\mathrm{y}) = \mathrm{n}_0 \cdot \exp\left(\frac{e\phi(\mathrm{y})}{\mathrm{k_B T}}\right). \tag{3.5}$$

The charge density in the semiconductor is calculated using the Poisson equation:

$$\frac{\mathrm{d}^2\phi}{\mathrm{dy}^2} = -\frac{\rho(\mathrm{y})}{\varepsilon_0\varepsilon_\mathrm{r}} \tag{3.6}$$

with the charge density $\rho(\mathrm{y}) = e\left(\mathrm{p}_\phi(\mathrm{y}) - \mathrm{p}_0 - (\mathrm{n}_\phi(\mathrm{y}) - \mathrm{n}_0)\right)$, the electric permittivity of the vacuum ε_0 and the relative permittivity of the semiconductor ε_r. $\rho(\mathrm{y})$ can be expressed using equations 3.4 and 3.5. Integration of equation 3.6 from the bulk ($\phi(\mathrm{y} \to \infty) = 0$) to the gate dielectric/semiconductor interface ($\phi(\mathrm{y} = 0) = \phi_\mathrm{S}$) yields:

$$\int_0^{\phi_S} \frac{d^2\phi}{dy^2} d\phi =$$

$$-\frac{e}{\varepsilon_0 \varepsilon_r} \int_0^{\phi_S} \left\{ p_0 \cdot \left[\exp\left(-\frac{e\phi(y)}{k_B T} \right) - 1 \right] + n_0 \cdot \left[\exp\left(\frac{e\phi(y)}{k_B T} \right) - 1 \right] \right\} d\phi. \tag{3.7}$$

Together with Gauss' Law $Q_S = -\varepsilon_0 \varepsilon_r E_S$, where E_S is the electric field created by the charge density Q_s at the surface, and the utilization of the relation [71]

$$\int_0^{\phi_S} \frac{d^2\phi}{dy^2} d\phi = \frac{1}{2} E_S^2, \tag{3.8}$$

the surface charge density Q_S is derived:

$$(Q_S)^2 = \left(\pm \sqrt{2\varepsilon_0 \varepsilon_r k_B T} \right)^2 \cdot p_0 \cdot \left[\exp\left(-\frac{e\phi_S}{k_B T} \right) + \frac{e\phi_S}{k_B T} - 1 \right] +$$

$$\left(\pm \sqrt{2\varepsilon_0 \varepsilon_r k_B T} \right)^2 \cdot n_0 \cdot \left[\exp\left(\frac{e\phi_S}{k_B T} \right) - \frac{e\phi_S}{k_B T} + 1 \right]. \tag{3.9}$$

In Figure 3.2b on page 23 the room-temperature surface charge per unit area for a p-doped semiconductor is shown for a hole density of 10^{17} cm^{-3} and an electron density of 10^{11} cm^{-3}. The graph consists of five regions and describes the typical behavior of an n-channel MOSFET. Excess holes are accumulated at the gate dielectric/semiconductor interface if a negative surface potential is applied (**accumulation**). For zero surface potential, the so called **flat-band** condition is fulfilled and there is no band bending at the interface. A small positive potential causes the **depletion** of free holes (which exist in the semiconductor due to the doping) followed by a **weak inversion**, where the concentration of electrons becomes larger than the concentration of holes. For a high positive potential the region of **strong inversion** is reached and electrons are induced at the gate dielectric/semiconductor interface.

3.1.2 Adaptability to intrinsic (organic) semiconductors

Surface charge density for intrinsic semiconductors

Equation 3.9 describes the surface-charge density for a p-doped semiconductor. However, neglecting unintentional impurity doping by external factors, organic semiconductors are considered as intrinsic semiconductors. For equal concentrations of electrons and holes,

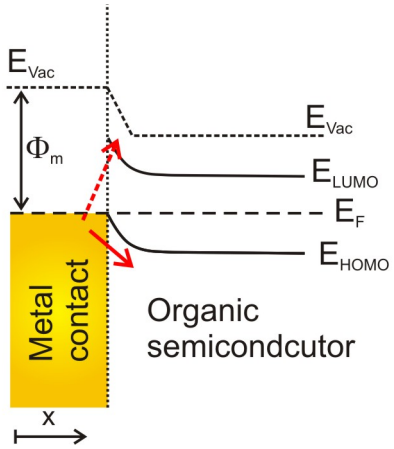

Figure 3.3: Contact metal/semiconductor interface. The schematic indicates a small (ohmic) contact barrier for the transfer of charge carriers from the metal into the HOMO, but a large contact barrier into the LUMO of the organic semiconductor. This interface is useful to realize p-channel transistors.

$p_0 = n_0 = n_i$, equation 3.9 reads:

$$Q_S = \pm\sqrt{2\varepsilon_0\varepsilon_r k_B T} \cdot \sqrt{n_i \cdot \left[\exp\left(-\frac{e\phi_S}{k_B T}\right) - \exp\left(\frac{e\phi_S}{k_B T}\right)\right]}. \tag{3.10}$$

The room-temperature surface charge per unit area as a function of the surface potential for an intrinsic semiconductor is illustrated in Figure 3.2b. Depending on the sign of ϕ, either electron or hole accumulation is possible. Depletion or inversion regions are not present, since these would require the existence of donors or acceptors. Note, that it is not immediately clear where the accumulated charge carriers are coming from. It may be appropriate to consider the source contact as a reservoir for the accumulated charge carriers, so that the energy barrier between the organic semiconductor and the metal contacts should be as small as possible to allow the accumulation of a large charge-carrier density in the organic semiconductor.

Metal/organic semiconductor contact

At the interface between a metal and an (in)organic semiconductor an energy barrier is usually formed. The height of the barrier depends on the work functions of the two materials [70, 73, 74]. For inorganic transistors, for instance single-crystalline silicon MOSFETs, the barrier between the source/drain contacts and the semiconductor is adjusted by selectively doping the contact area [75, 76]. In contrast, for organic TFTs contact doping is challenging and will be introduced in detail in chapter 8. In organic TFTs the barrier height can be reduced by selecting a metal with a work function that matches the LUMO or HOMO energy of the organic semiconductor [77]. Figure 3.3 illustrates the contact

barrier between a metal and an organic semiconductor, indicating a small contact barrier to the HOMO and a larger contact barrier to the LUMO. In this situation, the TFT is operated as a p-channel transistor, while operation as n-channel transistor is greatly suppressed. This explains the p-channel character of many organic semiconductors (the HOMO energy level is typically 4-5 eV, and most often high-work-function metals are utilized for the source/drain contacts). A second mechanism leading to the unipolar character of many organic semiconductors is the stronger trapping rate for electrons at the gate dielectric/semiconductor interface [78].

3.1.3 Drain-current calculation

Equation 3.9 describes the charge density in the transistor channel in general. This charge density is influenced not only by the gate-source voltage $\phi(y)$, but also by the potential $\psi_{\mathrm{DS}}(\mathrm{x})$ along the channel, which is created by the the drain-source voltage. Therefore, the channel potential becomes a two-dimensional function $\phi(\mathrm{x,y}) = \phi(\mathrm{y}) - \psi_{\mathrm{DS}}(\mathrm{x})$. To derive an analytical expression for the drain current $\mathrm{I_D}$ along the channel, several assumptions must be made:

- The gate/gate dielectric/semiconductor capacitor is an ideal MIS capacitor, which means there are neither interface traps nor mobile oxide charges present. To account for this ideal assumption, the gate-source voltage $\mathrm{V_{GS}}$ is replaced by $(\mathrm{V_{GS}} - \mathrm{V_{th}})$, with the threshold voltage $\mathrm{V_{th}}$ accounting for a vanishing surface-charge density on the gate dielectric surface (flat band condition).
- There are no diffusion currents in the transistor and only drift currents are considered.
- The longitudinal electric field $\mathrm{E_x}$ along the channel is much smaller than the transverse electric field $\mathrm{E_y}$ across the gate dielectric (gradual-channel approximation).

With these assumptions and by replacing the potential $\phi(\mathrm{y})$ with $\phi(\mathrm{x,y})$ in equation 3.9, the following relation is obtained:

$$(\mathrm{Q_S})^2 = \left(\pm\sqrt{2\varepsilon_0\varepsilon_\mathrm{r}\mathrm{k_B T}}\right)^2 \cdot \mathrm{p_0} \cdot \left[\exp\left(-\frac{e\left(\phi_\mathrm{S} - \psi_{\mathrm{DS}}(\mathrm{x})\right)}{\mathrm{k_B T}}\right) + \frac{e\phi_\mathrm{S}}{\mathrm{k_B T}} - \exp\left(\frac{e\psi_{\mathrm{DS}}}{\mathrm{k_B T}}\right)\right] +$$

$$\left(\pm\sqrt{2\varepsilon_0\varepsilon_\mathrm{r}\mathrm{k_B T}}\right)^2 \cdot \mathrm{n_0} \cdot \left[\exp\left(\frac{e\left(\phi_\mathrm{S} - \psi_{\mathrm{DS}}(\mathrm{x})\right)}{\mathrm{k_B T}}\right) - \frac{e\phi_\mathrm{S}}{\mathrm{k_B T}} - \exp\left(-\frac{e\psi_{\mathrm{DS}}}{\mathrm{k_B T}}\right)\right]. \tag{3.11}$$

Finally, the drain current is given by

$$\mathrm{I_D} = \mathrm{W} \cdot \mathrm{Q_S}(\mathrm{x}) \cdot \mathrm{v}(\mathrm{x}) \tag{3.12}$$

with v(x) being the average charge-carrier velocity given by $v = E \cdot \mu_0$ and W the transistor channel width. Since the drain current must be constant along the channel, this equation can be transformed to

$$I_D = \frac{W}{L} \int_0^L Q_S(x) \cdot v(x) dx = \frac{\mu_0 W}{L} \int_0^L Q_S(x) \cdot E(x) dx =$$

$$\frac{\mu_0 W}{L} \int_0^{V_{DS}} Q_S(x) \cdot \frac{d\psi_{DS}}{dx} dx \tag{3.13}$$

using $E = -\frac{d\psi}{dx}$. In the most general form equation 3.11 must be inserted into 3.12 and the drain current is derived by integration, but even for the assumptions of intrinsic semiconductors ($p_0 = n_0 = n_i$) this equation has complicated solutions. Following standard textbooks a simple solution can be derived using the *charge-sheet model* [70]. This model assumes a charge sheet as accumulation layer controlled by a plate capacitor consisting of the gate electrode, the gate dielectric, and the semiconductor. The thickness of this charge sheet is zero, so that the potential drop across it is also zero. Then, the surface charge density Q_S is given by

$$Q_S(x) = C_i \cdot V(x) = C_i \cdot (V_{GS} - V_{th} - \psi_{DS}(x)) \tag{3.14}$$

with C_i being the gate capacitance per unit area of the gate dielectric. Inserting equation 3.14 into equation 3.12 yields:

$$I_D = \frac{\mu_0 W}{L} \int_0^{V_{DS}} C_i \cdot (V_{GS} - V_{th} - \psi_{DS}(x))\, d\psi_{DS}. \tag{3.15}$$

Integration of equation 3.15 under the assumption of an electric-field-independent mobility leads to the transistor drain current in the on-state. Strictly speaking, the assumption of a field-independent mobility fails for organic semiconductors [72, 79, 80], but for simplicity it will be used for now. Details on the field-dependent mobility are discussed in section 6.2.2. Figure 3.4 shows the drain current as a function of the gate-source voltage (**transfer characteristics**) and the drain current as a function of the drain-source voltage (**output characteristics**). The on-state region described by the charge-sheet model is composed of two regions, the linear and the saturation region.

On-state region - linear current

For small drain-source voltages, $V_{DS} < V_{GS} - V_{th}$, the voltage drop along the transistor channel is homogeneous and equation 3.15 reads:

$$I_D = \frac{\mu_0 W C_i}{L} \cdot \left(V_{GS} - V_{th} - \frac{V_{DS}}{2} \right) \cdot V_{DS} \ \text{(linear region)}. \tag{3.16}$$

This equation describes the drain current in the linear region of operation (Figure 3.4).

On-state region - saturation current

When the drain-source voltage is increased and approaches $V_{GS} - V_{th}$, the accumulated charge density underneath the drain contact is more and more reduced by the drain potential. For $V_{DS} = V_{GS} - V_{th}$, the charge density under the drain contact is zero and the conducting channel is pinched-off. A further increase of the drain-source voltage beyond $V_{GS} - V_{th}$ shifts this pinch-off point towards the source contact, causing the drain current to saturate (Figure 3.4). By replacing V_{DS} with $V_{GS} - V_{th}$ in equation 3.16, the drain current in the saturation region is obtained:

$$I_D = \frac{\mu_0 W C_i}{2 \cdot L} \cdot (V_{GS} - V_{th})^2 \quad \text{(saturation region)}. \tag{3.17}$$

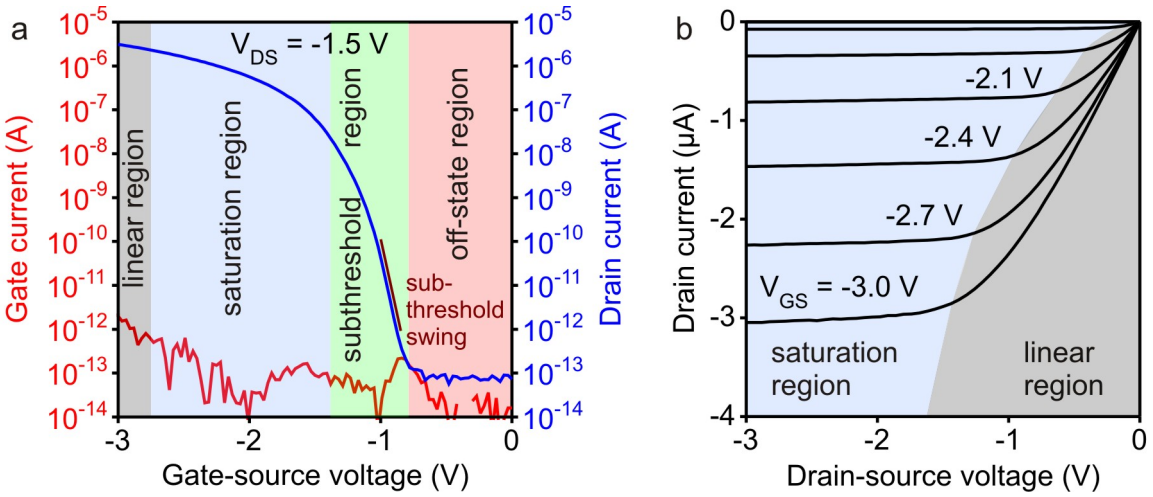

Figure 3.4: Electrical characteristics of thin-film transistors operated in accumulation. a) The transfer characteristics show the drain current as a function of the gate-source voltage (for a fixed drain-source voltage). In the characteristics the off-state, the subthreshold, the saturation and the linear region can be distinguished. The gate current indicates the current measured at the gate electrode: it is determined by the insulating properties of the gate dielectric. b) The output characteristics display the drain current as a function of the drain-source voltage for several gate-source voltages. Ideally, the drain current increases linearly and saturates for $V_{DS} > V_{GS} - V_{th}$.

Subthreshold region

The charge density in the subthreshold region (and in the off-state region) depends non-linearly on the gate-source voltage, so that the charge-sheet model is not applicable. Although it is in principle possible to derive an analytical solution for this region using

equations 3.11 and 3.15, this will not be done here. In the subthreshold region the charge density depends exponentially on the gate-source voltage [70]:

$$I_D \sim \exp\left(\frac{e\phi_S}{k_B T}\right), \tag{3.18}$$

so that a small change of the gate-source voltage has a drastic effect on the drain current. The slope of the drain current in this region is denoted as subthreshold swing S and is described by [3]:

$$S \equiv (\ln 10) \cdot \frac{kT}{q}\left(\frac{C_i + qN_{traps}}{C_i}\right), \tag{3.19}$$

where N_{traps} is the trap density at the gate dielectric/semiconductor interface. A steep subthreshold swing is useful to drive the transistors within a small gate-source-voltage range. Note, that the theoretical minimum for the subthreshold swing at room temperature is 60 mV/decade [70]. From equation 3.19 it is obvious that a steep subthreshold swing is achievable by increasing the gate dielectric capacitance or by utilizing a gate dielectric which forms less trap states at the gate dielectric/semiconductor interface. The subthreshold swing is a useful measure of the interface trap density.

Off-State region

In the off-state region the drain current does not significantly depend on the drain-source voltage (exceptions are discussed in section 3.3.1), but strongly depends on the doping concentration in the semiconductor. In this region the drain current is described by [71]:

$$I_D \sim \sqrt{\frac{N_V n_A}{n_D}} \cdot \sqrt{V_{GS}} \cdot V_{DS}. \tag{3.20}$$

Gate current

So far, the gate current I_G has been neglected, since the dielectric in the MIS capacitor (section 3.1.1) has been considered as a perfect insulator. In reality, however, there is a gate (leakage) current which is undesired for two reasons. First, the leakage current of one transistor multiplied by the number of transistors employed in an integrated circuit and multiplied by the supply voltage equals the minimum standby power consumption, which should be minimized. Second, a large leakage current limits the on/off current ratio (see next section) which should be, however, as large as possible, especially for transistors employed in active-matrix displays.

Organic TFTs require a charge-carrier density of about $10^{12} - 10^{13}\,\mathrm{cm}^{-2}$ in the transistor channel in the on-state. Ideally, this charge density should be accumulated at low voltages

(< 10 V) to allow the integration in portable devices. According to the charge-sheet model, the gate capacitance per unit area is given by

$$C_i = \frac{Q_S}{V_{GS} - V_{th}} = \frac{\varepsilon_0 \varepsilon_r}{t_{diel}}, \tag{3.21}$$

which can be solved for the thickness t_{diel} of the gate dielectric. Assuming an ε_r of 5-10 and an operation voltage of 10 V the gate dielectric thickness should be:

$$t_{diel} = \frac{\varepsilon_0 \varepsilon_r}{Q_S} \cdot V_{GS} \sim 1 - 10\,\text{nm}. \tag{3.22}$$

In this work, a hybrid gate dielectric with a thickness of ∼5 nm and a leakage current density of 10^{-5} $\frac{A}{cm^2}$ at ∼3 V was utilized [12], so that the gate current of the transistors is typically around ∼1-10 pA, depending on the exact transistor geometry. Details on this particular gate dielectric are introduced in chapter 4.

3.1.4 Transistor parameters

The current-voltage characteristics of transistors are useful to extract different characteristic parameters, such as the transconductance, the field-effect mobility of the charge carriers, the subthreshold swing, the threshold voltage, the on/off current ratio, the contact resistance, and the sheet resistance [3, 72, 81, 82]. These parameters are useful to benchmark transistors manufactured with different technologies, or transistors manufactured within the same technology, but with different lateral dimensions.

Transconductance

The transconductance is defined as $g_m = \frac{\partial I_D}{\partial V_{GS}}$ (unit: Siemens, S) and describes the response of the drain current to changes of the gate-source voltage. To compare transistors of different channel width W, the transconductance is often normalized to the channel width (unit: S/m). According to equations 3.16 and 3.17 one derives:

$$g_m = \frac{\mu_0 W C_i}{L} \cdot V_{DS} \;\; (\text{linear region}) \tag{3.23}$$

and

$$g_m = \frac{\mu_0 W C_i}{L} \cdot (V_{GS} - V_{th}) \;\; (\text{saturation region}). \tag{3.24}$$

The transconductance is inversely proportional to the channel length. In other words, the transconductance can be increased by reducing the channel length of the transistor. This

is important for the dynamic operation of transistors (section 3.2).

Field-effect mobility

Similar to the transconductance the field-effect mobility of the charge carriers (or simply mobility) in the transistor channel can be extracted. From equations 3.16 or 3.17 one gets:

$$\mu_{\mathrm{lin}} = \frac{\mathrm{L}}{\mathrm{WC_i V_{DS}}} \frac{\mathrm{dI_D}}{\mathrm{dV_{GS}}} \quad (\text{linear region}) \tag{3.25}$$

and

$$\mu_{\mathrm{sat}} = \frac{2\mathrm{L}}{\mathrm{WC_i}} \left(\frac{\mathrm{d}\sqrt{\mathrm{I_D}}}{\mathrm{dV_{GS}}} \right)^2 \quad (\text{saturation region}). \tag{3.26}$$

Subthreshold swing

The subthreshold swing was already introduced and is given by equation 3.19.

Threshold voltage

In single-crystalline silicon MOSFETs the threshold voltage is defined as the gate-source voltage at the onset of inversion in the transistor channel. Organic transistors do not operate in inversion, so that this definition is not useful. Instead, the threshold voltage in organic TFTs is often considered as the gate-source voltage necessary to fill all traps states at the gate dielectric/semiconductor interface. For a transistor with an intrinsic semiconductor the threshold voltage is expressed as [70]:

$$\mathrm{V_{th}} = \phi_{\mathrm{ms}} - \frac{\mathrm{Q_f}}{\mathrm{C_i}} \tag{3.27}$$

where ϕ_{ms} is the work function difference between the metal and the semiconductor and $\mathrm{Q_f}$ describes in general the density of trap at the gate dielectric/semiconductor interface or in the gate dielectric itself. Ideally, ϕ_{ms} is zero and there are no fixed charges present in the gate dielectric, so that the threshold voltage is zero. In reality, the mismatch between the work function of the gate metal and the semiconductor, and the presence of traps generate a non-zero threshold voltage. In the literature on organic TFTs the threshold voltage is often estimated by extrapolating the drain current in the transfer characteristics to the intersection with the x-axis (in the linear region of the transfer characteristics). An alternative approach utilized in this work is the constant-current approach [83], where the threshold voltage is defined as the gate-source voltage for a certain drain current (100 pA in this work). A detailed study on various threshold voltage extraction methods is found in [84].

On/off current ratio

The ratio between the on-state drain current (maximum V_{GS}) and the off-state drain current ($V_{GS} = 0$ V) is called on/off current ratio. In terms of technical applications this ratio should be as large as possible. Typical values for the on/off current ratio are six to seven orders of magnitude.

Contact and sheet resistance

The contact and sheet resistance are discussed in sections 3.3.2 and 6.2 in detail.

3.2 Dynamic operation

In digital applications the on-state and off-state of the transistor resemble the logic states "1" and "0". Switching the transistor between these two states requires the gate capacitance to be charged or discharged. During this charging or discharging process a displacement gate current i_G flows into or out of the gate electrode. This displacement gate current is proportional to the charge on the gate electrode q_G and inversely proportional to the time interval ∂t of the charging and discharging process. The change in charge on the

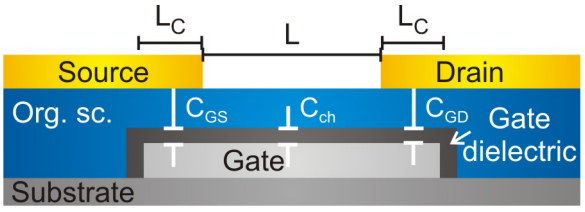

Figure 3.5: Schematic of the capacitances in a thin-film transistor. The image illustrates the intrinsic capacitance of the accumulation channel and the parasitic capacitances created by the overlap between the source and drain contacts and the gate electrode. The operation frequency of the transistor can be increased by reducing the parasitic capacitances and/or the channel capacitance.

gate electrode is given by $\partial q_G = C_G \cdot \partial v_{GS}$, with the gate capacitance C_G. The gate capacitance is the sum of the parasitic gate-to-source and gate-to-drain capacitances (C_{GS} and C_{GD}, Figure 3.5), and the channel capacitance (C_{ch}, Figure 3.5):

$$C_G \sim C_{GS} + C_{ch} + C_{GD} \sim C_i \cdot W \cdot (L + 2 \cdot L_C) \tag{3.28}$$

Thus, the displacement gate current reads

$$i_G = \frac{\partial q_G}{\partial t} = C_G \frac{\partial v_{GS}}{\partial t} = j2\pi \cdot f \cdot C_G \cdot v_{GS} \tag{3.29}$$

and is proportional to the frequency f of the gate-source voltage (j: imaginary number) [3]. The total gate current equals the sum of the frequency-dependent displacement gate current and a frequency-independent contribution given by the gate leakage current through the gate dielectric. However, the latter is usually much smaller than the displacement gate current and can be neglected here. The drain current is frequency-independent and given by $i_D = g_m v_{GS}$. The current gain of a transistor, which is defined as the ratio of the drain current and gate current, consequently decreases with increasing frequency. If the ratio of the two numbers is unity, the transistor is no longer properly working and this situation is defined as the cut-off frequency f_T:

$$f_T = f\left(\frac{I_D}{I_G} = 1\right) = \frac{g_m}{2\pi \cdot C_G} = \frac{\mu \cdot V_{DS}}{2\pi \cdot L \cdot (L + 2 \cdot L_C)}. \tag{3.30}$$

Equation 3.30 shows that the cut-off frequency can be increased by using an (organic) semiconductor with a larger mobility or by applying higher voltages. However, the evolution of the mobility in organic semiconductors over the last years does not promise orders-of-magnitude improvements in the near future (Figure 1.1 on page 11). Also, high supply voltages are not realistic for most battery-powered (portable) applications. But equation 3.30 shows that the cut-off frequency can be also increased by reducing the channel length L and the parasitic overlap L_C, and this is one of the objectives of this thesis.

3.3 Nonidealities of the transistor characteristics

3.3.1 Short-channel effects

If the channel length of a transistor is reduced, the thickness of the gate dielectric must also be reduced, in order to keep the ratio between channel length L and gate dielectric thickness t_{diel} well above 10 (ideally $\frac{L}{t_{diel}} \geq 20$). This requirement was first rationalized by Dennard and co-workers for silicon MOSFETs and became a cornerstone in the continuous scaling of silicon MOSFETs [75]. If the dielectric scaling requirement is ignored, the influence of the lateral electric field ($\frac{V_{DS}}{L}$) relative to the transverse electric field ($\frac{V_{GS}}{L}$) in determining the electric potential along the transistor channel becomes too large. This generates several undesired short-channel effects [85]:

- At a gate-source voltage at which the carrier density in the channel should be near zero and the drain current should be suppressed (i.e., when the transistor is expected to be turned "off"), large amounts of carriers will still enter the channel, so the off-state drain current will be large and the transistor will have a small on/off current ratio and the transistor turns on earlier (drain-induced barrier lowering, DIBL).

- The shift of the pinch-off point towards the source contact for higher drain-source voltages reduces the effective channel length, especially for transistors with a small channel length. Therefore, the channel resistance is drastically reduced and the drain current does not saturate, but increases continuously (channel length modulation, CLM).

In short, ignoring the dielectric scaling requirement leads to a large off-state current, small on/off current ratio, poor current saturation, and threshold-voltage roll-off. This can be seen in many previous reports of short-channel organic TFTs [14, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95].

3.3.2 Contact resistance

Origin of the contact resistance

The drain current of organic transistors is often limited by the energy barrier at the interface between the semiconductor and the source/drain contacts. This barrier is reduced by choosing a source/drain contact metal with a proper work function that matches the LUMO or HOMO energy of the organic semiconductor [77, 96]. For example, pentacene p-channel TFTs (electron affinity of ∼4.9 eV) with gold contacts (work function ∼4.9 eV) have a contact resistance of ∼ 2 kΩ·cm which is much smaller compared to p-channel pentacene transistors with calcium contacts (work function ∼2.9 eV) having a contact resistance of ∼ 85 kΩ·cm [77]. It is important to note that the metal work function consist of a contribution from the bulk and a contribution from the surface-dipole created by the electron cloud tails [97]. As a result, the energy barrier does not simply correspond to the energy difference of the HOMO (or LUMO) and the metal work function. This has been explored by photo-electron spectroscopy (PES) [98]. Note that the sample geometries utilized for PES significantly differ from those utilized in real transistors, so that the contact properties revealed by PES can be different from the contact properties extracted using organic TFTs. For example, the interface between gold (work function of 4.9 eV) and pentacene (HOMO energy of ∼4.9 eV) provides good contacts (low contact resistance) for organic TFTs, even though PES studies have revealed an interface dipole of 1 eV [23, 99], which would be expected to prohibit any charge flow between the contact metal and the organic semiconductor.

3.3.3 Consequences on the transistor parameters

The total transistor resistance R_{TFT} equals the sum of the contact resistance R_C and the channel resistance R_{ch}:

$$R_{TFT} = R_C + R_{ch},$$

with the contact resistance being the sum of the source resistance and the drain resistance: $R_C = R_S + R_D$. To account for the contact resistance in equations 3.16 and 3.17, V_{DS} is replaced by $V_{DS} - I_D R_C$ [100], which yields in the linear region:

$$I_{D,lin} = \frac{\mu_0 W C_i}{L} \cdot \left(V_{GS} - V_{th} - \frac{V_{DS}}{2} + \frac{I_D R_C}{2} \right) \cdot (V_{DS} - I_{D,lin} R_C) \,. \tag{3.31}$$

In the linear region for $V_{GS} - V_{th} \gg \frac{V_{DS}}{2} - \frac{I_{D,lin} R_C}{2}$, and by solving equation 3.31 for I_D using equation 3.25, the effective (field-effect) mobility in the linear region is obtained as follows [100]:

$$\mu_{eff,lin} = \mu_0 \frac{L}{L + \mu_0 W C_i R_C (V_{GS} - V_{th})}. \tag{3.32}$$

In analogy one can write for the drain current in saturation:

$$I_{D,sat} = \frac{\mu_0 W C_i}{2 \cdot L} \cdot (V_{GS} - V_{th})^2 - (I_{D,sat} R_C)^2. \tag{3.33}$$

Replacing V_{DS} with $V_{GS} - V_{th}$ in equation 3.31, and using equation 3.26, the effective mobility in the saturation region [100] can be written as:

$$\mu_{eff,sat} = \mu_0 \left(1 - \left(\frac{\mu_0 W C_i R_C (V_{GS} - V_{th})}{L + \mu_0 W C_i R_C (V_{GS} - V_{th})} \right)^2 \right). \tag{3.34}$$

Equations 3.32 and 3.34 describe the effective (field-effect) mobility μ_{eff} extracted from the transistor characteristics including the influence of the contact resistance. From these equations it can be seen that the effective mobility is reduced for a short transistor channel, because the portion of the drain-source voltage dropping at the contacts significantly increases. The intrinsic (field-effect) mobility μ_0 indicates the mobility that would be measured in the TFT configuration if the contact resistance was negligible.

4 Manufacturing process

Organic TFTs are thin-film transistors in which the semiconductor is a thin layer of conjugated organic molecules. These can be either small molecules or polymers. In this thesis only small-molecule organic TFTs are considered. The other three TFT layers can be either manufactured from organic or inorganic materials. For example, the gate electrode can be either an inorganic metal (Al, Cr, Mo, ...) or an inherently conducting (i.e., chemically doped) conjugated polymer (e.g. PEDOT:PSS). The gate dielectric can be an insulating metal oxide (e.g. AlO_x) or an insulating polymer (e.g. PVP, [101]). The source/drain contacts are usually made from a noble metal (Au, Pd) or using a conducting poylmer. There are a variety of methods to pattern and deposit these individual layers. For this work it is important to vary the channel length L of the transistors over a wide range. Therefore several common techniques which are useful to pattern source/drain contacts of organic TFTs will be briefly discussed and the advantages/disadvantages of these technqiues explained. For more details on these methods, but in particular on the different fabrication methods for gate electrodes, gate dielectrics, and organic semiconducting layers, the interested reader is referred to the literature [102, 103, 104].

The source/drain contacts of organic TFTs are ususally prepared by photolithography or electron-beam lithography in combination with the thermal evaporation of metals in vacuum and wet-chemical etching or lift-off. Using these lithography techniques organic

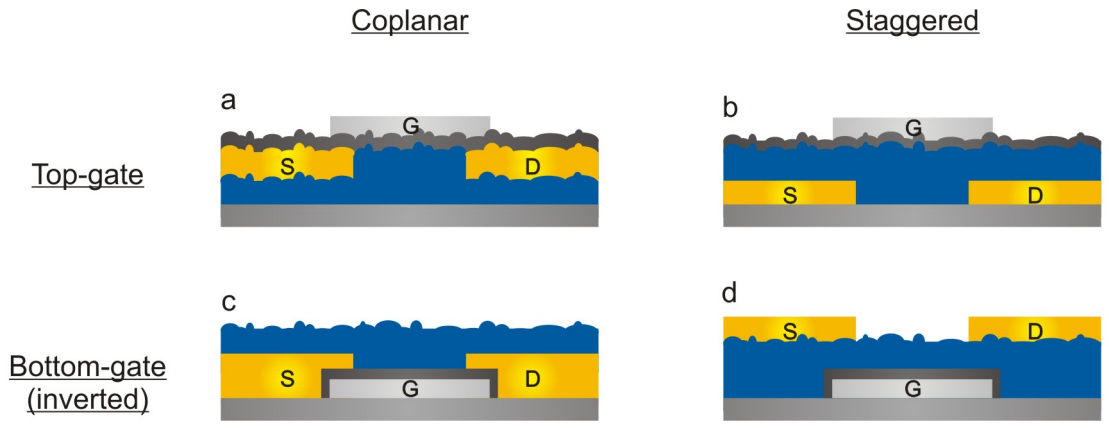

Figure 4.1: Schematics of thin-film transistor geometries. a) Top-gate coplanar, b) top-gate staggered, c) bottom-gate (inverted) coplanar and d) bottom-gate (inverted) staggered geometry.

TFTs with a source/drain contact spacing (channel length) down to 0.01 µm have been realized by several groups [88, 105, 106, 107, 108]. However, all of these TFTs were made in the top-gate staggered or bottom-gate (inverted) co-planar geometry (Figure 4.1b,c). For both of these geometries, the source/drain contacts are fabricated prior to the deposition of the organic semiconductor. This has the advantage that the sensitive thin-film morphology of the organic semiconductor is not disturbed by high temperatures (resist baking) or organic solvents (wet-chemical etching, lift-off) as employed in standard lithography techniques. For example, Ji and co-workers reported on the degradation of pentacene TFTs when exposed to elevated temperatures ($>$ 80°C) [109] and Gundlach and co-workers reported on a phase transition of pentacene films and a degradation of pentacene TFTs when exposed to organic solvents [22]. Therefore it is not useful to fabricate source/drain metal contacts by standard lithography on top of thin films of small-molecule organic semiconductors (top-gate coplanar, bottom-gate (inverted) staggered geometry, Figure 4.1a,d).

In addition, coplanar TFTs (Figure 4.1a,c) typically have a large contact resistance [23, 79, 110] unless the work function of the source/drain contacts is modified using self-assembled monolayers [111, 112] or thin conducting oxide layers [113, 114]. This is particularly problematic in short-channel TFTs.

The top-gate geometry (especially top-gate staggered geometry, Figure 4.1b) is useful for polymer TFTs [11, 14], but not for TFTs based on small-molecule semiconductors, because thin films of small-molecules often exhibit a rough three-dimensional growth (in contrast to the smooth amorphous films of spin-coated polymers), so that the gate dielectric/semiconductor interface would be also very rough and the mobility small.

In this work, the focus is therefore placed on top-contact TFTs (bottom-gate (inverted) staggered geometry, Figure 4.1d) which benefit from a smooth dielectric/semiconductor interface and typically have a smaller contact resistance than coplanar TFTs [23] (also: appendix D, Figure D.1). In top-contact TFTs the source/drain contacts are usually manufactured by evaporating the contact material through a shadow mask [10, 115, 116]. This has the advantage that neither resist baking (high temperatures) nor lift-off (organic solvents) are required. Shadow masks are usually made of a thin sheet of metal or polyimide into which openings are fabricated by a high-energy laser beam. The laser spot size limits the resolution to $\sim$10 µm, which is sufficient for low-end applications (e.g. e-ink displays), but not for a detailed study on aggressively reduced lateral dimensions.

It is possible to pattern staggered transistors (including top-contact TFTs) with much smaller channel length by soft lamination [89, 108], self-aligned printing (SAP) [14, 117], or sub-femtoliter inkjet printing [118]. However, for soft-lamination the mask alignment is problematic, SAP is only useful for top-gate polymer TFTs, and sub-femtoliter printing is limited to Ag as the contact metal.

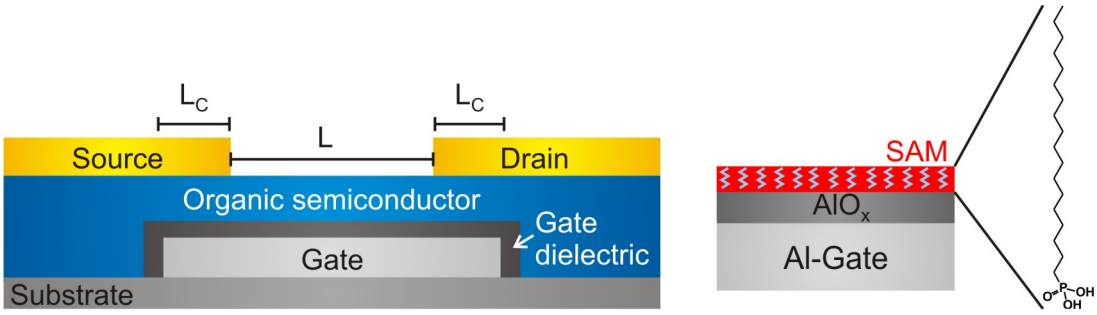

Figure 4.2: Schematic of a top-contact organic thin-film transistor. The images illustrate the 30 nm thick aluminum bottom gate, the hybrid gate dielectric consisting of the ∼4 nm thick plasma-grown aluminum oxide layer and the ∼2 nm thick self-assembled monolayer, the 30 nm thick organic semiconductor, and the 25 nm thick gold top contacts. The channel length L and the contact length L_C are labeled.

In this thesis a top-contact TFT process combining high-resolution silicon stencil masks [119, 120] with the vacuum-deposition process introduced in [12, 121] has been developed. The silicon stencil masks were provided by the Instiut für Mikroelektronik (IMS Chips, Stuttgart). With this method the lateral transistor dimensions have been reduced down ∼1 µm [122]. The combination of high-resolution stencil masks with thermal evaporation in vacuum is often denoted as **stencil lithography** [123, 124] and details on this process are discussed in section 4.1.

This stencil lithography process is not yet useful to fabricate top-contact transistors with a channel length below ∼1 µm. For such extremely scaled transistors an approach reported by the RIKEN group has been adopted [25, 92, 93, 125], in which electron-beam lithography is utilized to create a suspended resist bridge. This suspended resist bridge is created prior to the organic semiconductor deposition and later serves as a high-resolution shadow mask for the top-contact patterning. The manufacturing process is discussed in section 4.2.

4.1 Stencil lithography process

Stencil lithography has been shown to be useful to pattern magnetic films [126], nanometer-scale scanning sensors [127], metallic nanowires [123, 128, 129], and the source/drain contacts of organic transistors [130, 131]. The stencil-mask-paterrned top-contact organic TFTs reported in the literature have lateral dimensions as small as 2 to 4 µm [130, 131]. They were processed on thermally oxidized silicon substrates in a global-back-gate configuration [130] or with a focus on full wafer-scale fabrication of organic TFTs [131].

Stencil lithography (and shadow masking in general) is compatible with a variety of substrates, such as rigid silicon wafers, glass substrates, or flexible polyethylene naphthalate foils [10, 131, 132, 133]. In this work silicon wafers or glass substrate have been utilized.

For dynamic measurements, non-conducting substrates (e.g. glass) are more useful than conducting silicon to avoid large parasitic capacitances between the probe pads and the conducting substrate.

A schematic overview of a top-contact organic transistor manufactured in this work is illustrated in Figure 4.2. For the local (patterned) gate electrode 30 nm thick aluminum was thermally evaporated through a stencil mask using a current-heated wolfram coil as evaporation source (10-12 Å/s deposition rate , 10^{-6} mbar base pressure). AFM measurements on 30 nm thick aluminum on a silicon wafer and on glass (Corning Eagle 2000) show a surface roughness of ∼1 nm for both substrates (not shown here). Therefore, no differences in the electrcial characteristics of the transistors fabricated on either of the substrates are expected. The probe pads of the aluminum gate electrodes are covered with a thermally evaporated 30 nm thick film of gold (1-2 Å/s deposition rate, 10^{-6} mbar base pressure). This prevents the formation of an insulating layer on the probe pads (next process step) that would prevent a low-resistance contact between the probe pad and the probe needle [12].

The gate dielectric is fabricated in a two-step process. First, the aluminum gate electrode is briefly exposed to an oxygen plasma (200 W power, 0.17 mbar base pressure) to increase the thickness of the native AlO_x layer to 3.6 nm and the density of hydroxyl groups on the surface. The hydroxyl groups are necessary to enable the condensation from solution of a self-assembled monolayer (SAM) on top of the AlO_x in the second process step [12]. The self-assembling molecules (dissolved in a 2-propanol) consist of an alkyl chain with a phosphonic acid anchor group [$C_nH_{(2n+1)}PO(OH)_2$)] (Figure 4.2). For the formation of the SAM on the Al/AlO_x surface the substrate must be kept in the molecule solution at least for an hour, followed by a brief rinsing with 2-propanol and 10 minutes post-baking on a hot plate at ∼100°C. The SAM drastically reduces the leakage current density through the plasma-oxidized AlO_x and completes the formation of the low-temperature hybrid gate dielectric [12]. Note, that the phosphonic acid anchor groups do not condensate on a gold surface, so that the aluminum/gold probe pads are still accessible for electrical measurements.

Here, phosphonic acids with alkyl chain lengths of 14 arbon atoms (C14-SAM, 1.7 nm molecule length) and 18 carbon atoms (C18-SAM, 2.1 nm molecule length) have been utilized. The total hybrid-gate-dielectric thickness (molecule length and plasma-grown AlO_x layer) is 5.3 nm and 5.7 nm with a capacitance of 810 nF/cm^2 and 700 nF/cm^2, respectively. These capacitances are sufficiently high to operate the transistors at voltages as small as 3 V. The gate dielectric has a low surface energy of 20 mN/m [134] that is useful to achieve a high charge-carrier mobilitiy in small-molecule films deposited on top of this gate dielectric [3]. A hydrophobic gate dielectric surface also reduces the hysteresis in the current-voltage characteristics of organic transistors [135].

In the beginning of this thesis, the gate dielectrics were based on the C18-SAM, but further experiments indicated a slightly reduced gate leakage current for the C14-SAM gate dielectric (probably owing to a denser packing of the molecules on the surface). Consequently, the process was adapted to the C14-SAM gate dielectric, but the effects on the charge-carrier mobility are negligible [136].

For the organic semiconductor a 30 nm thick layer of DNTT is deposited by sublimation in vacuum from a current-heated molybdenum source (0.5 Å/s deposition rate, $\sim 10^{-6}$ mbar base pressure). The substrate is kept at an elevated temperature of 60°C during the deposition. The elevated substrate temperature facilitates the formation of well-ordered organic films with a high charge-carrier mobility [137].

The source/drain contacts consist of 25 nm thermally evaporated gold (deposition rate 0.3 Å/s, $\sim 10^{-6} - 10^{-7}$ mbar base pressure) and complete the organic TFT. Gold has a work function of 5.0 eV, so that a low energy barrier to the HOMO of DNTT ((5.3±0.1) eV, [35]) is ensured and the transistors are operated as **p-channel TFTs**. The HOMO/LUMO gap is ∼2 eV, so that an injection of electrons from the gold contacts into the LUMO is unlikely.

Figure 4.3a,b shows scanning electron microscopy (SEM) images of parts of a high-resolution stencil mask. The apertures in the 20 µm thick silicon membrane were produced by electron-beam lithography and angle-controlled dry etching [119, 120] (also: appendix A). The mask features seen in these images were designed to define the source and drain contacts of a top-contact organic TFT with a channel length of 0.8 µm. The SEM image in Figure 4.3c depicts the 0.8 µm long channel of a DNTT transistor fabricated by stencil lithography. The atomic force microscopy (AFM) image in Figure 4.3d illustrates 25 nm thick gold source/drain contacts on a 30 nm thick aluminum film. The contact length L_C was 2 µm.

A main concern of stencil lithography are variations between the defined patterns in the stencil mask and the deposited patterns on the substrate [123, 128]. These effects are discussed in appendix B on page 117.

4.2 Electron-beam lithography process

To realize top-contact organic transistors with a sub-µm channel length, the RIKEN group developed a clever electron-beam lithography (EBL) process to create a suspended resist bridge on the substrate **prior to the organic semiconductor deposition** [25, 92, 93, 125]. This resist bridge then serves as a high-resolution shadow mask to define the source/drain contacts after the organic semiconductor deposition. With this process they realized top-contact transistors with a channel length of 150 nm. For the gate electrode a

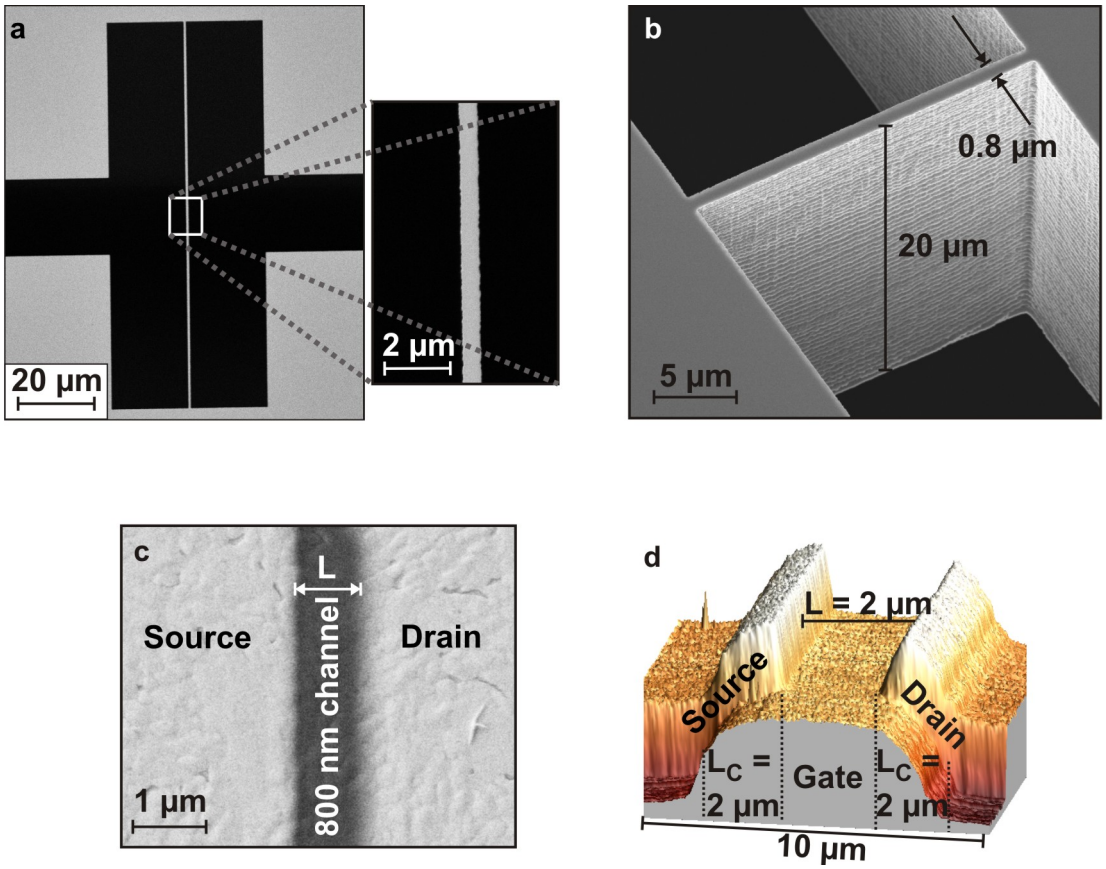

Figure 4.3: High-resolution silicon stencil masks and patterned structures. a, b) Scanning electron microscopy (SEM) images showing parts of a high-resolution stencil mask. The apertures in the 20 µm thick silicon membrane were produced by electron-beam lithography and angle-controlled dry etching. The mask features seen in these images were designed to define the source/drain contacts of a top-contact organic TFT with a channel length of 0.8 µm. c) SEM image of the channel region of a TFT with a channel length of 0.8 µm. d) Atomic force microscope image of 25 nm thick gold source /drain contacts on a 30 nm thick aluminum gate electrode (which was also patterned using a high-resolution silicon stencil mask). The contact length L_C is 2 µm.

heavily doped silicon wafer with a thin layer of thermally grown SiO_2 as the gate dielectric was employed. In this work, their process was further developed to realize top-contact organic TFTs with a channel length of less than 100 nm on local (patterned) metal gate electrodes.

To avoid charging of the substrate during the electron-beam lithography process silicon wafers with a 100 nm thick thermally grown SiO_2 layer are used as a substrate. Areas for the local metal gate electrodes are defined on the SiO_2 surface by EBL and 30 nm thick aluminum is deposited by thermal evaporation. In the same manner as described above, a hybrid gate dielectric consisting of AlO_x and a SAM is realized. During the oxygen-plasma treatment and the SAM formation, the areas outside the aluminum gate electrodes remain covered by electron-beam resist. This ensures the formation of the hydrophobic SAM only

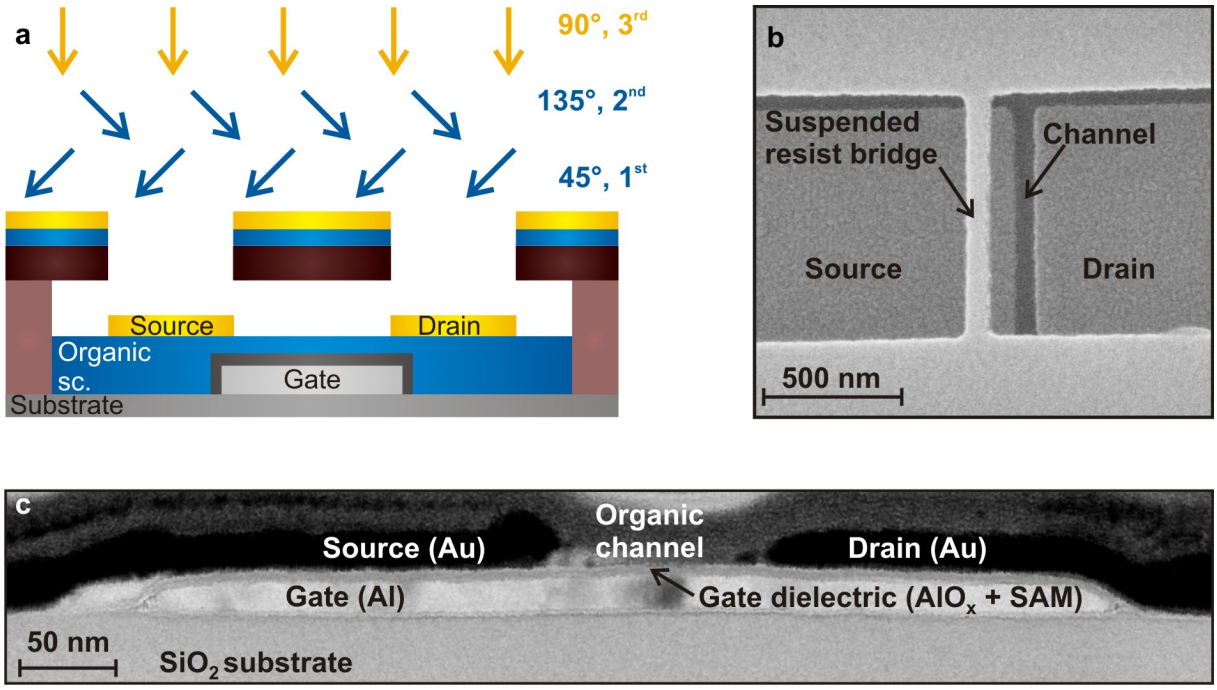

Figure 4.4: Electron-beam lithography based process. a) The schematic illustrates the nanoscale transistor manufacturing process. The suspended resist bridge is fabricated prior to the deposition of the organic semiconductor, which is evaporated by two angled evaporations (45° and 135°) to grow a closed film underneath the resist bridge. During the gold source/drain top-contact deposition the suspended resist bridge acts as high-resolution shadow mask. b) Scanning electron microscopy image showing the suspended resist bridge and the patterned gold source/drain contacts. During imaging the sample was tilted. c) Cross-section transmission electron microscope image of a completed nanoscale top-contact transistor. The channel length is 100 nm and the contact length is 200 nm.

on the gate electrodes, while the rest of the substrate is left hydrophilic. The latter is useful, since a hydrophobic substrate would be more difficult to coat with resist for the following electron-beam lithography process step. After formation of the AlO_x/SAM gate dielectric, the electron-beam resist is stripped in order to remove the aluminum outside of the gate areas. Several tests have been conducted to confirm that the lift-off process does not harm the Al/AlO_x/SAM structure [138, 139].

To fabricate a suspended resist bridge that later acts as a shadow mask, the substrate is then coated with three layers of electron-beam resist. The first (bottom) layer is a 400 nm thick PMMA[1]/MMA[2] copolymer layer with high electron-beam sensitivity (dose to clear: 25 µC/cm^2). The second (middle) layer is a 120 nm thick PMMA 200K layer and the third (top) layer is a 140 nm thick PMMA 950K layer, both having a low electron-beam sensitivity (dose to clear: 100 µC/cm^2). If the source/drain contact spacing is less than about 500 nm, the dose of electrons back-scattered from the substrate surface during

[1]Poly(methyl methacrylate)
[2]Methyl methacrylate

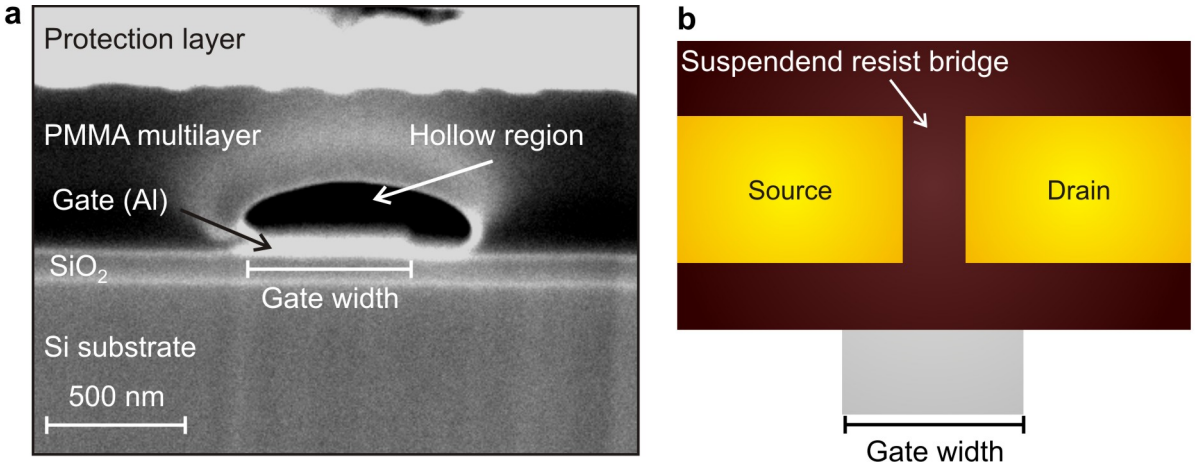

Figure 4.5: Electron-beam lithography process limitation. a) The scanning electron microscopy image shows a local electron-beam-lithography processed gate electrode, covered with three layers of PMMA resist. The hollow region above the local gate electrode forms because the PMMA does not wet the hydrophobic surface of the SAM-covered gate electrode. This hollow region affects the stability of the suspended resist bridge if the gate width is larger than 600 nm. b) Schematic to illustrate the gate width in more detail.

the electron-beam process is sufficient to expose the high-sensitivity bottom layer in the (nominally unexposed) regions between the source/drain contacts. The low-sensitivity middle and top layers (between the source/drain contacts) are not affected by the back-scattered electrons during this exposure. As a result, a suspended resist bridge is formed across the channel region of the transistors during development of the resist stack (i.e., the bottom layer is dissolved, while the middle and top layers remain, Figure 4.4a). In the next step, the organic semiconductor layer is deposited. In order to form a continuous layer underneath the suspended resist bridge, the substrate is tilted at angles of 45° and 135° while the organic semiconductor is deposited by sublimation in vacuum. The total thickness of the semiconductor film for these transistors is 20 nm (10 nm deposited at an angle of 45°, plus 10 nm deposited at an angle of 135°, without breaking the vacuum, Figure 4.4a). Finally, the 25 nm thick source/drain contacts are deposited by thermal evaporation with the substrate held at an angle of 90° and with the suspended resist bridge serving as a high-resolution shadow mask to define the channel length of the transistors (Figure 4.4a,b). Figure 4.4c shows a cross section transmission electron microscopy image of a completed nanoscale top-contact organic transistor. The channel length is 100 nm and the contact length is 200 nm. During the deposition of the gold source/drain contacts, it is critically important that the deposited gold layer breaks across the edges of the resist patterns, so that the gold that remains on the electron-beam resist outside the active TFT area is disconnected from the contact pads for source, drain, and gate. To confirm this, the electrical resistance between the various probe pads and the gold layer on the resist was measured, which is greater than $10^{12}\,\Omega$.

It must be noted that this process works only for a narrow gate width (∼600 nm). The SEM image in Figure 4.5 shows a cross-sectional view of the PMMA resist on top of a narrow local gate electrode. A hollow region above the SAM-covered gate electrode, caused by PMMA resist detaching from the hydrophobic surface, is visible. As long as the gate width is less than 600 nm, this hollow region is not affecting the process. However, for a larger gate width the stability of the suspended resist bridge is affected. This effect limits the maximum contact length L_C to a few hundred nanometers.

Conclusion

The two manufacturing processes described in this chapter allow the fabrication of top-contact organic TFTs with channel length L and contact length L_C ranging from 0.1 µm to 200 µm. The properties of these transistors are reported in the following chapters.

5 Morphology and crystal structure of DNTT films

The charge-transport efficiency in organic semiconductor films depends critically on the molecular order. For many vacuum-deposited conjugated organic molecules, for instance pentacene, it is known that the molecules form three-dimensional films on low-energy surfaces [63]. The molecules stand with the long axis approximately perpendicular on the insulating substrate, which leads to a strong interaction between neighboring molecules within the organic film. This is a beneficial arrangement for the charge transport in organic transistors from the source to the drain contact. The molecular order of vacuum-deposited DNTT films on the low-energy gate dielectrics utilized in this work is investigated in the following chapters.

5.1 Morphology

The atomic force microscopy (AFM) amplitude images in Figure 5.1 indicate the morphology of DNTT films with a nominal thickness of 5, 10, and 30 nm deposited on silicon/aluminum/aluminum oxide/SAM (Si/Al/AlO_x/C14-SAM) substrates. The substrates were kept at 60°C during the DNTT deposition. For a nominally 5 nm thick film (Figure 5.1a) an island-like growth of DNTT on the substrate is visible. Approximately one half of the substrate is covered by DNTT islands and the other half remains uncovered. When the film thickness is increased to nominally 10 nm, almost the whole substrate is covered with DNTT (Figure 5.1b) and only small areas remain uncovered. For a film thickness of 30 nm (Figure 5.1c), as utilized for the transistors in this work, the DNTT film covers the whole substrate.

Figure 5.2a contains the AFM height and amplitude images of a nominally 30 nm thick film of DNTT grown on a Si/Al/AlO_x/SAM substrate. The three-dimensional growth and the polycrystalline structure are visible. The height profile along the arrow in the AFM images (Figure 5.2a,b) resolves terrace steps with a height of ∼1.6 nm. This step size corresponds well to the calculated length of a DNTT molecule (1.59 nm, calculated using CS Chem 3D Pro) and indicates that the molecules stand approximately perpendicular

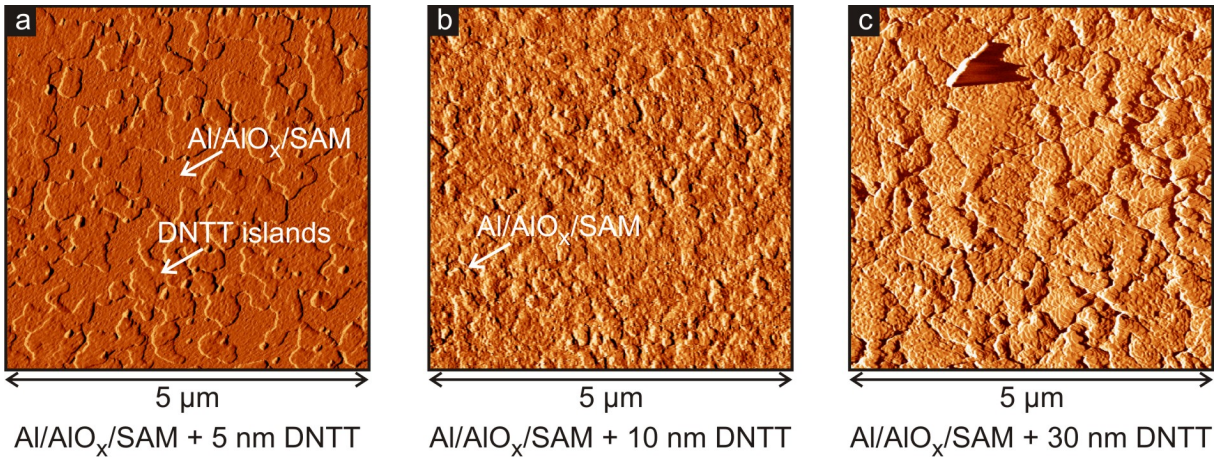

Figure 5.1: Morphology of DNTT films with different nominal thickness grown on a gate dielectric. The atomic force microscopy (amplitude) images show the growth of DNTT films with a nominal thickness of 5, 10, and 30 nm deposited by thermal evaporation onto a silicon/aluminum/aluminum oxide/C14-SAM substrate. During the deposition, the substrate was kept at 60°C. For a nominally 5 nm thick film (a), the island-like growth of DNTT on the substrate is clearly visible. If the film thickness is increased to 10 nm, almost the whole substrate is covered with DNTT (b). For a film thickness of 30 nm (c), as utilized for the transistors studied in this work, the DNTT film is covering the whole substrate.

on the surface, similar to pentacene films.

5.2 Crystal structure

The X-ray diffraction (XRD) pattern of a 30 nm thick DNTT film grown on a Si/Al/-AlO$_x$/SAM substrate is shown in Figure 5.2c. Using the Bragg equation [140]

$$2 \cdot \mathrm{d} \cdot \sin\theta = \mathrm{m} \cdot \lambda$$

with the diffraction angle θ, the wavelength λ (Cu K$_\alpha$, 0.154 nm) and the diffraction order m, an out-of-plane lattice spacing d of 16.3 Å is calculated. This result is in good agreement with measurements on DNTT single-crystals [26] and confirms the conclusion drawn from the AFM images (section 5.1), namely that the molecules stand approximately perpendicular on the surface without a significant tilt angle. It is noteworthy that the Bragg peaks are resolved to the 7th order which is indicating a high degree of out-of-plane order within the DNTT film (perpendicular to the surface), similar to previous reports on polycrystalline pentacene films [140]. The Scherrer-formula [140]

$$\triangle\theta = \frac{0.9 \cdot \lambda}{\mathrm{B} \cdot \cos\theta}$$

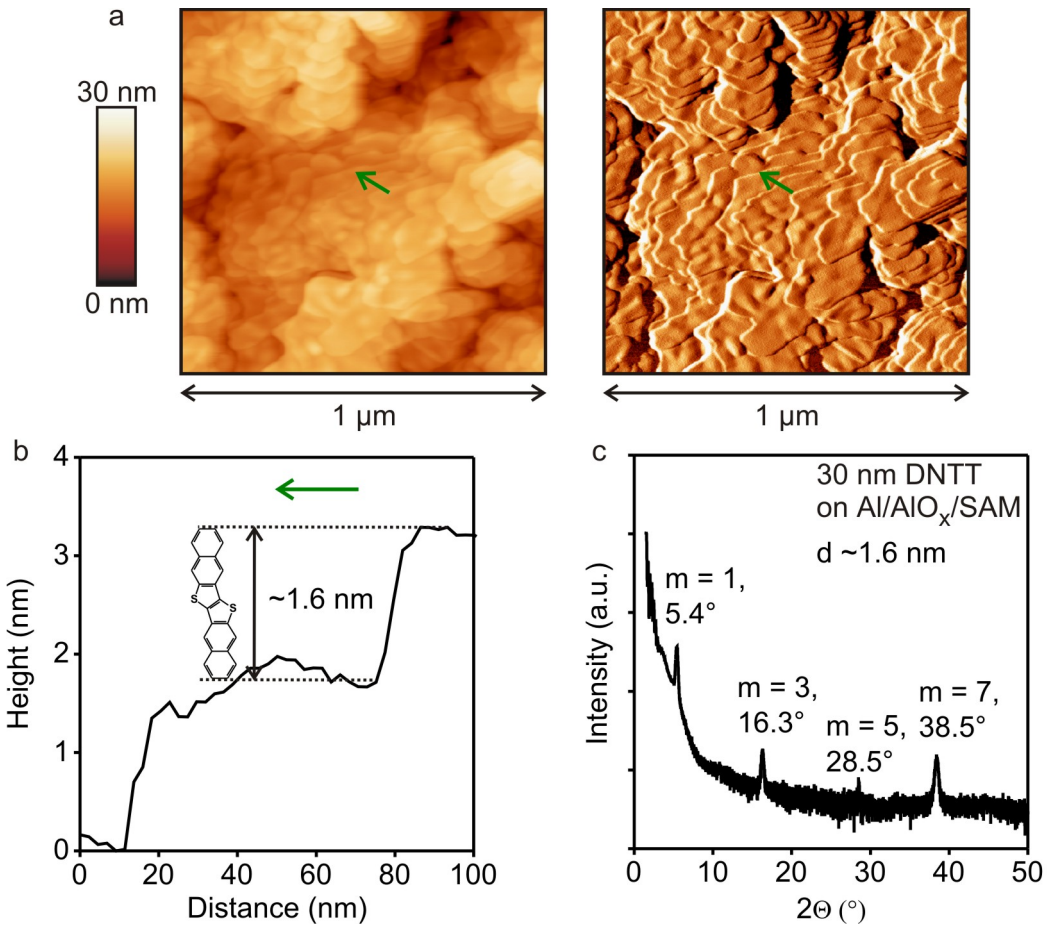

Figure 5.2: DNTT films grown on a gate dielectric analyzed using AFM and XRD. a) Atomic force microscopy (AFM) topography and amplitude images of a nominally 30 nm thick film of DNTT grown on a silicon/aluminum/aluminum oxide/SAM substrate. The three-dimensional polycrystalline growth is seen. b) Height profile corresponding to the AFM images shown in (a). Each of the terrace steps is $\sim$ 1.6 nm in height, which corresponds to the length of one DNTT molecule. c) X-ray diffraction pattern of a 30 nm thick DNTT film grown on a silicon/aluminum/aluminum oxide/SAM substrate. The calculated lattice plane distance is 16.3 Å and the average crystallite height is 29 nm. Since the diffraction peaks are resolved to the 7th peak, the lattice plane order perpendicular to the surface is very high.

is useful to estimate the average crystallite height B, where $\triangle\theta$ is the full width at half maximum (FWHM) and θ the angle corresponding to the analyzed peak in the XRD pattern. An average height of 29 nm is extracted from the data, which is in good agreement with the nominal DNTT film thickness of 30 nm (measured during the deposition using a quarz crystal balance). XRD patterns of polycrystalline thin films of pentacene often exhibit the diffraction peaks of two different phases, the *thin-film* phase and the *bulk* phase, with the out-of-plane lattice distances varying by $\sim$1 Å [22]. The XRD pattern of the DNTT film in Figure 5.2c shows no evidence for different phases, though one cannot fully rule out that under different growth conditions additional phases might appear.

Note that the AFM technique only elucidates the surface of the DNTT films and the XRD

measurement probes the bulk properties of the DNTT film. So far, all results indicate a three-dimensional growth and that the molecules stand approximately perpendicular on the surface. However, none of these methods is useful to probe specifically the gate dielectric/semiconductor interface, which is the critical region for the charge transport in an organic transistor under operation. For instance, in the case of the organic semiconductor hexadecafluorocopperphthalocyanine (F_{16}CuPc) it has been discovered that the molecules form a disordered interface layer when deposited onto an insulating surface [67, 68]. This disordered interface layer is the reason for the poor electrical performance of F_{16}CuPc TFTs. However, this interface layer is buried under a highly ordered polycrystalline layer during subsequent stages of deposition. This has caused significant confusion in the past, since AFM and XRD only reveal the highly ordered regions (bulk and surface) of the film. A similar effect cannot be completely ruled out for the DNTT films studied in this work. However, due to the high mobilities achieved in this work (which are within a factor of 2-3 of single-crystals made from DNTT) the formation of such a disordered interface layer is unlikely.

Conclusion

The molecular order of DNTT molecules on a silicon/aluminum/aluminum oxide/SAM substrate was investigated using AFM and XRD. The measurements indicate a three-dimensional growth of DNTT and show that the molecules stand perpendicular on the surface. The obtained results are in good agreement with previous studies on DNTT single-crystals [34] and indicate a beneficial arrangement for the charge transport in organic transistors.

6 DNTT transistors: downscaling of the lateral dimensions

In the previous chapter it was shown that the morphology of vacuum-deposited DNTT films promotes the charge transport in DNTT TFTs. The electrical characteristics of DNTT TFTs with large channel length and large contact length are discussed in section 6.1. For large lateral dimensions the total resistance of the transistor is dominated by the channel resistance, and nonlinearities (section 3.3) are not expected. The obtained results will be considered as reference values for DNTT TFTs with reduced lateral dimensions that will be discussed later. In section 6.2 the contact resistance of the DNTT TFTs is discussed in detail and the transmission line method is introduced. This method can be used to analyze the relation between the contact length and the contact resistance. TFTs with a channel length of less than 100 nm and their physical limitations are reported in section 6.3. Concluding remarks on the reproducibility of the stencil-lithography process are found in section 6.4.

6.1 Transistor characteristics

The electrical characteristics of a p-channel top-contact DNTT TFT with a channel length L of 60 µm, a channel width W of 200 µm, and a contact length L_C of 200 µm are shown in Figure 6.1. From the characteristics a transconductance of 0.04 $\frac{S}{m}$, an effective (field-effect) mobility for holes of 2.8 $\frac{cm^2}{Vs}$ (in the saturation region) and 2.6 $\frac{cm^2}{Vs}$ (in the linear region), an on/off current ratio of 10^6, a subthreshold swing of 100 mV/decade, and a threshold voltage V_{th} of -1.3 V for both drain-source voltages (-0.1 V and -1.5 V) can be extracted. The gate current is a few pA for V_{GS} = 0 V and increases to 400 pA for V_{GS}= -3 V. When the large overlap area between the gate electrode and the source/drain contacts of $8 \cdot 10^{-4}$ cm^2 (200 x 200 µm^2 for each contact) is considered, this corresponds to a reasonably small gate-current density of $\sim 10^{-6}$ $\frac{A}{cm^2}$. The drain current in Figure 6.1b increases linearly for low drain-source voltages and saturates for $V_{DS} > V_{GS} - V_{th}$. The channel length of this TFT is large, so that the channel resistance dominates over the contact resistance and nonlinearities are not observed. The extracted values for the effective mobility and the on/off current ratio of this low-voltage transistor are in good

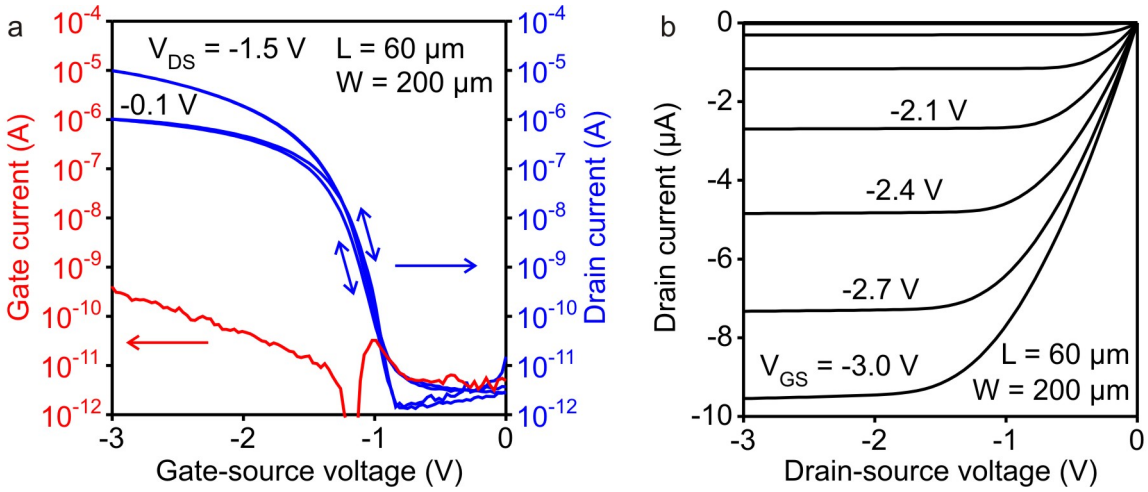

Figure 6.1: Transfer and output characteristics of a top-contact DNTT TFT. The TFT has a channel length of 60 µm, a channel width of 200 µm, and a contact length of 200 µm. a) From the transfer characteristics a transconductance of 0.04 $\frac{S}{m}$, an effective mobility of 2.8 $\frac{cm^2}{Vs}$, an on/off current ratio of 10^6, a subthreshold swing of 100 mV/decade, and a threshold voltage of -1.3 V for both drain-source voltages are extracted. The gate current density is not larger than 10^{-6} A/cm^2. b) In the output characteristics the drain current increases linearly, and the saturation is pronounced.

agreement with reports on DNTT TFTs which utilized a thick gate dielectric (SiO_2 layer with a SAM of octyltrichlorosilane, and V_{DS},V_{GS} ~60 V) [27].

A hole mobility of ~3 $\frac{cm^2}{Vs}$ is among the highest values reported for polycrystalline organic TFTs. Mobilities up to 7 $\frac{cm^2}{Vs}$ have been reported for pentacene TFTs, however most groups reported mobilities of $\leq$ 1 $\frac{cm^2}{Vs}$ [39, 65, 141, 142, 143, 144, 145, 146]. Sanchez-Carrera and co-workers attributed the large hole mobility in DNTT films to the sulfur atoms. These have a pronounced intermolecular S···S interaction and thus promote a strong interaction between neighboring molecules, so that the charge-carrier mobility is large. But sulfur atoms also introduce a large intramolecular reorganization energy via low-frequency vibrations into the molecule, so that the interaction of neighboring molecules is reduced [35]. However, for DNTT there are only two sulfur atoms per molecule, so that this negative influence is suppressed [35] and higher mobilities compared to pentacene, which has no sulfur atoms in its molecular structure, are expected. Indeed, the mobility in DNTT TFTs is 4-5 times larger compared to pentacene TFTs (0.5 $\frac{cm^2}{Vs}$) that employ the same aspect ratio and manufacturing process [136].

In addition, the anisotropy of the mobility in the ab-plane of DNTT is small [35, 54], so that a direct charge transport from the source to the drain contact, independent of the orientation of the individual crystallites, is likely. For pentacene, the mobility is anisotropic in the ab-plane [147, 148] and the charge carriers might be transported on a more percolated way. This demonstrates the superior charge-transport properties of

DNTT and indicates the great potential of hybrid thiophene-acene semiconductors for organic electronics applications.

6.2 Contact-resistance analysis

The physical reasons for the contact resistance between the metal source/drain contacts and the organic semiconductor have been discussed in the theoretical part of this thesis (section 3.3.2). Common approaches to extract the contact resistance of individual (organic) TFTs are simulations [149, 150], measurements of the local potential along the channel and across the contacts (Kelvin Probe measurements) [151, 152], and four-probe measurements [77].

Another frequently used technique to extract the contact resistance of TFTs is the transmission line method (TLM) [81, 108, 153, 154, 155, 156, 157, 158]. For this method a set of TFTs with different channel lengths is required. In many publications the theoretical aspects of the TLM focus only on the extraction of the contact resistance. This approach is reasonable, since organic TFTs are often fabricated on a global back-gate geometry, so that the contact resistance is the only important parameter. However, the TLM is also useful to extract the sheet resistance of the semiconductor, the contact resistivity, and the transfer length of the TFTs. The impact of the transfer length, which is a characteristic length over which 63% of the current is transferd from the contact into the semiconductor, increases for transistors fabricated on local-gate electrodes [81, 150].

Details on the theoretical aspects of the transmission line method can be found in [81] or in the appendix C on page 121, though the most important equations will be introduced here. According to the TLM the *width-normalized resistance* (for simplicity in the following only *resistance*) of a transistor is described by

$$R_{TFT} \cdot W = R_C \cdot W + R_{sheet} \cdot L \tag{6.1}$$

with the total transistor resistance R_{TFT}, the contact resistance R_C, and the sheet resistance R_{sheet} of the semiconductor. The total contact resistance underneath the source/drain contacts is considered as a resistor network [81, 154, 157] and given by:

$$R_C = \frac{V}{I} = 2 \cdot R_{sheet} \cdot L_T \cdot \coth\left(\frac{L_C}{L_T}\right). \tag{6.2}$$

with the transfer length L_T [81, 150] and the contact length L_C. Equation 6.2 depicts that the contact resistance increases when the contact length is shorter than the transfer

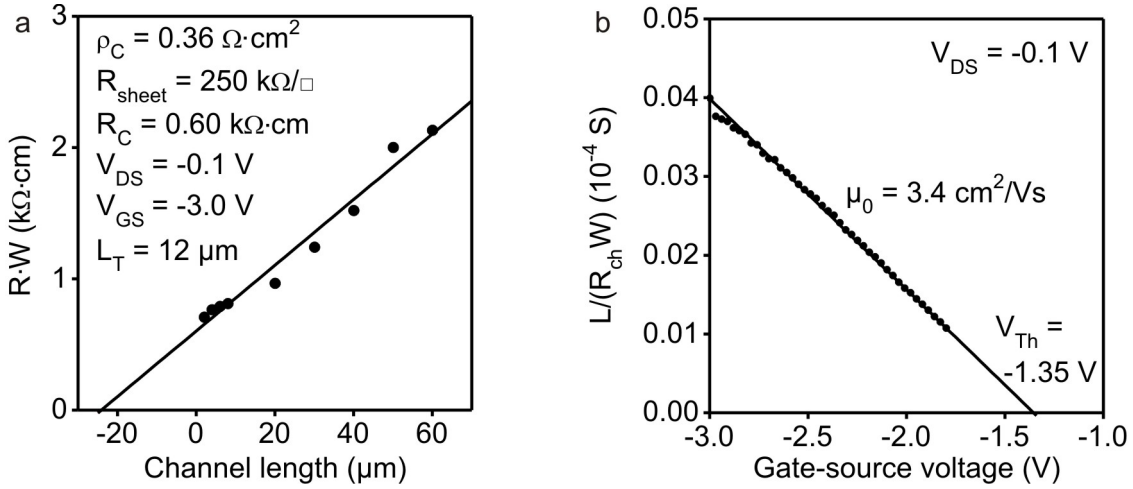

Figure 6.2: Analysis of the transistor resistance and the intrinsic transistor properties. a) Width-normalized total transistor resistance as a function of the channel length. From the least-square linear fit a contact resistance of 600 Ω·cm, a sheet resistance of 250 $\frac{\text{k}\Omega}{\square}$, and a transfer length of 12 µm are extracted. b) Inverse sheet resistance as a function of the gate-source voltage. From the least-square linear fit an intrinsic mobility of 3.4 $\frac{\text{cm}^2}{\text{Vs}}$ and an intrinsic threshold voltage of -1.35 V are extracted.

length. The transfer length itself is described by

$$\text{L}_\text{T} = \sqrt{\frac{\rho_\text{C}}{\text{R}_\text{sheet}}}, \tag{6.3}$$

in which ρ_C is the contact resistivity of the semiconductor/contact interface. Therefore, by plotting the width-normalized resistance of the transistors as a function of the channel length (Figure 6.2a), one can extract the width-normalized contact resistance (in the following called "contact resistance") at the intersection with the y-axis $\text{R}_\text{C} \cdot \text{W} = \text{R}_\text{TFT} \cdot \text{W}(\text{L} = 0)$ and the sheet resistance from the slope of this relation (see appendix C on page 121):

$$\text{R}_\text{sheet} = \frac{\Delta\left(\text{R}_\text{TFT} \cdot \text{W}\right)}{\Delta\text{L}}. \tag{6.4}$$

Furthermore, one can show that

$$\frac{1}{\text{R}_\text{sheet}} = \frac{\text{L}}{\text{R}_\text{ch} \cdot \text{W}} = \mu_0 \text{C}_\text{i} \cdot \left(\text{V}_\text{GS} - \text{V}_\text{th}\right), \tag{6.5}$$

and plot the inverse sheet resistance as a function of the gate-source voltage. This yields the intrinsic mobility μ_0 from the slope of equation 6.5 and the intrinsic threshold voltage V_th from the intersection with the x-axis [153]. Here, *intrinsic* denotes the material properties without the influence of the contact resistance.

Figure 6.2a shows the width-normalized resistance of a series of DNTT TFTs with a channel length L ranging from 1 to 60 µm and a contact length L_C of 200 µm. The values

have been extracted for a low drain-source voltage of -0.1 V, so that an approximately linear relation between the drain current and the drain-source voltage is ensured. A least-square linear fit according to equation 6.1 yields a contact resistance of 600 Ω·cm, a sheet resistance of 250 $\frac{k\Omega}{\square}$, a transfer length of 12 µm, and a contact resistivity of 0.36 Ω·cm^2. In table 6.2 the contact resistance and the transfer length of organic transistors reported in the literature are summarized. The transfer length of 12 µm extracted for the DNTT TFTs in this work is in good agreement with other reports on organic TFTs[1]. The contact resistance of 600 Ω·cm is among the lowest values reported for intrinsic contacts (without doping or a surface modification) for organic TFTs, independent of the device geometry. Compared to top-contact pentacene TFTs (for which a contact resistance of 1000 Ω·cm has been reported [23, 77]), the DNTT TFTs reported in this thesis have a smaller contact resistance. For bottom-contact single-crystal rubrene organic transistors the lowest reported contact resistance is 100 Ω·cm [159] and for bottom-contact polycrystalline pentacene TFTs the contact resistance is usually around $5{\cdot}10^4$ Ω·cm [77, 152]. Considering also reports on contact-modified transistors, the work by Stadlober and co-workers on ozone-treated gold bottom-contacts with a contact resistance of 80 Ω·cm is the lowest value [114]. However, this contact modification technique is not compatible with TFTs based on SAM gate dielectrics, since the plasma treatment would destroy the SAM.

The plot of the inverse sheet resistance as a function of the gate-source voltage to extract the intrinsic mobility and threshold voltage according to equation 6.5 is shown in Figure 6.2b. An intrinsic mobility of 3.4 $\frac{cm^2}{Vs}$ and an intrinsic threshold voltage of -1.35 V are extracted with a least-square linear fit. Note, that the intrinsic mobility extracted by this method only reflects the value for the top-contact polycrystalline DNTT TFTs studied in this work. For example, higher mobilities up to 8.3 $\frac{cm^2}{Vs}$ have been reported for single-crystalline DNTT transistors [69].

6.2.1 Influence of the channel length

In contrast to the contact resistance which is constant for a fixed contact length, the channel resistance is a function of the channel length. Thus, the fraction of the drain-source voltage that drops along the channel decreases when the channel length is reduced, and the extracted effective mobility μ_{eff} becomes smaller than the intrinsic mobility μ_0 (section 3.3.2). Figure 6.3a,b contains the transfer and output characteristics of a DNTT TFT with a channel length of 1 µm, a channel width of 50 µm, and a contact length of 200 µm. The transconductance is 0.5 $\frac{S}{m}$, the effective mobility is 0.7 $\frac{cm^2}{Vs}$ (saturation region) and 0.3 $\frac{cm^2}{Vs}$ (linear region), the on/off current ratio 10^8, the subthreshold swing 100 mV/decade, and the threshold voltage -1.3 V. The extracted effective mobilities are

[1] These publications report only a value for the transfer length, but contain no detailed study on the relation between the contact resistance and the contact length.

Author	Semicondcutor and contact materials	Patterning method	R_C (kΩ·cm)	L_T (µm)
This work	DNTT/gold	shadow mask	0.6	12
Zaumseil [160]	pentacene/gold	soft contact lamination	2	9.7
Richards [150]	F8T2/gold	photolithography	-	15
Hoppe [161]	DH7T/gold	photolithography	∼10	1-5
Gundlach [23]	pentacene/gold	shadow mask	∼3	∼20
Pesavento [77]	pentacene/gold	shadow mask	∼1.3	-
Wang [24]	pentacene/copper	shadow mask	3-4	20

Table 6.2: Contact resistance, transfer length, and sheet resistance of various organic semiconductor/metal interfaces. The data are primarily extracted in the inverted staggered structure.

smaller compared to the reference TFT with a channel length of 60 µm, and the difference is more significant in the linear region. This observation is consistent with the nonlinear drain-current increase in the output characteristics of the TFT with shorter channel length, which is often attributed to the contact resistance. Details on this phenomenon are discussed later. Figure 6.3c shows the effective mobility extracted in the linear region (V_{DS} = -0.1 V) and saturation region (V_{DS} = -1.5 V) for DNTT TFTs with a channel length between 1 µm and 60 µm and a contact length of 200 µm. The effective mobility is constant (∼2.6 $\frac{cm^2}{Vs}$) as long as the influence of the contact resistance on the total transistor resistance is small (L > 30 µm). However, when the channel length is reduced, the effective mobility decreases to ∼0.3 $\frac{cm^2}{Vs}$ for L = 1 µm. The dependence of the effective mobility on the channel length can be described by

$$\mu_{eff}(L) = \frac{\mu_0}{1 + \frac{L_{1/2}}{L}}, \tag{6.6}$$

where $L_{1/2}$ is the channel length at which channel resistance and contact resistance are equal [162]. In other words, for a channel length of $L_{1/2}$, 50% of the applied drain-source voltage drops across the contacts and 50% along the channel. The extracted effective mobility μ_{eff} is half of the intrinsic mobility μ_0, when the channel length is $L_{1/2}$. Using equation 6.6 a channel length $L_{1/2}$ of 14.1 µm in the linear region and 7.4 µm in the saturation region is extracted. The intrinsic mobility μ_0 was taken as 3.4 $\frac{cm^2}{Vs}$ (Figure 6.2b).

The data indicate that the contact-resistance influence is smaller in the saturation region than in the linear region. One possible reason for this observation is the channel pinch-off in the saturation region. For higher drain-source voltages, the accumulated charge-carrier density underneath the drain contact is reduced, so that the channel resistance increases.

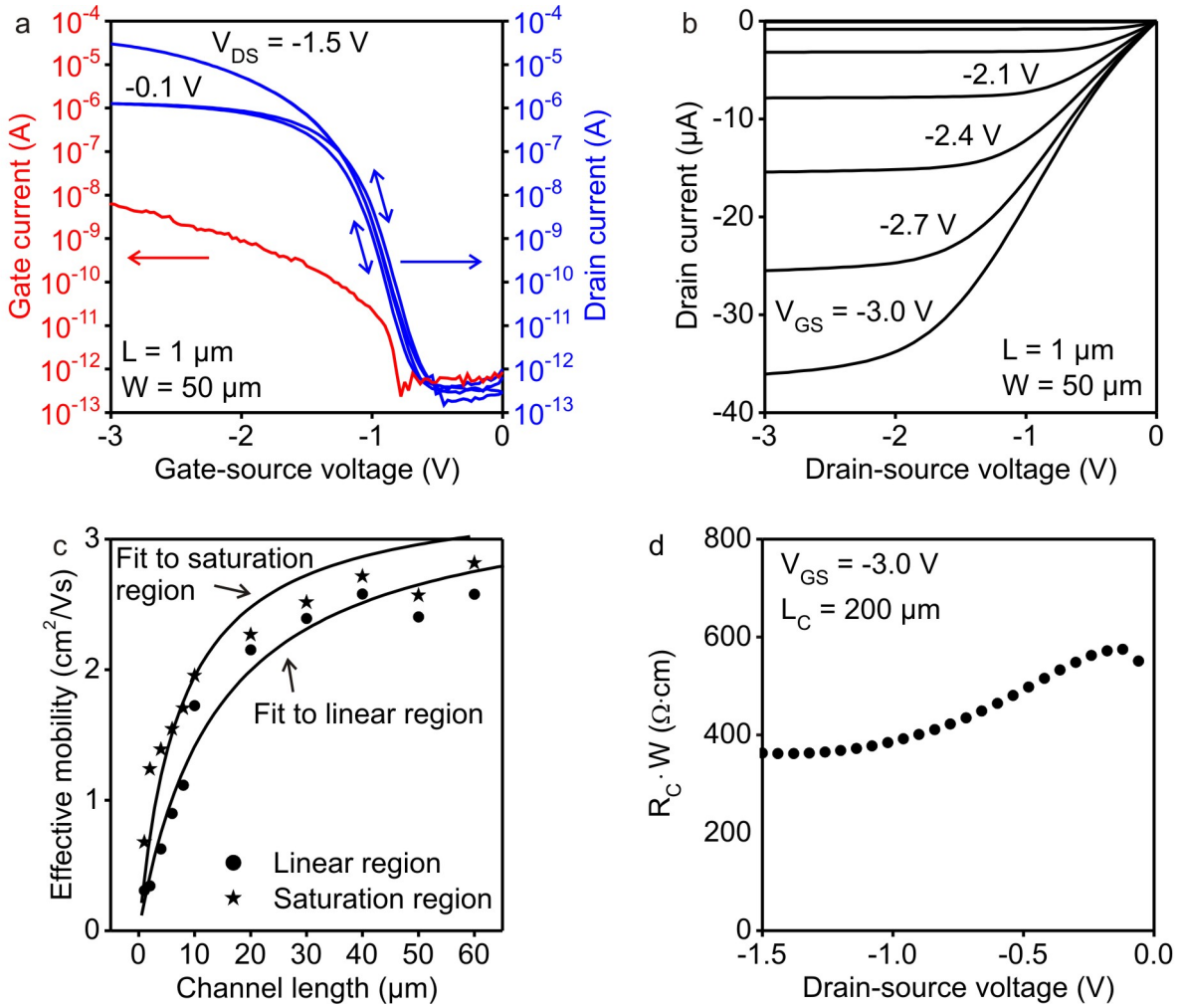

Figure 6.3: Electrical characteristics of DNTT TFTs with reduced channel length. a,b) The TFT has a channel length of 1 µm, a channel width of 50 µm, and a contact length of 200 µm. From the transfer characteristics a transconductance of 0.5 $\frac{S}{m}$, an effective mobility of 0.7 $\frac{cm^2}{Vs}$, an on/off current ratio of 10^8, a subthreshold swing of 100 mV/decade, and a threshold voltage of -1.3 V for both drain-source voltage are extracted. The drain current increases nonlinearly and the saturation is pronounced. c) Effective mobility as a function of the channel length for DNTT TFTs with a channel length between 1 µm and 60 µm extracted in the linear and saturation region of operation. With a simple model the channel length at which channel resistance and contact resistance are equal ($L_{1/2}$) can be derived. In the linear region one obtains 14.1 µm and in the saturation region 7.4 µm for $L_{1/2}$. d) Contact resistance as a function of the drain-source voltage. For increasing drain-source voltage the contact resistance decreases by ∼33%.

Thus, the relative contribution of the contact resistance to the total transistor resistance decreases. But it is also possible that the absolute value of the contact resistance is reduced for higher drain-source voltages, as seen in Figure 6.3d. Possible mechanisms which may account for a voltage-dependent contact resistance will be discussed in the next section.

6.2.2 Influence of the contact length

When the contact length L_C is smaller than the transfer length L_T, the contact resistance increases (equation 6.2). This influence was reported for amorphous silicon TFTs [153, 154] and recently for microcrystalline silicon, carbon-nanotube, and silicon-nanowire field-effect transistors. The transfer length for amorphous and microcrystalline silicon transistors is ∼3-7 µm [5], and for nanotube and nanowire transistors ∼0.1-0.2 µm [8, 9]. To pattern contacts with a contact length of a few microns down to a few hundred nanometers, photolithography and electron-beam lithography are often used in the literature. These techniques are not useful for top-contact organic transistors, since the organic semiconductor is damaged by exposure to organic solvents or heat (section 4.1). Methods like subfemto-liter inkjet printing [118] or high-resolution stencil masks [130, 131] are useful to pattern organic TFTs with a contact length of a few microns. However, these methods have only recently become available, so that no detailed study on the relation between contact length and contact resistance has been reported for organic TFTs so far. The high-resolution stencil masks introduced in section 4.1 make it possible to reduce the contact length to 2 µm. This has allowed us to study the influence of the contact length on the contact resistance in bottom-gate, top-contact organic TFTs in detail for the first time.

DNTT TFTs with a channel length ranging from 1 to 60 µm and a contact length of 200, 20, 5, and 2 µm were fabricated. In Figure 6.4a-c the output characteristics of TFTs with a channel length of 2 µm and a contact length of 200, 20, and 5 µm are shown. An almost ideal linear drain-current increase is seen for the TFT with a contact length of 200 µm, which is much larger than the transfer length of 12 µm. When the contact length is reduced to 20 and 5 µm, i.e. close to and far below the transfer length, the drain current increases nonlinearly with drain-source voltage. The effective mobilities summarized in Figure 6.4d also reflect this observation. In the linear region the effective mobility drops by ∼66% (0.6 $\frac{cm^2}{Vs}$ for L_C = 200 µm; 0.2 $\frac{cm^2}{Vs}$ for L_C = 5 µm) and in the saturation region by ∼20% (0.8 $\frac{cm^2}{Vs}$ for L_C = 200 µm; 0.6 $\frac{cm^2}{Vs}$ for L_C = 5 µm).

Discussion of the nonlinearities

The nonlinear drain-current increase that is seen for instance in Figure 6.4c, is usually attributed to the contact resistance [14, 85, 105, 107]. In the subsequent paragraphs different physical models that may account for this observation are discussed.

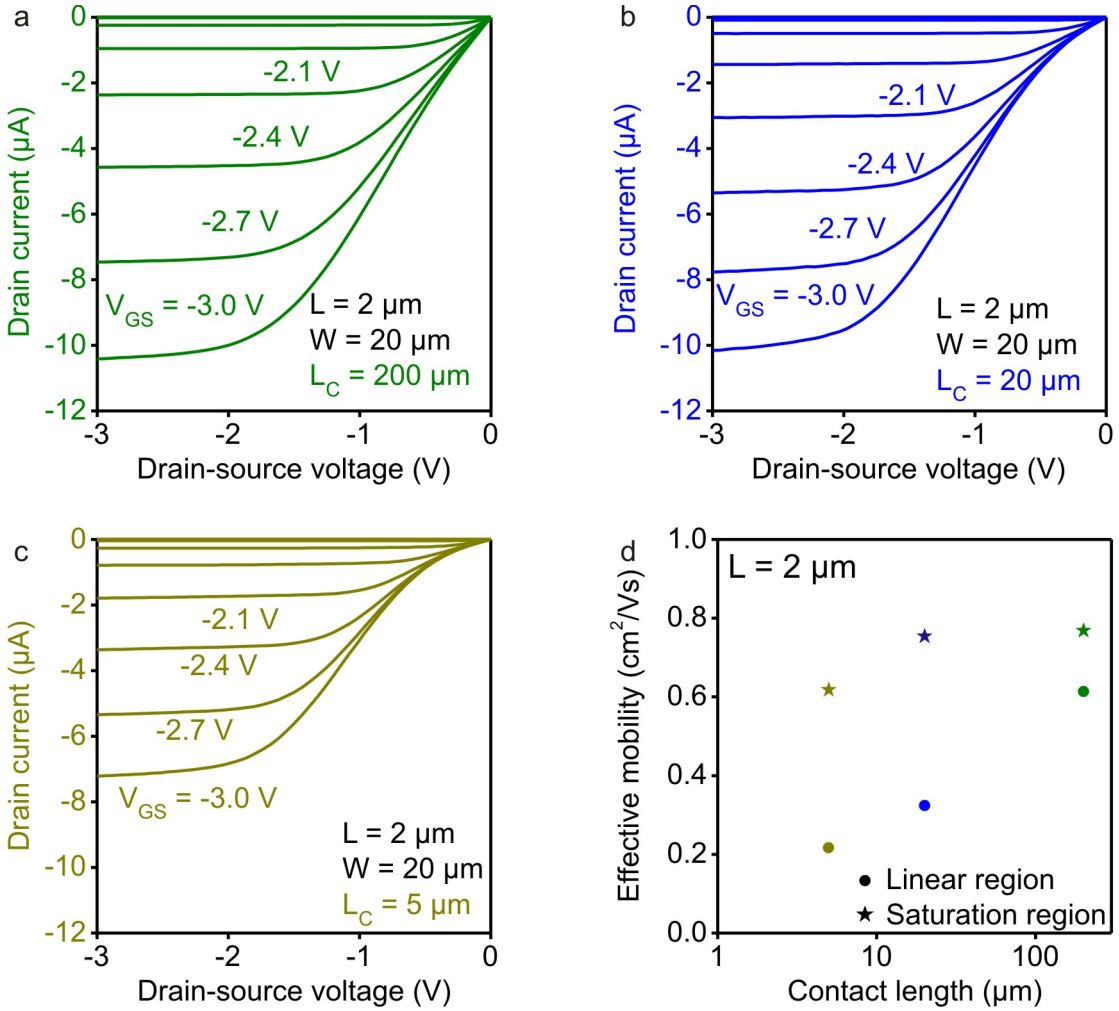

Figure 6.4: Electrical characteristics of DNTT TFTs with reduced contact length. a-c) The DNTT TFTs have a channel length of 2 µm, a channel width of 20 µm, and a contact length of 200, 20, and 5 µm. For a contact length of 200 µm (a) the drain current increases almost linearly with the drain-source voltage. However, when the contact length is reduced (b,c), the nonlinearity in the drain-current increase becomes stronger. This is attributed to a larger influence of the contact resistance. d) Effective mobility of DNTT TFTs with a channel length of 2 µm as a function of the contact length. When the contact length is reduced from 200 to 5 µm the effective mobility in the linear region decreases by ∼66% and in the saturation region by ∼20% .

Schottky barrier at the organic semiconductor/metal interface

Many reports in the literature attribute the nonlinear drain-current increase to the Schottky barrier at the semiconductor/metal interface [23, 149] (Figure 6.5a). Such a barrier produces a superlinear drain-current increase in the forward direction. However, under the assumption of identical Schottky barriers at the source and the drain contact[2], the current in the transistor is always limited by the backward-biased Schottky barrier. Thus,

[2]Since both the source and the drain contact are fabricated within the same process step, this assumption is appropriate.

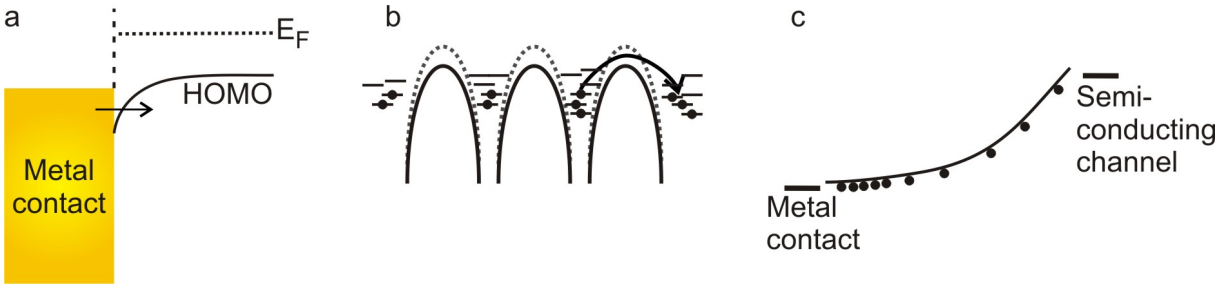

Figure 6.5: Possible mechanisms accounting for the observed nonlinearities in the output characteristics. a) Schottky barrier at the semiconductor/metal interface. A Schottky barrier in forward direction or a Schottky barrier with a field-dependent barrier can account for the nonlinearity observed in the output characteristics. b) Field-dependent mobility (Poole-Frenkel effect) perpendicular to the gate dielectric from the metal contacts down to the accumulation channel. This is also the direction (c-axis) of low mobility within the DNTT film, so that the trap density is indeed expected to be large. A strong electric field reduces the barrier height between the localized states (see schematic), so that the rate of thermally activated charge carriers increases. c) Space charge limited current (SCLC) perpendicular to the gate dielectric from the metal contacts down to the accumulation channel. The model assumes a low contact resistance between the organic semiconductor and the metal, but a non-efficient charge transport along the c-axis.

the nonlinear drain-current increase would not be observable [79]. However, due to image forces which act on the barrier and traps or interface states at the semiconductor/metal interface [163] it is possible that the Schottky barrier is bias-dependent in the reverse direction. This can lead to a deviation from a pure Schottky diode characteristic (rectifying behavior), so that the drain current in the output characteristics may increase nonlinearly [82, 163, 164]. For example, this concept was useful to explain the contact effects in zinc oxide nanowire field-effect transistors [165] and might be transferable to organic TFTs. This model also explains the increase in nonlinearity when the contact length is reduced (Figure 6.4a-c). A smaller contact area increases the contact resistance and therefore increases the relative portion of the drain-source voltage drop across the contacts. Consequently, the influence of the bias-dependent Schottky barrier increases (compared to the channel resistance) and the superlinear drain-current increase is more pronounced.

Anisotropic mobility

In polycrystalline films of small molecules the individual molecules often stand approximately perpendicular on the gate dielectric [66, 166] (and chapter 5). This molecular order causes a large mobility in the direction parallel to the gate dielectric (strong interaction of neighboring molecules), and a smaller mobility perpendicular to the gate dielectric (weaker interaction of neighboring molecules) [35, 167]. Experimental [168] and theoretical studies [169] demonstrated that the contact resistance in staggered organic TFTs has a minimum

value for a film thickness of 20-40 nm, which confirms the significant influence of the charge transport perpendicular to the gate dielectric. There are two mechanisms which can explain the charge transport in this region and can lead to the observed nonlinearities, a *field-dependent mobility* or a *space charge limited current*, as discussed below.

Field-dependent mobility: Vacuum-deposited organic films contain defects acting as trap states within the band gap (section 2.1). Depending on the density of trap states the charge-carrier mobility can be electric-field-dependent and can be simulated by the **Poole-Frenkel effect**. This was first reported by Yakov Frenkel to explain the conductivity in insulating materials under the influence of a high electric field [170]. It is assumed that the charge carriers are trapped in localized states separated by an energy barrier, which is only occasionally overcome by thermal activation. However, under the influence of a strong electric field, the barrier between the localized states is reduced and less thermal energy is required to release charge carriers (6.5b). Thus, the charge carriers are more frequently released and the mobility increases. The field-dependent mobility in organic TFTs is typically described by [79, 171]:

$$\mu\left(\mathrm{E_x}\right) = \mu_0 \exp\left(\gamma\sqrt{\mathrm{E_x}}\right), \tag{6.7}$$

where γ is a prefactor and depends on the materials. In simulations the field-dependent mobility is often considered along the source-drain electric field (for electric fields $> 10^5$ V/cm), i.e. along the transistor channel. This concept proofed useful to explain the nonlinearities in the output characteristics of transistors based on amorphous organic semiconductors [79, 171]. However, preliminary simulations on these DNTT TFTs yielded only a very weak field-dependent mobility along the channel [172]. This is evident, since the DNTT films exhibit a high molecular order (chapter 5), so that a very high density of trap states is not expected.

When the contact length is reduced, the contribution of the drain-source voltage drop across the contacts increases. Consequently, the electric field (drain-source voltage) along the channel decreases, so that one would expect a reduction of the nonlinear drain-current increase. But the experiments demonstrate an increase in nonlinearity when the contact length is reduced. This suggests within the concept of the Poole-Frenkel mechanism a field-dependent mobility from the contacts down to the accumulation channel (perpendicular to the gate dielectric). Since the interaction of the DNTT molecules perpendicular to the gate dielectric is weaker [35], this transport direction might be affected more strongly by defects that introduce trap states.

Space charge limited current: The assumption of a space charge limited current (SCLC) was useful to model the current in a vertical organic diode [173]. The SCLC

model assumes that the contact resistance between the organic semiconductor and the metal is small, but that the charge transport in the organic semiconductor is not efficient. A high charge-carrier density will thus remain close to the contact (Figure 6.5c) and will influence the contact barrier. This concept was successfully adopted by Sohn and co-workers to describe the transport mechanism in top-contact organic TFTs from the contacts down to the accumulation channel [169]. The SCLC in its general form is described by [169, 173]:

$$I \propto \mu_0 \frac{V^2}{t_{film}^3}, \tag{6.8}$$

and creates a superlinear current increase. V is the voltage across the SCLC region and t_{film} the thickness of the same region (thickness of the organic semiconductor). This model also explains that a reduction of the contact length increases the relative voltage drop across this region, so that the nonlinear drain-current increase is more pronounced.

Contact resistance

For each series of transistors with different contact length (200, 20, 5, and 2 µm) the TLM method was used to extract the contact resistance and the channel resistance at a drain-source voltage of -0.1 V (table 6.3). It was found that the contact resistance increases from 0.6 kΩ·cm (L_C = 200 µm) to 2.2 kΩ·cm (L_C = 2 µm) with decreasing contact length. The symbols in Figure 6.6a show the extracted contact resistances as a function of the contact length. A contact resistance of 9.8 kΩ·cm for a contact length of 0.2 µm was found for transistors manufactured with the electron-beam lithography process (section 4.2). These DNTT TFTs will be discussed in the next section in detail. The dashed line in Figure 6.6a displays the theoretically expected relation between the contact resistance and the contact length given by equation 6.2. The sheet resistance, contact resistance, and transfer length extracted for TFTs with a contact length of 200 µm were utilized for the simulation. In the TLM theory only vertical currents between the contacts and the semiconductor are considered. However, there are three mechanisms which can lead to a higher current in the TFT, so that the extracted contact resistance is smaller than expected (as observed in the experiments).

- The organic semiconductor next to the gate electrode is intrinsically not conducting, but diagonal field lines accumulate a certain charge-carrier density in the vicinity next to the gate electrode [79]. For TFTs with $L_C < L_T$ a certain fraction of the total current can flow in a diagonal direction between the contacts and the organic semiconductor, making the effective area available for the charge flow larger than L_C·W (Figure 6.6b).
- The three-dimensional growth of the DNTT film introduces contact/semiconductor

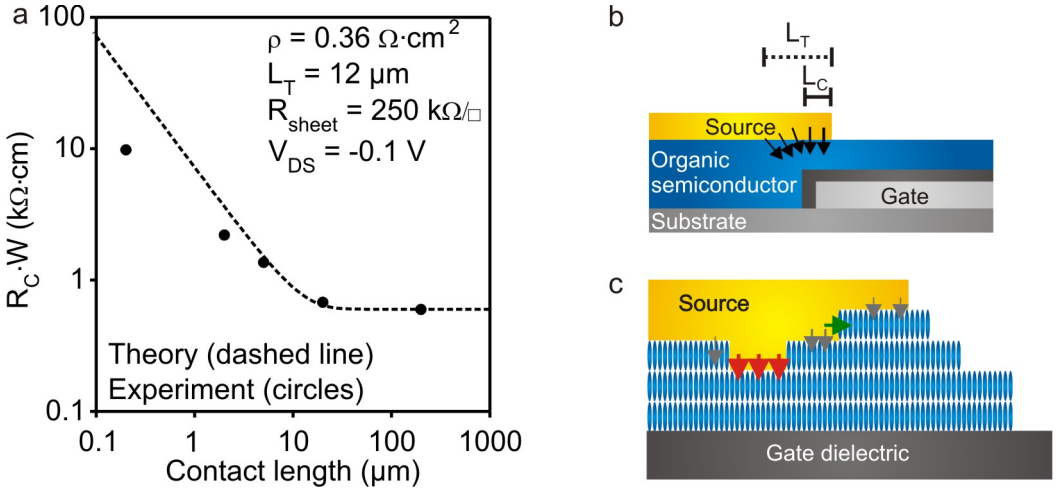

Figure 6.6: Experimental analysis of the relation between contact resistance and contact length and schematics of the contact/semiconductor interface. a) Width-normalized contact resistance as a function of the contact length. The data points indicate the contact resistances of 0.60, 0.69, 1.36, 2.20, and 9.80 kΩ·cm that have been meeasured for a contact length of 200, 20, 5, 2, and 0.2 µm, respectively. The TFTs with a contact lemgth of 200, 20, 5, and 2 µm have been manufactured using stencil lithography. The TFTs with a contact length of 0.2 µm have been realized using an electron-beam lithography assisted process and will be discussed in detail in section 6.3. The dashed line represents the theoretically predicted relation between the contact resistance and the contact length. b) Schematic to illustrate the hypothesis of a non-vertical charge flow between the contact and the semiconductor. c) Schematic to indicate the preferable charge flow in a valley.

Contact length (µm)	Contact resistance (kΩ·cm)	Sheet resistance ($\frac{kΩ}{□}$)
200	0.60	250
20	0.68	280
5	1.36	420
2	2.20	1300

Table 6.3: Contact and sheet resistance for DNTT TFTs with a contact length of 200, 20, 5 and 2 µm.

interface regions closer to (valley) and further away from gate dielectric surface (Figure 6.6c). Due to the higher resistance of the organic semiconductor along the c-axis (compared to the ab-plane), the current transfer between the contact and the semiconductor will occur mainly in the valley (red arrows in Figure 6.6c). Therefore, the presence of a valley may be the dominating region of charge transfer, and the actual contact length is less important than predicted by the TLM theory.

- A minor current contribution not considered in the TLM theory might be given by a charge flow between the contact and the semiconductor in the direction parallel to the gate dielectric as indicated in Figure 6.6c (green arrow).

Remarks

Even if the contact length of a top-contact TFT is reduced to 0 µm, in other words, even if there is no overlap between the gate electrode and the source/drain contacts, there will be a non-zero density of charge carriers underneath the contacts, so that the contact resistance should still be smaller than that of transistors manufactured in the bottom-contact (coplanar) geometry [79]. This should be another important advantage of the staggered over the coplanar organic TFTs.

Also note that the gate-source voltage controls the density of charge carriers that are accumulated in the transistor channel and therefore determines the sheet resistance. However, the effective gate-source voltage, which is applied to the transistor channel, depends on the serial (source-side) contact resistance. When the contact resistance increases (e.g. for a reduced contact length), the effective gate-source voltage is reduced, so that less charge carriers are accumulated in the transistor channel and the DNTT sheet resistance is increased (table 6.3).

6.3 Nanoscale organic transistors

There have been many efforts to reduce the channel length of (organic) transistors, with the goal of increasing the maximum operation frequency ($f_T \sim \frac{1}{L^2}$, section 3.2). However, if the scaling requirements addressed in section 3.3.1 are not observed, such transistors will show strong short-channel effects, especially for a channel length of 100 nm or less. Ideally, the thickness of the gate dielectric is a factor of ∼20 smaller than the transistor channel length. This guarantees that the accumulated charge in the channel is controlled by the gate electrode rather than by the drain contact [75]. Many sub-100 nm organic transistors reported in the literature utilize a silicon wafer as a *global back-gate* with a reasonably thin layer (5 to 50 nm thick) of SiO_2 or SiN_x as the gate dielectric, so that short-channel effects are reduced [25, 87, 89, 105, 107]. However, these gate dielectrics are not compatible with a low-temperature process as desired for organic transistors. Collet and co-workers reported on a monolayer of tetradecylenyltrichlorosilane utilized as a low-temperature ultra-thin gate dielectric on a silicon wafer, but their transistor with a channel length of ∼100 nm still suffers from severe short-channel effects [86].

So far, most reports on *local-gate* organic transistors with a channel length ∼100 nm utilized relatively thick gate dielectrics. The ratio of channel length to gate-dielectric thickness is not larger than 5-6 [14] and not surprisingly the transistors exhibit strong short-channel effects such as absence of drain-current saturation. The local-gate TFTs in this thesis employ an ultra-thin low-temperature gate dielectric ($t_{diel} = 5.7\,nm$), so that no severe short-channel effects for a channel length as small as ∼100 nm are expected

($\frac{L}{t_{diel}} \gtrsim 20$). All TFTs have a channel length between 90 and 300 nm, a channel width of 500 nm, and a contact length of 200 nm, and have been fabricated with the electron-beam lithography process described in section 4.2.

6.3.1 Device characteristics

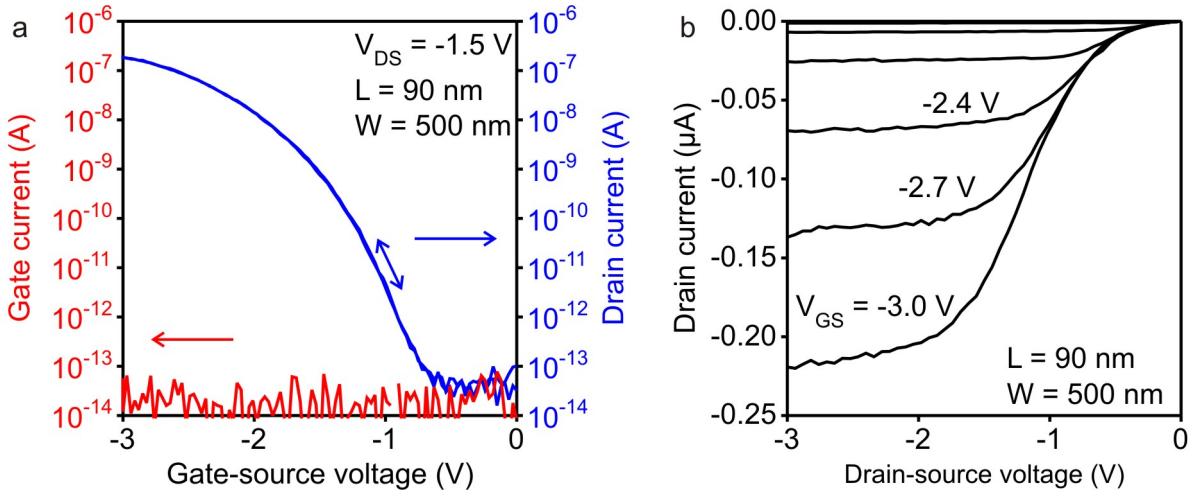

Figure 6.7: Transfer and output characteristics of a top-contact DNTT TFT. The TFT has a channel length of 90 nm, a channel width of 500 nm, and a contact length of ∼200 nm. a) From the transfer characteristics a transconductance of 0.4 $\frac{S}{m}$, an effective mobility of 0.04 $\frac{cm^2}{Vs}$, an on/off current ratio of 10^7, a subthreshold swing of 170 mV/decade, and a threshold voltage of -1.35 V are extracted. The ratio between the channel length and the gate dielectric thickness (5.7 nm) is sufficiently large to facilitate a strong gate coupling, so that the off-state drain current is only 0.1 pA. The gate current is also not larger than 0.1 pA b) In the output characteristics the drain current increases nonlinearly, but the saturation is reasonably pronounced.

The electrical characteristics of a DNTT TFT with a channel length of 90 nm, a channel width of 500 nm, and a contact length of ∼200 nm are shown in Figure 6.7. The transconductance is 0.4 $\frac{S}{m}$, the effective mobility 0.04 $\frac{cm^2}{Vs}$, the on/off current ratio $\sim 10^7$, the subthreshold swing 170 mV/decade, and the threshold voltage -1.35 V. The ratio between the channel length and the dielectric thickness is sufficiently large to facilitate a strong gate coupling and the transistor clearly turns off ($\sim 10^{-13}$A). The on/off current ratio is similar to that of the long-channel transistors (L = 30 µm) reported in section 6.1, and it is by far the largest on/off ratio reported for a sub-100 nm organic TFT. The output characteristics show the nonlinear current increase attributed to the contact resistanc, but good current saturation for higher drain-source voltages. The width of the semiconducting layer and the width of the source/drain contacts are identical, since both are defined by the same resist pattern (Figure 4.4b on page 43). Therefore, the channel width of the TFTs is precisely defined and the possibility of fringe currents flowing between source and drain outside of the contact width are effectively eliminated.

6.3.2 Discussion of short-channel effects

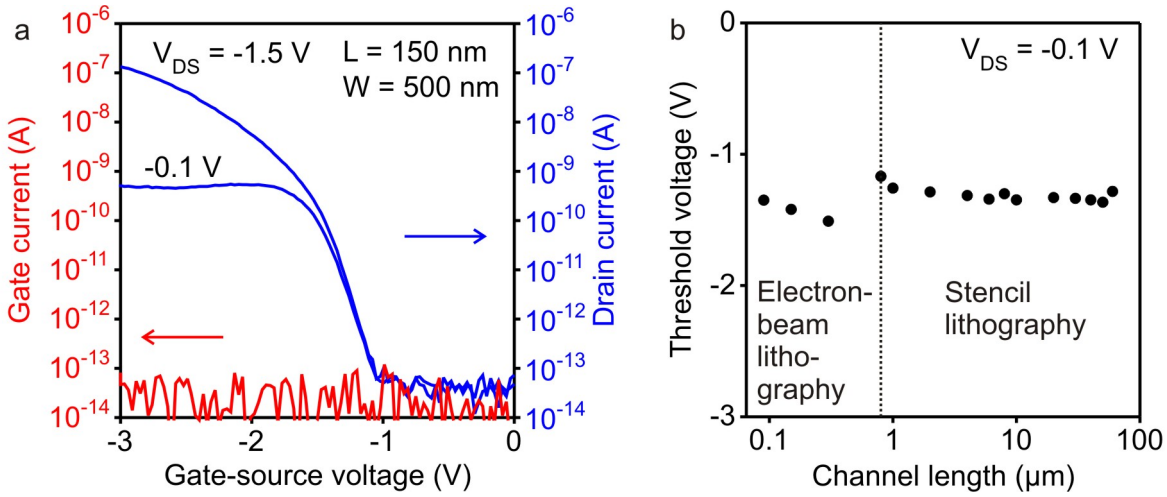

Figure 6.8: Analysis of short-channel effects. The DNTT TFTs have a channel length between 0.09 µm and 60 µm and employ an ultra-thin gate dielectric (5-6 nm thick) to suppress short-channel effects. a) Transfer characteristics of a DNTT TFT with a channel length of 150 nm for two different drain-source voltages. The off-state drain current, the threshold voltage and the subthreshold swing are independent of the applied drain-source voltage (absence of drain-induced barrier lowering). b) The threshold voltage is essentially independent of the transistor channel length (0.09-60 µm), and no threshold voltage roll-off behavior is observed.

The deviations from the ideal electrical characteristics for transistors, when the gate dielectric scaling requirements are not observed, have been already introduced in section 3.3.1.

The transfer characteristics of a TFT with a channel length of 150 nm for drain-source voltages of -0.1 V and -1.5 V are shown in Figure 6.8a. Despite the very small channel length the off-state drain current, the threshold voltage, and the subthreshold swing are independent of the applied drain-source voltage (absence of drain-induced barrier lowering).

Figure 6.8b shows the threshold voltage (extracted in the linear region) of DNTT TFTs with a channel length between 0.09 µm and 60 µm. The threshold voltage of a TFT with a channel length of 60 µm is -1.30 V and for a channel length of 0.09 µm it is -1.35 V. Compared to reports on organic TFTs with a thicker gate dielectric the dependence of the threshold voltage on the channel length (threshold-voltage roll-off) is negligible [85]. (Note that the threshold voltages of the TFTs fabricated by electron-beam lithography are systematically larger by about 100 mV than those of the TFTs fabricated by stencil lithography, likely due to small amounts of resist residue.

The saturation of the drain current in the output characteristics of the long-channel TFT (L = 60 µm) in Figure 6.1b is very pronounced and the output conductance $g_d = \frac{\partial I_D}{\partial V_{DS}}$ is

essentially zero. The 90 nm long TFT in Figure 6.7b has similar characteristics, showing that the channel-length modulation is greatly suppressed.

In short, using an ultra-thin gate dielectric to observe the scaling requirements introduced by R.H. Dennard [75] is a powerful method to suppress short-channel effects in organic transistors with a channel length as small as 100 nm.

6.3.3 Contact limitation

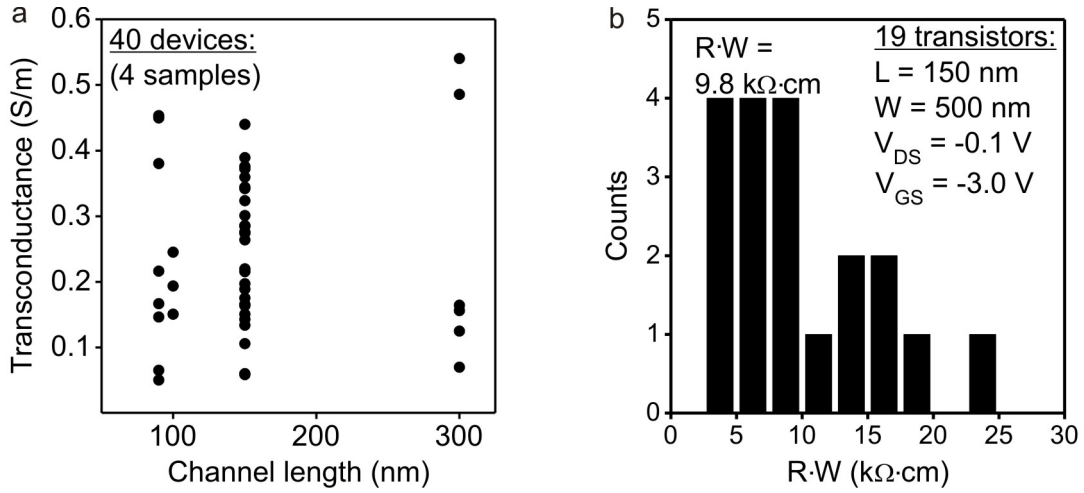

Figure 6.9: Statistical analysis of the transconductance and width-normalized resistance of nanoscale DNTT TFTs. a) Transconductance as a function of the channel length for 40 DNTT TFTs with a channel length between 90 and 300 nm. The theoretically predicted relationship between transconductance and channel length ($g_m \sim \frac{1}{L}$) is not observed, so that methods such as the TLM cannot be applied to these data. b) Width-normalized resistance of 19 DNTT TFTs with a channel length of 150 nm calculated at a fixed drain-source voltage of -0.1 V. The average resistance of the TFTs is 9.8 kΩ·cm and the contact resistance is assumed to be only slightly smaller.

Figure 6.9a shows the transconductance per channel width as a function of the channel length (90 nm, 150 nm, or 300 nm) of 40 nanoscale TFTs measured on four substrates. The TFTs have a channel width of 500 nm and a contact length of ∼200 nm. The variation of the measured values for a specific channel length is substantial and the theoretically predicted relation between transconductance and channel length ($g_m \sim \frac{1}{L}$) is not observed, so that an analysis of the data using the transmission line method is not possible. Due to the extremely small channel length of these TFTs, the most important parameter limiting the transconductance is the contact resistance, so it is reasonable to assume that the large variation in transconductance is caused by variations in the contact resistance. In contrast to the previously discussed long-channel TFTs (L > 1 µm), where the influence of the contact resistance on the device characteristics is small, the characteristics of nanoscale TFTs are heavily dependent on the efficiency of the contacts. Indeed,

scanning photocurrent microscopy experiments on pentacene TFTs have shown that the efficiency of the charge transfer at the contacts can vary significantly, not only from one device to the next, but even along the contact edge within the same device [174, 175]. The nanoscale TFTs have a channel width of 500 nm and a contact length of 200 nm, so that one contact may cross a grain boundary and another contact is located on a single grain. These variations are usually not observed for the long-channel TFTs with a channel width and contact length of several microns.

To estimate an upper limit for the contact resistance of the nanoscale TFTs, the total resistance of a large number of TFTs with identical channel length (L = 150 nm) was measured and the mean value of the width-normalized total resistance was calculated. For nanoscale TFTs, the contribution of the channel resistance to the total resistance is very small, so that the contact resistance is expected to be only slightly smaller than the total resistance. In Figure 6.9b the distribution of the total resistance of 19 nanoscale TFTs calculated for a drain-source voltage of -0.1 V is shown. The mean value of the total resistance is 9.8 kΩ·cm.

6.4 Reproducibility of stencil lithography

In contrast to the electron-beam lithography process, the stencil lithography process exhibits a remarkable reproducibility of the transistor characteristics. Figure 6.10a shows the transfer characteristics of 16 DNTT transistors fabricated on one substrate for a drain-source voltage of -1.5 V. The TFTs have a channel length of 1 µm, a channel width of 10 µm, and a contact length of 20 µm. The off-state drain current, subthreshold swing, threshold voltage, on-state drain current, and gate current show very little variations. For example, the average extracted transconductance is $(0.47 \pm 0.02)\ \frac{\mathrm{S}}{\mathrm{m}}$. The little variation in transconductance is mainly attributed to the well-defined channel length enabled by the stencil masks. The energy dispersive x-ray map for gold of a TFT with a channel length of 10 µm in Figure 6.10c demonstrates the sharp edges of the gold contact. During the manufacturing process no significant amount of gold was inadvertently deposited underneath the stencil mask into the transistor channel. These conclusions are supported by the SEM image shown in Figure 4.3c on page 42.

The threshold voltage of 62 TFTs with a channel length of 5, 2, and 1 µm fabricated on four different substrates on different days is summarized in Figure 6.10b. Since the DNTT TFTs show essentially no threshold-voltage roll-off for a channel length as short as 0.09 µm, the consideration of transistors with different channel length in this statistical analysis is legitimate. The extracted average threshold voltage is (0.95 ± 0.03) V and varies by only a few percent. A uniform threshold voltage was also extracted for pentacene

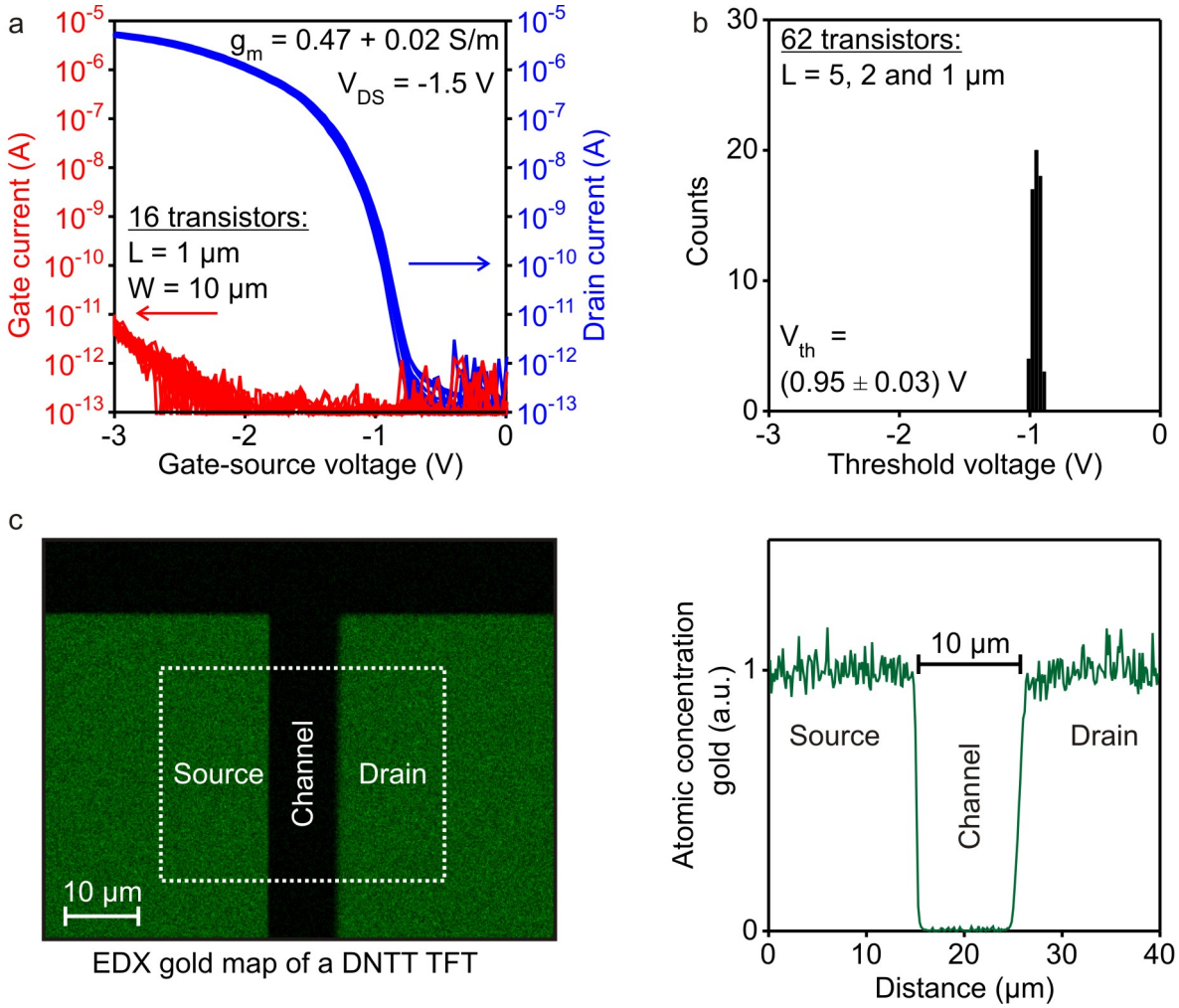

Figure 6.10: Statistics on the stencil lithography manufacturing process. a) Transfer characteristics of 16 DNTT TFTs with a channel length of 1 µm, a channel width of 10 µm, and a contact length of 20 µm. The average transconductance of the transistors is $(0.47 \pm 0.02)\ \frac{\mathrm{S}}{\mathrm{m}}$. The tight distribution is attributed to the smooth contact edges enabled by the use of high-resolution silicon stencil masks. b) Threshold voltage of 62 TFTs with a channel length of 5, 2, and 1 µm fabricated on four different substrates with an average threshold voltage of (0.95 ± 0.03) V. The consideration of different channel lengths is justified since the TFTs show no threshold voltage roll-off for a channel length as short as 0.09 µm (section 6.3). c) Energy dispersive x-ray map of gold and corresponding data analysis of a TFT with a channel length of 10 µm. The sharp source/drain contact edges are visible.

top-contact TFTs manufactured with polyimide shadow masks [12]. Therefore, the tight threshold voltage distribution is attributed to the uniform organic film growth on top of the hydrophobic gate dielectric, rather than to the utilization of high-resolution stencil masks.

Conclusion

The top-contact DNTT TFTs manufactured in this work have an intrinsic hole mobility of 3.4 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$. For TFTs with large lateral dimensions (large channel length and large contact length) the influence of the contact resistance on the device characteristics is negligible and the extracted effective mobility (2.8 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$) is close to the intrinsic mobility. A transfer length of 12 µm is extracted using the transmission line method. Therefore, the contact resistance strongly increases from 0.6 kΩ·cm for a contact length of 200 µm to 9.8 kΩ·cm for a contact length of 200 nm. As a result, DNTT TFTs with a reduced contact and channel length (∼100 nm) exhibit a much smaller effective mobility of 0.04 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$, since most of the drain-source voltage drops across the contacts and not along the channel. However, thanks to the ultra-thin gate dielectric utilized in this work, short-channel effects are greatly suppressed. TFTs with a channel length of 90 nm have an on/off current ratio of 10^7 and a steep subthreshold swing of 170 mV/decade, which is comparable to long-channel TFTs. The manufacturing process based on stencil lithography is characterized by a remarkable reproducibility. The electrical characteristics, such as the off-state drain current, the subthreshold swing, the threshold voltage, the on-state drain current, and the gate current, of TFTs with identical lateral dimensions vary by only a few percent. For example, the average transconductance for 16 TFTs with a channel length of 1 µm is (0.47 ± 0.02) $\frac{\mathrm{S}}{\mathrm{m}}$ and the average threshold voltage of 62 TFTs is (0.95 ± 0.03) V.

7 Time-dependent effects

Organic semiconductors often suffer from a rapid degradation during exposure to oxygen, water vapor (humidity), or ozone. Common methods to avoid this degradation are encapsulations of the transistors [50] or storage under an inert atmosphere [176]. Air-stable semiconductors obviously greatly simplify the handling of the materials during manufacturing and the characterization in research labs, but also in an industrial environment. The shelf-life stability of the organic semiconductor DNTT during exposure to ambient conditions is investigated in section 7.1. Interestingly, the electrical characteristics of the DNTT TFTs exhibit essentially no degradation during exposure to ambient conditions (over a period of a few months). In fact, the TFT performance initially improves. This surprising effect depends on the channel length of the transistor and is analyzed in section 7.2.

7.1 Air stability of DNTT

The electrical performance of organic TFTs exposed to oxygen, water vapor (humidity), or ozone often degrades over time. This has been reported for organic TFTs based on pentacene [177, 178, 179] and is the result of an oxidation at the central ring of the molecule by which hydrogen atoms are replaced by oxygen atoms [180]. Since oxygen atoms are linked to the carbon atoms via double bonds (in contrast to hydrogen atoms, which are linked by single bonds), the oxidation leads to a loss in conjugation and a change of the HOMO energy (section 2.1). This hinders the charge-carrier exchange between oxidized and non-oxidized molecules. Moreover, the shape of the oxidized molecules is different and causes distortions, that act as scattering centers within the organic semiconductor [55] and reduce the mobility. One strategy towards air-stable organic semiconductors is to increase the ionization potential (= reduction of the HOMO energy level) to reduce the oxidation probability of the molecule. This was demonstrated for di(phenylvinyl) anthracene (DPVAnt) with an ionization potential of -5.4 eV (compared to an ionization potential of -5.0 eV for pentacene). DPVAnt transistors show a better air stability than pentacene transistors. However, the mobility in low-voltage DPVAnt TFTs with a channel length of 30 µm and a contact length of 30 µm is only 0.5 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$, and the subthreshold swing was found to increases over time [132].

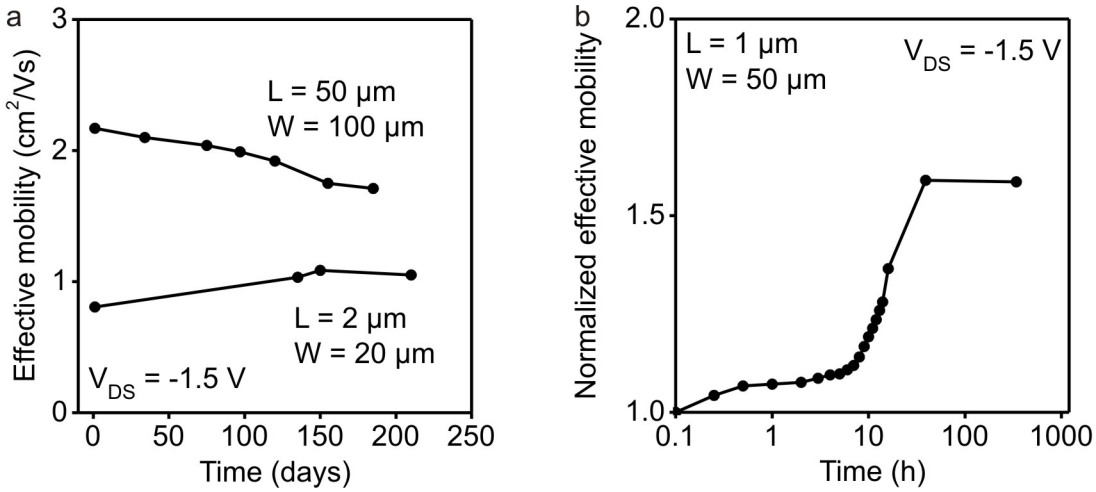

Figure 7.1: Shelf-life stability of DNTT TFTs. a) Effective mobility as a function of time for two DNTT TFTs with a channel length of 2 µm and 50 µm and a channel width of 20 µm and 100 µm, respectively. The contact length is 20 µm for both transistors. After 200 days the effective mobility is still within 10% of its original value. b) Normalized effective mobility as a function of time for a DNTT TFT with a channel length of 1 µm extracted in the saturation region. Within 30 hours, the effective mobility increases by 60%.

The DNTT molecule has a HOMO energy level of -5.4 eV [26], which is sufficiently low to avoid a strong oxidation under ambient conditions. In Figure 7.1a the effective mobilities of two DNTT TFTs with channel lengths of 2 µm and 50 µm are plotted as a function of time. The contact length of both TFTs is 20 µm. The transistors have been stored and measured in a clean room with a humidity of 40%-70%. The effective mobility of the transistor with a channel length of 2 µm is $\sim$1 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$ and that of the transistor with a channel length of 50 µm is $\sim$2 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$. The difference in effective mobility is explained by the different contributions of the contact resistance to the total transistor resistance (section 6.2.1). Over the observed period of 210 days, there is essentially no degradation in mobility for both transistors. For comparison, the effective mobility of pentacene TFTs fabricated with the same process and the same lateral dimensions is initially only 0.5 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$ (channel length of 50 µm) and decreases by more than one order of magnitude within 30 days [177].

Closer inspection of the data reveals a slight increase in effective mobility, but only for the TFT with the small channel length (2 µm). Figure 7.1b illustrates the time evolution of the normalized effective mobility (extracted in the saturation region) of a DNTT TFT with a channel length of 1 µm, a channel width of 50 µm, and a contact length of 200 µm. The mobility was normalized to its initial value that was extracted immediately after the device fabrication. The effective mobility is approximately constant for the first few hours. Then, an increase in effective mobility by $\sim$ 60% within $\sim$30 h is observed, followed by a "saturation region". The mechanism of this improvement is discussed in the next section.

7.2 Time-dependent contact-resistance improvement

7.2.1 Electrical characteristics and effective mobility

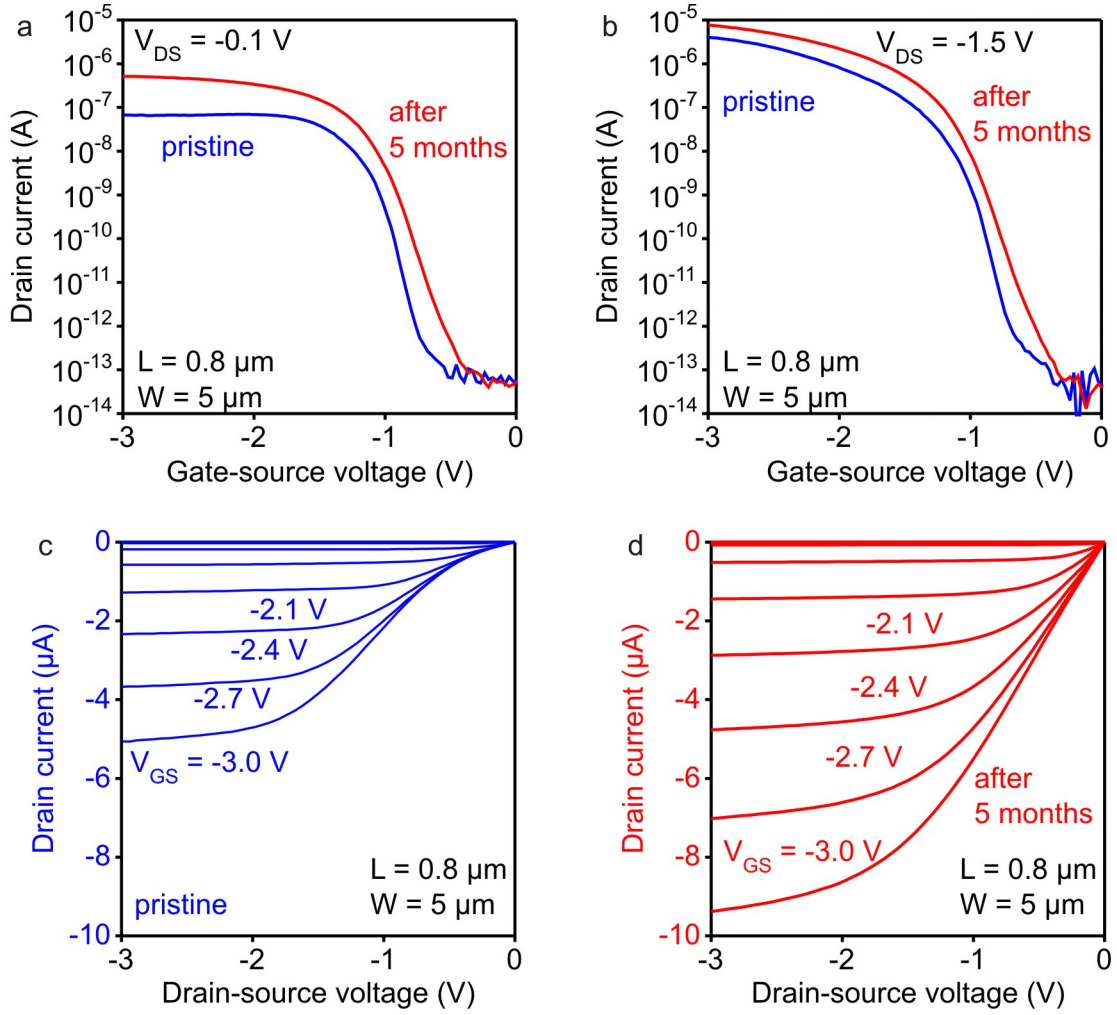

Figure 7.2: Transfer and output characteristics of a top-contact DNTT TFT measured immediately and 5 months after its fabrication. The DNTT TFT has a channel length of 0.8 µm, a channel width of 5 µm, and a contact length of 20 µm. a,b) For the pristine transistor the effective mobilities are 0.2 $\frac{cm^2}{Vs}$ and 0.7 $\frac{cm^2}{Vs}$ in the linear and the saturation region, respectively. After 5 months the effective mobilities have increased to 0.8 $\frac{cm^2}{Vs}$ in the linear and 0.9 $\frac{cm^2}{Vs}$ in the saturation region. The transconductance is 1 $\frac{S}{m}$ (after 5 months) which is the largest transconductance reported for an organic transistor with an on/off ratio of more than 10^3. c,d) In the output characteristics the pristine transistor shows the nonlinear drain current increase which has disappeared 5 months after fabrication.

Figure 7.2 shows the transfer and output characteristics of a DNTT TFT with a channel length of 0.8 µm, a channel width of 5 µm, and a contact length of 20 µm measured initially and 5 months after the fabrication. Initially, the transconductance is 0.7 $\frac{S}{m}$, the effective mobility is 0.7 $\frac{cm^2}{Vs}$, and the on/off current ratio is 10^8. After 5 months, the effective mobility has improved to 0.9 $\frac{cm^2}{Vs}$ and the transconductance to 1.0 $\frac{S}{m}$, which is the largest

transconductance reported for an organic transistor. There are a few reports of organic transistors with a transconductance of 4 $\frac{S}{m}$ where the gap in a broken carbon nanotube was utilized as a very short ($\sim$ 10 nm) transistor channel [181], but these transistors were made in a global back-gate geometry and the on/off current ratio is only 10^3.

The characteristics of the DNTT TFT recorded after 5 month show a threshold voltage shift towards more positive values by 0.1 V and a minor subthreshold swing increase by 20 mV to 120 mV/decade compared to the pristine characteristics (Figure 7.2). The nonlinear drain-current increase in the output characteristics disappears after 5 months. The extracted mobilities are 0.7 $\frac{cm^2}{Vs}$ (pristine) and 0.9 $\frac{cm^2}{Vs}$ (5 months) in the saturation and 0.2 $\frac{cm^2}{Vs}$ (pristine) and 0.8 $\frac{cm^2}{Vs}$ (5 months) in the linear region. The more distinct mobility increase in the linear region and the improvement of the linearity of the drain current for small drain-source voltages suggest a time-dependent improvement of the contact-resistance.

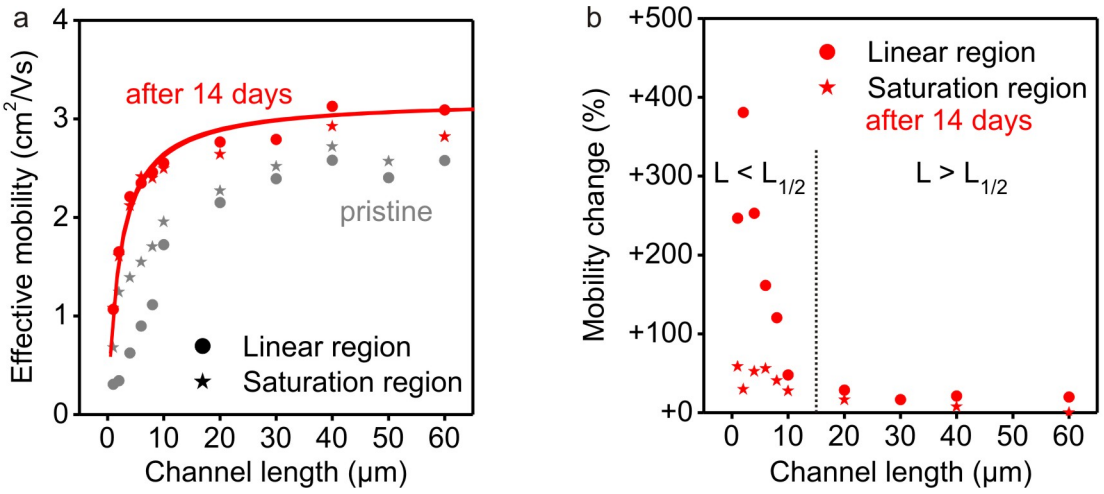

Figure 7.3: Time dependence of the effective mobility of DNTT TFTs with various channel length. a) Change of the effective mobility over a period of 14 days as a function of channel length. b) Relative mobility improvement as a function of channel length. For transistors with a channel length longer than 20 µm the effective mobility increases by 20% in the linear and the saturation region. For transistors with a channel length of less than 20 µm, the increase in relative mobility increases dramatically, when the channel length is reduced. In the linear region the effective mobility increase is as large as 300%, whereas an increase of only 60% is observed in the saturation region.

For all subsequent experiments the transistors were measured immediately and 14 days after the fabrication to ensure that the mechanisms of the mobility improvement are completed. Figure 7.3a shows the effective mobility in the linear and the saturation region as a function of the channel length (1-60 µm) for pristine and 14 days old transistors. The relative mobility increase in percent as a function of the channel length is shown in 7.3b. Recalling the parameter $L_{1/2} \sim$ 10-15 µm (describing the transistor channel length for equal channel and contact resistance, section 6.2.1), the transistors can be roughly divided

into two categories. The **channel-dominated** TFTs have a channel length that is larger than $L_{1/2}$, and the **contact-dominated** TFTs have a channel length that is smaller than $L_{1/2}$. The effective mobility increases by only 20% in the channel-dominated TFTs in both the linear and saturation region. In contrast, for the contact-dominated TFTs the effective mobility increases by 50% in the saturation region, and by as much as 300% in the linear region. A fit of the data in Figure 7.3a to equation 6.6 yields ∼2.2 µm for $L_{1/2,\text{after 14 days}}$ in the linear and in the saturation region. This means that $L_{1/2}$ decreases by as much as a factor of 7 over a period of 14 days, suggesting that the contact resistance decreases during this period due to a "room-temperature annealing" effect.

Comparison to pentacene

Similar results on a room-temperature improvement of the electrical characteristics have previously been reported for top-contact pentacene transistors (L = 450 µm) by Kalb and co-workers [182]. In their studies the pentacene TFTs were stored **in an ultrahigh-vacuum chamber** to prevent oxidative degradation. The DNTT TFTs discussed in this work have an excellent air stability, so that the measurements can be performed in air. For the pentacene TFTs measured by Kalb and co-workers the channel resistance improved by a factor ∼2, the contact resistance by one order of magnitude, and the trap density in the pentacene film decreased within **a few days** [182]. Kalb and co-workers concluded that a reduction of the trap density in the pentacene film improves the charge transport, especially perpendicular to the surface from the contacts to the accumulation channel. This transport direction can significantly affect the contact resistance in top-contact transistors. Additional experiments at variable temperatures and in variable gas atmospheres indicated that this processes is driven by thermal energy, rather than by chemical doping with oxygen.

A thermally driven process is also consistent with XRD measurements on postfabrication annealed ($\sim 50 - 70$°C) pentacene films [80, 183, 184, 185]. The peak intensity of the XRD patterns have been stronger for pentacene layers annealed at moderate temperatures after fabrication which indicates an improvement in film crystallinity. For postfabrication annealing of pentacene transistors several groups reported a mobility increase **under ambient conditions** (channel length ∼50 µm, measured within **a few hours** after exposure to ambient conditions) [109, 184, 185], when the channel length is not larger than 50 µm.

Therefore, the significant improvement of the effective mobility observed for the DNTT TFT studied in this thesis (Figure 7.3a) may be attributed indeed to a "room-temperature annealing" effect.

7.2.2 Contact and sheet resistance

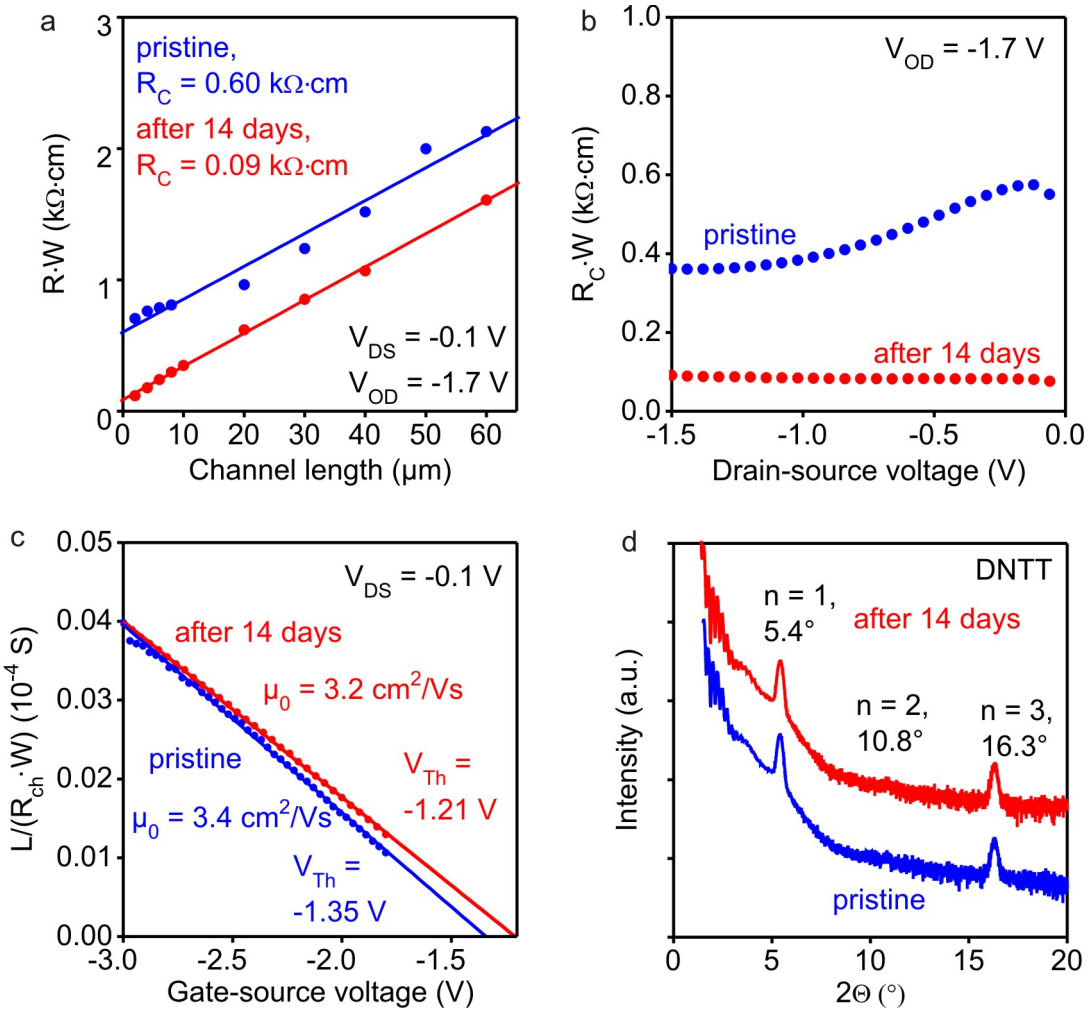

Figure 7.4: Contact and sheet resistance analysis of DNTT TFTs measured immediately and 14 days after fabrication. a) TLM to extract the contact resistance, the sheet resistance and the transfer length of pristine (blue) and 14 days old (red) transistors. Initially, the contact resistanc is 600 Ω·cm, the sheet resistance 250 $\frac{k\Omega}{\square}$ and the transfer length 12 µm. After 14 days the contact resistance is 90 Ω·cm, the sheet resistance 250 $\frac{k\Omega}{\square}$ and the transfer length 3-4 µm. b) Contact resistance as a function of the drain-source voltage. The contact resistance of the pristine transistors depends on the drain-source voltage, however, after 14 days there is essentially no dependence on the drain-source voltage. c) Inverse sheet resistance plotted as a function of the gate-source voltage to extract the intrinsic mobility and threshold voltage of the DNTT TFTs. Initially, the intrinsic mobility is 3.4 $\frac{cm^2}{Vs}$ and the threshold voltage -1.35 V. After 14 days, the intrinsic mobility is essentially unchanged (3.2 $\frac{cm^2}{Vs}$) and the threshold voltage has shifted to -1.21 V. d) XRD pattern of a 30 nm thick DNTT film measured immediately after the fabrication and again 14 days later. There is neither a change in peak position nor in peak intensity and sharpness, and the lattice plane distance is 16.3 Å for both measurements.

The data shown in Figure 7.3b strongly suggest that the observed improvement is due to a time-dependent decrease of the contact resistance. In order to rule out that the observed improvement is caused by a modification of the DNTT sheet resistance during

	Pristine	After 14 days
Contact resistance (Ω·cm)	600	90
Contact resistivity (Ω·cm^2)	0.360	0.031
Channel sheet resistance ($\frac{k\Omega}{\square}$)	25	25
Transfer length (µm)	12	3.5
Intrinsic mobility ($\frac{cm^2}{Vs}$)	3.4	3.2
Intrinsic threshold voltage (V)	-1.35	-1.21
Lattice plane distance (nm)	1.63	1.63
Crystallite height (nm)	29	26

Table 7.1: Parameters extracted from the XRD and TLM measurements. The same samples have been used for the pristine and the repeated (after 14 days) measurements.

the observed period further experiments were carried out. The TLM method is useful to separate the contributions of the contact resistance and the sheet resistance to the total transistor resistance. In addition, XRD measurements on a pristine DNTT film and 14 days later were taken to identify any morphological changes induced by the "room-temperature annealing". A summary of the XRD and TLM results is given in table 7.1.

Contact resistance

Figure 7.4a illustrates the TLM for a set of DNTT TFTs with a channel length between 1 and 60 µm and a contact length of 200 µm. The transistors were measured immediately and 14 days after the fabrication. The data in Figure 7.4a are plotted for an overdrive voltage V_{OD} = -1.7 V. The overdrive voltage is defined as a fixed gate-source voltage above the threshold voltage, so that the accumulated charge-carrier density in the channel is identical for both sets of data, even if the TFTs had different threshold voltages. The pristine transistors exhibit a contact resistance of 600 Ω·cm, a sheet resistance of 250 $\frac{k\Omega}{\square}$, a contact resistivity of 0.36 Ω·cm^2, and a transfer length of 12 µm.

After 14 days, the contact resistance has decreased by a factor of 6 to 90 Ω·cm, which is the lowest contact resistance reported for organic polycrystalline TFTs (without source/drain contact modifications or doping). Figure 7.4b shows the relation between the contact resistance and the applied drain-source voltage. The contact resistance of the pristine transistors exhibits a pronounced dependence on the drain-source voltage. After 14 days this dependence has disappeared, which also explains the improved linearity of the drain current in the output characteristics.

Sheet resistance

In contrast to the contact resistance, the sheet resistance of the DNTT TFTS does not significantly change during the first 14 days and remains unaltered at ∼250 $\frac{k\Omega}{\square}$. This is also evident when the intrinsic mobility and threshold voltage of the transistors are calculated. Following equation 6.5 on page 54 the inverse sheet resistance as a function of the gate-source voltage for the pristine and 14 days old transistors is plotted (Figure 7.4c). The least-square linear fit yields an intrinsic mobility of 3.4 $\frac{cm^2}{Vs}$ for the pristine TFTs. After 14 days, the intrinsic mobility is 3.2 $\frac{cm^2}{Vs}$, which is almost identical to that of the pristine TFT. The reduction in contact resistance is equivalent to a reduction in contact resistivity (table 7.1), so that the transfer length is reduced to 3.5 µm after 14 days.

In addition, the molecular order of the pristine and 14 days old DNTT films was evaluated using x-ray diffraction techniques (Figure 7.4d). The films have a thickness of 30 nm and were vacuum-deposited onto a Si/Al/AlO_x/SAM substrate. Neither the characteristic angles of the peaks nor the peak intensities and sharpness change significantly during the first 14 days. (Note, however, that this XRD method is not reliable to identify very small changes in the molecular order of the DNTT film, so that the occurrence of such changes cannot be completely ruled out.)

7.2.3 Influence of ambient conditions

Kalb and co-workers observed a reduction of the contact resistance in pentacene transistors independent of the atmospheric conditions, so that a chemical doping of the pentacene TFTs is excluded [182]. The pentacene TFTs were fabricated *in situ*, that is without any exposure to ambient conditions between the pentacene evaporation, the metal contact deposition, and the electrical characterization in different gas atmospheres. The technical setup by Kalb and co-workers is very useful to avoid any influences introduced by oxygen, ozone, or water vapor during the manufacturing process and the electrical characterization. However, the minimum lateral resolution for top-contact transistors fabricated within that setup is limited to relatively large dimensions of ∼450 µm.

In the present work the focus is placed on very small lateral dimensions (∼1 µm). This requires to align the stencil masks *ex situ*. Therefore, it is not possible to protect the transistors against atmospheric influences during the manufacturing process and detailed experiments on the influence of different gas atmospheres are not possible. However, simple experiments were performed to draw conclusions on the influence of ambient conditions on the TFTs investigated in this work.

In the following paragraphs only the parameters extracted from a single transfer charac-

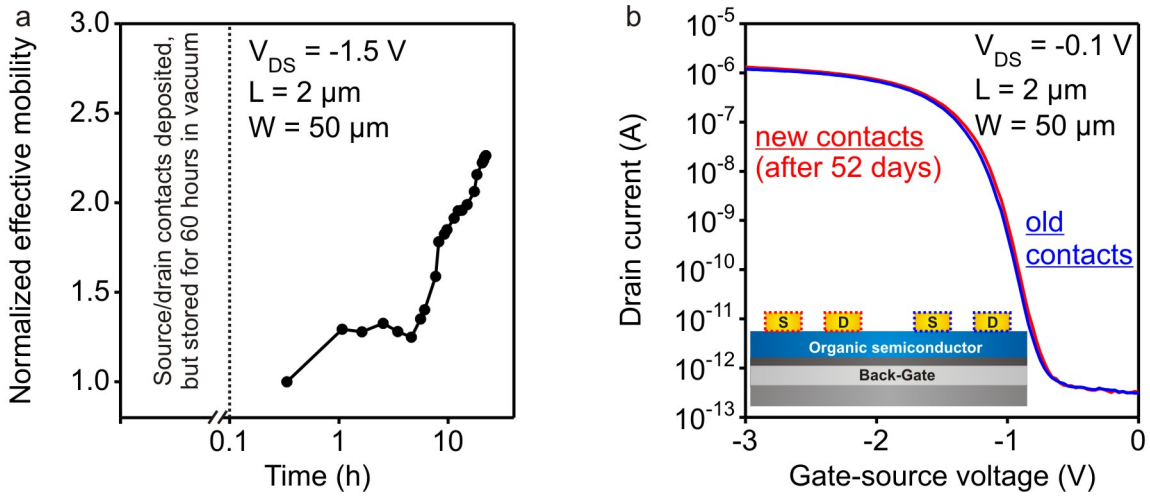

Figure 7.5: Influence of ambient conditions on the contact annealing. a) Normalized effective mobility (extracted in the saturation region) as a function of time for a DNTT TFT. The transistor was stored for 60 hours in vacuum prior to the electrical characterization. The channel length is 2 µm, the channel width 50 µm, and the contact length 200 µm. The effective mobility improves first on exposure to ambient conditions. b) Transfer characteristics of DNTT TFTs with a channel length of 2 µm, a channel width of 50 µm, and a contact length of 200 µm. The "old contacts" describe the TFT initially fabricated onto this substrate. The "new contacts" describe the TFT with source/drain contacts fabricated after 52 days onto the same substrate (sample stored under ambient conditions in a clean room in darkness). The extracted effective mobilities (0.6 $\frac{cm^2}{Vs}$) and the threshold voltages (-1.3 V) are identical for both TFTs.

teristics are studied. Nevertheless, all observations are attributed to a contact-resistance modification and not to a channel-resistance modification. Note that without the experiments discussed in the previous section this conclusion would not be possible.

In the first experiment, a DNTT TFT has been fabricated as described in section 4.1, but it was stored after the source/drain contact deposition for 60 hours in vacuum. Figure 7.5a shows the normalized effective mobility (extracted in the saturation region) as a function of time for this DNTT TFT. The mobility was normalized to its initial value that was extracted immediately after exposure to ambient conditions. The TFT has a channel length of 2 µm, a channel width of 50 µm, and a contact length of 200 µm. Similar to the TFT in Figure 7.1b on page 72 the effective mobility is constant for several hours on exposure to ambient conditions. Then, an increase in effective mobility by $\sim$ 100% within $\sim$30 h is observed, followed by a "saturation region". This indicates that the contact resistance is not decreased when the TFT is stored for 60 hours in vacuum. Thus, the presence of oxygen, ozone, or water vapor may be required to observe the "room-temperature annealing".

In a second experiment, TFTs in a global back-gate configuration have been utilized. Here, 30 nm of aluminum have been thermally deposited onto a silicon wafer that was

utilized as back-gate electrode. Then, the hybrid gate dielectric was formed on top of the aluminum film and a 30 nm thick (unpatterned) DNTT film was vacuum-deposited. Only the gold source/drain contacts were patterned using a stencil mask.

The DNTT TFT on this substrate has a channel length of 2 µm, a channel width of 50 µm, and a contact length of 200 µm. The TFT was electrically characterized immediately after the manufacturing process and is labeled with "**old contacts**" in Figure 7.5b (blue line). Then, the substrate was stored for 52 days under ambient conditions in a clean room in darkness. After this time period of 52 days additional gold source/drain contacts have been deposited onto the same substrate to pattern a new DNTT TFT (with a 52 days old DNTT film). Again, the DNTT TFT has a channel length of 2 µm, a channel width of 50 µm, and a contact length of 200 µm. The TFT was electrically characterized immediately after the manufacturing process and is labeled with "**new contacts**" in Figure 7.5b (red line). The transfer characteristics of both DNTT TFTs (with the old and the new contacts) are identical. The extracted effective mobilities are 0.6 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$ and the threshold voltages -1.3 V. This experiment supports the hypothesis that the DNTT film itself is not modified on exposure to ambient conditions. Note, also for the TFT with "**new contacts**" an increase in mobility on exposure to ambient conditions was observed.

Conclusion

DNTT TFTs have been stored and measured in a clean room (40%-70% humidity) during a period of 200 days. The extracted effective mobility was essentially constant. Actually, for transistors with a small channel length (< 5 µm), a strong increase in the effective mobility within a few days was observed (followed by a constant value for the remaining period). Depending on the exact channel length this increase can be as strong as 300% (in the linear region). The dramatic increase in the effective mobility in the linear region is accompanied by a transition from a nonlinear to an (ideal) linear drain-current increase in the output characteristics. Further experiments including X-ray diffraction measurements and the transmission line method show that this increase is attributed to a contact-resistance reduction from 600 Ω·cm to 90 Ω·cm under ambient conditions. The sheet resistance (= intrinsic mobility in the TFTs without the influence of the contact resistance) and the crystal structure remain unaffected by this "room-temperature annealing" effect.

8 Organic doping for organic thin-film transistors

The drain current of organic transistors is often limited by the energy barrier at the interface between the semiconductor and the source/drain contacts (unless the channel resistance is much larger than the contact resistance). This barrier can be reduced by choosing a source/drain contact metal with a proper work function that matches the LUMO/HOMO energy of the organic semiconductor (section 3.3.2, [77]). However, this method usually works only to a certain extent.

For the bottom-contact geometry a further reduction of the contact resistance is often possible by modifying the work function of the source/drain contacts with a self-assembled monolayer [91, 186]. The most prominent example is the modification of gold bottom contacts with a thiol-based SAM, for which a contact resistance as small as 800 Ω·cm has been reported [91]. The contact resistance of bottom-contact TFTs can also be reduced by inserting a thin conducting metal oxide layer between the source/drain contacts and the organic semiconductor. This oxide layer (usually only a few nanometers thick) can either be deposited in vacuum (MoO_x, WO_x) [187] or it can be obtained by oxidizing the surface of the contacts in an O_2-plasma (AuO_x). With the latter method, a contact resistance of 80 Ω·cm has been reported for bottom-contact pentacene TFTs [114]. However, this approach is not applicable to organic TFTs with a SAM-based gate dielectric, since the SAM would be destroyed by the oxygen plasma.

In the top-contact geometry the contact resistance can be reduced when a thin layer of a charge-carrier dopant is inserted between the organic semiconductor and the metal contacts. This layer can reduce the energy barrier and increase the charge flow between the contacts and the semiconductor. This is explained in section 8.1. In section 8.2 the organic dopant that was utilized for the top-contact TFTs studied in this work is introduced. The influence of contact doping on the TFT characteristics and on the contact resistance, but also the positional stability of the organic dopant are discussed in sections 8.3, 8.4, and 8.5.

For all experiments discussed here (unless explicitly mentioned), the electrical characteristics have been recorded within a few hours after the manufacturing process. This is

necessary to avoid any significant contributions from the "room-temperature annealing" effects discussed in the previous chapter.

8.1 Doping of organic semiconductors

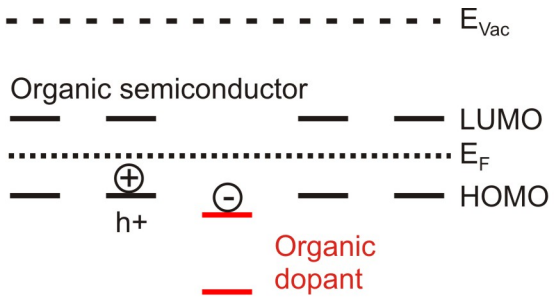

Figure 8.1: Mechanism for p-type doping in organic semiconductors. The schematic illustrates the incorporation of an organic dopant into an organic semiconductor (host material). The organic dopant is a strong electron acceptor that has its LUMO energy below the HOMO energy of the organic semiconductor, so that electrons are transferred from the HOMO of the organic semiconductor into the LUMO of the dopant, leaving excess holes in the host material.

In silicon MOSFETs, the contact resistance is reduced by incorporating elements from the third or fifth column of the periodic table into the contact regions. When the dopants assume positions in the silicon lattice, charge carriers are exchanged between the dopants and the lattice, thus increasing the free carrier density and the electrical conductivity. If the dopant atoms introduce additional holes (electrons) the semiconductor is p-doped (n-doped). In small-molecule organic semiconductors, p-type doping can be achieved by incorporating "impurity" molecules into the host lattice. If the LUMO energy of the dopant is smaller than the HOMO energy of the host, electrons are transferred from the HOMO of the host to the LUMO of the dopant. Thus, excess holes are generated in the host material and the conductivity increases [29, 30, 31, 188, 189] (Figure 8.1). This doping concept has been successfully applied to organic light-emitting diodes, in which the molecular doping greatly reduces the voltage drop across the contacts and along the transport layers [30, 188].

For organic top-contact TFTs the concept of contact doping has previously been applied to TFTs with channel lengths between 50 µm and 0.3 µm [25, 93, 125, 190, 191, 192, 193, 194, 195, 196, 197]. This was realized by employing a thin layer of MoO_x[1] [192],

[1] Molybdenum oxide

$FeCl_3$[2] [25, 191, 195], m-MTDATA[3] [193], $Mo(tfd)_3$[4] [196], TCNQ[5] [93], or F4-TCNQ[6] [125, 190, 194, 197] between the semiconductor and the metal source/drain contacts. The smallest contact resistance of 500 Ω·cm was realized for pentacene transistors doped with a thin film of $Mo(tfd)_3$ [196]. In all these reports, however, a global back-gate electrode was utilized, so that the contact length was very large (> 100 µm). This has the distinct advantage that the charge injection from the contact into the semiconductor spreads across a large contact area (section 6.2.2) [81, 150]. But it has the disadvantage of producing a large parasitic capacitance that limits the maximum frequency at which the transistors can be operated (equation 3.30, page 33). So, a key question that has so far not been addressed is, how useful the concept of contact doping is for organic TFTs with reduced channel length and contact length (to reduce the parasitic capacitances).

8.2 Organic dopant: NDP-9

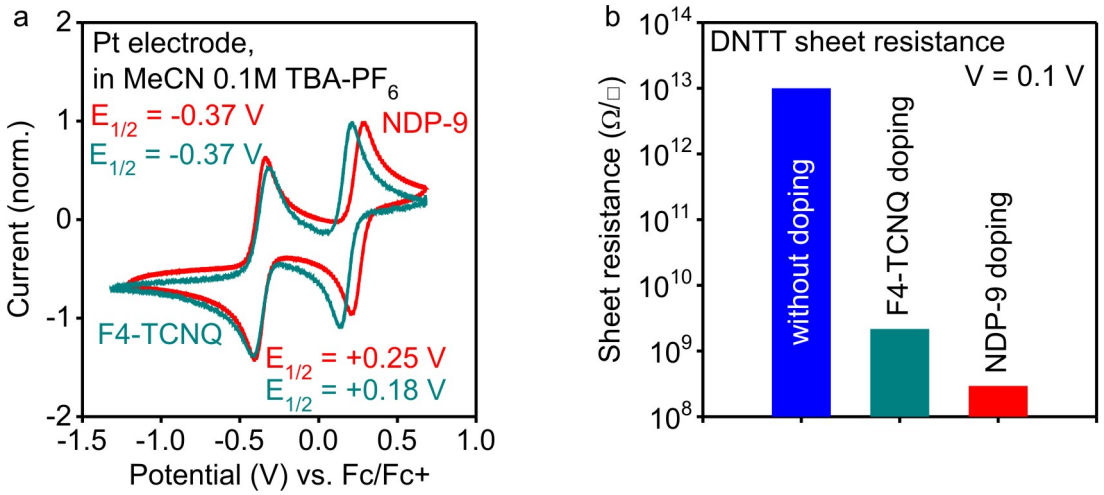

Figure 8.2: Doping strength of the organic dopant. a) Cyclic voltammetry measurements on F4-TCNQ and NDP-9 molecules. The HOMO of NDP-9 is more negative by 0.1 eV than the HOMO of F4-TCNQ (measurements adapted from Novaled AG). b) Sheet resistance of DNTT films without doping, with F4-TCNQ doping and with NDP-9 doping. Without doping the DNTT film has a high sheet resistance of $10^{13}\ \frac{\Omega}{\square}$, by doping with a nominally 1 nm thick layer of either F4-TCNQ or NDP-9 on top of the DNTT film, the sheet resistance is reduced to $2.2{\cdot}10^{9}\ \frac{\Omega}{\square}$ and $3.0{\cdot}10^{8}\ \frac{\Omega}{\square}$.

The proprietary organic dopant "Novaled dopant p-type, number 9" (NDP-9), which is useful for p-type doping in organic light-emitting diodes, will be introduced for contact doping in p-channel top-contact organic TFTs. Many groups utilize the organic dopant

[2] Iron(III) chloride
[3] 4,4,4-trisN-3-methylphenyl-N-phenylamino-triphenylamine
[4] Molybdenum tris-[1,2-bis(trifluoromethyl)ethane-1,2-dithiolene]
[5] Tetracyano-p-quinodimethane
[6] Tetrafluorotetracyano-p-quinodimethane

F4-TCNQ for contact doping [125, 190, 194, 197], but cyclic voltammetry measurements indicate that NDP-9 is more electronegative by about 0.1 eV than F4-TCNQ (Figure 8.2a). Therefore, NDP-9 is expected to be a stronger dopant than F4-TCNQ. To elucidate whether this hypothesis is legitimate, the sheet resistance of 30 nm thick polycrystalline DNTT films doped with a nominally 1 nm thick layer of either the dopant NDP-9 or the dopant F4-TCNQ was measured. The dopant layers were deposited by vacuum sublimation directly onto the DNTT films. During the dopant depositions the substrates were held at room temperature. Gold was utilized for the contacts. Figure 8.2b shows the sheet resistance of a DNTT film **without doping**, **with F4-TCNQ doping** and **with NDP-9 doping**. The DNTT layer without doping has a sheet resistance of 10^{13} $\frac{\Omega}{\square}$, but organic doping reduces this value by more than three orders of magnitude. Note that the effect of NDP-9 is seven times stronger than doping with F4-TCNQ. These measurements suggest that NDP-9 is a more appropriate dopant for DNTT films compared with F4-TCNQ.

Figure 8.3 shows AFM images of a 30 nm thick DNTT film on a Si/Al/AlO_x/C18-SAM substrate, onto which a layer of NDP-9 with a nominal thickness of 1, 5, or 15 nm has been deposited. The Figure indicates that a 1 nm thick layer of NDP-9 deposited on a DNTT film leads to isolated clusters that coalesce into a continuous layer when more than 1 nm NDP-9 is deposited.

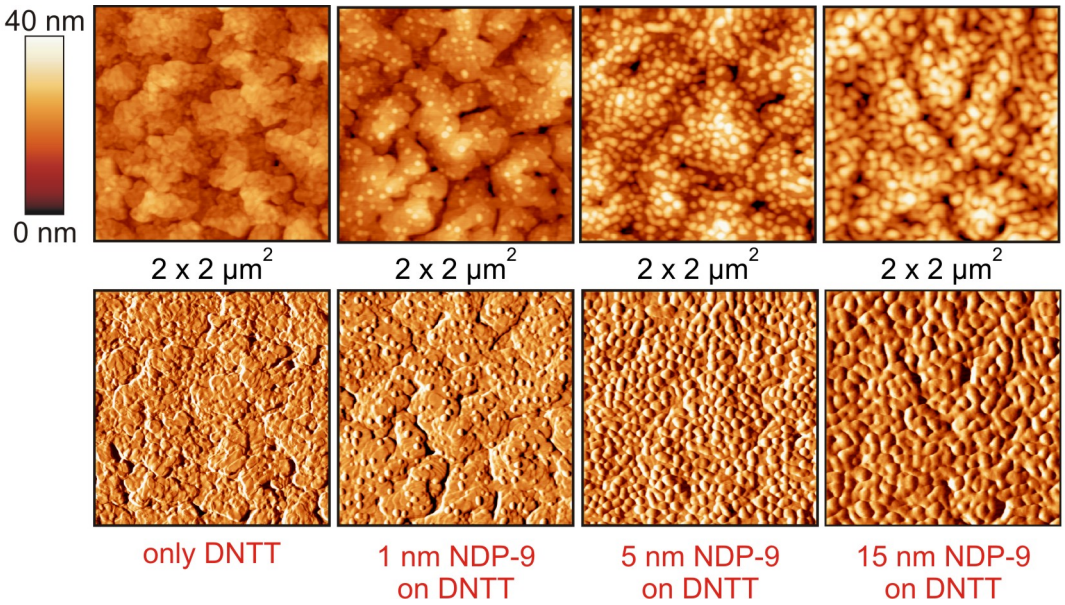

Figure 8.3: Growth of the organic dopant on a DNTT film. Atomic force microscopy images (top row: topography images; bottom row: amplitude images) of 30 nm thick films of the organic semiconductor DNTT (deposited on aluminum/aluminum oxide/C18-SAM structure) without dopant and with three different amounts of the organic dopant NDP9 deposited on top of the DNTT film. The images show that a nominally 1 nm thick layer of the dopant NDP-9 forms isolated clusters when deposited on DNTT. When the nominal thickness of the deposited NDP-9 is increased, the clusters eventually begin to coalesce into a continuous film.

8.3 Electrical characterization of transistors with doping

The TFTs discussed in this chapter are manufactured with the stencil-lithography process described in section 4.1. For (area-selective) contact doping two evaporation sources (one containing the organic dopant NDP-9 and one containing the gold for the source/drain contacts) are simultaneously mounted into the evaporation chamber. A nominally 1 nm thick layer of the dopant is vacuum-deposited (substrate kept at room temperature), immediately followed by the evaporation of the 25 nm thick source/drain gold contacts without breaking the vacuum.

8.3.1 Electrical activity of the organic dopant

The transfer characteristics of DNTT TFTs with a channel length of 4 µm, a channel width of 50 µm, and a contact length of 200 µm **without doping**, **with contact doping** and **with channel and contact doping** are shown in Figure 8.4. The TFT **without doping** has an effective mobility of 0.6 $\frac{cm^2}{Vs}$, a threshold voltage of -1.3 V, and an on/off current ratio of 10^6. By **contact doping**, the effective mobility increases by ∼100% to 1.3 $\frac{cm^2}{Vs}$. The threshold voltage and the on/off current ratio do not change. The TFT **with channel and contact doping** has an effective mobility of 1.4 $\frac{cm^2}{Vs}$ and a threshold voltage of -1.2 V. The on/off current ratio of 10^4 is two orders of magnitude smaller than that of the other two TFTs. These results confirm that the organic dopant NDP-9 is indeed chemically active in the DNTT host and influences the electrical characteristics of DNTT TFTs. Two mechanism can account for the observed modification of DNTT TFTs with doping: a reduction of the *contact resistance* and a reduction of the *trap density*. The analysis of the contact resistance of DNTT TFTs with contact doping will be discussed in section 8.4 in detail.

The reduction of the trap density is elucidated by comparing the electrical characteristics of the TFT **with channel and contact doping** to the TFT **with contact doping**. This comparison is useful, since the effect of doping on the contact resistance (in other words the effect of dopant molecules underneath the contacts) is expected to be identical for both TFTs. Thus, the observed differences must be attributed to the dopant molecules deposited into the channel region. The effective mobility for the TFT **with channel and contact doping** is marginally larger. In addition, the on/off current ratio of the TFT **with channel and contact doping** is two orders of magnitude smaller than that of the TFT **with contact doping**. That means, even without the accumulation of charge carriers by the external gate-source voltage, the TFT channel is conducting. Both effects, the larger mobility and the higher off-state current, can be explained by excess charge

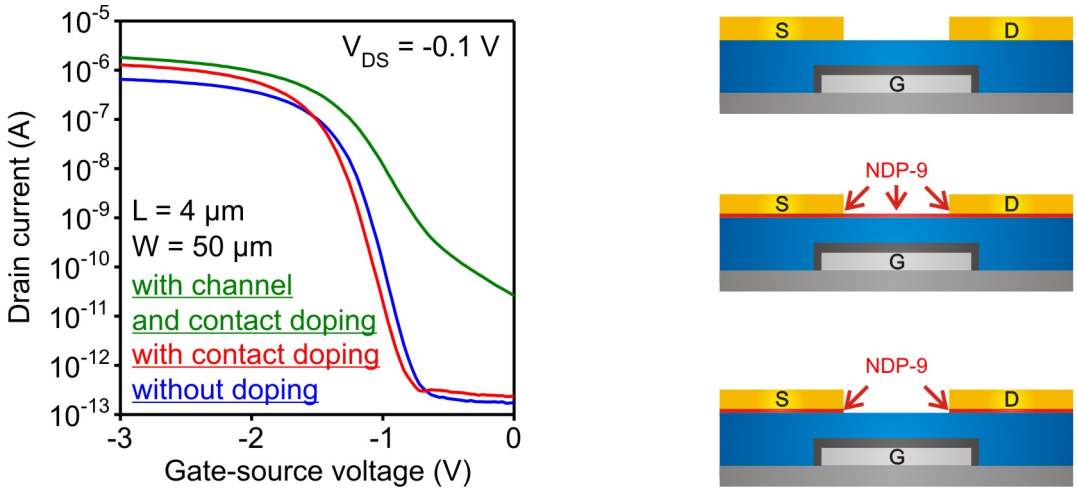

Figure 8.4: Electrical characteristics of TFTs with doping. Transfer characteristics of three TFTs, each having a channel length of 4 µm, a channel width of 50 µm, and a contact length of 200 µm. The TFTs are fabricated without doping, with (area-selective) contact doping and with contact and channel doping. Without doping, the effective mobility is 0.6 $\frac{cm^2}{Vs}$, and the on/off current ratio is 10^6. By channel and contact doping, the effective mobility increases to 1.4 $\frac{cm^2}{Vs}$, but the on/off current ratio reduces to 10^4. This reduction is attributed to excess holes on top of the DNTT film. The TFT with (area-selective) contact doping has a mobility of 1.3 $\frac{cm^2}{Vs}$, while the on/off current ratio is 10^6 (identical to the TFT without doping).

carriers created by doping with NDP-9. The excess charge carriers fill the trap states in the polycrystalline DNTT film, so that the charge-carrier mobility (slightly) increases. When most trap states are filled, the excess holes produce an intrinsic conductivity in the DNTT film, so that a finite current for $V_{GS} = 0\,V$ is observed. Note that a 30 nm thick film of NDP-9 (without any organic semiconductor) is not electrically conducting, so that the organic dopant itself cannot account for the finite current at $V_{GS} = 0\,V$.

To estimate the excess charge-carrier density incorporated in the DNTT film, one can utilize the following approach. The DNTT film between the gate dielectric (aluminum oxide/SAM) and the NDP-9 clusters on top of the DNTT film is insulating for $V_{GS} = 0\,V$ (Figure 8.5a). This assumption demands that the excess charge carriers created by doping are limited to the surface of the DNTT film and do not diffuse into the bulk. Under this hypothesis the DNTT film can be considered as an additional dielectric, which has a thickness of 30 nm and a relative permittivity ε_r of 2-3 [198]. This yields an additional capacitance per area C_{sc} of 70 $\frac{nF}{cm^2}$. The additional capacitance dominates over the gate dielectric capacitance ($C_i \sim 700\,\frac{nF}{cm^2}$), so that the total dielectric capacitance per area is $\sim 70\,\frac{nF}{cm^2}$ ($\frac{1}{C_{total}} = \frac{1}{C_{sc}} + \frac{1}{C_i}$). For the TFT **with channel and contact doping** one can estimate a "threshold voltage" $V_{th,doped}$ of approximately +1 V to turn the TFT off (at a drain current of 1 pA). Thus, using the relation

$$n = \frac{1}{e} \cdot C_{total} \cdot V = \frac{1}{e} \cdot C_{total} \cdot \mid V_{GS} - V_{th,doped} \mid, \tag{8.1}$$

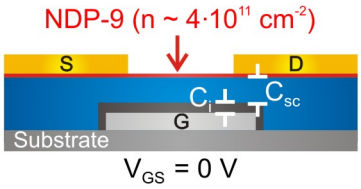

Figure 8.5: Excess hole density introduced by organic doping. a) The schematic illustrates the total capacitance for V_{GS} = 0 V that consists of a series connection of the gate dielectric capacitance C_i (aluminum oxide/SAM) and the non-conducting organic semiconductor capacitance C_{sc}. The image describes the effective total capacitance of the TFT, when the drain current is dominated by the excess charge-carrier density on top of the DNTT film.

with the elementary charge e ($1.6{\cdot}10^{-19}$ A·s), a surface charge-carrier density of $4 \cdot 10^{11}$ cm^{-2} created by the organic dopant is estimated (for V_{GS} = 0 V).

8.3.2 Thin-film transistors with reduced lateral dimensions

The electrical characteristics of a TFT **without doping** and a TFT **with (area-selective) contact doping** are shown in Figure 8.6. Both TFTs have a channel length of 2 µm, a channel width of 20 µm, and a contact length of 5 µm. Without doping, the effective mobility is 0.1 $\frac{cm^2}{Vs}$ in the linear region and 0.6 $\frac{cm^2}{Vs}$ in the saturation region, and the on/off current ratio is 10^6. The small contact length of the TFT accounts for a significant contact resistance, so that the drain current increases nonlinearly and the effective mobility is small. In contrast, by contact doping the linearity of the drain-current increase is greatly improved and the maximum drain current ($V_{GS} = V_{DS}$ = -3 V) is higher compared to the TFT without doping. Therefore, the effective mobility of the TFT with contact doping is 0.4 $\frac{cm^2}{Vs}$ in the linear region (+300% compared to the TFT without doping) and 0.7 $\frac{cm^2}{Vs}$ in the saturation region (+20% compared to the TFT without doping). The off-state drain current (10^{-13} A for both TFTs), the threshold voltage (-1.2 V), and the subthreshold swing (~85 mV/decade) are not affected by contact doping .

Nonlinearities

The beneficial effect of contact doping manifests itself in an improved linearity of the output characteristics (Figure 8.6d). Figure 8.7 shows the schematics of the three mechanisms that have been already introduced in section 6.2.2 on page 58 to describe the nonlinear drain-current increase. In the following, these three models will be taken into account and discussed in the framework of doped contacts.

- The excess charge density in the semiconductor increases by doping, so that the screening length in the semiconductor is reduced. Thus, the width of the **field-**

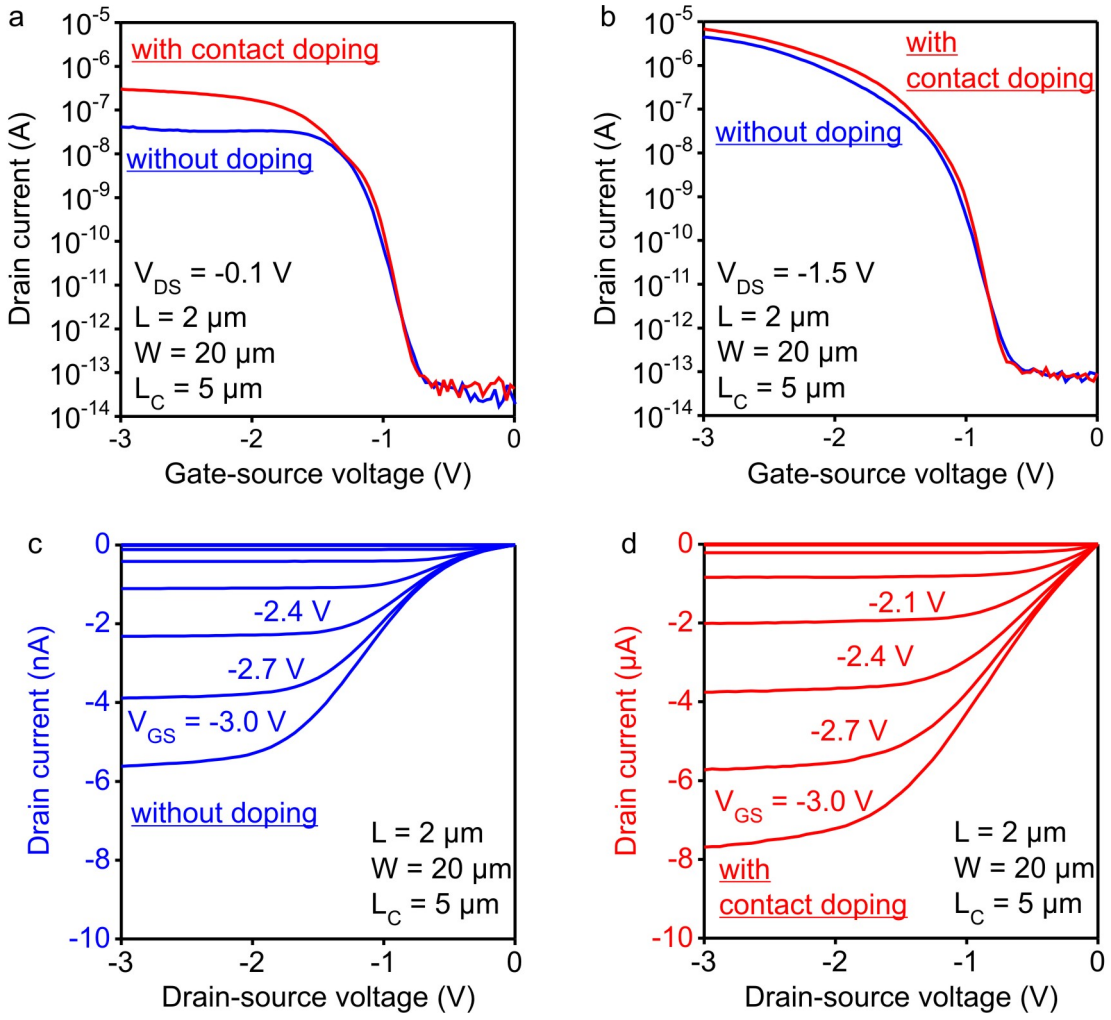

Figure 8.6: Electrical characteristics of DNTT TFTs without doping and with contact doping. The TFTs have a channel length of 2 µm, a channel width of 20 µm, and a contact length of 5 µm. a, b) Transfer characteristics in the linear (a) and saturation (b) region of the two TFTs. In the linear region, the mobility increases from 0.1 $\frac{cm^2}{Vs}$ to 0.4 $\frac{cm^2}{Vs}$ (+300%) and in the saturation region from 0.6 $\frac{cm^2}{Vs}$ to 0.7 $\frac{cm^2}{Vs}$ (+20%) by contact doping. c, d) Output characteristics of the TFTs without doping (c) and with contact doping (d). Contact doping greatly improves the linearity of the output characteristics.

dependent Schottky barrier decreases (Figure 6.5a) and the amount of charge carriers that tunnel across this barrier increases. Therefore, by contact doping the contact resistance is decreased and the drain-source voltage drop along the channel is increased, so that the nonlinear drain-current increase is reduced.

- As introduced in section 6.2.2, the nonlinearity may be also caused by a **field-dependent mobility** from the contacts down to the accumulation layer (Poole-Frenkel effect). Contact doping reduces the average trap energy and trap density, so that the thermal energy necessary to release charge carriers is reduced and the mobility is increased (Figure 8.7b). Thus, the resistance of the limiting contact

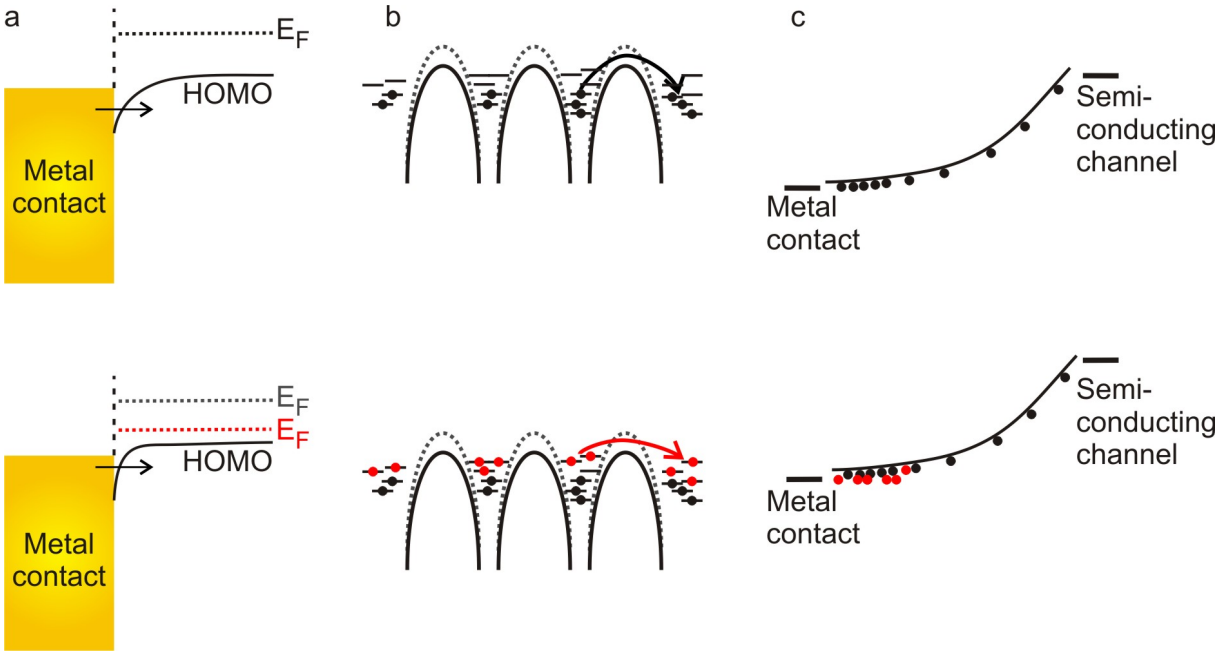

Figure 8.7: Possible mechanisms accounting for the reduction of the observed nonlinearities in the output characteristics by organic doping. a) Schottky barrier at the semiconductor/contact interface. By doping the density of holes in the organic semiconductor is increased and the width of the Schottky barrier is reduced and the rate of charge carriers that tunnel across the interface increases. b) Field-dependent mobility (Poole-Frenkel effect) from the metal contacts down to the accumulation channel at the gate dielectric/semiconductor interface. When the average trap energy is reduced by the incorporation of excess holes, the thermal energy necessary to release charge carriers is reduced and the mobility is higher. c) Space-charge limited current (SCLC) from the metal contacts down to the accumulation channel at the dielectric/semiconductor interface.

region may be decreased and the contribution to the total transistor resistances is smaller, so that the nonlinearity is reduced.

- The **SCLC model** was also proposed to account for the nonlinearity in the output characteristics (section 6.2.2). In this model a high charge-carrier density is assumed that remains in the semiconductor close to the contacts. Previously it was assumed that the dopants are located on top of the organic semiconductor. Under this hypothesis doping of the contact area would further increase the charge-carrier density in semiconductor, so that no beneficial effect on the contact resistance by contact doping may be expected (Figure 6.5c).

In summary, it may be possible to increase the field-dependent mobility perpendicular to the gate dielectric by doping. However, the equation describing the Poole-Frenkel effect (equation 6.7 on page 62) is dominated by the drain-source voltage rather than the charge-carrier mobility μ. Therefore, the model which is most likely describing the reduction of the nonlinear drain-current increase is the field-dependent Schottky-barrier model.

8.4 Contact resistance analysis

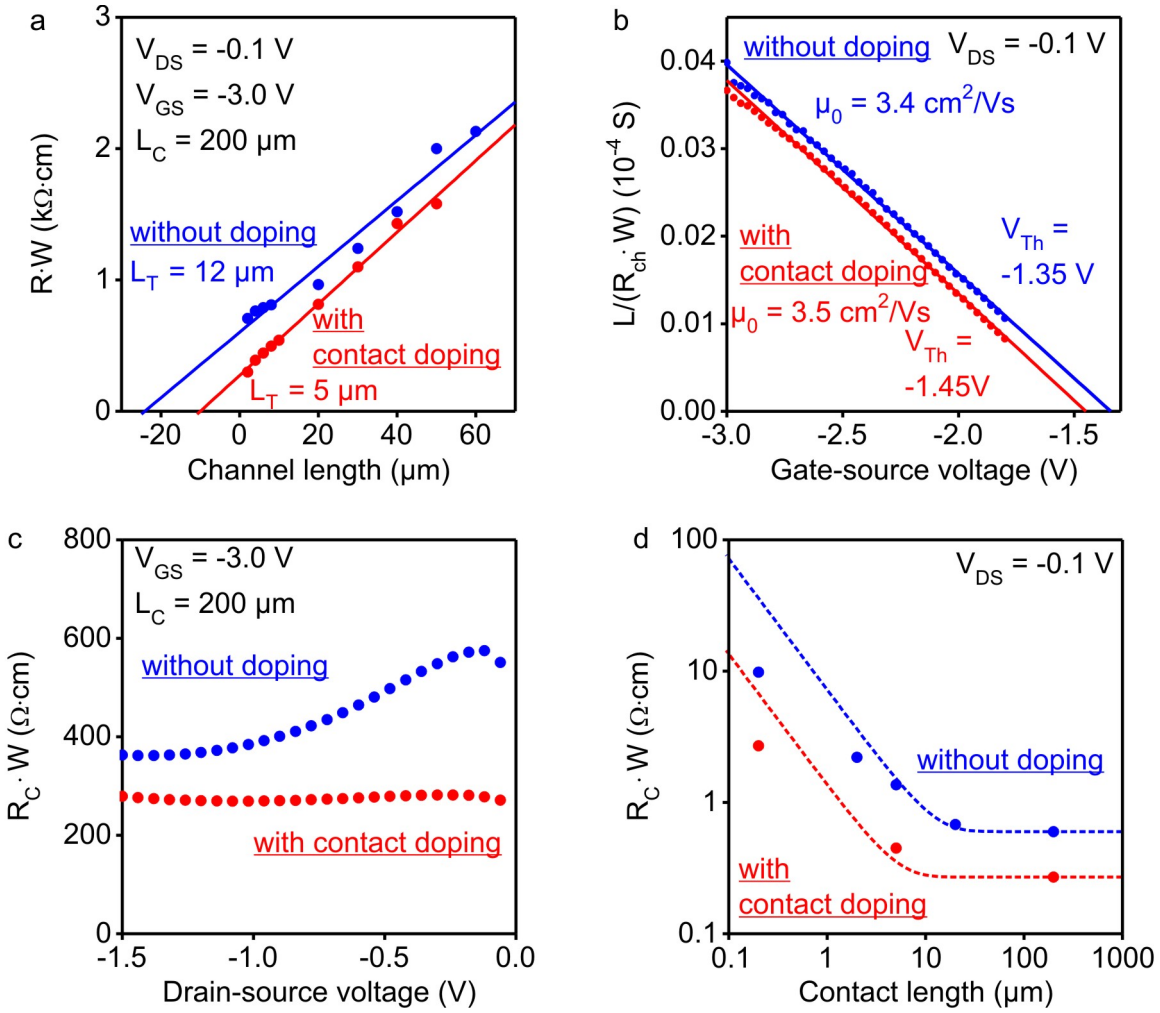

Figure 8.8: Electrical characteristics of transistors without doping and with contact doping. a) Transmission line method for a set of TFTs with a contact length of 200 µm to extract the contact resistance and transfer length. Without contact doping, the contact resistance is 600 Ω·cm and the transfer length 12 µm. By contact doping the contact resistance and the transfer length are reduced to 270 Ω·cm and 5 µm, respectively. b) Extraction of the intrinsic mobility and threshold voltage for both types of TFTs. The intrinsic mobility is 3.4 $\frac{cm^2}{Vs}$ without doping and 3.5 $\frac{cm^2}{Vs}$ with contact doping. The intrinsic threshold changes by only 0.1 V. c) Contact resistance as a function of the drain-source voltage. The drain-source voltage dependence for TFTs with contact doping is greatly reduced. d) Contact resistance as a function of the contact length for both types of TFTs indicating the beneficial effect of contact doping. The TFTs with contact doping have a contact resistance of 270 Ω·cm (contact length of 200 µm), 450 Ω·cm (contact length of 5 µm), and 2700 Ω·cm (contact length of 0.2 µm).

To analyze the effect of contact doping on the contact resistance, the transmission line method (section 6.2 on page 53) was applied to a set of TFTs **without doping** and **with contact doping** (Figure 8.8 and table8.1). The TFTs have a channel length between 1 and 60 µm, a channel width of 200 µm, and a contact length of 200 µm. The TFTs

	without doping	with contact doping
Contact resistance (Ω·cm)	600	270
Sheet resistance $\left(\frac{k\Omega}{\square}\right)$	250	270
Transfer length (µm)	12	5
Contact resistivity (Ω·cm^2)	0.36	0.07
Intrinsic mobility $\left(\frac{cm^2}{Vs}\right)$	3.4	3.5
Intrinsic threshold voltage (V)	-1.35	-1.45

Table 8.1: Electrical characteristics of DNTT TFTs without doping and with contact doping extracted using the transmission line method.

without doping have a contact resistance of 600 Ω·cm, a sheet resistance of 250 $\frac{k\Omega}{\square}$, a transfer length of 12 µm, and a contact resistivity of 0.36 Ω·cm^2. In contrast, the TFTs **with contact doping** have a substantially reduced contact resistance of 270 Ω·cm, a reduced transfer length of 5 µm, and a reduced contact resistivity of 0.07 Ω·cm^2. The DNTT sheet resistance is not affected by contact doping. The intrinsic mobility of the TFTs with contact doping is 3.5 $\frac{cm^2}{Vs}$ and the intrinsic threshold voltage is -1.4 V (Figure 8.8b, extracted using equation 6.5 on page 54), which is in principle identical to TFTs without doping (section 6.2).

Strictly speaking, the TLM can be only applied when the sheet resistance is constant along the entire transistor channel [81]. In the TFTs without contact doping, this is indeed the case, so the TLM can be safely used for these TFTs. For the TFTs with contact doping the charge-carrier density might not be constant along the entire channel. Therefore, the TLM results from the TFTs with contact doping have to be taken with caution and serve here only as a rough guidance.

Figure 8.8c illustrates the contact resistance as a function of the drain-source voltage. For the TFTs with contact doping the contact resistance is independent of the drain-source voltage (in contrast to the TFTs without doping). This is consistent with the improved linearity of the output characteristics.

The contact resistance as a function of the contact length for TFTs without doping and with contact doping is shown in Figure 8.8d. The principle relation between the contact resistance and the contact length for TFTs without doping and with contact doping is identical. However, TFTs with contact doping have a contact resistance of 270 Ω·cm (for a contact length of 200 µm), 450 Ω·cm (for a contact length of 5 µm), and 2700 Ω·cm (for a contact length of 0.2 µm, appendix D, Figure D.2 on page 126). The differences between the experimentally obtained results and the theoretically simulated values can be again explained by the mechanisms discussed in Figure 6.6b on page 63.

8.5 Diffusion of dopant molecules

Organic transistors with contact doping often exhibit transfer characteristics with a high off-state drain current [25, 191, 196]. This is most likely induced by unintentional doping of the transistor channel, so that the excess charge-carrier density in the channel increases. One reason for this might be the utilization of small charged metallic ions for doping, which easily diffuse along the electric field from the source to the drain contact [25]. Another reason might be an unintentional sliding of the shadow mask when the evaporation chamber is opened between the dopant and the source/drain contact material evaporation. The restart of the vacuum pumps can cause vibrations, so that the shadow mask shifts between theses two evaporations. Again, in this work the dopant and the source/drain contact material are deposited without breaking the vacuum. Since the organic dopants and the host material interact via weak van der Waals forces (∼meV), the dopant molecules might also diffuse (driven by thermal energy) from the contact area into the channel area.

Bias-stress measurements on a nanoscale DNTT TFT have been performed to verify the positional stability of NDP-9 molecules in the contact area. The TFT with contact doping has a channel length of 150 nm, a channel width of 500 nm, and a contact length of 200 nm. Figure 8.9a,b shows the transfer characteristics of the same TFT recorded before and immediately after the bias-stress measurement. The drain current during bias stress is also shown. A continuous gate-source voltage and drain-source voltage of -3 V were applied for one hour. This produces an electric field of 5.2 $\frac{\mathrm{MV}}{\mathrm{cm}}$ across the gate dielectric and 200 $\frac{\mathrm{kV}}{\mathrm{cm}}$ from the source to the drain contact. A large gate-source electric field accumulates a large charge-carrier density in the channel. Thus, the trapping rate is large and the reduction in drain current is more significant than for a weak gate-source electric field [177, 199]. The drain-current decrease and threshold-voltage shift for the DNTT TFT with contact doping is on the same time scales as observed for DNTT TFTs without doping [177]. More importantly, the **off-state drain current** is not affected by the time and bias-dependent measurement and stays at 1 pA. It can be concluded that no significant amount of the dopant capable of modifying the drain current is diffusing/drifting into the 150 nm long TFT channel during the observed period.

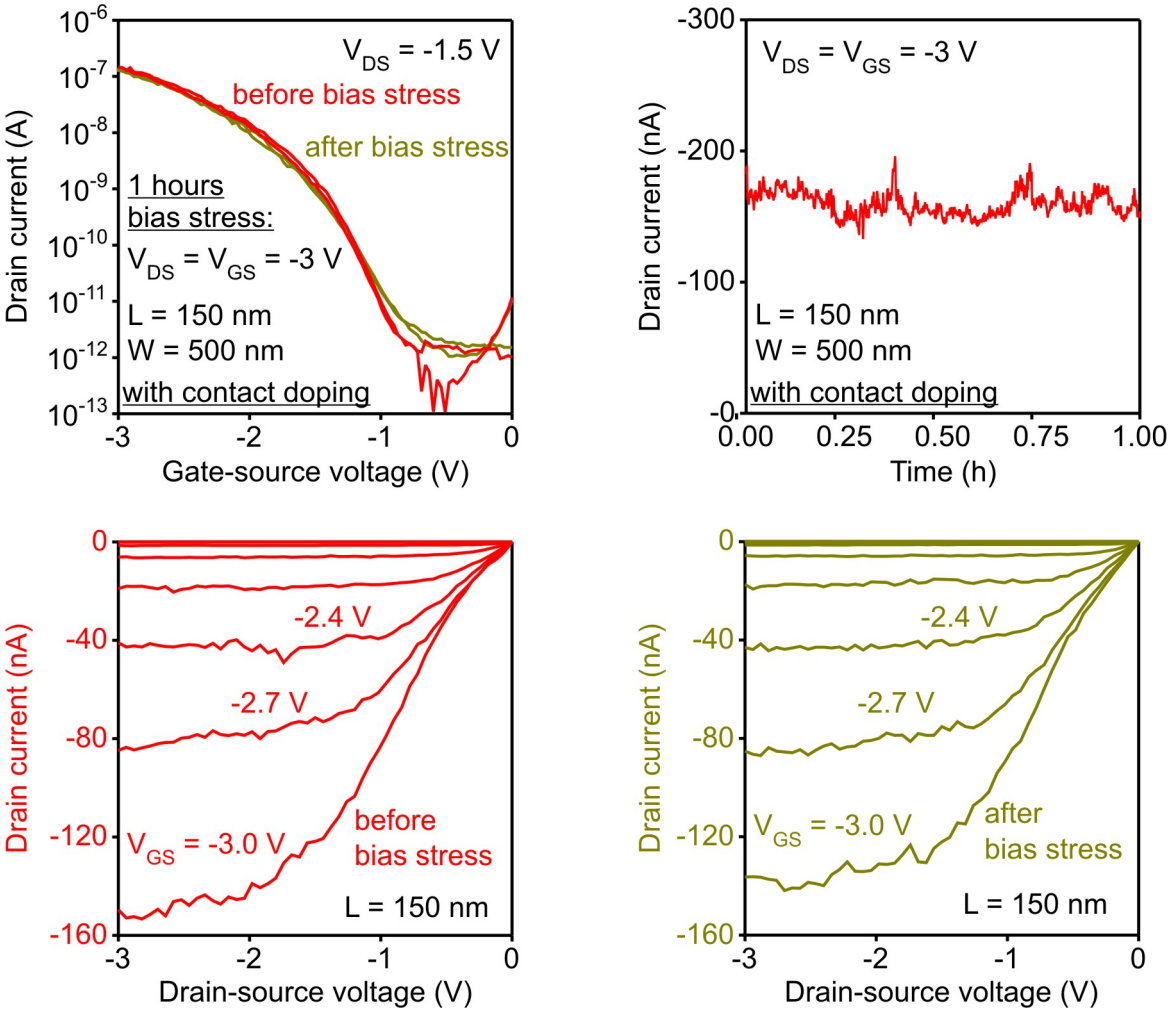

Figure 8.9: Verification of the positional stability of the organic dopant in nanoscale transistors. The TFT with contact doping has a channel length of 150 nm, a channel width of 500 nm, and a contact length of 200 nm. For bias stress a constant drain-source and gate-source voltage of -3 V was applied for 1 hour. a) Transfer characteristics recorded before and directly after the bias stress. The off-state drain current is below 1 pA before and after the bias stress indicating that no significant amount of dopants influencing the electrical characteristics diffused/drifted into the channel region. b) Drain current during bias stress. c, d) The output characteristics of the TFT before (c) and after (d) the bias stress indicate no significant changes.

Conclusion

The strong electron acceptor NDP-9, which proofed useful to increase the excess hole density and hole transport efficiency in organic light-emitting diodes, was utilized for doping DNTT TFTs. It was demonstrated that a nominally 1 nm thick layer of NDP-9 increases the conductivity of a DNTT film by more than four orders of magnitude. When the organic dopant is area-selectively deposited underneath the contacts, the energy barrier between the gold contacts and the DNTT film is modified. For a contact length of 200 µm the contact resistance is reduced by a factor of two and is 270 kΩ·cm. The most beneficial effect is achieved for a contact length of 200 nm, in which the contact resistance is reduced from 9800 kΩ·cm to 2700 kΩ·cm. A DNTT TFT with a channel length of 2 µm and a contact length of 5 µm has a much higher mobility (0.4 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$) **with contact doping** than **without doping** (0.1 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$). The on/off current ratio, the subthreshold swing, and the threshold voltage are not affected by contact doping.

9 Integrated circuits: dynamic characterization

The investigation of the dynamic properties of organic transistors is essential for their implementation in real applications, such as active-matrix displays. In this chapter, the experimental results on the dynamic properties of organic transistors **without contact doping** will be presented. There are different possibilities to measure the cut-off frequency of a transistor, such as the *unity-gain method*, the dynamic characterization of an *individual inverter*, or the utilization of a *ring oscillator*.

The unity-gain method has the distinct advantage that only one single transistor is required. The transistor is operated in the transdiode region and the constant drain-source and gate-source voltages are superimposed with alternating current (AC) voltages [14, 200]. The AC drain and gate currents are measured as a function of the input-voltage frequency. The AC gate current is proportional to the frequency (since the displacement current across the gate dielectric is frequency-dependent). In contrast, the AC drain current is independent of the input-voltage frequency. When both AC currents have identical values, the current gain is zero and the cut-off frequency is reached (section 3.2). For a transistor with a channel length of 1 µm, a contact length of 1 µm, a mobility of 1 $\frac{cm^2}{Vs}$, and a supply voltage of 1 V a cut-off frequency of 5 MHz is expected according to equation 3.30 on page 33. Precise current measurements at such high frequencies are quite challenging. Therefore, the AC currents are often measured up to a frequency of less than 10 kHz and the cut-off frequency is extrapolated using a linear regression [14, 200].

In contrast, simple integrated circuits such as individual inverters and ring oscillators require the recording of high-frequency voltages, which can be done by simply using an oscilloscope. Therefore, inverters and ring oscillators using the stencil-lithography process introduced in section 4.1 have been fabricated. Each circuit needs at least one probe pad with a size of 200 x 200 µm^2. If the circuits were made on a silicon wafer with 100 nm SiO_2 (33 $\frac{nF}{cm^2}$), these probe pads would introduce a parasitic capacitance of 13 pF. However, a transistor with a channel length of 1 µm, a channel width of 10 µm, and a contact length of 2 µm has a capacitance of only 0.35 pF (C_i = 700 $\frac{nF}{cm^2}$). This means that the dynamic performance of the circuits would be limited by the parasitic capacitances of the probe pads, rather than the TFTs. Therefore, all inverters and ring oscillators in this work have

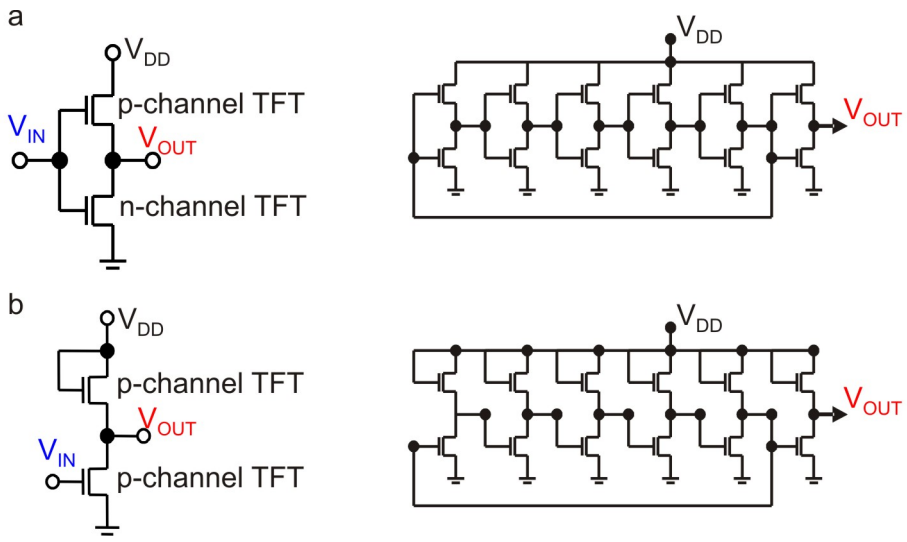

Figure 9.1: Circuit diagrams of various inverters and ring oscillators. a) Complementary inverter and complementary 5-stage ring oscillator circuits diagram. b) Unipolar saturated load inverter and unipolar saturated-load 5-stage ring oscillator circuit diagram.

been manufactured on insulating substrates (glass) to avoid any limitations introduced by the probe pads.

The steady-state transfer characteristics of inverters are discussed in section 9.1. Dynamic measurements on inverters and ring oscillators are presented in section 9.2. Concluding remarks on the expected dynamic performance of organic transistors with extremely scaled lateral dimensions (without doping and with contact doping) are discussed in section 9.3.

9.1 Steady-state inverter characteristics

The inverter is the fundamental building block of all digital circuits. It inverts an input signal (logic "1", high level) and directs it to the output node (logic "0", low level). The inverter is a four-terminal device, consisting of an input, output, supply, and ground node. Inverters are composed of a drive and a load element and are either complementary or unipolar. Complementary inverters consist of a p-channel transistor and an n-channel transistor, in which both transistors alternately work as drive or load element (Figure 9.1a). In contrast, unipolar inverters utilize only p-channel (or n-channel) transistors as drive and as load elements (Figure 9.1b). The gate electrode of the load element can be connected to the output node (depletion load) or to the supply node (saturated load). It is also possible to replace the load transistor with an adequate resistor [201].

The basic mode of operation is identical for all types of inverters. It will be briefly discussed for a complementary inverter. Here, the supply voltage V_{DD} is positive (+3 V) and the input voltage V_{IN} is switched between 0 V and +3 V. When the input voltage is

0 V, the n-channel transistor is in its off-state and the p-channel transistor is in its on-state (ΔV_{GS} = -3 V). Thus, the output voltage V_{OUT} is +3 V (high level). In contrast, when the input voltage is +3 V, the p-channel transistor is in the off-state and the n-channel transistor is in the on-state, so that the output voltage is 0 V (low level).

The advantage of the complementary design over the unipolar design is the greatly reduced steady-state power dissipation. In complementary inverters current flows only when switching between the high-level and the low-level state. In the steady-state operation only the gate leakage current between the gate electrode and the contacts is present. In contrast, for unipolar inverters there is always a finite (high) current flowing when the inverter is in the high-level state.

9.1.1 Complementary inverters

Organic semiconductors for n-channel transistors

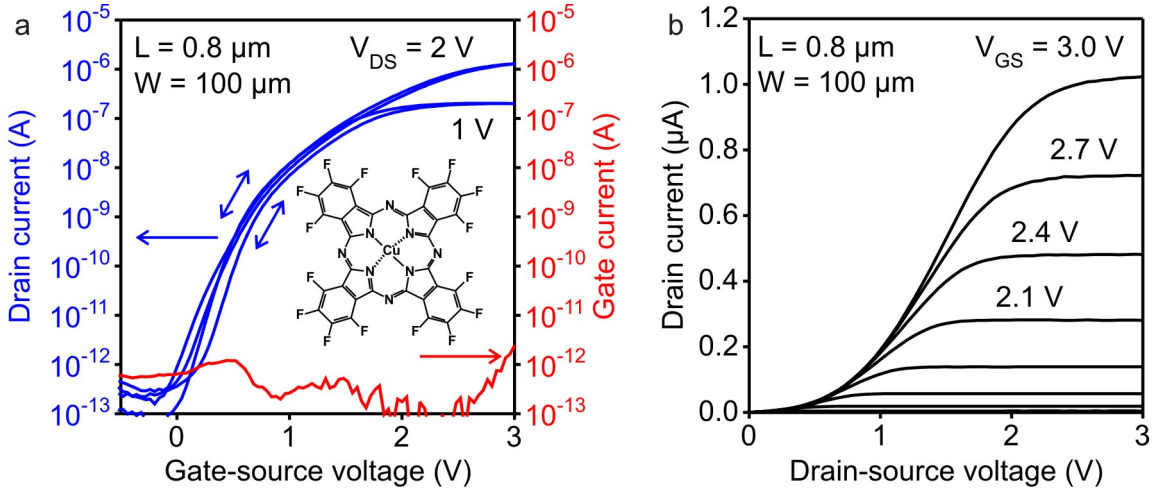

Figure 9.2: Electrical characteristics of an n-channel F_{16}CuPc transistor. Transfer and output characteristics of a hexadecafluorocopperphthalocyanine (F_{16}CuPc, chemical structure shown in the inset of graph) transistor with a channel length of 0.8 µm, a channel width of 100 µm, and a contact length of 20 µm. a) The transconductance is 0.01 $\frac{S}{m}$, the effective mobility 0.008 $\frac{cm^2}{Vs}$, the on/off current ratio 10^7, the subthreshold slope 140 mV/decade, the threshold voltage +0.9 V, and the maximum gate current a few pA. b) The drain current as a function of the drain-source voltage shows a strong nonlinear increase due to the contact resistance, but a pronounced saturation for higher drain-source voltages.

Up to this point in this thesis, all experiments were based on the organic semiconductor DNTT, which is useful to manufacture p-channel transistors. For complementary circuits the combination of p-channel TFTs and n-channel TFTs on the same substrate is required. In n-channel TFTs the energy barrier between the source/drain contacts and the LUMO energy level of the organic semiconductor must be small to allow efficient elec-

tron transport between the contacts and the semiconductor. Simultaneously the energy barrier to the HOMO energy level must be large to avoid ambipolar charge transport. In the literature this was demonstrated for various organic semiconductors with a low LUMO energy level (between -2.5 and -3.0 eV) using low-work-function contact metals (for instance calcium). Electron mobilities of $\sim 10^{-1}$ $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$ have been achieved with this approach [202]. However, organic semiconductors and contact metals with such small electron affinity easily oxidize. Therefore, electrical measurements on these TFTs require an inert atmosphere [202, 203]. One strategy towards air-stable electron transport in organic TFTs is to use a semiconductor in which some or all of the hydrogen atoms are replaced by fluorine atoms. This reduces the HOMO and LUMO energy levels, so that a stable transport of electrons is possible. The concept was successfully demonstrated by Bao and co-workers, who substituted the 16 hydrogen atoms of copperphthalocyanine (CuPc) by 16 fluorine atoms to realize the molecule hexadecafluorocopperphthalocyanine (F_{16}CuPc) [204]. Indeed, the LUMO level of F_{16}CuPc is -4.5 eV [205], which allows the utilization of high-work-function air-stable metals (for instance gold) as a contact metal to realize air-stable n-channel TFTs with an electron mobility of 0.03 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$ [3]. The relatively small mobility (two orders of magnitude smaller than the mobility in DNTT) of the charge carriers is explained by the formation of a disordered interfacial layer at the gate dielectric, which hinders an effective charge transport [67, 68]. Recently, the concept of hydrogen substitution with fluorine was adapted to naphthalene [206] and perylene [207, 208] derivatives and was useful to fabricate air-stable organic n-channel TFTs with a mobility as large as 1.3 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$.

In this work, the commercially available F_{16}CuPc molecule was utilized to fabricate n-channel TFTs. The manufacturing process is similar to that of the DNTT TFTs (section 4.1, page 37). However, during the vacuum deposition of F_{16}CuPc the substrates were kept at 90°C (as opposed to 60°C for the DNTT TFTs). The source/drain contacts also consist of a 25 nm thick gold film. Figure 9.2 shows the transfer and output characteristics of an n-channel F_{16}CuPc TFT with a channel length of 0.8 µm, a channel width of 100 µm, and a contact length of 20 µm. The TFT has a transconductance of 0.01 $\frac{\mathrm{S}}{\mathrm{m}}$, an effective mobility of 0.008 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$, an on/off current ratio of 10^7, a subthreshold swing of 140 mV/decade, and a maximum gate current of 2 pA.

There are reports on F_{16}CuPc TFTs fabricated with a similar process and a mobility of 0.02 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$ [12]. However, those transistors have a much larger channel length of 30 µm, so that the influence of the contact resistance is much smaller. Here, in contrast, the channel length is only 1 µm and the influence of the contact resistance is significant, so that the effective mobility is smaller.

Characterization of complementary inverters

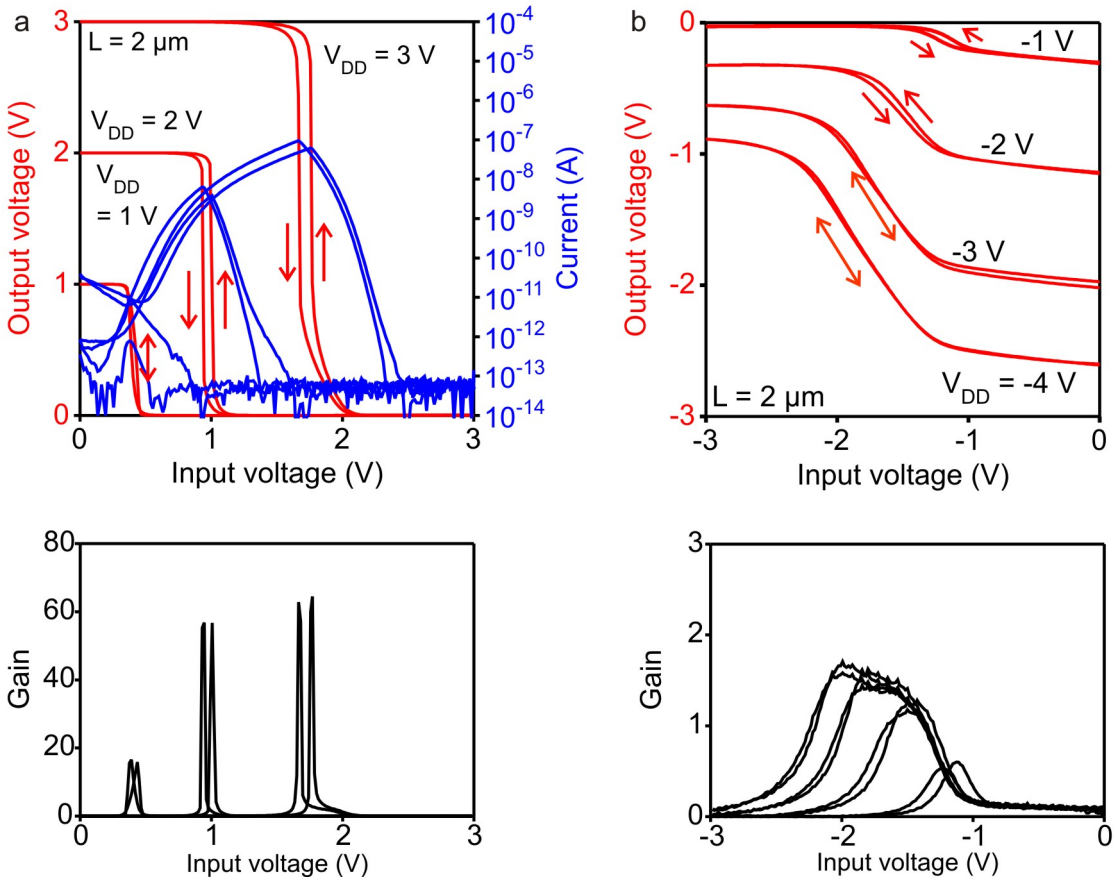

Figure 9.3: Steady-state transfer characteristics of complementary and unipolar inverters. a) The complementary inverter employs a p-channel DNTT TFT with a channel length of 2 µm and a channel width of 10 µm and an n-channel F_{16}CuPc TFT with a channel length of 2 µm and a channel width of 100 µm. The inverter shows sharp rail-to-rail switching with a maximum small-signal gain of 60. The off-state current is only 0.1 pA, so that the steady-state power consumption is ∼0.1 pW. b) The unipolar saturated-load inverter comprises a p-channel DNTT TFT as the drive transistor with a channel length of 2 µm and a channel width of 20 µm, and a p-channel DNTT TFT as the load transistor with a channel length of 10 µm and a channel width of 10 µm. The small signal gain of the inverter is 1.7.

Figure 9.3a contains the steady-state transfer characteristics and the small-signal gain of a complementary inverter. The inverter consists of a p-channel DNTT TFT with a channel length of 2 µm and a channel width of 10 µm, and an n-channel F_{16}CuPc TFT with a channel length of 2 µm and a channel width of 100 µm. Both TFTs have a contact length of 20 µm. The output voltage was measured for input voltages between 0 and 3 V. The supply voltages were kept at fixed values of 1, 2, and 3 V. The inverter displays sharp rail-to-rail switching, a maximum small-signal gain of about 60, and a small steady-state power dissipation of ∼0.1 pW.

9.1.2 Unipolar inverters

The steady-state transfer characteristics and the small-signal gain of a unipolar saturated-load inverter based on DNTT TFTs is shown in Figure 9.3b. The drive TFT has a channel length of 2 µm, a channel width of 20 µm, and a contact length of 5 µm. The load TFT has a channel length and width of 10 µm, and a contact length of 5 µm. The output voltage was measured for an input-voltage sweep between 0 and -3 V. The supply voltages were kept at fixed values of -1, -2, -3, and -4 V. A maximum gain of 1.7 was extracted. This is close to the expected value of 2.3 which is calculated by [209]

$$\text{gain} \leq \sqrt{\left(\frac{\mathrm{W_D} \cdot \mathrm{L_L}}{\mathrm{W_L} \cdot \mathrm{L_D}}\right)}. \tag{9.1}$$

The indices D and L denote the drive and load transistor, respectively. The output-voltage swing is 50% of the input-voltage swing for a supply voltage of -4 V. This lack of full output swing is often observed for unipolar inverters and is caused by the finite resistance of the load element for high input voltages (here: -3 V).

9.2 Dynamic characterization

A ring oscillator is an ideal tool to extract the signal delay of an individual transistor. The ring oscillator consists of an odd number of inverter stages connected in a chain. The output of the last inverter is connected to the input of the first inverter. Like an inverter, a ring oscillator can be either of complementary or unipolar type (Figure 9.1 on page 96). One additional inverter is employed to couple the output signal to an oscilloscope for signal recording. In contrast to an individual inverter, which can be operated and studied at a specific input frequency, a ring oscillator spontaneously starts oscillating when the supply voltage is above a certain threshold voltage. It always operates at the maximum frequency for a specific supply voltage. The capacitance of every individual inverter stage delays the signal propagation by a time τ. The output signal oscillates between two voltages at a frequency f [209]:

$$\mathrm{f} = \frac{1}{2 \cdot \mathrm{n} \cdot \tau}. \tag{9.2}$$

The number of inverter stages is given by n. The signal delay per stage of the ring oscillator is simply obtained by calculating τ.

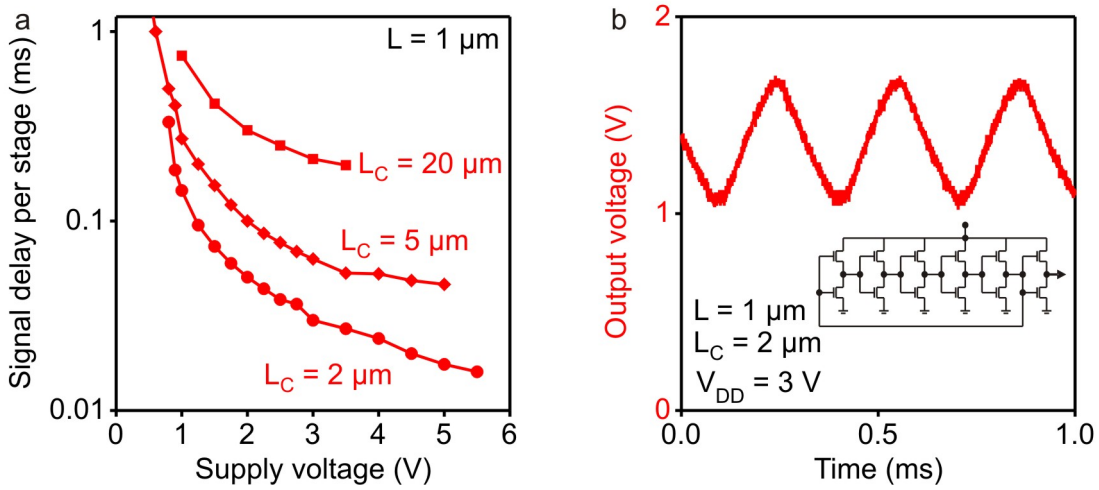

Figure 9.4: Dynamic characterization of 5-stage complementary ring oscillators. The ring oscillators employ p-channel DNTT and n-channel F_{16}CuPc TFTs. a) Signal delay per stage as a function of the supply voltage for 5-stage complementary ring oscillators with a channel length of 1 µm and a contact length of 20, 5, and 2 µm. The reduction of the contact length decreases the parasitic capacitance and increases the dynamic performance. b) Output signal of a 5-stage complementary ring oscillator with a channel length of 1 µm and a contact length of 2 µm. The measured signal propagation delay is 30 µs per stage at a low supply voltage of 3 V.

9.2.1 Complementary integrated circuits

Figure 9.4a shows the signal delay per stage as a function of the supply voltage for three different 5-stage complementary ring oscillators. The TFTs in each ring oscillator has a channel length of 1 µm, a channel width of 10 µm for the p-channel DNTT TFTs and a channel width of 100 µm for the n-channel F_{16}CuPc TFTs. The contact length for the TFTs is 20, 5, and 2 µm. The parasitic capacitances decrease when the contact length is reduced and the signal propagates faster through the ring oscillator. For a supply voltage of 5 V a signal delay per stage of 18 µs is measured for the ring oscillator with a contact length of 2 µm. Note that the speed of these ring oscillators is limited by the smaller mobility in the n-channel TFTs.

It is also remarkable that all ring oscillators operate at a supply voltage of only 1 V. However, the signal delay per stage for these low supply voltages is essentially identical for all three ring oscillators. This effect can be explained by the dominating influence of the contact resistance of F_{16}CuPc TFTs for smaller voltages. In analogy to the DNTT TFTs discussed in section 7.2 and 8.4, the nonlinear drain current increase implies a drain-source voltage dependent contact resistance. Thus, the voltage drop across the contacts decreases and the effective mobility increases for higher operation voltages.

9.2.2 Unipolar integrated circuits

Unipolar ring oscillator

The photograph in Figure 9.5a shows an 11-stage unipolar ring oscillator. In contrast to the saturated-load approach with a single supply voltage V_{DD} shown in Figure 9.1b, here, the gate electrode is not connected to the drain node and an additional voltage V_{Bias} is required. Figure 9.5b shows the measured signal delay of an 11-stage ring oscillator employing only p-channel DNTT TFTs. The drive TFTs have a channel length of 1 µm, a channel width of 72 µm, and a contact length of 5 µm. The load TFTs have the same channel and contact length, but the channel width is 24 µm. For a supply voltage of 4 V and a bias voltage of -1 V the output voltage oscillates with a period of 6 µs.

Figure 9.5c summarizes the signal delay per stage as a function of the supply voltage for two different 11-stage ring oscillators. One ring oscillator has a channel length of 4 µm, a contact length of 20 µm, and a channel width of 110 µm and 24 µm for the drive and load TFTs, respectively. The other ring oscillator employs TFTs with a channel length of 1 µm, a contact length of 5 µm, and a channel width of 72 µm and 24 µm, respectively. The signal delay per stage is as small as 230 ns at a supply voltage of 4.2 V for the ring oscillator with the smaller lateral dimensions. It is noteworthy that this ring oscillator has a signal delay per stage of less than 1 µs for a supply voltage of 1.2 V.

Unipolar inverter

In addition, an individual inverter was dynamically characterized using an active probe needle. Figure 9.5d contains the dynamic characteristics of this unipolar saturated-load inverter. The DNTT drive TFT has a channel length of 1 µm and a channel width of 20 µm. The DNTT load TFT has a channel length and width of 10 µm. The contact length for both TFTs is 2 µm. An AC voltage with an amplitude of 3 V at a frequency of 1 MHz was applied to the input node while the supply voltage was kept at -5 V. Since the total capacitance of this inverter is only 1.5 pF, a high-input-impedance active probe needle was utilized. This allows recording the output signal without limitations that are introduced by the measurement setup capacitances. One possible tool is the Picoprobe® 12C distributed by GGB Industries, which is directly connected to the output node and conducts the signal to an oscilloscope for signal recording. The output signal in Figure 9.5d clearly follows the input signal for a frequency as high as 1 MHz. Assuming a simple exponential decay for the charging of the drive TFT $\left(\sim \exp\left(-\frac{t}{\tau}\right)\right)$, a time delay constant of 46 ns is extracted. A DNTT TFT with a channel length of ∼1 µm has a mobility of approximately 0.7 $\frac{cm^2}{Vs}$ (Figure 7.2b on page 73). For a supply voltage of 5 V and a contact length of 2 µm one expects a cut-off frequency of ∼10 MHz (= 50 ns for the charging or

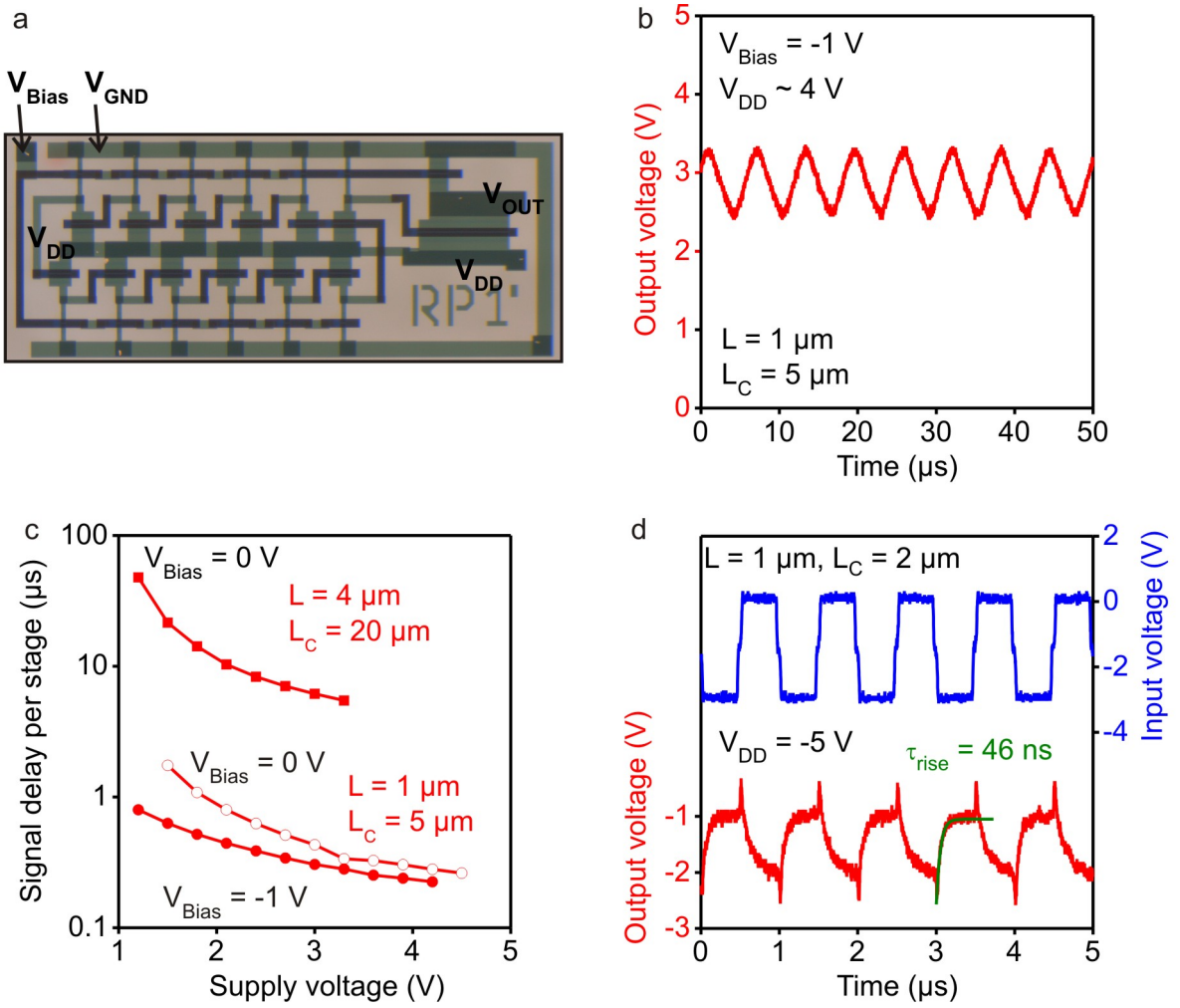

Figure 9.5: Dynamic characteristics of 11-stage unipolar ring oscillators and of an individual inverter. The ring oscillators and the inverter employ p-channel DNTT TFTs. a) Photograph of an 11-stage unipolar ring oscillator. The resistance of the load TFT can be tuned using the bias voltage V_{Bias}. b) Output signal of a unipolar ring oscillator with a channel length of 1 µm and a contact length of 5 µm at a supply voltage of ~4 V. The measured signal oscillation period is 6 µs. c) Signal delay per stage as a function of the supply voltage for 11-stage unipolar ring oscillators with a channel length of 4 µm (contact length of 20 µm) and a channel length of 1 µm (contact length of 5 µm). For the latter a signal delay per stage as small as 230 ns was measured. d) AC input and output voltage of a unipolar inverter at a frequency of 1 MHz. The drive TFT has a channel length of 1 µm and a channel width of 20 µm, and the load TFT a channel length and width of 10 µm. The contact length for both TFTs is 2 µm. The output signal clearly follows the input signal for a supply voltage of -5 V. Assuming a simple exponential decay a time constant of 46 ns is extracted.

discharging process) according to equation 33. This result is in good agreement with the time delay constant of 46 ns that has been measured (Figure 9.5d).

9.2.3 Discussion

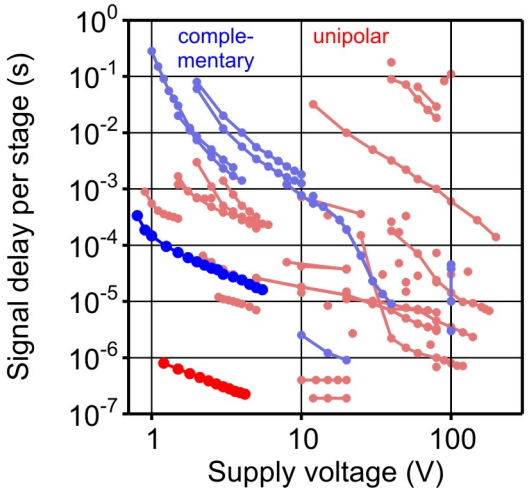

Figure 9.6: Literature summary on the signal delay per stage of organic ring oscillators. The literature summary on the signal delay per stage of organic complementary (light blue) and unipolar (light red) ring oscillators measured in air is mainly adapted from [3]. In addition, the signal delay per stage of the complementary (dark blue) and unipolar (dark red) ring oscillators, each with a channel length of 1 µm, fabricated in this thesis are also shown.

Figure 9.6 contains a literature summary on the signal delay per stage of organic complementary (light blue) and unipolar (light red) ring oscillators measured in air but also under inert or vacuum conditions. The graph considers reports on organic ring oscillators between 1995 and 2010 and was mainly adapted from [3]. In addition, the signal delay per stage of the complementary (dark blue) and unipolar (dark red) ring oscillators, each with a channel length of 1 µm, fabricated in this thesis are added to the diagram.

For complementary ring oscillators, the record dynamic performance with a stage delay of less than 1 µs for a supply voltage of 20 V was reported by Bode and co-workers for p-channel pentacene and n-channel C60 transistors [176]. However, n-channel transistors based on C60 are not air-stable, so that the ring oscillators had to be measured under inert conditions. For air-stable complementary ring oscillators the value of 30 µs at a supply voltage of 3 V obtained in this work is a factor of 100 faster than the previous record at a comparable supply voltage [12]. It is also within a factor of 3 of the fastest air-stable organic complementary ring oscillator, which required a much larger supply voltage of 100 V [210].

Among the unipolar (air-stable) ring oscillators the record signal delay per stage of 190 ns was reported by the IMEC group using pentacene transistors driven at a supply voltage

of 13 V and with lateral dimensions of 2 µm [211]. This signal delay per stage is only 20% faster compared to the results reported in this work, however, the supply voltage used by the IMEC group is 300% higher compared to this work. For low-voltage operation (< 5 V) the organic ring oscillators demonstrated in this work are the fastest reported.

9.3 Influence of the contact length - simulation

In section 6.2 on page 53 it was demonstrated that the contact resistance depends on the contact length. Thus, the effective mobility decreases when the contact length is reduced. Simulations have been carried out for TFTs **without contact doping** and **with contact doping** to elucidate the influence of the contact length on the cut-off frequency.

Without contact doping - simulation

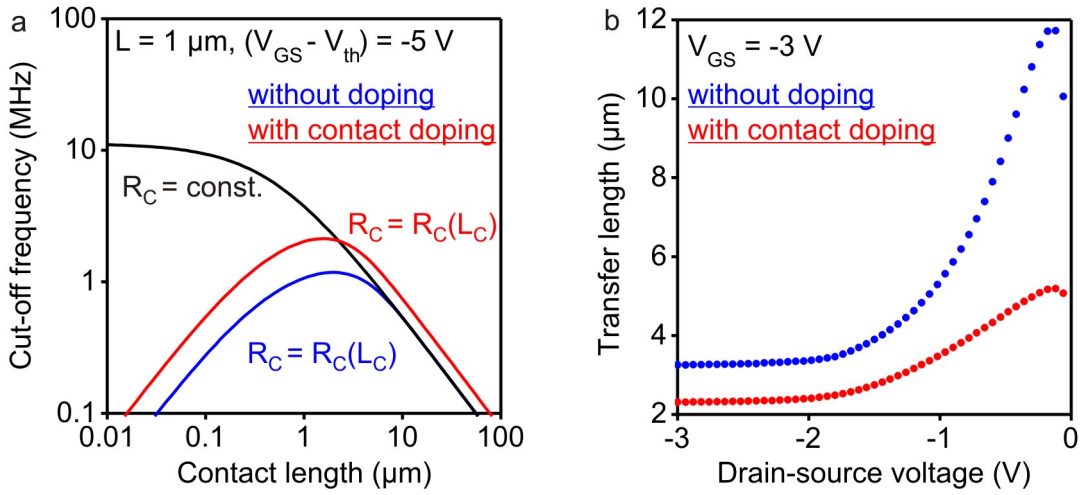

Figure 9.7: Simulations of the relation between the contact length and the cut-off frequency of an individual TFT. a) Simulation of the cut-off frequency as a function of the contact length for a TFT with a channel length of 1 µm, an intrinsic mobility of 3.4 $\frac{cm^2}{Vs}$ and a supply voltage of 5 V. The graph contains the simulations for two TFTs **without doping**. One of those has a **constant** contact resistance of 400 Ω·cm (black curve), and the other one has a contact resistance that **depends on the contact length** (L_T = 3.5 µm) (blue curve). In addition, a third TFT **with contact doping** and a contact resistance that **depends on the contact length** (L_T = 2.5 µm) (red curve) is shown. When the contact resistance depends on the contact length, the strong reduction in effective mobility causes a maximum in the cut-off frequency. Contact doping is useful to reduce the contact resistance and to improve the cut-off frequency. b) Experimentally derived transfer length as a function of the drain-source voltage for TFTs without and with contact doping. The transfer length decreases when the drain-source voltage increases. This observation is attributed to a reduction of the contact resistance for higher drain-source voltages.

The cut-off frequency (in the saturation region) is given by

$$f_T = \frac{\mu_{eff} \cdot (V_{GS} - V_{th})}{2\pi \cdot L \cdot (L + 2 \cdot L_C)}. \tag{9.3}$$

If one combines equations 9.3 and 3.34, which describes the mobility under the influence of the contact resistance, one obtains for the cut-off frequency:

$$f_T = \mu_0 \left(1 - \left(\frac{\mu_0 \cdot W \cdot C_i \cdot R_C \cdot (V_{GS} - V_{th})}{L + \mu_0 \cdot W \cdot C_i \cdot R_C \cdot (V_{GS} - V_{th})}\right)^2\right) \cdot \frac{(V_{GS} - V_{th})}{2\pi \cdot L \cdot (L + 2 \cdot L_C)}. \tag{9.4}$$

Equation 9.4 is useful to simulate the relation between the cut-off frequency and the contact length. This is shown in Figure 9.7a for a TFT with a channel length of 1 µm, an intrinsic mobility μ_0 of 3.4 $\frac{cm^2}{Vs}$, a **constant contact resistance** of 400 Ω·cm, and a supply voltage $(V_{GS} - V_{th})$ of -5 V. When the contact length is reduced, the parasitic capacitances also decrease and the cut-off frequency increases. When the contact length approaches the limit $L_C \to 0$, the cut-off frequency reaches a limit.

In reality, however, the contact resistance is not constant, but it **depends on the contact length** (chapter 6.2.2). Therefore, the constant contact resistance R_C in equation 9.4 must be replaced by

$$R_C = 2 \cdot R_{sheet} \cdot L_T \cdot \coth\left(\frac{L_C}{L_T}\right). \tag{9.5}$$

The effect on the cut-off-frequency simulation of a TFT with a channel length L of 1 µm, an intrinsic mobility μ_0 of 3.4 $\frac{cm^2}{Vs}$, a supply voltage $(V_{GS} - V_{th})$ of -5 V, a sheet resistance of 560 $\frac{k\Omega}{\square}$, and a transfer length of 3.5 µm is shown in Figure 9.7a. For $L_C > L_T$ the contact resistance is constant and not affecting the effective mobility (see equation 6.2 on page 53), so that the cut-off frequency is identical to the previous situation for a constant contact resistance. However, when the contact length approaches the value of the transfer length, the contact resistance significantly increases. Thus, the effective mobility in the TFT decreases, so that the relation between the cut-off frequency and the contact length shows a maximum. When the contact length is further reduced, the cut-off frequency actually **decreases**. This demonstrates that there is an ideal contact length to achieve the highest possible cut-off frequency (for a specific semiconductor/metal interface).

The simulations assume a contact resistance that is given by the TLM theory (equation 9.5). However, in section 6.2 on page 53 several mechanisms have been discussed that can cause a smaller contact resistance in DNTT TFTs than expected. Therefore, the simulations in Figure 9.7a describe a lower limit of the cut-off frequency. For instance, the unipolar DNTT inverter and ring oscillator discussed in section 9 on page 95 exhibit a cut-off frequency > 1 MHz, which is slightly higher than simulated in Figure 9.7a.

With area-selective contact doping - simulation

The relation between the cut-off frequency and the contact length in Figure 9.7 is also discussed for a TFT with area-selective contact doping. The contact resistance and the transfer length of organic TFTs can be reduced by incorporating a thin doping layer between the source/drain contacts and the organic semiconductor (chapter 8), so that one expects an increase in cut-off frequency.

Figure 9.7a contains the cut-off-frequency simulation of a TFT with contact doping, that has a channel length L of 1 µm, an intrinsic mobility μ_0 of 3.4 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$, a supply voltage ($\mathrm{V_{GS}} - \mathrm{V_{th}}$) of -5 V, a sheet resistance of 560 $\frac{\mathrm{k}\Omega}{\square}$, and a transfer length of 2.5 µm. The overall relation between the cut-off frequency and the contact length is identical to the TFT without doping. However, by contact doping the same cut-off frequency (compared to the TFT without doping) may be realized with a larger contact length (that is a larger parasitic capacitance). In addition, the maximum achievable cut-off frequency may be also higher.

However, as shown in Figure 9.7b, the difference in transfer length between TFTs without doping and with contact doping is small for high drain-source voltage. Therefore, the beneficial effect of doping at high voltages cannot be easily confirmed with experiments. On the other hand, the difference in transfer length is large for small drain-source voltages, so one would expect a significant benefit of contact doping whenever the TFTs are operated with extremely low voltages. Unfortunately, the unipolar ring oscillators presented in this work require a relatively large supply voltage of more than 1 V which hinders the experimental verification of this hypothesis.

Remark on the simulation parameters

The sheet resistance and the transfer length for the TFT without doping and for the TFT with contact doping have been extracted for a drain-source voltage of -1.8 V (Figure 9.7b). This approach is reasonable, since the experiments in this work and the simulations by Sohn and co-workers [169] demonstrate a reduction of the contact resistance and the transfer length for higher drain-source voltage. A higher drain-source voltage corresponds to a higher supply voltage.

Conclusion

The ultra-thin gate dielectric introduced in section 4.1 and the high-resolution stencil lithography process allow the fabrication of low-voltage inverters and ring oscillators with excellent dynamic characteristics. For unipolar ring oscillators based on p-channel DNTT TFTs with a channel length of 1 µm and a contact length 5 µm a signal delay per stage of 230 ns was measured at a supply voltage of 4 V. Complementary ring oscillators that consist of p-channel DNTT and n-channel $F_{16}CuPc$ TFTs with a channel length of 1 µm and a contact length of 2 µm have a signal delay per stage of 18 µs for a supply voltage of 5 V. These are the smallest signal delays reported so far for unipolar and complementary organic ring oscillators operating with voltages below ∼5 V.

In addition, a theoretical relation between the cut-off frequency and the contact length has been proposed. The increase in frequency due to the reduction of the parasitic capacitances is competing with a decrease in effective mobility when the contact length is reduced. Thus, the cut-off frequency shows a maximum value for a certain contact length. The simulations propose that contact doping might be useful to reduce the limiting influence of the contact resistance.

10 Summary and outlook

Organic thin-film transistors (TFTs) with aggressively reduced lateral dimensions have been fabricated and analyzed. The p-channel transistors are based on the recently introduced semiconductor dinaphtho[2,3-b:2´3´-f]thieno[3,2-b]thiophene ($C_{22}H_{12}S_2$, DNTT) [26]. In general, (organic) TFTs can be processed in a variety of geometries, each of which has its advantages and disadvantages. Small-molecules (e.g. DNTT) often exhibit a three-dimensional growth, so that a smooth dielectric/semiconductor interface cannot be manufactured on top of the semiconductor film. Therefore, a bottom-gate structure was chosen, which has the advantage of a smooth dielectric/semiconductor interface that promotes a large charge-carrier mobility. The bottom-gate top-contact geometry (source/drain contacts on top of the semiconductor film) has the advantage of a smaller contact resistance compared to the bottom-gate bottom-contact structure (source/drain contacts below the organic semiconductor film) [23]. Thus, the top-contact geometry is useful for TFTs with reduced lateral dimensions, so that the relative influence of the contact resistance is minimized. However, it is challenging to reduce the lateral dimensions of top-contact organic TFTs. Standard lithography techniques are not useful to pattern metal contacts on top of small-molecule films, since these undergo a phase transition when exposed to heat [109] or organic solvents [22], so that the TFT characteristics would degrade.

Shadow-masking has the advantage that neither heat nor organic solvents are required for patterning metal contacts. In the past it has been possible to reduce the lateral dimensions of top-contact organic TFTs to ∼10 µm using polyimide shadow masks [12, 177]. The TFTs are made of a 30 nm thick aluminum bottom-gate electrode and a 5.7 nm thick hybrid gate dielectric, that consists of a plasma-grown aluminum oxide layer and a self-assembled monolayer (SAM) of an alkyl chain with a phosphonic acid anchor group. The manufacturing process is completed by vacuum-deposition of a 30 nm thick layer of an organic semiconductor and 25 nm thick gold top contacts [12]. Here, this process has been adapted using high-resolution silicon stencil masks [120, 119] (in cooperation with the Institut für Mikroelektronik, IMS CHIPS), so that the critical dimensions of the TFTs are reduced from 10 µm to 0.8 µm.

In order to also realize top-contact organic TFTs with a channel length below what is currently possible with silicon stencil masks (i.e. 100 nm), a process reported by Yagi and

co-workers has been adapted [92]. Using electron-beam lithography, a suspended resist bridge that acts as a high-resolution shadow mask for the source/drain contacts is manufactured. This process is limited to lateral dimensions ranging from 90 nm to 500 nm. In combination with the silicon stencil mask it is therefore possible to get a complete insight into the device physics of top-contact organic TFTs with lateral dimensions between 0.09 µm and 200 µm.

For the charge-carrier transport in organic transistors the alignment of the molecules on the gate dielectric is critically important. The growth of thin films of DNTT on a silicon/aluminum/aluminum oxide/SAM structure was investigated using an atomic force microscopy and X-ray diffraction (XRD). The measurements indicate a three-dimensional growth of DNTT with the long axis of the molecules perpendicular to the substrate surface. The obtained results are in good agreement with previous studies on DNTT single-crystals [34]. The molecular order is beneficial for an effective charge transport in organic transistors in the direction parallel to the gate dielectric.

The top-contact DNTT TFTs manufactured in this thesis have an intrinsic hole mobility of 3.4 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$. For transistors with large lateral dimensions the influence of the contact resistance can be neglected, since most of the drain-source voltage drops along the channel. The extracted effective mobility of 2.8 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$ for a transistor with a channel length of 60 µm is close to the intrinsic mobility. Using the transmission line method (TLM) a transfer length of 12 µm has been extracted. The transfer length is the minimum contact length that is necessary for an effective charge flow between the metal contacts and the organic semiconductor. The contact resistance strongly increases from 600 Ω·cm (for a contact length of 200 µm) to 9800 Ω·cm (for a contact length of 0.2 µm). DNTT TFTs with a reduced contact and channel length (∼0.1 µm) exhibit a much smaller effective mobility of 0.04 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$, since most of the drain-source voltage drops across the contacts and not along the channel. However, owing to the ultra-thin gate dielectric, short-channel effects are greatly suppressed. Transistors with a channel length of 90 nm have an on/off current ratio of 10^7, a steep subthreshold swing of 170 mV/decade, and a threshold voltage of -1.3 V, which are comparable to the long-channel transistors.

To reduce the significant influence of the contact resistance a common approach is doping of the contact area. By doping, the excess hole concentration in the organic semiconductor is increased, so that the energy barrier to the metal contacts is reduced. When a thin layer of the organic dopant (here: NDP-9, provided by Novaled AG) is deposited between the organic semiconductor and the contacts, the energy barrier between the gold contacts and the DNTT film is reduced. For a contact length of 200 µm the contact resistance is reduced by a factor of two and is 270 Ω·cm. The most beneficial effect is achieved for a contact length of 0.2 µm where the contact resistance decreases from 9800 Ω·cm to 2700 Ω·cm. The relative voltage drop along the channel is increased when the contribution

of the contact resistance to the total transistor resistance is made smaller. For instance, a DNTT TFT with a channel length of 2 µm and a contact length of 5 µm has a much higher effective mobility **with contact doping** ($0.4\ \frac{\mathrm{cm}^2}{\mathrm{Vs}}$) than **without doping** ($0.1\ \frac{\mathrm{cm}^2}{\mathrm{Vs}}$). The on/off current ratio, the subthreshold swing, and the threshold voltage are not affected by contact doping, in agreement with theoretical expectations.

Many organic semiconductors rapidly degrade when exposed to oxygen, ozone, or water vapor [3]. The DNTT molecule utilized in this work has a highest occupied molecular orbital energy level of -5.4 eV [26], so that the transport of holes in the material is greatly protected against oxidation. DNTT TFTs have been stored and measured in a clean room (40%-70% humidity) during a period of 200 days. The extracted effective mobility was essentially constant. Actually, for transistors with a small channel length (< 5 µm), a strong increase in the effective mobility within a few days was observed (followed by a constant value for the remaining period). Depending on the exact channel length this increase can be as strong as 300% (in the linear region of operation). The significant increase in the effective hole mobility in the linear region is accompanied by a transition from a nonlinear to an (ideal) linear drain-current increase in the output characteristics. Further experiments such as XRD and TLM indicate that this increase can be attributed to a reduction of the contact resistance from 600 Ω·cm to 90 Ω·cm (for a contact length of 200 µm). The sheet resistance (= intrinsic mobility in the TFTs without the influence of the contact resistance) and the crystal structure remain unaffected by this mechanism.

To study the dynamic performance of these TFTs, low-voltage organic ring oscillators employing as many as 22 transistors for one circuit have been fabricated. Unipolar ring oscillators based on p-channel DNTT TFTs with a channel length of 1 µm and a contact length of 5 µm have a signal delay per stage of 230 ns at a supply voltage of ∼4 V. Complementary ring oscillators consisting of p-channel DNTT TFTs and n-channel F_{16}CuPc TFTs that are integrated on one substrate have been also manufactured. The integrated TFTs have a channel length of 1 µm and a contact length of 2 µm. A signal delay per stage of 18 µs for a supply voltage of 5 V has been measured. These are the smallest signal delays reported so far for unipolar and complementary organic ring oscillators operating with voltages below 10 V.

The combination of the high-resolution stencil lithography process with the ultra-thin gate dielectric [12] provides excellent uniformity of the TFT parameters. The on-state drain current, the off-state drain current, the subthreshold swing, the threshold voltage, and the gate current of transistors with the same lateral dimensions vary by only a few percent. For example, the average transconductance of 16 TFTs with a channel length of 1 µm is $(0.47 \pm 0.02)\ \frac{\mathrm{S}}{\mathrm{m}}$ and the average threshold voltage of 62 transistors is (0.95 ± 0.03) V.

Owing to the excellent process uniformity and excellent dynamic performance it is possible to consider more sophisticated integrated circuits. For instance, in cooperation with

the Institut für Mikroelektronik the integration of as many as 129 p-channel TFTs on one substrate to manufacture a 6-bit binary-weighted current-steering digital-to-analog converter was realized [212]. But the demonstrated operation frequency of a few megahertz for an individual transistor also allows us to consider the realization of an amplitude modulated (AM) radio, which requires at least one transistor working beyond one megahertz.

However, this work also depicts that the dynamic performance is often significantly limited by the contact length of the TFTs, and a theoretical relation between the cut-off frequency and the contact length has been proposed. The increase in frequency due to the reduction of the parasitic capacitances is competing with a decrease in effective mobility when the contact length is smaller than the transfer length (the characteristic length over which most of the drain current is transfered between the contacts and the semiconductor). Thus, the cut-off frequency shows a maximum value for a certain contact length and aggressive scaling of the contact length may not necessarily increase the transistor performance. For high-frequency ($\sim$MHz) applications it will be necessary to develop methods that reduce the characteristic transfer length (in organic TFTs) and allow a higher operation frequency for TFTs with aggressively reduced lateral dimensions. In this thesis it was demonstrated that the transfer length is reduced by a factor of 2-3 when a strong electron acceptor is employed underneath the source/drain contacts. The simulations indicate an improvement in the dynamic performance by a factor of two when the contacts are doped. Thus, the research on even stronger organic dopants should be intensified, so that the contact resistance limitations in organic TFTs with reduced dimensions can be further alleviated.

The simulations by Sohn and co-workers, but also the results in chapter 9, indicated a dependence of the transfer length on the drain-source voltage. This relation may be further investigated by scanning photocurrent microscopy (SPCM), which is a powerful method to anaylze the contact barriers at metal/semiconductor interfaces [174, 175, 213, 214]. It may be possible with this technique to extract the extension of the active contact region in a top-contact organic TFT. Thus, the relation between the drain-source voltage and the transfer length, but also the microscopic contact properties may be analyzed in more detail.

Preliminary experiments on DNTT TFTs with asymmetric contact lengths for the source and the drain contact indicated a larger transfer length at the source side than at the drain side. Systematic experiments on TFTs with different asymmetric contact lengths are required (ideally in combination with SPCM characterization) to gain a deeper understanding of this observation. An asymmetric contact length would be essential in terms of applications. On the one hand the contact length at the source contact should be larger to minimize the contact resistance. On the other hand, the contact length at the drain

contact should be smaller to minimize the parasitic capacitances.

Recent simulations obtained a non-zero density of charge carriers underneath the contacts, even if the contact length of a top-contact TFT is reduced to 0 µm, in other words, even if there is no overlap between the gate electrode and the source/drain contacts [79]. These simulations also indicate that the contact resistance in a staggered geometry (top-contacts) should be still smaller compared to the coplanar geometry (bottom-contacts), even without any overlap between the source/drain contacts and the gate electrode. To verify this proposed important advantage of the staggered over the coplanar organic TFTs, further experiments focusing on zero-overlap are planned.

But not only a deeper understanding of the influence of the transistor geometry on the electrical performance is necessary. Also further improvements in the functional electronic materials are desirable. Especially the intrinsic mobility in air-stable n-channel TFTs is almost one order of magnitude lower than that in air-stable p-channel TFTs. Thus, air-stable organic complementary circuits are usually limited by the low performance of the n-channel TFTs. There is already a focus placed on the development of organic semiconductors with a high electron mobility and excellent air stability [206, 207, 208]. In addition, the development of strong n-type dopants might be useful to reduce a possible limiting influence of the transfer length in n-channel organic TFTs.

From a technological aspect it is interesting to investigate the limitations in the presented stencil-lithography process. In this thesis, the silicon stencil masks have a thickness of 20 µm. In these masks, silicon bars with a width of less than 800 nm (to pattern source/drain contacts with a spacing of less than 800 nm) easily break by strain during the mask fabrication or by distortions when aligning the stencil masks on the substrates. However, there are reports in the literature on the fabrication of metallic nanowires with a diameter down to 70 nm using silicon membranes with a thickness of 100 nm [128]. In the future different mask features will be considered to achieve a reproducible source/drain spacing of less than 800 nm. This task requires different mask geometries (e.g. different mask thickness), but probably also improvements in the material deposition techniques to further reduce the geometrical broadening of the patterned structures.

In the past organic transistors have been mainly considered for low-performance applications such as e-ink displays or large-area sensor arrays, in which the individual transistors have relatively large lateral dimensions (>10 µm) and operate with frequencies of approximately 1 kHz. Here, it was demonstrated that the critical lateral dimensions of organic transistors can be reduced to ∼1 µm using a solvent-free, room-temperature manufacturing process based on silicon stencil masks. The demonstrated individual transistors operate at frequencies of more than 1 MHz. In the future it may be possible to develop a full wafer-scale stencil-mask process to manufacture organic transistors with small lateral dimensions on large areas. Using such a manufacturing technique organic transistors may

be considered not only for low-performance applications, but also for high-performance products such as high-definition active-matrix organic light-emitting diode displays (AM-OLED displays) in which the individual transistors operate with frequencies of about 1 MHz.

A Silicon stencil mask fabrication

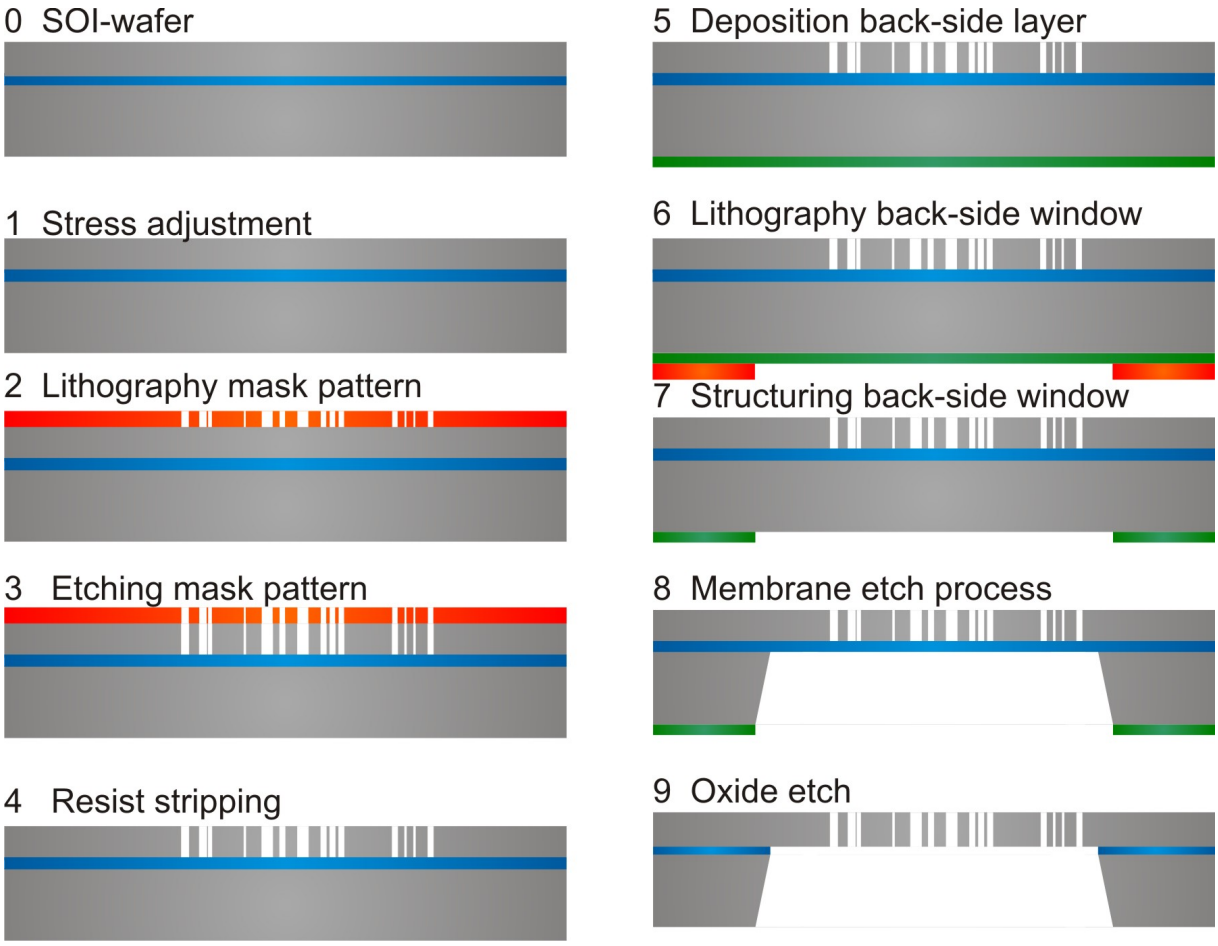

Figure A.1: Silicon stencil mask process flow. The silicon stencil masks were fabricated on silicon-on-insulator (SOI) wafers, with the buried SiO_2 serving as an etch stop during the formation and patterning of a 20 µm thick silicon membrane [120, 119]. Apertures in the silicon membrane were opened by electron-beam lithography and dry etching from the wafer front side. Over an area of 20×20 mm^2 the bulk silicon was then removed by etching from the wafer back side (using a SiO_xN_y masking layer), leaving the patterned silicon membrane anchored to a robust 5 mm wide wafer frame.

B Structure variations in stencil lithography

A major concern in stencil lithography are variations between the defined patterns in the stencil mask and the processed patterns on the substrate. These discrepancies mainly depend on a gap between the mask and the substrate, but also on the material composition, the film thickness, the temperature, and the deposition rate, so that the patterned structures are usually broadened [123, 128]. The structure broadening is separated in a **geometrical** and a **halo** broadening [123]. Note, that a broadening of the source and drain contacts narrows the transistor channel length, so that is useful to discuss the effect on the patterned transistor channel in total, and not the influence on an individual contact.

The *geometrical channel narrowing* (= broadening of the source/drain contacts) is mainly due to the gap G between the stencil mask and the substrate. This gap causes deposition of material underneath the stencil mask during the evaporation (Figure B.1a). The geometrical channel narrowing N can be estimated by [123]

$$N = \frac{G \cdot S}{D}, \tag{B.1}$$

where S is the evaporation source size (1 cm) and D the distance from this evaporation source to the substrate (50 cm). For this estimation, S << D, N << G and A << S (A is the width of the pattern in the stencil mask) is assumed. Vazquez-Mena and coworkers estimated an intrinsic gap of 5 µm between their 100 nm thick stencil membrane and the substrate [123]. Considering also a gap of 5 µm between the silicon stencil mask and the substrate, a source size of 1 cm, a distance between the evaporation source and the substrate of 50 cm, and using equation B.1, one yields a channel narrowing of approximately 100 nm. However, different SEM images revealed a geometrical channel narrowing of less than 100 nm corresponding to a gap G of less than 5 µm.

Stencil membranes with a thickness of a few hundred nanometers can deform on the surface, so that the gap between mask and substrate increases [215]. Here, the rigid silicon stencil mask with a thickness of 20 µm (fixed with clamps on the 5 mm wide mask frame) might prohibit a bending on the substrate, so that the intrinsic gap between the

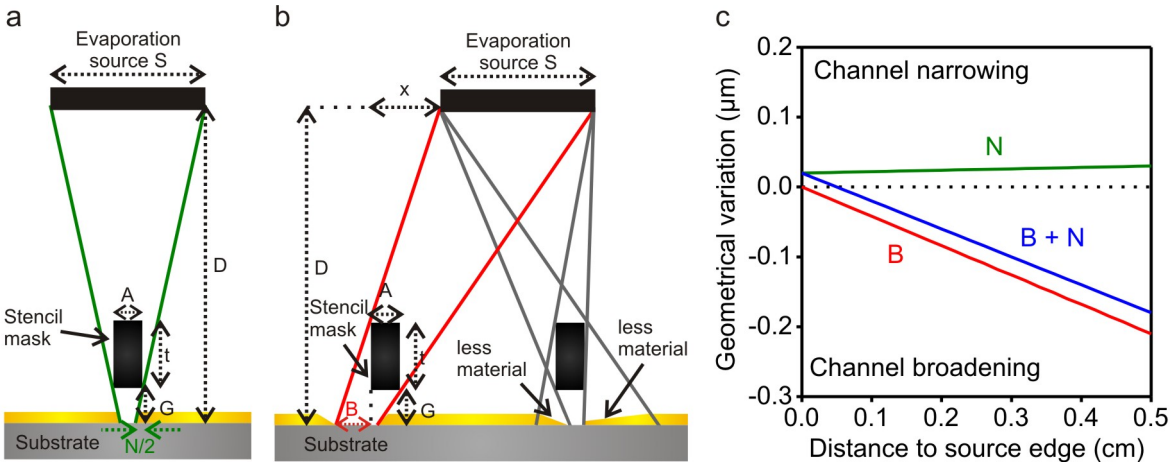

Figure B.1: Geometrical narrowing and broadening of structures in stencil lithography. a) The schematic illustrates the channel narrowing produced by a finite gap between the mask and the substrate. b) The schematic illustrates the channel broadening if the mask pattern is displaced by a certain distance next to the evaporation source and the unequal source/drain contacts if the mask pattern is not centered below the evaporation source. c) The graph illustrates the channel narrowing N and the channel broadening B as function of the distance next to the evaporation source edge. The superposed effect (B+N) of the two independent mechanisms is also illustrated.

mask and the substrate is not further increased.

However, the finite thickness t of the stencil mask also causes two disadvantages that are indicated in Figure B.1b, namely a *geometrical channel broadening* B (transistor channel length increases) and an *asymmetric slope of the contact edges*. The geometrical channel broadening only appears for structures displaced by a length x from the evaporation source edge (Figure B.1b, red lines) and is described (for B $<<$ x) by

$$B = \frac{x \cdot (t + G)}{D}. \tag{B.2}$$

Here, the stencil mask size is 2 x 2 cm^2, so that the structures can be displaced not more than 0.5 cm from the evaporation source edge (S = 1 cm, when the mask is centered above the evaporation source). Figure B.1 shows the geometrical channel narrowing N, the channel broadening B, and the superposed effect of the two independent mechanisms as a function of the distance to the evaporation source edge (for a gap of 1 µm). To keep the channel length error small, the structures must be displaced by not more than 0.2 cm from the evaporation source edge.

The finite thickness t of the stencil mask also causes an asymmetric contact slope. For structures not exactly centered below the evaporation source, the source and drain contacts receive different amounts of material during the deposition (B.1b, black lines). This asymmetric contact slopes are also shown in the atomic force microscopy image in Fig-

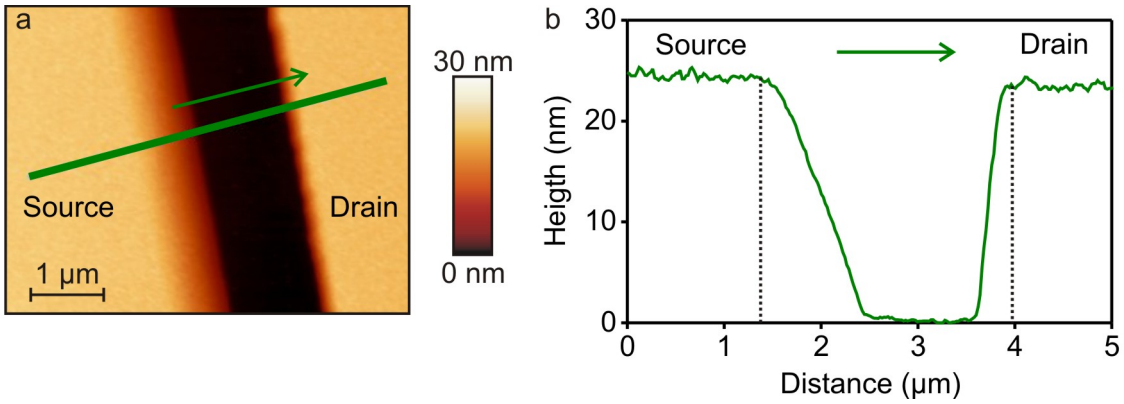

Figure B.2: Asymmetric source/drain contact edges. The Atomic force microscope image and the corresponding height profile illustrate the asymmetry in the 25 nm thick source/drain contact edges.

ure B.2.

The halo broadening (due to a diffusion of material on the surface) depends on the film thickness, deposition rate and temperature [123]. It can be as small as 400 nm for 45 nm of aluminum evaporated at 1 Å/s and for a relatively large gap between the mask and the substrate of 7.5 µm (and the halo broadening is expected to be smaller for a reduced film thickness, deposition rate, and gap between the mask and the substrate) [123]. In this work, the critical structures (source/drain contacts) have a thickness of only 25 nm and these have been deposited at a rate of 0.3 Å/s to redcue the halo broadening. To investigate the halo broadening in more detail, further experiments are required.

C Transmission line method

Contact and sheet resistance

The first reports on the transmission line method (TLM) by Murrmann and Widmann date back to 1969 [156] and further improvements followed by Berger [157, 158] in 1972. Here, a more recent approach reported by Schroder [81] will be considered to derive the most important equations of this theory. The total transistor resistance R_{TFT} is given by the sum of the contact resistance R_C and channel resistance R_{ch}.

$$\frac{V_{DS}}{I_D} = R_{TFT} = R_C + R_{ch}. \tag{C.1}$$

For simplification the contact resistance will be considered as ohmic for now, even though this assumption is not reflecting the true nature of the metal contact/organic semiconductor interface. The contact and channel resistances are inversely proportional to the channel width W, so that the following normalization is useful:

$$R_{TFT} \cdot W = R_C \cdot W + R_{ch} \cdot W. \tag{C.2}$$

Considering the relation between the channel resistance and the sheet resistance R_{sheet},

$$R_{sheet} = \frac{R_{ch} \cdot W}{L}, \tag{C.3}$$

one can rewrite equation C.2 as follows:

$$R_{TFT} \cdot W = R_C \cdot W + R_{sheet} \cdot L. \tag{C.4}$$

Therefore, by plotting the width-normalized resistance of the transistors as a function of the channel length (Figure 6.2a), one can extract the width-normalized contact resistance (in the following called "contact resistance") at the intersection with the y-axis $R_C \cdot W = R_{TFT} \cdot W(L = 0)$ and the sheet resistance from the slope of this relation:

$$R_{sheet} = \frac{\Delta\left(R_{TFT} \cdot W\right)}{\Delta L}. \tag{C.5}$$

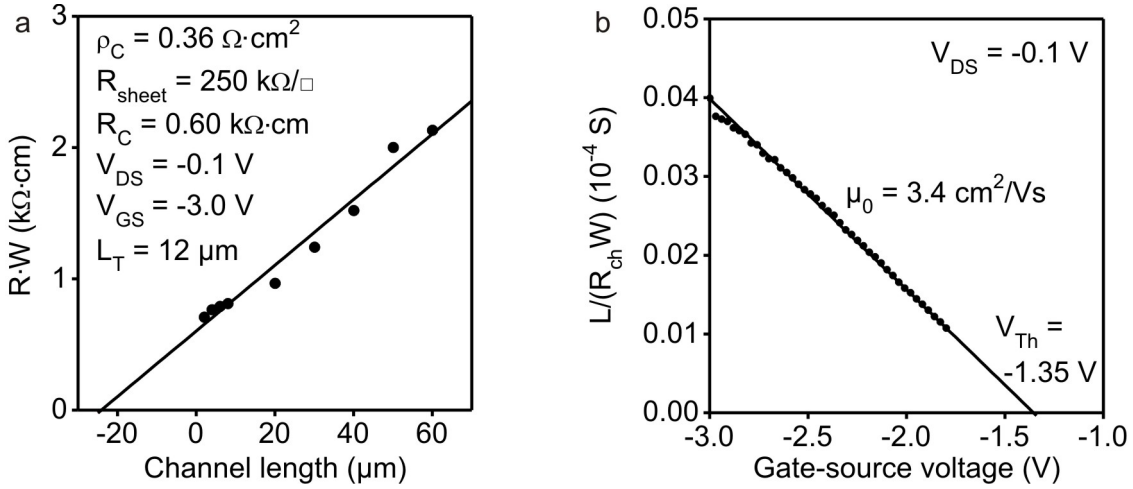

Figure C.1: Analysis of the transistor resistance and the intrinsic transistor properties. a) Width-normalized total transistor resistance as a function of the transistor channel length. From the linear least square fit a contact resistance of 600 Ω·cm, a sheet resistance of 250 $\frac{k\Omega}{\square}$, and a transfer length of 12 µm was extracted. b) Inverse sheet resistance as a function of the gate-source voltage. From the linear least square fit an intrinsic mobility of 3.4 $\frac{cm^2}{Vs}$ and an intrinsic threshold voltage of -1.35 V is extracted.

To account for the linear relation between the contact and channel resistance all values should be extracted at low drain-source voltages.

Transfer length

With the TLM method the transfer length, a characteristic length over which 63% of the charge flow between the contacts and the semiconductor transfers, can be extracted [81, 150]. The contact resistance below the source/drain contacts is considered as a resistor network, so that the potential distribution below the contact is not uniform, but given by the relation [81, 154, 157]:

$$\frac{d^2V(x)}{dx^2} = \frac{1}{L_T^2}V(x), \tag{C.6}$$

with the characteristic transfer length for a specific contact/semiconductor material combination

$$L_T = \sqrt{\frac{\rho_C}{R_{sheet}}} \tag{C.7}$$

and the the contact resistivity ρ_C. The current flow is assumed vertical between the contacts and the semiconductor. Considering the maximum current flowing at the front contact edge (x = 0) and no current flowing at the end contact edge (x = L_C) as boundary conditions, equation C.6 can be solved analytically [81, 154, 157] to yield the potential

distribution V(x). The contact resistance, which is also called front contact resistance, is given by

$$R_C = \frac{V}{I} = 2 \cdot R_{sheet} \cdot L_T \cdot \coth\left(\frac{L_C}{L_T}\right), \tag{C.8}$$

whereat a factor of two was introduced to account for the condition $R_S = R_D = \frac{R_C}{2}$. Equation C.8 is only valid for staggered transistor geometries (section 3) which have an extended area (overlap area between the contacts and the gate electrode) available for the charge flow between the contacts and the semiconductor. Equation C.8 describes the important relation between the transfer length and the contact resistance in a general way. If the contact length L_C is much larger than the transfer length L_T ($L_C \gg L_T$), equation C.8 simplifies to:

$$R_C \approx 2 \cdot \frac{\rho_C}{L_T \cdot W} \tag{C.9}$$

and the contact resistance is independent on the contact length. In this situation the contact is only partially active (area: $L_T \cdot W$), but the charge flow between the semiconductor and the contact is effective. On the other side, when the contact length is much smaller than the transfer length ($L_C \ll L_T$), the contact is too small (area: $L_C \cdot W$) and the charge flow is not effective. In this limit equation C.8 reads

$$R_C \approx 2 \cdot \frac{\rho_C}{L_C \cdot W} \tag{C.10}$$

and the contact resistance is inversely proportional to the contact length and increasing when the contact length is reduced. Inserting equation C.7 and C.9 in C.4 yields

$$R_{TFT} \cdot W = R_{sheet} \cdot (L + 2 \cdot L_T), \tag{C.11}$$

and the transfer length is extracted at the intersection with the x-axis (Figure 6.2a):

$$L_T = -\frac{L(R_{TFT} \cdot W = 0)}{2}. \tag{C.12}$$

Intrinsic material parameters

To extract the intrinsic mobility μ_0 and intrinsic threshold voltage V_{th} for the DNTT TFTs without the influence of the contact resistance, one starts with equation 3.31:

$$I_D = \frac{\mu_0 W C_i}{L} \cdot (V_{GS} - V_{th}) \cdot (V_{DS} - I_D R_C). \tag{C.13}$$

This equation can be solved for I_D and divided by V_{DS} to yield the total transistor resistance as sum of the contact resistance and the channel resistance.

$$R_{TFT} = R_C + \frac{L}{\mu_0 W C_i \cdot (V_{GS} - V_{th})} = R_C + R_{ch}. \tag{C.14}$$

In equation C.14 the contributions of the contact resistance and the channel resistance are separated. The later addend reads as sheet resistance multiplied by the channel length and divided by the channel width (equation C.5), $R_{ch} = \frac{R_{sheet} \cdot L}{W}$, so that one can rewrite the second summand of equation C.14:

$$\frac{1}{R_{sheet}} = \frac{L}{R_{ch} \cdot W} = \mu_0 C_i \cdot (V_{GS} - V_{th}) \,. \tag{C.15}$$

From the slope of this relation the intrinsic mobility μ_0 and from the intersection with the x-axis the intrinsic threshold voltage V_{th} is derived (Figure 6.2b).

D Supporting DNTT TFTs

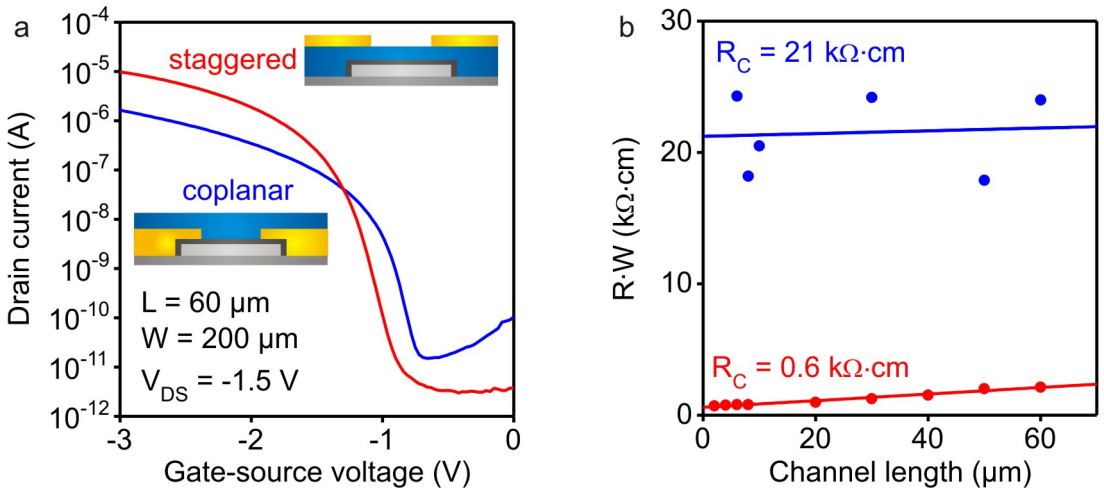

Figure D.1: Comparison of coplanar and staggered transistor structure. a) Transfer characteristics of DNTT TFTs in the coplanar (or bottom-contact) and inverted staggered (or top-contact) transistor structure, both with a channel length of 60 µm and a channel width of 200 µm. The staggered transistor has a contact length of 200 µm. The mobility extracted in the saturation region is 0.4 $\frac{\text{cm}^2}{\text{Vs}}$ for the coplanar and 2.4 $\frac{\text{cm}^2}{\text{Vs}}$ for the staggered transistor. b) Transmission line method to extract the contact resistance for a set of transistors in the coplanar and in the staggered geometry. The contact resistance is 21 k$\Omega \cdot$ cm for the former and 0.6 k$\Omega \cdot$ cm for the latter geometry.
The significant difference in effective mobility and contact resistance demonstrates the superior properties of staggered structures compared to coplanar structures.

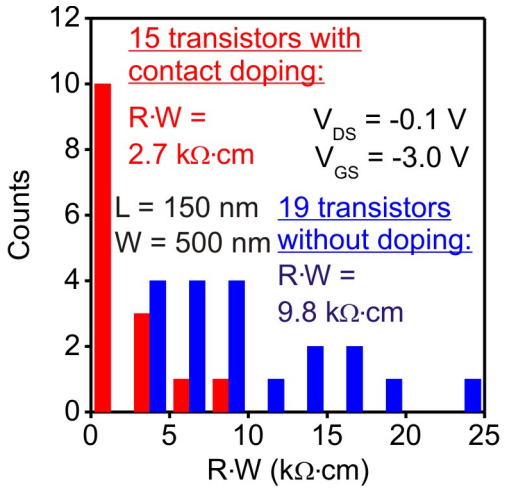

Figure D.2: Width-normalized resistance of submicron DNTT TFTs without doping and with contact doping. b) Width-normalized resistance of 19 DNTT TFTs without doping and 15 DNTT TFTs with contact doping, all having a channel length of 150 nm, calculated at a fixed drain-source voltage of -0.1 V. The average resistance of the transistors without doping is 9.8 kΩ·cm and with contact doping is 2.7 kΩ·cm. The contact resistance is assumed to be only slightly smaller.

E Mass spectrum of DNTT

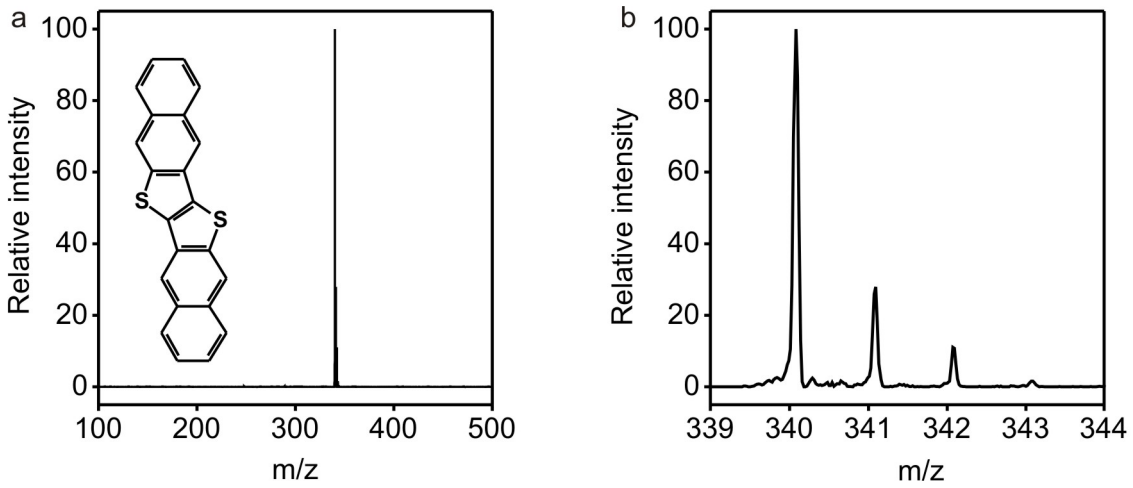

Figure E.1: Mass spectrum of DNTT. The film was grown on a aluminum/aluminum oxide/SAM structure as utilized for the organic transistors fabricated in this work. a) The image shows the mass spectrum taken from a 30 nm thick film of DNTT using a time-of-flight laser desorption/ionization mass spectrometry. The measured mass is 340.08 u and corresponds well to the theoretical calculated mass is of 340.04 u. b) The image illustrates the measured isotope distribution.

Bibliography

[1] R.W. Price, *Roadmap to entrepreneurial success: Powerful strategies for building a high-profit business*, AMACOM/American Management Association, 2004.

[2] C. McNairy and R. Bhatia, "Montecito: A dual-core, dual-thread Itanium processor", *Micro, IEEE*, vol. 25, no. 2, pp. 10–20, 2005.

[3] H. Klauk, "Organic thin-film transistors", *Chemical Society Reviews*, vol. 39, no. 7, pp. 2643–2666, 2010.

[4] R. Hilsch and R.W. Pohl, "Steuerung von Elektronenstroemen mit einem Dreielektrodenkristall und ein Modell einer Sperrschicht", *Zeitschrift fuer Physik A Hadrons and Nuclei*, vol. 111, no. 5, pp. 399–408, 1938.

[5] M. Marinkovic, E. Hashem, K.Y. Chan, A. Gordijn, H. Stiebig, and D. Knipp, "Microcrystalline silicon thin-film transistors operating at very high frequencies", *Applied Physics Letters*, vol. 97, pp. 073502, 2010.

[6] B. Hekmatshoar, S. Wagner, and J.C. Sturm, "Tradeoff regimes of lifetime in amorphous silicon thin-film transistors and a universal lifetime comparison framework", *Applied Physics Letters*, vol. 95, no. 14, pp. 143504, 2009.

[7] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors", *Nature*, vol. 432, no. 7016, pp. 488–492, 2004.

[8] A.D. Franklin, A.A. Bol, and Z. Chen, "Channel and contact length scaling in carbon nanotube transistors", in *Device Research Conference (DRC), 2010*. IEEE, 2010, pp. 275–276.

[9] J.T. Smith, Y. Zhao, C. Yang, and J. Appenzeller, "Effects of nanoscale contacts to silicon nanowires on contact resistance: Characterization and Modeling", in *Device Research Conference (DRC), 2010*. IEEE, 2010, pp. 139–140.

[10] T. Someya, T. Sekitani, S. Iba, Y. Kato, H. Kawaguchi, and T. Sakurai, "A large-area, flexible pressure sensor matrix with organic field-effect transistors for artificial skin applications", *Proceedings of the National Academy of Sciences of the United States of America*, vol. 101, no. 27, pp. 9966, 2004.

[11] H. Sirringhaus, T. Kawase, R.H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, and EP Woo, "High-resolution inkjet printing of all-polymer transistor circuits", *Science*, vol. 290, no. 5499, pp. 2123, 2000.

[12] H. Klauk, U. Zschieschang, J. Pflaum, and M. Halik, "Ultralow-power organic complementary circuits", *Nature*, vol. 445, no. 7129, pp. 745–748, 2007.

[13] H. Sirringhaus, "Device physics of solution-processed organic field-effect transistors", *Advanced Materials*, vol. 17, no. 20, pp. 2411–2425, 2005.

[14] Y.Y. Noh, N. Zhao, M. Caironi, and H. Sirringhaus, "Downscaling of self-aligned, all-printed polymer thin-film transistors", *Nature Nanotechnology*, vol. 2, no. 12, pp. 784–789, 2007.

[15] T. Sekitani, H. Nakajima, H. Maeda, T. Fukushima, T. Aida, K. Hata, and T. Someya, "Stretchable active-matrix organic light-emitting diode display using printable elastic conductors", *Nature Materials*, vol. 8, no. 6, pp. 494–499, 2009.

[16] T. Sekitani, T. Yokota, U. Zschieschang, H. Klauk, S. Bauer, K. Takeuchi, M. Takamiya, T. Sakurai, and T. Someya, "Organic Nonvolatile Memory Transistors for Flexible Sensor Arrays", *Science*, vol. 326, no. 5959, pp. 1516, 2009.

[17] A. Pochettino, "Sul comportamento foto-elettrico dell antracene", *Acad. Lincei Rend*, vol. 15, pp. 355, 1906.

[18] C.K. Chiang, C.R. Fincher Jr, Y.W. Park, A.J. Heeger, H. Shirakawa, E.J. Louis, S.C. Gau, and A.G. MacDiarmid, "Electrical conductivity in doped polyacetylene", *Physical Review Letters*, vol. 39, no. 17, pp. 1098–1101, 1977.

[19] H. Koezuka, A. Tsumura, and T. Ando, "Field-effect transistor with polythiophene thin film", *Synthetic Metals*, vol. 18, no. 1-3, pp. 699–704, 1987.

[20] M. Noda, N. Kobayashi, M. Katsuhara, A. Yumoto, S. Ushikura, R. Yasuda, N. Hirai, G. Yukawa, I. Yagi, K. Nomoto, et al., "47.3: A Rollable AM-OLED Display Driven by OTFTs", SID, 2010.

[21] K. Myny, S. Steudel, S. Smout, P. Vicca, F. Furthner, B. van der Putten, AK Tripathi, GH Gelinck, J. Genoe, W. Dehaene, et al., "Organic Electronics", *Organic Electronics*, vol. 11, pp. 1176–1179, 2010.

[22] D.J. Gundlach, T.N. Jackson, D.G. Schlom, and S.F. Nelson, "Solvent-induced phase transition in thermally evaporated pentacene films", *Applied Physics Letters*, vol. 74, pp. 3302, 1999.

[23] D.J. Gundlach, L. Zhou, J.A. Nichols, T.N. Jackson, P.V. Necliudov, and M.S. Shur, "An experimental study of contact effects in organic thin film transistors", *Journal of Applied Physics*, vol. 100, pp. 024509, 2006.

[24] S.D. Wang, Y. Yan, and K. Tsukagoshi, "Understanding contact behavior in organic thin film transistors", *Applied Physics Letters*, vol. 97, pp. 063307, 2010.

[25] K. Tsukagoshi, F. Fujimori, T. Minari, T. Miyadera, T. Hamano, and Y. Aoyagi, "Suppression of short channel effect in organic thin film transistors", *Applied Physics Letters*, vol. 91, pp. 113508, 2007.

[26] T. Yamamoto and K. Takimiya, "Facile Synthesis of Highly π-Extended Heteroarenes, Dinaphtho chalcogenophenes, and Their Application to Field-Effect Transistors", *Journal of the American Chemical Society*, vol. 129, no. 8, pp. 2224–2225, 2007.

[27] T. Yamamoto and K. Takimiya, "FET Characteristics of Dinaphthothienothiophene (DNTT) on Si/SiO 2 Substrates with Various Surface-Modifications", *Journal of Photopolymer Science and Technology*, vol. 20, no. 1, pp. 57–59, 2007.

[28] M. Schwoerer and H.C. Wolf, *Organic molecular solids*, Vch Verlagsgesellschaft Mbh, 2007.

[29] M. Pfeiffer, A. Beyer, T. Fritz, and K. Leo, "Controlled doping of phthalocyanine layers by cosublimation with acceptor molecules: A systematic Seebeck and conductivity study", *Applied Physics Letters*, vol. 73, pp. 3202, 1998.

[30] M. Pfeiffer, K. Leo, X. Zhou, J.S. Huang, M. Hofmann, A. Werner, and J. Blochwitz-Nimoth,

"Doped organic semiconductors: Physics and application in light emitting diodes", *Organic Electronics*, vol. 4, no. 2-3, pp. 89–103, 2003.

[31] J. Blochwitz, T. Fritz, M. Pfeiffer, K. Leo, D.M. Alloway, P.A. Lee, and N.R. Armstrong, "Interface electronic structure of organic semiconductors with controlled doping levels", *Organic Electronics*, vol. 2, no. 2, pp. 97–104, 2001.

[32] N. Von Malm, J. Steiger, R. Schmechel, and H. von Seggern, "Trap engineering in organic hole transport materials", *Journal of Applied Physics*, vol. 89, pp. 5559, 2001.

[33] C.D. Dimitrakopoulos and D.J. Mascaro, "Organic thin-film transistors: A review of recent advances", *IBM Journal of research and development*, vol. 45, no. 1, pp. 11–27, 2001.

[34] J. Nishida, S. Ando, J. Yamaguchi, K. Itaka, H. Koinuma, H. Tada, S. Tokito, and Y. Yamashita, "High-Performance Organic Field-Effect Transistors Based on π-Extended Tetrathiafulvalene Derivatives", *Journal of the American Chemical Society*, vol. 127, no. 29, pp. 10142–10143, 2005.

[35] R.S. Sanchez-Carrera, S. Atahan, J. Schrier, and A. Aspuru-Guzik, "Theoretical Characterization of the Air-Stable, High-Mobility Dinaphtho[2,3-b:2'3'-f]thieno[3,2-b]-thiophene Organic Semiconductor", *The Journal of Physical Chemistry C*, vol. 114, no. 5, pp. 2334–2340, 2010.

[36] H. Haken and H.C. Wolf, "Molekuelphysik und Quantenchemie", 2006.

[37] P.Y. Bruice, "Organic Chemistry, fiftth ed", *Person Prentice Hall, New Jersey*, pp. 1041–1045, 2007.

[38] A. Troisi and G. Orlandi, "Band structure of the four pentacene polymorphs and effect on the hole mobility at low temperature", *The Journal of Physical Chemistry B*, vol. 109, no. 5, pp. 1849–1856, 2005.

[39] H. Klauk, D.J. Gundlach, J.A. Nichols, and T.N. Jackson, "Pentacene organic thin-film transistors for circuit and display applications", *IEEE Transactions on Electron Devices*, vol. 46, no. 6, pp. 1258–1263, 1999.

[40] G. Horowitz, "Organic thin film transistors: From theory to real devices", *Journal of Materials Research*, vol. 19, no. 7, pp. 1946–1962, 2004.

[41] C.D. Dimitrakopoulos and P.R.L. Malenfant, "Organic thin film transistors for large area electronics", *Advanced Materials*, vol. 14, no. 2, pp. 99–117, 2002.

[42] H. Klauk, "Personal communication".

[43] NF Mott, "Electrons in disordered solids, I', *Advan. in Phys*, vol. 16, pp. 49–144, 1967.

[44] M. Vissenberg and M. Matters, "Theory of the field-effect mobility in amorphous organic transistors", *Physical Review B*, vol. 57, no. 20, pp. 12964–12967, 1998.

[45] P.G. Le Comber and W.E. Spear, "Electronic transport in amorphous silicon films", *Physical Review Letters*, vol. 25, no. 8, pp. 509–511, 1970.

[46] G. Horowitz, R. Hajlaoui, and P. Delannoy, "Temperature dependence of the field-effect mobility of sexithiophene. Determination of the density of traps", *Journal de Physique III*, vol. 5, no. 4, pp. 355–371, 1995.

[47] Z. Bao, A. Dodabalapur, and A.J. Lovinger, "Soluble and processable regioregular poly (3-hexylthiophene) for thin film field-effect transistor applications with high mobility", *Applied Physics*

Letters, vol. 69, pp. 4108, 1996.

[48] M. Mas-Torrent, M. Durkut, P. Hadley, X. Ribas, and C. Rovira, "Correlation between Crystal Structure and Mobility in Organic Field-Effect Transistors Based on Single Crystals of Tetrathiafulvalene Derivatives", *J. Am. Chem. Soc.*, vol. 126, pp. 8546–8553, 2004.

[49] C.K. Chan, L.J. Richter, B. Dinardo, C. Jaye, B.R. Conrad, H.W. Ro, D.S. Germack, D.A. Fischer, D.M. DeLongchamp, and D.J. Gundlach, "High performance airbrushed organic thin film transistors", *Applied Physics Letters*, vol. 96, pp. 133304, 2010.

[50] H.E. Katz, "Recent advances in semiconductor performance and printing processes for organic transistor-based electronics", *Chemistry of Materials*, vol. 16, no. 23, pp. 4748–4756, 2004.

[51] M. Mas-Torrent, M. Durkut, P. Hadley, X. Ribas, and C. Rovira, "High mobility of dithiophene-tetrathiafulvalene single-crystal organic field effect transistors", *Journal of the American Chemical Society*, vol. 126, no. 4, pp. 984–985, 2004.

[52] V.C. Sundar, J. Zaumseil, V. Podzorov, E. Menard, R.L. Willett, T. Someya, M.E. Gershenson, and J.A. Rogers, "Elastomeric transistor stamps: Reversible probing of charge transport in organic crystals", *Science*, vol. 303, no. 5664, pp. 1644, 2004.

[53] J. Takeya, M. Yamagishi, Y. Tominari, R. Hirahara, Y. Nakazawa, T. Nishikawa, T. Kawase, T. Shimoda, and S. Ogawa, "Very high-mobility organic single-crystal transistors with in-crystal conduction channels", *Applied Physics Letters*, vol. 90, no. 10, pp. 2120, 2007.

[54] M. Uno, Y. Tominari, M. Yamagishi, I. Doi, E. Miyazaki, K. Takimiya, and J. Takeya, "Moderately anisotropic field-effect mobility in dinaphtho thiophenes single-crystal transistors", *Applied Physics Letters*, vol. 94, pp. 223308, 2009.

[55] O.D. Jurchescu, J. Baas, and T.T.M. Palstra, "Effect of impurities on the mobility of single crystal pentacene", *Applied Physics Letters*, vol. 84, pp. 3061, 2004.

[56] T. Yasuda, K. Fujita, H. Nakashima, and T. Tsutsui, "Organic field-effect transistors with gate dielectric films of poly-p-xylylene derivatives prepared by chemical vapor deposition", *Japanese Journal of Applied Physics*, vol. 1, no. 42, pp. 6614, 2003.

[57] U. Zschieschang, F. Ante, M. Schlorholz, K. Kern, and H. Klauk, "Deterministic and continuous control of the threshold voltage and noise margin of organic thin-film transistors and organic complementary circuits using mixed phosphonic acid self-assembled monolayer gate dielectrics", in *Device Research Conference, 2009. DRC 2009*. IEEE, 2009, pp. 181–182.

[58] U. Zschieschang, K. Amsharov, R.T. Weitz, M. Jansen, and H. Klauk, "Low-voltage organic n-channel thin-film transistors based on a core-cyanated perylene tetracarboxylic diimide derivative", *Synthetic Metals*, vol. 159, no. 21-22, pp. 2362–2364, 2009.

[59] D.J. Gundlach, L.L. Jia, and T.N. Jackson, "Pentacene TFT with improved linear region characteristics using chemically modified source and drain electrodes", *IEEE Electron Device Letters*, vol. 22, no. 12, pp. 571, 2001.

[60] P.V. Necliudov, M.S. Shur, D.J. Gundlach, and T.N. Jackson, "Contact resistance extraction in pentacene thin film transistors", *Solid-State Electronics*, vol. 47, no. 2, pp. 259–262, 2003.

[61] S. Rauschenbach, F.L. Stadler, E. Lunedei, N. Malinowski, S. Koltsov, G. Costantini, and K. Kern, "Electrospray ion beam deposition of clusters and biomolecules", *Small*, vol. 2, no. 4, pp. 540–547, 2006.

[62] H.J. Raeder, A. Rouhanipour, A.M. Talarico, V. Palermo, P. Samorì, and K. Muellen, "Processing of giant graphene molecules by soft-landing mass spectrometry", *Nature materials*, vol. 5, no. 4, pp. 276–280, 2006.

[63] A.A. Virkar, S. Mannsfeld, Z. Bao, and N. Stingelin, "Organic Semiconductor Growth and Morphology Considerations for Organic Thin-Film Transistors", *Advanced Materials*.

[64] S. Lukas, G. Witte, and C. Woell, "Novel mechanism for molecular self-assembly on metal substrates: Unidirectional rows of pentacene on Cu (110) produced by a substrate-mediated repulsion", *Physical Review Letters*, vol. 88, no. 2, pp. 28301, 2001.

[65] M. Shtein, J. Mapel, J.B. Benziger, and S.R. Forrest, "Effects of film morphology and gate dielectric surface preparation on the electrical characteristics of organic-vapor-phase-deposited pentacene thin-film transistors", *Applied Physics Letters*, vol. 81, pp. 268, 2002.

[66] S. Schiefer, M. Huth, A. Dobrinevski, and B. Nickel, "Determination of the crystal structure of substrate-induced pentacene polymorphs in fiber structured thin films", *Journal of the American Chemical Society*, vol. 129, no. 34, pp. 10316–10317, 2007.

[67] D.G. de Oteyza, E. Barrena, J.O. Ossó, S. Sellner, and H. Dosch, "Thickness-dependent structural transitions in fluorinated copper-phthalocyanine (F16CuPc) films", *Journal of the American Chemical Society*, vol. 128, no. 47, pp. 15052–15053, 2006.

[68] D.G. de Oteyza, E. Barrena, S. Sellner, J.O. Ossó, and H. Dosch, "Structural rearrangements during the initial growth stages of organic thin films of F16CuPc on SiO2", *The Journal of Physical Chemistry B*, vol. 110, no. 33, pp. 16618–16623, 2006.

[69] S. Haas, Y. Takahashi, K. Takimiya, and T. Hasegawa, "High-performance dinaphtho-thieno-thiophene single crystal field-effect transistors", *Applied Physics Letters*, vol. 95, pp. 022111, 2009.

[70] S.M. Sze, *Semiconductor Devices: Physics and Technology*, John Wiley & Sons, New York, 2nd edition edition, 1981.

[71] R.T. Weitz, *Electrical Properties of Functionalized Nanowire Field Effect Transistors*, PhD thesis, École Polytechnique Fédérale de Lausanne, 2008.

[72] G. Horowitz, "Organic field-effect transistors", *Adv. Mater.*, vol. 10, pp. 365–377, 1998.

[73] I.G. Hill, D. Milliron, J. Schwartz, and A. Kahn, "Organic semiconductor interfaces: electronic structure and transport properties", *Applied Surface Science*, vol. 166, no. 1-4, pp. 354–362, 2000.

[74] I.G. Hill, A. Rajagopal, A. Kahn, and Y. Hu, "Molecular level alignment at organic semiconductor-metal interfaces", *Applied Physics Letters*, vol. 73, no. 5, pp. 662, 1998.

[75] R.H. Dennard, F.H. Gaensslen, H.N. Yu, V.L. Rideout, E. Bassous, and A.R. LeBlanc, "Design of ion-implanted MOSFETs with very small physical dimensions", *Proceedings of the IEEE*, vol. 87, no. 4, pp. 668, 1974.

[76] Y. Taur, "CMOS design near the limit of scaling", *IBM Journal of Research and Development*, vol. 46, no. 2-3, pp. 213–222, 2002.

[77] P.V. Pesavento, R.J. Chesterfield, C.R. Newman, and C.D. Frisbie, "Gated four-probe measurements on pentacene thin-film transistors: Contact resistance as a function of gate voltage and temperature", *Journal of Applied Physics*, vol. 96, pp. 7312, 2004.

[78] C. Siol, C. Melzer, and H. von Seggern, "Electron trapping in pentacene based p-and n-type organic field-effect transistors", *Applied Physics Letters*, vol. 93, pp. 133303, 2008.

[79] S. Scheinert and G. Paasch, "Interdependence of contact properties and field-and density-dependent mobility in organic field-effect transistors", *Journal of Applied Physics*, vol. 105, pp. 014509, 2009.

[80] T. Komoda, Y. Endo, K. Kyuno, and A. Toriumi, "Field-dependent mobility of highly oriented pentacene thin-film transistors", *Japanese Journal of Applied Physics*, vol. 1, no. 41, pp. 2767, 2002.

[81] D.K. Schroder, *Semiconductor material and device characterization*, Wiley-IEEE Press, 2006.

[82] S.M. Sze, *Semiconductor Devices: Physics and Technology*, John Wiley & Sons, New York, 1985.

[83] A. Ortiz-Conde, F.J. Garcia Sanchez, J.J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, "A review of recent MOSFET threshold voltage extraction methods", *Microelectronics Reliability*, vol. 42, no. 4-5, pp. 583–596, 2002.

[84] D. Boudinet, G. Le Blevennec, C. Serbutoviez, J.M. Verilhac, H. Yan, and G. Horowitz, "Contact resistance and threshold voltage extraction in n-channel organic thin film transistors on plastic substrates", *Journal of Applied Physics*, vol. 105, pp. 084510, 2009.

[85] J.N. Haddock, X. Zhang, S. Zheng, Q. Zhang, S.R. Marder, and B. Kippelen, "A comprehensive study of short channel effects in organic field-effect transistors", *Organic Electronics*, vol. 7, no. 1, pp. 45–54, 2006.

[86] J. Collet, O. Tharaud, A. Chapoton, and D. Vuillaume, "Low-voltage, 30 nm channel length, organic transistors with a self-assembled monolayer as gate insulating films", *Applied Physics Letters*, vol. 76, no. 14, pp. 1941–1943, 2000.

[87] M.D. Austin and S.Y. Chou, "Fabrication of 70 nm channel length polymer organic thin-film transistors using nanoimprint lithography", *Applied Physics Letters*, vol. 81, pp. 4431, 2002.

[88] Y. Zhang, J.R. Petta, S. Ambily, Y. Shen, D.C. Ralph, and G.G. Malliaras, "30 nm channel length pentacene transistors", *Advanced Materials*, vol. 15, no. 19, pp. 1632–1635, 2003.

[89] J. Zaumseil, T. Someya, Z. Bao, Y.L. Loo, R. Cirelli, and J.A. Rogers, "Nanoscale organic transistors that use source/drain electrodes supported by high resolution rubber stamps", *Applied Physics Letters*, vol. 82, pp. 793, 2003.

[90] L. Wang, D. Fine, T. Jung, D. Basu, H. von Seggern, and A. Dodabalapur, "Pentacene field-effect transistors with sub-10-nm channel lengths", *Applied Physics Letters*, vol. 85, pp. 1772, 2004.

[91] G.S. Tulevski, Q. Miao, A. Afzali, T.O. Graham, C.R. Kagan, and C. Nuckolls, "Chemical complementarity in the contacts for nanoscale organic field-effect transistors", *Journal of the American Chemical Society*, vol. 128, no. 6, pp. 1788–1789, 2006.

[92] I. Yagi, K. Shigeto, K. Tsukagoshi, and Y. Aoyagi, "Alignment-free top-contact formation for organic thin film transistors with submicron-length channel", *Japanese Journal of Applied Physics*, vol. 44, pp. L479–L481, 2005.

[93] K. Tsukagoshi, K. Shigeto, I. Yagi, and Y. Aoyagi, "Interface modification of a pentacene field-effect transistor with a submicron channel", *Applied Physics Letters*, vol. 89, pp. 113507, 2006.

[94] F. Fujimori, K. Shigeto, T. Hamano, T. Minari, T. Miyadera, K. Tsukagoshi, and Y. Aoyagi, "Current transport in short channel top-contact pentacene field-effect transistors investigated with the selective molecular doping technique", *Applied Physics Letters*, vol. 90, pp. 193507, 2007.

[95] L. Herlogsson, Y.Y. Noh, N. Zhao, X. Crispin, H. Sirringhaus, and M. Berggren, "Downscaling of Organic Field-Effect Transistors with a Polyelectrolyte Gate Insulator", *Advanced Materials*, vol.

20, no. 24, pp. 4708–4713, 2008.

[96] L. Diao, C.D. Frisbie, D.D. Schroepfer, and P.P. Ruden, "Electrical characterization of metal/pentacene contacts", *Journal of Applied Physics*, vol. 101, pp. 014510, 2007.

[97] X. Crispin, V. Geskin, A. Crispin, J. Cornil, R. Lazzaroni, W.R. Salaneck, and J.L. Brédas, "Characterization of the interface dipole at organic/metal interfaces", *Journal of the American Chemical Society*, vol. 124, no. 27, pp. 8131–8141, 2002.

[98] N. Koch and A. Vollmer, "Electrode-molecular semiconductor contacts: Work-function-dependent hole injection barriers versus Fermi-level pinning", *Applied Physics Letters*, vol. 89, pp. 162107, 2006.

[99] N.J. Watkins, L. Yan, and Y. Gao, "Electronic structure symmetry of interfaces between pentacene and metals", *Applied Physics Letters*, vol. 80, pp. 4384, 2002.

[100] A. Benor and D. Knipp, "Contact effects in organic thin film transistors with printed electrodes", *Organic Electronics*, vol. 9, no. 2, pp. 209–219, 2008.

[101] H. Klauk, M. Halik, U. Zschieschang, G. Schmid, W. Radlik, and W. Weber, "High-mobility polymer gate dielectric pentacene thin film transistors", *Journal of Applied Physics*, vol. 92, pp. 5259, 2002.

[102] H. Klauk, *Organic electronics*, Wiley-VCH Weinheim, 2006.

[103] F. So, *Organic Electronics: Materials, Processing, Devices and Applications*, CRC, 2009.

[104] Z. Bao and J.J. Locklin, *Organic field-effect transistors*, CRC, 2007.

[105] M. Leufgen, U. Bass, T. Muck, T. Borzenko, G. Schmidt, J. Geurts, V. Wagner, and L.W. Molenkamp, "Optimized sub-micron organic thin-film transistors: the influence of contacts and oxide thickness", *Synthetic Metals*, vol. 146, no. 3, pp. 341–345, 2004.

[106] A. Hoppe, J. Seekamp, T. Balster, G. Goetz, P. Baeuerle, and V. Wagner, "Tuning the contact resistance in nanoscale oligothiophene field effect transistors", *Applied Physics Letters*, vol. 91, pp. 132115, 2007.

[107] G. S. Tulevski, C. Nuckolls, A. Afzali, T. O. Graham, and C.R. Kagan, "Device scaling in sub-100 nm pentacene field-effect transistors", *Applied Physics Letters*, vol. 89, pp. 183101, 2006.

[108] J. Zaumseil, K.W. Baldwin, and J.A. Rogers, "Contact resistance in organic transistors that use source and drain electrodes formed by soft contact lamination", *Journal of Applied Physics*, vol. 93, pp. 6117, 2003.

[109] T. Ji, S. Jung, and V.K. Varadan, "On the correlation of postannealing induced phase transition in pentacene with carrier transport", *Organic Electronics*, vol. 9, no. 5, pp. 895–898, 2008.

[110] C.H. Shim, F. Maruoka, and R. Hattori, "Structural Analysis on Organic Thin-Film Transistor With Device Simulation", *IEEE Transactions on Electron Devices*, vol. 57, no. 1, pp. 195, 2010.

[111] Q.J. Cai, M.B. Chan-Park, Z.S. Lu, C.M. Li, and B.S. Ong, "Bottom-Contact Poly (3, 3"'-didodecylquaterthiophene) Thin-Film Transistors with Gold Source-Drain Electrodes Modified by Alkanethiol Monolayers", *Langmuir*, vol. 24, no. 20, pp. 11889–11894, 2008.

[112] H.E. Katz, J. Johnson, A.J. Lovinger, and W. Li, "Naphthalenetetracarboxylic diimide-based n-channel transistor semiconductors: structural variation and thiol-enhanced gold contacts", *Journal of the American Chemical Society*, vol. 122, no. 32, pp. 7787–7792, 2000.

[113] J. Li, L. Zhang, X.W. Zhang, H. Zhang, X.Y. Jiang, D. Yu, W.Q. Zhu, and Z.L. Zhang, "Reduction of the contact resistance in copper phthalocyanine thin film transistor with UV/ozone treated Au electrodes", *Current Applied Physics*, 2010.

[114] B. Stadlober, U. Haas, H. Gold, A. Haase, G. Jakopic, G. Leising, N. Koch, S. Rentenberger, and E. Zojer, "Orders-of-magnitude reduction of the contact resistance in short-channel hot embossed organic thin film transistors by oxidative treatment of Au-electrodes", *Advanced functional materials*, vol. 17, no. 15, pp. 2687–2692, 2007.

[115] M. Halik, H. Klauk, U. Zschieschang, G. Schmid, S. Ponomarenko, S. Kirchmeyer, and W. Weber, "Relationship between molecular structure and electrical performance of oligothiophene organic thin film transistors", *Advanced Materials*, vol. 15, no. 11, pp. 917–922, 2003.

[116] C.D. Dimitrakopoulos, S. Purushothaman, J. Kymissis, A. Callegari, and J.M. Shaw, "Low-voltage organic transistors on plastic comprising high-dielectric constant gate insulators", *Science*, vol. 283, no. 5403, pp. 822, 1999.

[117] M. Caironi, E. Gili, T. Sakanoue, X. Cheng, and H. Sirringhaus, "High Yield, Single Droplet Electrode Arrays for Nanoscale Printed Electronics", *ACS Nano*, vol. 4, no. 3, pp. 1451–1456, 2010.

[118] T. Sekitani, Y. Noguchi, U. Zschieschang, H. Klauk, and T. Someya, "Organic transistors manufactured using inkjet technology with subfemtoliter accuracy", *Proceedings of the National Academy of Sciences*, vol. 105, no. 13, pp. 4976, 2008.

[119] F. Letzkus, J. Butschke, B. Hoefflinger, M. Irmscher, C. Reuter, R. Springer, A. Ehrmann, and J. Mathuni, "Dry etch improvements in the SOI wafer flow process for IPL stencil mask fabrication", *Microelectronic Engineering*, vol. 53, no. 1-4, pp. 609–612, 2000.

[120] J. Butschke, A. Ehrmann, B. Hoefflinger, M. Irmscher, R. Kaesmaier, F. Letzkus, H. Loschner, J. Mathuni, C. Reuter, C. Schomburg, and R. Springer, "Soi wafer flow process for stencil mask fabrication", *Microelectronic Engineering*, vol. 46, no. 1-4, pp. 473 – 476, 1999, International Conference on Micro- and Nanofabrication.

[121] H. Klauk, U. Zschieschang, and M. Halik, "Low-voltage organic thin-film transistors with large transconductance", *Journal of Applied Physics*, vol. 102, no. 7, pp. 074514, 2007.

[122] F. Ante, F. Letzkus, J. Butschke, U. Zschieschang, JN Burghartz, K. Kern, and H. Klauk, "Top-contact organic transistors and complementary circuits fabricated using high-resolution silicon stencil masks", in *Device Research Conference (DRC), 2010*. IEEE, 2010, pp. 175–176.

[123] O. Vazquez-Mena, L.G. Villanueva, V. Savu, K. Sidler, P. Langlet, and J. Brugger, "Analysis of the blurring in stencil lithography", *Nanotechnology*, vol. 20, pp. 415303, 2009.

[124] V. Savu, M.A.F. van den Boogaart, J. Brugger, J. Arcamone, M. Sansa, and F. Perez-Murano, "Dynamic stencil lithography on full wafer scale", *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 26, pp. 2054, 2008.

[125] T. Minari, T. Miyadera, K. Tsukagoshi, Y. Aoyagi, and H. Ito, "Charge injection process in organic field-effect transistors", *Applied Physics Letters*, vol. 91, pp. 053508, 2007.

[126] B.D. Terris, L. Folks, D. Weller, J.E.E Baglin, A.J. Kellock, H. Rothuizen, and P. Vettiger, "Ion-beam patterning of magnetic films using stencil masks", *Applied Physics Letters*, vol. 75, pp. 403, 1999.

[127] AR Champagne, AJ Couture, F. Kuemmeth, and DC Ralph, "Nanometer-scale scanning sensors fabricated using stencil lithography", *Applied Physics Letters*, vol. 82, pp. 1111, 2003.

[128] O. Vazquez-Mena, G. Villanueva, V. Savu, K. Sidler, M.A.F. Van den Boogaart, and J. Brugger, "Metallic nanowires by full wafer stencil lithography", *Nano Letters*, vol. 8, no. 11, pp. 3675–3682, 2008.

[129] K. Sidler, O. Vazquez-Mena, V. Savu, G. Villanueva, M.A.F. van den Boogaart, and J. Brugger, "Resistivity measurements of gold wires fabricated by stencil lithography on flexible polymer substrates", *Microelectronic Engineering*, vol. 85, no. 5-6, pp. 1108–1111, 2008.

[130] S.H. Jin, K.D. Jung, H. Shin, B.G. Park, and J.D. Lee, "Grain size effects on contact resistance of top-contact pentacene TFTs", *Synthetic Metals*, vol. 156, no. 2-4, pp. 196–201, 2006.

[131] K. Sidler, N.V. Cvetkovic, V. Savu, D. Tsamados, A.M. Ionescu, and J. Brugger, "Organic Thin Film Transistors on Flexible Polyimide Substrates Fabricated by Full Wafer Stencil Lithography", *Sensors and Actuators A: Physical*, 2010.

[132] H. Klauk, U. Zschieschang, R.T. Weitz, H. Meng, F. Sun, G. Nunes, D.E. Keys, C.R. Fincher, and Z. Xiang, "Organic transistors based on di(phenylvinyl)anthracene: Performance and stability", *Advanced Materials*, vol. 19, no. 22, pp. 3882–3887, 2007.

[133] W. Xiong, Y. Guo, U. Zschieschang, H. Klauk, and B. Murmann, "A 3-V, 6-bit C-2C digital-to-analog converter using complementary organic thin-film transistors on glass", *IEEE Journal of Solid-State Circuits*, vol. 45, no. 7, 2010.

[134] U. Zschieschang, F. Ante, M. Schloerholz, M. Schmidt, K. Kern, and H. Klauk, "Mixed Self-Assembled Monolayer Gate Dielectrics for Continuous Threshold Voltage Control in Organic Transistors and Circuits", *Advanced Materials*.

[135] W.J. Kim, C.S. Kim, S.J. Jo, S.W. Lee, S.J. Lee, and H.K. Baik, "Observation of the Hysteresis Behavior of Pentacene Thin-Film Transistors in I–V and C–V Measurements", *Electrochemical and Solid-State Letters*, vol. 10, pp. H1, 2007.

[136] K. Fukuda, T. Hamamoto, T. Yokota, T. Sekitani, U. Zschieschang, H. Klauk, and T. Someya, "Effects of the alkyl chain length in phosphonic acid self-assembled monolayer gate dielectrics on the performance and stability of low-voltage organic thin-film transistors", *Applied Physics Letters*, vol. 95, no. 20, pp. 203301, 2009.

[137] D.J. Gundlach, Y.Y. Lin, T.N. Jackson, S.F. Nelson, and D.G. Schlom, "Pentacene organic thin-film transistors-molecular ordering and mobility", *IEEE Electron Device Letters*, vol. 18, no. 3, pp. 87–89, 1997.

[138] R.T. Weitz, U. Zschieschang, F. Effenberger, H. Klauk, M. Burghard, and K. Kern, "High-performance carbon nanotube field effect transistors with a thin gate dielectric based on a self-assembled monolayer", *Nano Letters*, vol. 7, no. 1, pp. 22–27, 2007.

[139] R.T. Weitz, U. Zschieschang, A. Forment-Aliaga, D. Kaelblein, M. Burghard, K. Kern, and H. Klauk, "Highly Reliable Carbon Nanotube Transistors with Patterned Gates and Molecular Gate Dielectric", *Nano Letters*, vol. 9, no. 4, pp. 1335–1340, 2009.

[140] M. Muench, *Strukturelle Beeinflussung der elektrischen Transporteigenschaften duenner organischer Schichten*, 2001.

[141] S.F. Nelson, Y.-Y. Lin, D.J. Gundlach, and T.N. Jackson, "Temperature-independent transport in high-mobility pentacene transistors", *Applied physics letters*, vol. 72, pp. 1854, 1998.

[142] D. Knipp, R.A. Street, and A.R. Voelkel, "Morphology and electronic transport of polycrystalline pentacene thin-film transistors", *Applied Physics Letters*, vol. 82, pp. 3907, 2003.

[143] R.A. Street, D. Knipp, and A.R. Voelkel, "Hole transport in polycrystalline pentacene transistors", *Applied Physics Letters*, vol. 80, pp. 1658, 2002.

[144] D. Knipp, RA Street, A. Voelkel, and J. Ho, "Pentacene thin film transistors on inorganic dielectrics: Morphology, structural properties, and electronic transport", *Journal of Applied Physics*, vol. 93, pp. 347, 2003.

[145] Y.W. Wang, H.L. Cheng, Y.K. Wang, T.H. Hu, J.C. Ho, C.C. Lee, T.F. Lei, and C.F. Yeh, "Influence of measuring environment on the electrical characteristics of pentacene-based thin film transistors", *Thin Solid Films*, vol. 467, no. 1-2, pp. 215–219, 2004.

[146] H.L. Cheng, Y.S. Mai, W.Y. Chou, and L.R. Chang, "Influence of molecular structure and microstructure on device performance of polycrystalline pentacene thin-film transistors", *Applied Physics Letters*, vol. 90, pp. 171926, 2007.

[147] G.A. de Wijs, C.C. Mattheus, R.A. de Groot, and T. Palstra, "Anisotropy of the mobility of pentacene from frustration", *Synthetic Metals*, vol. 139, no. 1, pp. 109–114, 2003.

[148] J.Y. Lee, S. Roth, and Y.W. Park, "Anisotropic field effect mobility in single crystal pentacene", *Applied Physics Letters*, vol. 88, pp. 252106, 2006.

[149] P.V. Necliudov, M.S. Shur, D.J. Gundlach, and T.N. Jackson, "Modeling of organic thin film transistors of different designs", *Journal of Applied Physics*, vol. 88, pp. 6594, 2000.

[150] T.J. Richards and H. Sirringhaus, "Analysis of the contact resistance in staggered, top-gate organic field-effect transistors", *Journal of Applied Physics*, vol. 102, pp. 094510, 2007.

[151] L. Buergi, T.J. Richards, R.H. Friend, and H. Sirringhaus, "Close look at charge carrier injection in polymer field-effect transistors", *Journal of Applied Physics*, vol. 94, pp. 6129, 2003.

[152] K.P. Puntambekar, P.V. Pesavento, and C.D. Frisbie, "Surface potential profiling and contact resistance measurements on operating pentacene thin-film transistors by Kelvin probe force microscopy", *Applied Physics Letters*, vol. 83, pp. 5539, 2003.

[153] S. Luan and G.W. Neudeck, "An experimental study of the source/drain parasitic resistance effects in amorphous silicon thin film transistors", *Journal of Applied Physics*, vol. 72, pp. 766, 1992.

[154] C. Chiang, S. Martin, J. Kanicki, Y. Ugai, T. Yukawa, and S. Takeuchi, "Top-gate staggered amorphous silicon thin-film transistors: Series resistance and nitride thickness effects", *Japanese Journal of Applied Physics*, vol. 37, pp. 5914, 1998.

[155] H. Klauk, G. Schmid, W. Radlik, W. Weber, L. Zhou, C.D. Sheraw, J.A. Nichols, and T.N. Jackson, "Contact resistance in organic thin film transistors", *Solid-State Electronics*, vol. 47, no. 2, pp. 297–301, 2003.

[156] H. Murrmann and D. Widmann, "Current crowding on metal contacts to planar devices", *Electron Devices, IEEE Transactions on*, vol. 16, no. 12, pp. 1022–1024, 1969.

[157] H.H. Berger, "Contact resistance and contact resistivity", *Journal of the Electrochemical Society*, vol. 119, pp. 507, 1972.

[158] H.H. Berger, "Models for contacts to planar devices* 1", *Solid-State Electronics*, vol. 15, no. 2, pp. 145–158, 1972.

[159] I.N. Hulea, S. Russo, A. Molinari, and A.F. Morpurgo, "Reproducible low contact resistance in rubrene single-crystal field-effect transistors with nickel electrodes", *Applied Physics Letters*, vol. 88, pp. 113512, 2006.

[160] J. Zaumseil and H. Sirringhaus, "Electron and ambipolar transport in organic field-effect transistors", *Chemical Reviews*, vol. 107, no. 4, pp. 1296–1323, 2007.

[161] A. Hoppe, D. Knipp, B. Gburek, A. Benor, M. Marinkovic, and V. Wagner, "Scaling limits of organic thin film transistors", *Organic Electronics*, vol. 11, no. 4, pp. 626–631, 2010.

[162] U. Bass, "Organische Molekular Strahl Deposition und elektrische Analyse von Feldeffekt-Transistoren", *Diplomarbeit an der Universitaet Wuerzburg*, 2004.

[163] V. Mikhelashvili, G. Eisenstein, and R. Uzdin, "Extraction of Schottky diode parameters with a bias dependent barrier height", *Solid-State Electronics*, vol. 45, no. 1, pp. 143–148, 2001.

[164] E.H. Rhoderick and R.H. Williams, "Metal-Semiconductor Contacts. 1978".

[165] Y.F. Lin and W.B. Jian, "The Impact of Nanocontact on Nanowire Based Nanoelectronics", *Nano Letters*, vol. 8, no. 10, pp. 3146–3150, 2008.

[166] D. Knipp, RA Street, B. Krusor, R. Apte, and J. Ho, "Polycrystalline pentacene thin films for large area electronic applications", *Journal of Non-Crystalline Solids*, vol. 299, pp. 1042–1046, 2002.

[167] A. Herasimovich, S. Scheinert, and I. Hoerselmann, "Influence of traps on top and bottom contact field-effect transistors based on modified poly (phenylene-vinylene)", *Journal of Applied Physics*, vol. 102, pp. 054509, 2007.

[168] P.V. Pesavento, K.P. Puntambekar, C.D. Frisbie, J.C. Mckeen, and P.P. Ruden, "Film and contact resistance in pentacene thin-film transistors: Dependence on film thickness, electrode geometry, and correlation with hole mobility", *Journal of Applied Physics*, vol. 99, pp. 094504, 2006.

[169] C.W. Sohn, T.U. Rim, G.B. Choi, and Y.H. Jeong, "Analysis of Contact Effects in Inverted-Staggered Organic Thin-Film Transistors Based on Anisotropic Conduction", *IEEE Transactions on Electron Devices*, vol. 57, pp. 986–994, 2010.

[170] J. Frenkel, "On pre-breakdown phenomena in insulators and electronic semi-conductors", *Physical Review*, vol. 54, pp. 647–648, 1938.

[171] S. Locci, M. Morana, E. Orgiu, A. Bonfiglio, and P. Lugli, "Modeling of Short-Channel Effects in Organic Thin-Film Transistors", *IEEE Transactions on Electron Devices*, vol. 55, no. 10, pp. 2561, 2008.

[172] S. Locci, "Personal communication".

[173] S. Steudel, K. Myny, V. Arkhipov, C. Deibel, S. De Vusser, J. Genoe, and P. Heremans, "50 MHz rectifier based on an organic diode", *Nature Materials*, vol. 4, no. 8, pp. 597–600, 2005.

[174] M. Fiebig, C. Erlen, M. Goellner, P. Lugli, and B. Nickel, "Spatially resolved photoresponse measurements on pentacene thin-film transistors", *Applied Physics A: Materials Science & Processing*, vol. 95, no. 1, pp. 113–117, 2009.

[175] A.W. Tsen, F. Cicoira, G.G. Malliaras, and J. Park, "Photoelectrical imaging and characterization of point contacts in pentacene thin-film transistors", *Applied Physics Letters*, vol. 97, pp. 023308, 2010.

[176] D. Bode, K. Myny, B. Verreet, B. van der Putten, P. Bakalov, S. Steudel, S. Smout, P. Vicca, J. Genoe, and P. Heremans, "Organic complementary oscillators with stage-delays below 1 μs", *Applied Physics Letters*, vol. 96, pp. 133307, 2010.

[177] U. Zschieschang, F. Ante, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani,

T. Someya, K. Kern, and H. Klauk, "Flexible Low-Voltage Organic Transistors and Circuits Based on a High-Mobility Organic Semiconductor with Good Air Stability", *Advanced Materials*, vol. 22, no. 9, pp. 982–985, 2010.

[178] J.H. Lee, G.H. Kim, S.H. Kim, S.C. Lim, Y.S. Yang, J.H. Youk, J. Jang, and T. Zyung, "Longevity enhancement of organic thin-film transistors by using a facile laminating passivation method", *Synthetic Metals*, vol. 143, no. 1, pp. 21–23, 2004.

[179] H. Jung, T. Lim, Y. Choi, M. Yi, J. Won, and S. Pyo, "Lifetime enhancement of organic thin-film transistors protected with organic layer", *Applied Physics Letters*, vol. 92, pp. 163504, 2008.

[180] F. De Angelis, M. Gaspari, A. Procopio, G. Cuda, and E. Di Fabrizio, "Direct mass spectrometry investigation on Pentacene thin film oxidation upon exposure to air", *Chemical Physics Letters*, vol. 468, no. 4-6, pp. 193–196, 2009.

[181] P. Qi, A. Javey, M. Rolandi, Q. Wang, E. Yenilmez, and H. Dai, "Miniature organic transistors with carbon nanotubes as quasi-one-dimensional electrodes", *Journal of the American Chemical Society*, vol. 126, no. 38, pp. 11774–11775, 2004.

[182] W.L. Kalb, F. Meier, K. Mattenberger, and B. Batlogg, "Defect healing at room temperature in pentacene thin films and improved transistor performance", *Physical Review B*, vol. 76, no. 18, pp. 184112, 2007.

[183] R. Ye, M. Baba, K. Suzuki, Y. Ohishi, and K. Mori, "Effect of thermal annealing on morphology of pentacene thin films", *Japanese Journal of Applied Physics*, vol. 1, no. 42, pp. 4473, 2003.

[184] SJ Kang, M. Noh, DS Park, HJ Kim, CN Whang, and C.H. Chang, "Influence of postannealing on polycrystalline pentacene thin film transistor", *Journal of Applied Physics*, vol. 95, pp. 2293, 2004.

[185] T. Ahn, H. Jung, H.J. Suk, and M.H. Yi, "Effect of postfabrication thermal annealing on the electrical performance of pentacene organic thin-film transistors", *Synthetic Metals*, vol. 159, no. 13, pp. 1277–1280, 2009.

[186] Q.J. Cai, M.B. Chan-Park, Q. Zhou, Z.S. Lu, C.M. Li, and B.S. Ong, "Self-assembled monolayers mediated charge injection for high performance bottom-contact poly (3, 3"'-didodecylquaterthiophene) thin-film transistors", *Organic Electronics*, vol. 9, no. 6, pp. 936–943, 2008.

[187] D. Kumaki, T. Umeda, and S. Tokito, "Reducing the contact resistance of bottom-contact pentacene thin-film transistors by employing a MoO carrier injection layer", *Applied Physics Letters*, vol. 92, pp. 013301, 2008.

[188] S. Reineke, F. Lindner, G. Schwartz, N. Seidler, K. Walzer, B. Luessem, and K. Leo, "White organic light-emitting diodes with fluorescent tube efficiency", *Nature*, vol. 459, no. 7244, pp. 234–238, 2009.

[189] S.D. Ha, Y. Qi, and A. Kahn, "Relative permittivity and Hubbard U of pentacene extracted from scanning tunneling microscopy studies of p-doped films", *Chemical Physics Letters*, 2010.

[190] J. Li, X.W. Zhang, L. Zhang, et al., "Improving organic transistor performance through contact-area-limited doping", *Solid State Communications*, vol. 149, no. 41-42, pp. 1826–1830, 2009.

[191] F. Fujimori, K. Shigeto, T. Hamano, T. Minari, T. Miyadera, K. Tsukagoshi, and Y. Aoyagi, "Current transport in short channel top-contact pentacene field-effect transistors investigated with the selective molecular doping technique", *Applied Physics Letters*, vol. 90, pp. 193507, 2007.

[192] M. Kano, T. Minari, and K. Tsukagoshi, "Improvement of subthreshold current transport by

contact interface modification in p-type organic field-effect transistors", *Applied Physics Letters*, vol. 94, pp. 143304, 2009.

[193] S.Y. Park, Y.H. Noh, and H.H. Lee, "Introduction of an interlayer between metal and semiconductor for organic thin-film transistors", *Applied Physics Letters*, vol. 88, pp. 113503, 2006.

[194] C. Vanoni, T.A. Jung, and S. Tsujino, "Temperature dependent charge-injection at the metal-organic semiconductor interface and density of states in pristine and doped pentacene", *Applied Physics Letters*, vol. 94, pp. 253306, 2009.

[195] R. Schroeder, L.A. Majewski, and M. Grell, "Improving organic transistor performance with Schottky contacts", *Applied Physics Letters*, vol. 84, pp. 1004, 2004.

[196] S.P. Tiwari, W.J. Potscavage Jr, T. Sajoto, S. Barlow, S.R. Marder, and B. Kippelen, "Pentacene organic field-effect transistors with doped electrode-semiconductor contacts", *Organic Electronics*, 2010.

[197] C. Vanoni, S. Tsujino, and T.A. Jung, "Reduction of the contact resistance by doping in pentacene few monolayers thin film transistors and self-assembled nanocrystals", *Applied Physics Letters*, vol. 90, pp. 193119, 2007.

[198] W.L. Kalb and B. Batlogg, "Calculating the trap density of states in organic field-effect transistors from experiment: A comparison of different methods", *Physical Review B*, vol. 81, no. 3, pp. 35327, 2010.

[199] U. Zschieschang, R.T. Weitz, K. Kern, and H. Klauk, "Bias stress effect in low-voltage organic thin-film transistors", *Applied Physics A: Materials Science & Processing*, vol. 95, no. 1, pp. 139–145, 2009.

[200] V. Wagner, P. Wobkenberg, A. Hoppe, and J. Seekamp, "Megahertz operation of organic field-effect transistors based on poly (3-hexylthiopene)", *Applied Physics Letters*, vol. 89, no. 24, pp. 243515, 2009.

[201] H. Ryu, D. Kaelblein, R.T. Weitz, F. Ante, U. Zschieschang, K. Kern, O.G. Schmidt, and H. Klauk, "Logic circuits based on individual semiconducting and metallic carbon-nanotube devices", *Nanotechnology*, vol. 21, pp. 475207, 2010.

[202] L.L. Chua, J. Zaumseil, J.F. Chang, E.C.W. Ou, P.K.H. Ho, H. Sirringhaus, and R.H. Friend, "General observation of n-type field-effect behaviour in organic semiconductors", *Nature*, vol. 434, no. 7030, pp. 194–199, 2005.

[203] M. Ahles, R. Schmechel, and H. von Seggern, "n-type organic field-effect transistor based on interface-doped pentacene", *Applied Physics Letters*, vol. 85, pp. 4499, 2004.

[204] Z. Bao, A.J. Lovinger, and J. Brown, "New air-stable n-channel organic thin film transistors", *Journal of the American Chemical Society*, vol. 120, no. 1, pp. 207–208, 1998.

[205] M. Gorgoi, *Electronic Properties of Phthalocyanines Deposited on H-Si (111)*, PhD thesis, Universitaetsbibliothek der Technischen Universitaet, 2006.

[206] H.E. Katz, A.J. Lovinger, J. Johnson, C. Kloc, T. Siegrist, W. Li, Y.-Y. Lin, and A. Dodabalapur, "A soluble and air-stable organic semiconductor with high electron mobility", *Nature*, vol. 404, no. 6777, pp. 478–481, 2000.

[207] B.A. Jones, M.J. Ahrens, M.H. Yoon, A. Facchetti, T.J. Marks, and M.R. Wasielewski, "High-Mobility Air-Stable n-Type Semiconductors with Processing Versatility: Dicyanoperylene-3, 4: 9,

10-bis (dicarboximides)", *Angewandte Chemie*, vol. 116, no. 46, pp. 6523–6526, 2004.

[208] R.T. Weitz, K. Amsharov, U. Zschieschang, E.B. Villas, D.K. Goswami, M. Burghard, H. Dosch, M. Jansen, K. Kern, and H. Klauk, "Organic n-channel transistors based on core-cyanated perylene carboxylic diimide derivatives", *Journal of the American Chemical Society*, vol. 130, no. 14, pp. 4637–4645, 2008.

[209] D. Gamota, *Printed organic and molecular electronics*, Springer Netherlands, 2004.

[210] B.K. Crone, A. Dodabalapur, R. Sarpeshkar, R.W. Filas, Y.-Y. Lin, Z. Bao, J.H. O'Neill, W. Li, and H.E. Katz, "Design and fabrication of organic complementary circuits", *Journal of Applied Physics*, vol. 89, pp. 5125, 2001.

[211] P. Heremans, J. Genoe, S. Steudel, K. Myny, S. Smout, P. Vicca, C. Grillberger, O.R. Hild, F. Furthner, B. van der Putten, et al., "Thin-film transistors and circuits on plastic foil", in *Electron Devices Meeting (IEDM), 2009 IEEE International*. IEEE, 2010, pp. 1–4.

[212] T. Zaki, F. Ante, U. Zschieschang, F. Letzkus, H. Richter, H. Klauk, and J.N. Burghartz, "A 3.3V 6b 100kS/s current-steering D/A converter using organic thin-film transistors on glass", in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International*. IEEE, 2011, pp. 324–325.

[213] E.J.H. Lee, K. Balasubramanian, R.T. Weitz, M. Burghard, and K. Kern, "Contact and edge effects in graphene devices", *Nature Nanotechnology*, vol. 3, no. 8, pp. 486–490, 2008.

[214] K. Balasubramanian, M. Burghard, K. Kern, M. Scolari, and A. Mews, "Photocurrent imaging of charge transport barriers in carbon nanotube devices", *Nano Letters*, vol. 5, no. 3, pp. 507–510, 2005.

[215] M. Lishchynska, V. Bourenkov, M.A.F. van den Boogaart, L. Doeswijk, J. Brugger, and J.C. Greer, "Predicting mask distortion, clogging and pattern transfer for stencil lithography", *Microelectronic Engineering*, vol. 84, no. 1, pp. 42–53, 2007.

Curriculum vitae

Personal information

Name	Frederik Sebastian Ante
Date of birth	28.05.1981
Place of birth	Würzburg, Germany
Nationality	German

Education

since July 2007	Research staff at the Max-Planck Institute for Solid State Research PhD student at the École Polytechnique Fédéral de Lausanne
May 2007	Diploma in Physics: University of Würzburg
2001 - 2007	Study of Physics at: University of Würzburg, Germany Swiss Federal Institute of Technology (ETH Zurich), Switzerland University of British Columbia, Vancouver, Canada
2000	"Abitur" at the Riemenschneider Gymnasium in Würzburg, Germany

Publications

- F. Ante, U. Zschieschang, R.T. Weitz, D. Kälblein, K. Kern, and H. Klauk, "Low-voltage metal-gate top-contact organic thin-film transistors and complementary inverters with submicron channel length", *IEEE Device Research Conference Technical Digest*, pp. 179-180 (2009)
- U. Zschieschang, F. Ante, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Someya, K. Kern, and H. Klauk, „Flexible Low-Voltage Organic Transistors and Circuits Based on a High-Mobility Organic Semiconductor with Good Air Stability", *Advanced Materials*, vol. 22, no. 9, pp. 982-985 (2010)
- U. Kraft, U. Zschieschang, F. Ante, D. Kälblein, C. Kamella, K. Amsharov, M. Jansen, K. Kern, E. Weber, and H. Klauk, „Fluoroalkylphosphonic acid self-assembled monolayer gate dielectrics for threshold-voltage control in low-voltage organic thin-film transistors", *Journal of Materials Chemistry*, vol. 20, no. 31, pp. 6416-6418 (2010)
- U. Zschieschang, F. Ante, M. Schlörholz, M. Schmidt, and H. Klauk, „Mixed Self-Assembled Monolayer Gate Dielectrics for Continuous Threshold Voltage Control in Organic Transistors and Circuits", Advanced Materials, vol. 22, no. 40, pp. 4489-4493 (2010)
- F. Ante, F, Letzkus, J. Butschke, U. Zschieschang, J.N. Burghartz, K. Kern, and H. Klauk, "Top-contact organic transistors and complementary circuits fabricated using high-resolution silicon stencil masks" *IEEE Device Research Conference Technical Digest*, pp. 175-176 (2010)
- H. Ryu, D. Kälblein, R.T. Weitz, F. Ante, U. Zschieschang, K. Kern, O.G. Schmidt, and H. Klauk, „Dynamic characteristics of integrated circuits based on individual carbon nanotube transistors on glass substrates", *Nanotechnology*, vol. 21, no. 47, pp. 475207/1-5 (2010)
- F. Ante, F. Letzkus, J. Butschke, U. Zschieschang, K. Kern, J.N. Burghartz, and H. Klauk, „Submicron Low-Voltage Organic Transistors and Circuits Enabled by High-Resolution Silicon Stencil Masks", *IEEE International Electron Devices Meeting Technical Digest*, pp. 516-519 (2010)

- T. Zaki, F. Ante, U. Zschieschang, F. Letzkus, H. Richter, H. Klauk, and J. N. Burghartz, "A 3.3V 6b 100kS/s current-steering D/A converter using organic thin-film transistors on glass," *IEEE International Solid-State circuits Conference Technical Digest*, pp. 324-325 (2011)
- F. Ante, D. Kälblein, U. Zschieschang, T.W. Canzler, A. Werner, K. Takimiya, M. Ikeda, T. Sekitani, T. Someya, and H. Klauk, "Contact Doping and Ultra-Thin Gate Dielectrics for Nanoscale Organic Thin-Film Transistors", *Small*, accepted
- U. Zschieschang, F. Ante, D. Kälblein, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Someya, J. Blochwitz-Nimoth, K. Kern, and H. Klauk "Performance and Stability of Low-Voltage Organic Thin Film Transistors Based on Dinaphtho-Thieno-Thiophene (DNTT)", submitted
- F. Ante, T. Zaki, F. Letzkus, H. Richter, U. Zschieschang, J.N. Burghartz, and H. Klauk, "Scaling effects and dynamic performance of DNTT transistors", in preparation
- F. Ante, T.W. Canzler, J. Blochwitz-Nimoth, F. Letzkus, J.N. Burghartz, U. Zschieschang, and H. Klauk, "Molecular Contact Doping for Organic n-Channel TFTs and Fast Complementary Circuits", in preparation

Acknowledgments

I am thankful to Prof. Klaus Kern for supervising my thesis and giving me the possibility to receive my PhD degree from an outstanding university and to work at a renowned institute.

I am grateful to Dr. Hagen Klauk for giving me the opportunity to work on my PhD in his "Organic Electronics" group at the Max Planck Institute (MPI) for Solid State Research in Stuttgart. I experienced three very exciting years in a rapid developing field of technology. I also thank him for all the discussions, advises, and continuous supports during my thesis.

I thank Prof. Olivier Schneider, Prof. Jürgen Brugger, Prof. Alberto Morpurgo, and Dr. Hagen Klauk for being part of my PhD jury.

I would also like to acknowledge my colleagues Daniel Kälblein, Hyeyeon Ryu, Ulrike Kraft, and Thomas Egerer for the amicable atmosphere in our office. I will keep in mind many resolving scientific discussions and entertaining conversations. I also thank my "extended office colleagues" Bernhard Fenk and Wolfgang Winter for tolerating occasionally intense discussions.

My special thanks goes to Dr. Ute Zschieschang and Dr. Thomas Weitz for introducing me to the technical equipments in the clean room facilities. I also remember many clarifying discussions, experimental suggestions, and diverse social activities.

I acknowledge helpful technical support by Prof. Joachim Burghartz, Dr. Florian Letzkus, Dr. Harald Richter, Dr. Jörg Butschke, and Tarek Zaki from the Institut für Mikroelektronik, IMS CHIPS, Stuttgart.

I would like to thank Dr. Tobias Canzler, Dr. Ansgar Werner, and Dr. Jan Blochwitz-Nimoth at Novaled AG, Dresden, for useful comments concerning the experiments on doping the organic semiconductor.

I appreciated the continuous technical support in the clean room facilities by Ulrike Weizmann, Thomas Reindl, Marion Hagel, Achim Güth, and Wolfgang Winter, but also by the diverse Service Groups located at the Max Planck Institute. My special thank goes to Bernhard Fenk for the continuous work at the X-Beam system.

I thank Sabine Birtel for all the paperwork support during my work at the MPI and all

the people working in the Kern department, especially Dr. Stephan Rauschenbach and Thomas Dufaux, for their continuous attendance in providing equipment for electrical measurements.

I appreciated the invitations of Prof. Klaus von Klitzing to the annual group meeting at Ringberg Castle, but also the invitations to diverse social events such as the annual Christmas party.

I am grateful to Prof. Peter van Aken and Kersten Hahn for giving me the possibility to anaylze my samples in the transmission electron microscopy system. I am also thankful to Prof. Jens Pflaum and Nis Hauke Hansen for taking and discussing the x-ray diffraction measurements.

My thanks also goes to all people who were not directly involved into my scientific work, but who contributed to the success of my thesis. Especially I like to thank Björn Moller and Dr. Timm Lohmann. I also thank my home-zone friends in Würzburg which helped to spend some time without thinking of my work waiting at the MPI.

Finally, I am grateful to my parents and my brother Thorsten. My family significantly contributed to the success of my work and I thank them for the continuous support during my studies and during my PhD thesis.