# Field-Effect Transistors Based on ZnO Nanowires

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to my family and Conny

# Abstract

Semiconductor nanowires are an emerging class of materials with great potential for applications in future electronic devices. The small footprint and the large charge-carrier mobilities of nanowires make them potentially useful for applications with high-integration density, but also to replace thin-film transistors in large-area electronics. This thesis investigates the use of wet-chemically grown ZnO nanowires for the fabrication of high-performance, low-voltage field-effect transistors (FETs).

The first part of this thesis addresses the electrical characteristics of the wet-chemically grown ZnO nanowires. The as-grown ZnO nanowires are highly conductive due to a large charge-carrier concentration caused by dopants unintentionally incorporated into the ZnO nanowires during the synthesis. This large charge-carrier concentration makes it difficult to modulate the conductivity of the nanowires by an external electric field, so that the as-grown wires are not suitable for FETs. A post-growth annealing step is employed to dramatically reduce the charge-carrier concentration of the nanowires which makes it possible to fabricate FETs with useful characteristics. ZnO-nanowire FETs in a global back-gate geometry based on annealed ZnO nanowires have a transconductance of 300 nS, an on/off current ratio of $10^7$ and a subthrehold slope of 500 mV/decade. The maximum field-effect mobility of the annealed ZnO nanowires is around 50 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$. An important requirement to obtain good FET characterisitcs is to minimize the influence of the source and drain contact resistance on the total device resistance. The material used for the source and drain contacts in this thesis is aluminum. It is demonstrated that the use of a plasma treatment in the contact regions prior to the evaporation of the aluminum contacts can greatly influence the contact properties between ZnO and aluminum. An argon-plasma treatment locally increases the charge-carrier concentration in the ZnO. It is shown that the doping effect of the argon-plasma treatment can be exploited to reduce the contact resistance between alumiunm and ZnO and improve the electrical performance of the FETs.

In the second part of this thesis, the influence of the ambient air on the electrical characteristics of the ZnO-nanowire FETs is investigated. The electrical conductivity of the FETs is strongly affected by the distinct atmospheric conditions, which makes it difficult to obtain reliable FET characteristics. The potential of a self-assembled monolayer (SAM) based on fluoroalkylphosphonic acid molecules to passivate the ZnO nanowires against the undesirable effects of the ambient and to stabilize the electrical performance of ZnO-nanowire FETs is demonstrated. The stabilizing effect is attributed to the formation of a densely packed, hydrophobic SAM on the surface of ZnO and aluminum oxide. The quality of the hydrophobic SAMs is confirmed by means of water-contact-angle measurements on SAM-covered ZnO single crystals that show a contact angle of more than 110°.

The third part of this thesis is dedicated to the fabrication of high-performance ZnO-nanowire FETs with patterned metal top-gate electrodes. A top-gate fabrication process is developed that uses a very thin gate dielectric consisting only of an alkylphosphonic acid SAM that can be deposited from solution. The insulating quality of the SAM is investigated for top-gate FETs that utilize either gold or aluminum for the top-gate electrode. Gold top-gate FETs show a transconductance of 1 µS, an on/off current ratio of $10^7$, and a steep subthreshold slope of 90 mV/decade. The thin gate dielectric makes it possible to operate the gold top-gate FETs at low voltages of 1 V and simultaneously reduces the undesired gate current by more than three orders of magnitude compared to gold top-gate FETs that have been fabricated without a gate dielectric (MESFETs). The gate current of the gold top-gate FETs with SAM gate dielectric is as low as 1 pA for gate-source voltages between -1 V and 0.5 V. When aluminum is used for the top-gate electrode, a hybrid dielectric is formed at the interface between the SAM and the aluminum, consisting of the SAM and a spontaneously formed aluminum oxide layer. Owing to the hybrid gate dielectric, the aluminum top-gate FETs are operated with gate currents below 1 pA for voltages up to 3 V.

The top-gate fabrication process does not require temperatures above 160 °C, which makes it possible to fabricate FETs on unconventional substrates that cannot tolerate high temperatures, such as glass or flexible plastics. Integrated circuits on single ZnO nanowires that are fabricated on glass and plastic substrates are demonstrated. The maximum switching frequency of the inverters is 1 MHz.

## Keywords:

Semiconductor nanowire, zinc oxide, field-effect transistor, hydrothermal synthesis, passivation, self-assembled monolayer

# Zusammenfassung

Halbleiternanodrähte sind eine neuartige Materialklasse mit großem Potential für Anwendungen in zukünftigen elektronischen Bauelementen. Das geringe Volumen und die hohe Ladungsträgerbeweglichkeit sind vielversprechend für die Verwendung von Nanodrähten sowohl in elektronischen Bauelementen mit hoher Integrationsdichte (z.B. Mikroprozessoren) als auch in elektronischen Bauelementen mit niedriger Integrationsdichte, z.B. als Ersatz für Dünnfilmtransistoren in Aktiv-Matrix-Displays. Im Rahmen dieser Arbeit wird die Verwendung nasschemisch gewachsener Zinkoxid (ZnO) Nanodrähte zur Herstellung von hochleistungsfähigen Feldeffekttransistoren (FETs) untersucht.

Der ersten Teil dieser Arbeit widmet sich der Untersuchung der elektrischen Eigenschaften von nasschemisch synthetisierten ZnO Nanodrähten. Aufgrund von Dotanden, welche während der Synthese unbeabsichtigt in die Nanodrähte eingebaut werden, weisen die Nanodrähte ohne weitere Behandlung eine hohe Ladungsträgerkonzentration und dadurch eine hohe Leitfähigkeit auf. Diese hohe Ladungsträgerkonzentration erschwert die Modulation der Leitfähigkeit mittels eines externen elektrischen Feldes. Daher eignen sich die Drähte ohne weitere Behandlung nicht für die Herstellung von FETs. Durch nachträgliches Ausheizen ist es möglich, die Ladungsträgerkonzentration in den ZnO Nanodrähten drastisch zu verringern und FETs mit guter Strom-Spannungs-Charakterisitik herzustellen. Die so hergestellten FETs mit ausgeheizten ZnO Nanodrähten weisen einen Durchgangsleitwert von 300 nS, ein Strommodulation über sieben Größenordnungen, einen Unterschwellanstieg von 500 mV pro Dekade und eine Feldeffektbeweglichkeit von bis zu 50 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$ auf.

Um optimale Strom-Spannungs-Kennlinien zu erhalten, ist es wichtig, den Einfluss des Kontaktwiderstandes an den Source- und Drainkontakten auf den Gesamtwiderstand des Transistors zu minimieren. Zur Kontaktierung der Nanodrähte wird in dieser Arbeit Aluminium verwendet. Es wird gezeigt das die Kontaktqualität zwischen ZnO und Aluminium stark modifiziert werden kann, wenn die Kontaktfläche des Nanodrahtes vor der Verdampfung des Aluminiums einer Plasmabehandlung unterzogen wird. Die Ladungsträgerkonzentration in den Nanodrähten wird erhöht, wenn der Draht einer Argonplasmabehandlung ausgesetzt wird. Dieser Effekt wird ausgenutzt, um den Anteil des Kontaktwiderstandes zwischen ZnO und Aluminium am Gesamtwiderstand zu verringern und die Strom-Spannungs-Charakterisitik der FETs zu verbessern.

Im zweiten Teil der Arbeit wird die Atmosphärenabhängigkeit der Strom-Spannungs-Kennlinien der ZnO-Nanodraht FETs untersucht. Die elektrische Leitfähigkeit der Transistoren wird stark von der Atmosphäre beeinflusst, was eine verlässliche Charakterisierung der Transistorkennlinien kompliziert. Um den unerwünschten Einfluss der Atmosphäre zu verringern und die Transistorkennlinien zu stabilisieren, werden die ZnO Nanodrähte

unter Verwendung einer selbstorganisierenden Monolage basierend auf Fluoroalkylphosphonsäuremolekülen passiviert. Die stabilisierende Wirkung wird der Ausbildung einer dichtgepackten, hydrophoben selbstorganisierten Monolage auf der Oberfläche von ZnO und Aluminiumoxid zugeschrieben. Die hohe Qualität der hydrophoben Monolagen auf ZnO wird durch Messung eines Wasserkontaktwinkels von über 110° auf ZnO Einkristallen bestätigt.

Der dritte Teil der Arbeit befasst sich mit der Herstellung von hochleistungsfähigen ZnO Nanodraht FETs mit lokalen Metallsteuerelektroden. Im Rahmen des entwickelten Fabrikationsprozesses dient eine aus Lösung aufgebrachte selbstorganisierende Monolage aus Alkylphosphonsäuremolekülen zur Isolation der Metallsteuerelektroden. Die Steuerelektroden werden dabei von oben auf den ZnO Nanodraht aufgedampft (top-gate Elektrode) nachdem die Monolage auf den Draht aufgebracht wurde. Die isolierende Wirkung des dünnen Dielektrikums wird unter Verwendung von Metallsteuerelektroden aus Gold und Aluminium untersucht. FETs mit Goldsteuerelektrode weisen einen hohen Durchgangsleitwert von 1 µS, eine Strommodulation von über sieben Größenordnungen und einen steilen Unterschwellanstieg von 90 mV pro Dekade auf. Aufgrund des dünnen Dielektrikums ist es möglich, die FETs mit niedrigen Versorgunsspannungen (1 V) zu betreiben. Gleichzeitig wird der unerwünschte Leckstrom zwischen Steuerelektrode und ZnO Nanodraht um mehr als drei Größenordnungen reduziert, wie ein Vergleich mit ZnO Nanodraht FETs mit Goldsteuerelektrode ohne Dielektrikum (MESFETs) zeigt. Der Absolutwert des Leckstroms der FETs mit Goldsteuerelektrode und Dielektrikum bestehend aus einer selbstorganisierten Monolage liegt unterhalb von 1 pA für Versorgungsspannungen zwischen -1 V und 0.5 V. Wird Aluminium anstelle von Gold als Steuerelektrode verwendet, führt die Verwendung des Dielektrikums aus einer selbstorganiserten Monolage zur Bildung eines Hybriddielektrikums bestehend aus der selbstorganisierten Monolage und einer Aluminiumoxidschicht, die sich spontan an der Grenze zwischen Monolage und Aluminiumsteuerelektrode ausbildet. Aufgrund des Hybriddielektrikums können FETs mit Aluminiumsteuerelektrode mit Spannungen von bis zu 3 V betrieben werden, ohne das der unerwünschte Leckstrom einen Wert von 1 pA überschreitet.

Die Herstellung der Feldeffekttransitoren erfordert keine hohen Temperaturen ($T < 160°C$), weshalb es möglich ist, Transistoren auch auf Substraten herzustellen, die den Einsatz hoher Temperaturen nicht zulassen. Die Herstellung integrierter Schaltkreise an einzelnen ZnO Nanodrähten auf Glas- und Plastiksubstraten wird demonstriert. Für ZnO Nanodraht Inverter auf Glas wird eine maximale Schaltfrequenz von 1 MHz gemessen.

## Schlagworte:

Halbleiternanodraht, Zinkoxid, Feldeffekttransitor, hydrothermale Synthese, Passivation, selbstorganisierende Monolage

# Contents

# 1 Introduction

Over the past two decades the field of semiconductor nanowires has been one of the most active areas of research, with an exponentially increasing number of publications every year and more than 5500 publications in 2010 [1]. The growing interest is accompanied by an increasing number of techniques to manufacture nanowires from many different semiconductor material systems, such as silicon, gallium arsenide, or zinc oxide to name just a few. In general, these fabrication techniques can be divided into two different categories, the top-down approach and the bottom-up approach. In the top-down approach, high-resolution patterning techniques, such as electron-beam lithography [2], stencil-mask lithography [3], nano-imprint lithography [4], or superlattice nanowire pattern transfer [5], are utilized to define quasi-one-dimensional nanowires by etching from three-dimensional bulk semiconductors or by metal evaporation. In contrast, the bottom-up approach relies on the assembly of atomic or molecular building blocks to build up the desired nanostructures. The potential of the bottom-up approach is the possibility to control the growth of nanostructures with near-atomic precision and to fabricate nanomaterials with distinct chemical composition and structure, which may not be accessible with conventional top-down fabrication methods [6, 7]. Common bottom-up techniques for the synthesis of nanowires are vapor-liquid-solid growth [8, 9], vapor-solid growth [10], or wet-chemical growth [11]. Due to substantial progress in the control of nanowire synthesis, it is now possible to grow nanowires with controlled diameters and lengths [12], radial and axial nanowire heterostructures [13], and even nanowires with controlled kinks [14]. The high level of control of the nanowire growth and the unique properties emerging from the quasi-one-dimensional structure of the nanowires have opened many novel applications for nanowires. To give an example, the group of Charles Lieber at Harvard University recently demonstrated the recording of electrical signals from the inside of a living cell using a specifically tailored V-shaped silicon nanowire [15].

The more traditional field for the potential application of nanowires is their use as active components in field-effect transistors (FETs) in future integrated circuits, such as microprocessors and non-volatile memories. The small dimensions of nanowires are promising for the realization of novel device geometries, such as gate-all around FETs [16] or vertical FETs [17, 18]. Compared to planar devices, the nanowire geometry is expected to provide better current control and allow for higher integration densities [19].

Besides the use in high-integration-density applications, semiconducting nanowires are also potentially useful to realize high-performance FETs in large-area electronics, such as active-matrix displays [20] or sensor arrays, which require less complex circuitry and smaller FET densities. In state-of-the-art active-matrix displays thin-film transistors (TFTs) based on hydrogenated amorphous silicon or polycrystalline silicon are usually

utilized to control the individual pixels. However, the processing of these materials typically requires temperatures above 300°C, which prevents their use on unconventional substrates, such as plastics or paper. Flexible polymeric substrates usually have a glass transition temperature below 200°C, so that semiconductors that can be processed at lower temperatures are required for the fabrication of large-area electronics on flexible substrates. Materials that are potentially useful for the fabrication of FETs on flexible substrates are organic semiconductors [21], amorphous metal-oxides [22] and also single-crystalline nanowires [23].

Although the synthesis of single-crystalline nanowires often requires temperatures above 200°C, the nanowires can be grown on a substrate that can tolerate these high temperatures and then be transferred to the target substrate for FET assembly. As long as the temperature during FET manufacturing is below the glass transition temperature of the substrate, FETs based on semiconducting nanowires can be realized on polymeric substrates. Compared to TFTs based on organic semiconductors and amorphous metal-oxides, the larger charge-carrier mobilities of single-crystalline nanowires make it possible to reduce the lateral dimensions of the FETs while providing the same current. This is especially beneficial for display applications, since the area consumption of the FET restricts the size of the pixel emitter and hence reduces the aperture ratio. A first successful demonstration of an active-matrix OLED display fully operated by FETs based on indium oxide nanowires was done by Ju et al. [20] in 2008.

The aim of this thesis is the development of high-performance, low-voltage, top-gate FETs based on single-crystalline ZnO nanowires that can be fabricated at low temperatures and can thus be implemented on flexible substrates. The use of an ultrathin self-assembled monolayer (SAM) of an aklylphosphonic acid as the gate-dielectric layer is investigated. Gate dielectrics based on SAMs are popular in the field of organic electronics and have shown low defect density, excellent insulating properties and large capacitances. However, their use for FETs based on inorganic semiconductors is much less investigated. The ZnO nanowires utilized in this thesis are grown via a wet-chemical (hydrothermal) synthesis. Since there are only a few reports on the use of hydrothermally grown ZnO nanowires for FETs, a detailed investigation of the electronic properties of the synthesized ZnO nanowires is performed. Furthermore, the optimizaion of the electrical properties with regard to the application in FETs is investigated.

This thesis is organized as follows. In chapter 2 a brief introduction to the material system ZnO is given, followed by a section about the theory of field-effect transistors (FETs). Within the theory section the focus is placed on the description of the current-voltage characteristics of FETs in different operation regimes. In chapter 3, different methods for the synthesis of semiconducting nanowires are summarized, and the hydrothermal synthesis employed for the growth of ZnO nanowires in the framework of this thesis is

briefly introduced. The electrical characteristics of the wet-chemically synthesized ZnO nanowires in a global back-gate FET configuration are investigated in the chapters 4-6. Starting from the as-grown ZnO nanowires, the improvement of the electrical properties with regard to the application in FETs is investigated. The effect of post-growth annealing treamtments, plasma treatments and temperature on the electrical properties of the ZnO-nanowire FETs are studied. In chapter 7 the influence of the ambient on the performance of ZnO-nanowire FETs is investigated. The ability of a self-assembled monolayer (SAM) based on fluoroalkylphosphonic acid molecules to stabilize the FET performance is investigated. A novel fabrication method for top-gate FETs based on ZnO nanowires that utilize a SAM as the gate dielectric is presented in chapter 8. The insulating properties of the SAM gate dielectric are analyzed for ZnO-nanowire FETs with gold top-gate electrodes and aluminum top-gate electrodes. Finally, in chapter 9 the fabrication of integrated circuts based on the top-gate process is presented and their dynamic performance is investigated.

# 2 Material ZnO and theory of field-effect transistors

## 2.1 Material system zinc oxide

ZnO is one of the most prominent II-VI compound semiconductors and has been investigated since the early 1930's [24, 25]. Within the last few years, a growing interest in the material system has been observed arising from the possibilities to grow high-quality ZnO single-crystals and ZnO nanostructures, which raise hope for applications in various fields.

ZnO is a wide-band-gap semiconductor with a direct gap of $E_G \sim 3.4$ eV at room temperature. It preferentially crystallizes in the hexagonal wurzite-type structure (see figure 2.1) which is the stable phase of ZnO at room temperature. Along the hexagonal c-axis, adjacent polar lattice planes of zinc and oxygen are found. Every oxygen atom is surrounded tetrahedrally by four zinc atoms and vice versa. Zinc-blende and rock-salt phases also exist, but these phases are only stable under high pressure. The bonding between adjacent atoms of zinc oxide is found to be covalent, but with a partial ionic bonding component. Due to the partially ionic bonding and the lack of an inversion center, ZnO is a piezoelectric material [26].

The current interest in ZnO involves research in many different areas and each of them is motivated with regard to different applications. In the following some of the most important current areas of research on ZnO are listed:

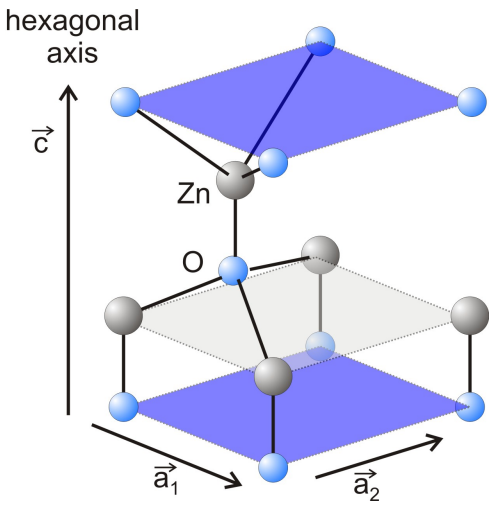


Figure 2.1: **Primitive unit cell of the crystal structure of wurzite-type ZnO.** The base plane is defined by the primitive translation vectors $\vec{a}_1$ and $\vec{a}_2$, and the c-axis is orthogonal to the base plane. Every unit cell contains two zinc and two oxygen atoms. Each of the two individual atom types form a sublattice which is hexagonally close-packed. Along the c-axis adjacent polar lattice planes of zinc and oxygen are found.

- Transparent electronics: The large band gap and the possibility to easily introduce large amounts of n-type dopants into ZnO (see chapter 4) make ZnO an attractive material for the fabrication of transparent conductors or transparent field-effect transistors [27].
- Blue/UV optoelectronics: ZnO is investigated in order to obtain a material for the fabrication of light-emitting diodes (LEDs) or laser diodes covering the blue and UV spectral range. The modulation of the band gap of ZnO over a broad range of 3-4 eV has been successfully demonstrated by alloying with magnesium and cadmium [24]. However, the main problem for these applications is the need for stable, reproducible p-type doping of ZnO, which has not been achieved so far.
- Photovoltaics: ZnO nanoparticles and nanowire arrays are investigated for the use as an electron transport layer in dye-sensitized solar cells [28, 29].
- Diluted ferromagnets: The doping of ZnO with magnetic impurities, like manganese, cobalt, or nickel is investigated in order to obtain a transparent room-temperature ferromagnet.
- Biosensing: ZnO is a non-toxic, environmentally friendly material, which is a distinct advantage compared to many other materials that can be utilized for the synthesis of semiconducting nanostructures (e.g. CdSe, carbon nanotubes), since it also permits to employ ZnO based devices for biosensing applications.

## 2.2 Fundamentals of field-effect transistors

### 2.2.1 Introduction

The term "transistor" originates from the combination of the two words "**trans**fer" and "res**istor**". In a transistor the resistance between two terminals can be transferred or controlled by a third terminal. In a bipolar transistor, the current between two terminals (collector and emitter) can be controlled by the usually much smaller current at the third terminal (the base). All three terminals are directly connected via a semiconductor. The first realization of a bipolar transistor was performed by Bardeen, Brattain and Shockley [30, 31] in 1947.

A different approach to realize a transistor was proposed already in 1925 by Lilienfeld [32]. In a so-called field-effect transistor (FET), the current flow between two terminals is monitored by the electric field from the third terminal. In contrast to the bipolar transistor, the third terminal is capacitevly coupled and is not in direct contact with the semiconductor. The first metal-oxide-semiconductor FET (MOSFET) was demonstrated by Kahng and Atalla in 1960 [33]. Figure 2.2 shows the schematic structure of a MOS-

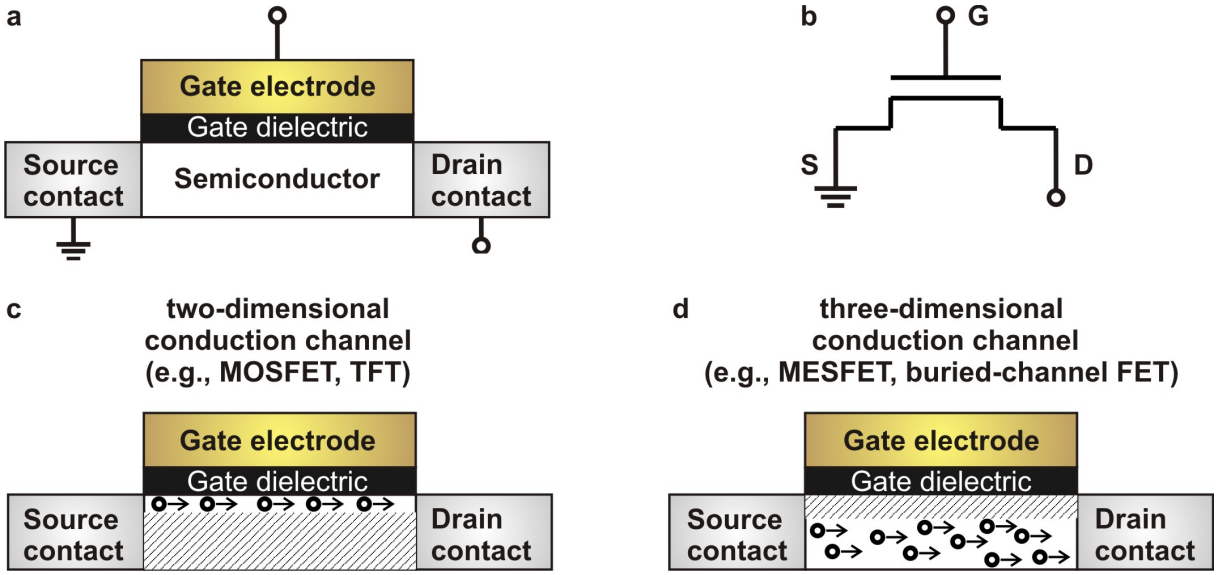


Figure 2.2: **Schematic of a field-effect transistor.**
(a) Schematic structure and (b) circuit diagram of a field-effect transistor. Two terminals (source and drain contacts) are in direct contact with the semiconductor, while a third terminal (gate electrode) is coupled capacitively to the semiconductor via the gate dielectric. The electric field from the gate electrode is utilized to monitor the current in the semiconductor flowing from the source contact to the drain contact. (c) Schematic of an FET with a 2D conduction channel (e.g. MOSFET). The drain current is modulated by varying the density of charge carriers in the 2D conduction channel. (d) Schematic of an FET with a 3D conduction channel. The drain current is modulated by varying the thickness of the conduction channel in the semiconductor.

FET. The three terminals in the MOSFET structure are labeled source, drain and gate. The source contact and the drain contact are connected via a semiconductor. The gate electrode is separated from the semiconductor by an electrically insulating gate-dielectric layer. Therefore, the gate electrode couples capacitively to the semiconductor and controls the electrostatic potential at the semiconductor/insulator interface. The MOSFET is the most common type of FET, but there are also other versions of FETs, i.e. thin film transistors (TFTs) or metal-semiconductor FETs (MESFETs).

There are several possibilities to categorize FETs. For instance, dependent on the type of majority charge carriers in the semiconductor, FETs are specified as n-channel devices when electrons are the majority charge carriers or as p-channel devices when holes are the majority charge carriers. Another possibility to categorize FETs is to classify them by the dimensionality of the conducting channel in the semiconductor. In MOSFETs and TFTs the charge carriers are confined to a two-dimensional charge sheet (2D conduction channel) next to the semiconductor/insulator interface (figure 2.2c). The bulk of the semiconductor is not conductive and the drain current is modulated by varying the density of charge carriers in the 2D conduction channel. In MESFETs or buried-channel MOSFETs

the whole semiconductor bulk is conductive (3D conduction channel), and therefore the whole semiconductor cross-section accounts for the drain current (figure 2.2d). The drain current is modulated by varying the thickness of the conduction channel in the semiconductor. Since both, surface and bulk conduction, are expected to contribute to the drain current of the FETs investigated in this thesis, a more detailed analysis of the different conduction mechanisms and their influence on the transistor characteristics is presented in the following sections.

### 2.2.2 Basic FET working principle

In an FET the drain current is modulated by varying the electric potentials applied to the three different terminals. The conductivity of the semiconductor is modulated by the gate-source voltage $V_{GS}$ and the drain-source voltage $V_{DS}$. According to the Drude model, the current along the semiconducting channel (drain current $I_D$) is given by:

$$I_D = \frac{A}{L} \cdot n \cdot \mu \cdot q \cdot V_{DS}, \tag{2.1}$$

with the cross-section area of the conducting channel A, the channel length L (the distance between source and drain contact), the charge-carrier mobility $\mu$, the elementary charge $q$, and the concentration of free charge carriers $n$. In an ideal FET the only parameter in equation 2.1 that depends on $V_{GS}$ is the concentration of free charge carriers $n$. The channel cross section of an FET consists of the metal gate electrode (M), the insulating gate dielectric (I) and the semiconductor (S) and therefore resembles a MIS capacitor. A schematic representation of a MIS capacitor in accordance with the band theory of solids is depicted in figure 2.3. The concentration of free charge carriers in the semiconductor depends exponentially on the energetic difference between the conduction-band edge $E_{CB}$ and the Fermi level $E_F$:

$$n = N_C \cdot \exp\left(-\frac{E_{CB} - E_F}{k_B T}\right) = N_C \cdot \exp\left(-\frac{E_{CB} - (\mu_{ch} + q \cdot \phi)}{k_B T}\right) = n_0 \cdot \exp\left(\frac{q \cdot \phi}{k_B T}\right), \tag{2.2}$$

with the density of states in the conduction band $N_C$, the energy of the conduction-band edge $E_{CB}$, the temperature T, the Boltzmann constant $k_B$, and the concentration of free charge carriers in the semiconductor $n_0$ obtained for $\phi = 0$. The Fermi level is determined by the sum of the chemical potential of the semiconducting material $\mu_{ch}$ and the electrostatic potential $q \cdot \phi$. Under the assumption of a perfect, single-crystalline semiconductor, the number of holes equals the number of electrons and the Fermi level will be positioned approximately in the middle of the band gap between the conduction band and the valence band. Such a semiconductor is commonly referred to as an intrinsic semiconductor. Typical values for the band gap in semiconductors are a few eV (e.g.

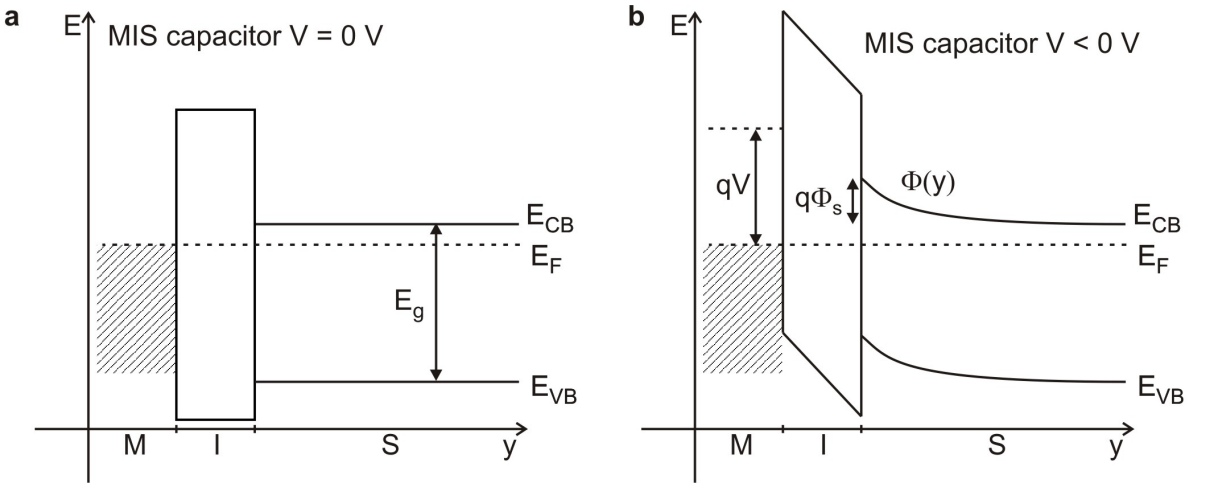


Figure 2.3: **Schematic band diagram of a Metal-Insulator-Semiconductor (MIS) structure.**
(a) MIS structure in thermal equilibrium, with the conduction-band edge $E_{CB}$, the valence-band edge $E_{VB}$, the band gap of the semiconductor $E_G$, and the Fermi level $E_F$. (b) Under application of an external voltage V, the electrostatic potential at the semiconductor/insulator interface $\phi_S$ is changed. For a negative potential, the bands in the semiconductor are bent upwards and electrons are repelled from the interface.

GaAs $\sim$ 1.55 eV, InP $\sim$ 1.34 eV [34]). As a consequence, the concentration of free charge carriers in intrinsic semiconductors is usually low ($\sim 10^9\,\mathrm{cm}^{-3}$) and thus intrinsic semiconductors are rather poor conductors. To modulate the density of free charge carriers and hence modulate the conductivity, one can either change the chemical potential of the material by the introduction of impurity atoms (i.e. doping of the semiconductor) and/or locally change the electrostatic potential in the semiconductor. The latter mechanism is utilized in an FET by applying a voltage $V_{GS}$ between the gate electrode and the source contact. A more detailed analysis of the potential change in the semiconductor by applying $V_{GS}$ is presented in the following.

### 2.2.3 Metal-Insulator-Semiconductor capacitor

The semiconductor employed in this thesis is ZnO. Due to the large band gap of ZnO ($E_G \sim 3.4\,\mathrm{eV}$) the intrinsic charge-carrier concentration is expected to be very low. However, a certain amount of unintentionally incorporated impurities are usually present in ZnO, and these impurities donate electrons to the semiconductor [26]. Therefore, ZnO usually displays n-type conductivity, and thus the following discussion will focus on a MIS structure with an n-type semiconductor.

When an external voltage V is applied between the metal and the semiconductor, the applied voltage drops across the insulator and the semiconductor. Consequently, the electrostatic potential at the semiconductor surface $\phi_S$ is changed from its equilibrium

value. The potential drop across the semiconductor is a function of y, with the boundary conditions $\phi(\infty) \rightarrow 0$ far away from the surface and $\phi(0) = \phi_S$ at the surface. The relation between the potential $\phi(\mathrm{y})$ and the charge density $\rho$ is given by the Poisson equation:

$$\frac{\partial^2 \phi(\mathrm{y})}{\partial \mathrm{y}^2} = -\frac{\rho(\mathrm{y})}{\varepsilon_s \varepsilon_0}, \tag{2.3}$$

with the semiconductor permittivity $\varepsilon_s$ and the vacuum permittivity $\varepsilon_0$. For a doped semiconductor at room temperature, it can be assumed that all donors have donated their excess electrons to the conduction band and are thus in an ionized state. Further, for a wide-band-gap semiconductor the number of free charge carriers obtained from dopants exceeds the number of intrinsic charge carriers generated by thermal excitations. Hence, the concentration of free electrons $n_0$ in the n-doped (p-doped) semiconductor is given by the number of ionized dopants and $n_0 = \mathrm{N_D^+}$ $\left(p_0 = \mathrm{N_A^-}\right)$. The total charge in a doped semiconductor consists of the free charge carriers and the ionized dopants:

$$\rho(\mathrm{y}) = q \cdot (p(\mathrm{y}) - n(\mathrm{y}) - \mathrm{N_A^-} + \mathrm{N_D^+}). \tag{2.4}$$

With the help of equation 2.2, the Poisson equation then reads:

$$\frac{\partial^2 \phi(\mathrm{y})}{\partial \mathrm{y}^2} = -\frac{q}{\varepsilon_s \cdot \varepsilon_0} \cdot \left( p_0 \cdot (\exp\left(\frac{-q \cdot \phi(\mathrm{y})}{\mathrm{k_B T}}\right) - 1) - n_0 \cdot (\exp\left(\frac{q \cdot \phi(\mathrm{y})}{\mathrm{k_B T}}\right) - 1) \right). \tag{2.5}$$

By integrating equation 2.5 over the potential $\phi(\mathrm{y})$ from the semiconductor bulk to the semiconductor surface the space charge per unit area (surface-charge density) $Q_S$ can be calculated. The integration of the left-hand side yields:

$$\int_0^{\phi_S} \frac{\partial^2 \phi(\mathrm{y})}{\partial \mathrm{y}^2} d\phi = \frac{1}{2} E_S^2 \quad \text{since} \quad \frac{d\phi}{dy} = -E(\mathrm{y}), \tag{2.6}$$

with the electric field at the surface $E_S$ generated by $Q_S$. With the help of Gauss's law $\nabla E = \frac{\rho}{\varepsilon_S \cdot \varepsilon_0}$, the surface-charge density is given by $Q_S = \varepsilon_S \cdot \varepsilon_0 \cdot E_S$ . By integrating over the right-hand side of equation 2.5 this results in

$$Q_S(\phi_S) = \mp \sqrt{2 \cdot \varepsilon_S \cdot \varepsilon_0 \cdot \mathrm{k_B} \cdot \mathrm{T}}$$

$$\cdot \sqrt{\left[ p_0 \cdot \left( \exp\left(\frac{-q \cdot \phi_S}{\mathrm{k_B} \cdot \mathrm{T}}\right) + \frac{q \cdot \phi_S}{\mathrm{k_B} \cdot \mathrm{T}} - 1 \right) - n_0 \cdot \left( \exp\left(\frac{q \cdot \phi_S}{\mathrm{k_B} \cdot \mathrm{T}}\right) - \frac{q \cdot \phi_S}{\mathrm{k_B} \cdot \mathrm{T}} - 1 \right) \right]}. \tag{2.7}$$

Figure 2.4 shows a plot of the surface-charge density $Q_S$ as a function of the surface potential $\phi_S$ for an n-type semiconductor with $\varepsilon_S = 9$, $\mathrm{T} = 300\,\mathrm{K}$, $n_0 = 10^{17}\,\mathrm{cm^{-3}}$, and $p_0 = 10^{10}\,\mathrm{cm^{-3}}$. As can be seen, $Q_S$ shows a strong dependence on the surface potential. For $\phi_S = 0$ the surface-charge density is zero, which is commonly referred to

as the flat-band condition. It is important to remark that zero surface-charge density does not necessarily correspond to zero conductivity of the semiconductor. For a doped semiconductor, zero surface-charge density is established when the free charge carriers compensate the charge of the ionized dopants. Depending on the doping concentration, the semiconductor bulk can be highly conductive at this point, since the concentration of free charge carriers is given by $n_0$ ($p_0$).

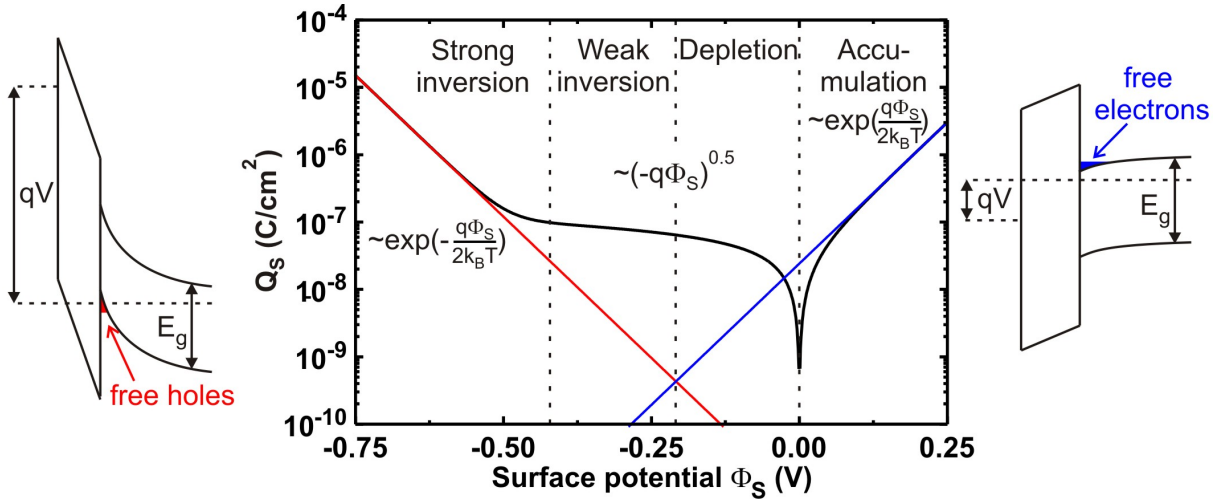


Figure 2.4: **Different regimes of the surface-charge density in an n-type semiconductor.**
Total surface-charge density (black), electron surface-charge density (blue) and hole surface-charge density (red) as a function of the surface potential at the semiconductor/insulator interface. Four different regimes can be identified. In the accumulation regime ($\phi_s > 0$) the electron concentration at the surface of the semiconductor increases exponentially with $\phi_S$. The schematic band diagram on the right of the graph shows the corresponding band bending. In the depletion/weak inversion regimes ($-2(\mathrm{E_F} - \mathrm{E_i}) < \phi_S < 0$), the surface-charge density is dominated by the charge of ionized dopants and follows a square-root relationship. The intersection of the electron and hole surface-charge densities indicates the transition from depletion to weak inversion. For the strong inversion regime ($\phi_S < -2(\mathrm{E_F} - \mathrm{E_i})$), the hole surface-charge density becomes dominant, and the total surface-charge density increases exponentially with $\phi_S$. The schematic on the left shows the band diagram in strong inversion regime.

In figure 2.4, four different regimes for the dependence of the surface-charge density on the surface potential can be identified. These are the accumulation regime, the depletion regime, the weak inversion regime, and the strong inversion regime.

### Accumulation regime

In the accumulation regime ($\phi_S > 0$), the last term of equation 2.7 dominates. The bands in the semiconductor are bent downwards and therefore free electrons are accumulated at

the semiconductor/insulator interface. The schematic band diagram is shown on the right-hand side of figure 2.4. The surface-charge density $Q_S$ is proportional to $\exp\left(\frac{q\cdot\phi_S}{2\cdot k_B\cdot T}\right)$. This is the regime in which thin-film transistors are typically operated.

### Depletion regime

The depletion regime is found for negative surface potential $-2\,(E_F - E_i) < \phi_S < 0$). $E_F - E_i$ is the energetic difference between the Fermi level and the middle of the band gap $E_i$. The bands in the semiconductor are bent slightly upwards and free electrons are repelled from the interface, leaving behind the ionized dopants (positively charged donors in the case of an n-type semiconductor). The surface-charge density in this regime increases with $\phi_S$ like $Q_S \sim \sqrt{-\phi_S}$. Figure 2.4 also shows the surface-charge density of electrons (blue) and holes (red) located at the semiconductor/insulator interface. The density of free charges at the interface is much smaller than the total surface-charge density. This shows that in this regime $Q_S$ emerges from the localized, ionized dopants in the doped semiconductor. This is important for the calculation of the drain current in the depletion regime (see section 2.2.7), since the actual surface-charge density is caused by immobile charges and therefore does not contribute to the drain current. When $\phi_S$ becomes even more negative the electron and hole densities at the surface become equal: $p_0 \cdot \exp\left(\frac{-q\cdot\phi_S}{k_B\cdot T}\right) = n_0 \cdot \exp\left(\frac{q\cdot\phi_S}{k_B\cdot T}\right)$. From this point on the operation regime is called weak inversion, but the relation between $Q_S$ and $\phi_S$ remains the same.

### Strong inversion regime

The onset of the strong inversion regime is identified for an even more negative surface potential $\phi_S < -2(E_F - E_i)$. The schematic band diagram for the strong inversion regime is shown on the left-hand side of figure 2.4. The surface-charge density is dominated by holes accumulated at the semiconductor/insulator interface, and the hole density at the interface is larger than the intrinsic electron density $n_0$. Equation 2.7 is dominated by the first term and $Q_S \sim \exp\left(\frac{-q\cdot\phi_S}{2\cdot k_B\cdot T}\right)$. The dependence of the surface-charge density on the surface potential is identical to the accumulation regime. The inversion regime is important, because state-of-the-art single-crystalline silicon MOSFETs are operated in this regime.

The FETs based on single-crystalline ZnO nanowires investigated in this thesis are operated in the accumulation regime as well as in the depletion regime. Due to the large band gap of 3.4 eV and the background n-type doping present in the material system, a large change of the surface potential would be required to access the inversion regime, which is difficult to realize under practical conditions.

### 2.2.4 Drain-current calculation

The modulation of the surface-charge density by $V_{GS}$ is the backbone of every FET operation and is well described by the MIS structure presented in the previous section. However, in order to derive the complete current-voltage characteristics of an FET, the potential drop between the drain and the source contact $V_{DS}$ has to be taken into account as well (see equation 2.1). In the so-called gradual-channel approximation [35] it is assumed that the longitudinal electric field from drain to source ($E_x$) is much smaller than the transverse electric field ($E_y$) between gate and source. This implies that the transverse electric field remains constant, and the same equations as derived in section 2.2.3 can be used to calculate $Q_S$ along the channel. The influence of the potential difference between the drain and the source contact $V_{DS}$ is accounted for by introducing an additional potential $\phi_{DS}(x)$ into the surface potential in equation (2.3) ($\phi(y) \rightarrow \phi(y) - \phi_{DS}(x)$). Under the assumption that $V_{DS}$ drops linearly along the channel, the drain current can then be calculated by:

$$I_D = \frac{W}{L} \int_0^L \mid Q_S(x) \mid v(x) dx, \tag{2.8}$$

with the width of the semiconductor W and the charge-carrier velocity along the channel v(x). Assuming a constant mobility along the semiconductor, $v(x) = \mu \cdot E(x) = \mu \frac{d\phi_{DS}}{dx}$ and equation 2.8 turns into:

$$I_D = \frac{W}{L} \mu \int_0^{V_{DS}} \mid Q_S(\phi_{DS}, \phi_S) \mid d\phi_{DS}. \tag{2.9}$$

For general values of $\phi_{DS}$ and $\phi_S$, equation 2.9 has no analytical solution and can only be solved numerically. However, since the relation between $Q_S$ and the surface potential can be simplified within the different operation regimes introduced in the preceding section, an analytical solution for 2.9 can be found [36].

### 2.2.5 FET characteristics in the accumulation regime

In the accumulation regime $Q_S$ is dominated by the exponential relation between the concentration of free electrons at the semiconductor/insulator interface and the surface potential. The contribution of free holes and ionized dopants can be neglected and equation 2.7 can be expressed by:

$$Q_S(\phi_S, \phi_{DS}) = \mp \sqrt{2 \varepsilon_S \varepsilon_0 k_B T} \cdot \sqrt{\left[ n_0 \cdot \left( \exp\left( \frac{q(\phi_S - \phi_{DS})}{k_B T} \right) - \exp\left( -\frac{q \phi_{DS}}{k_B T} \right) \right) \right]} \tag{2.10}$$

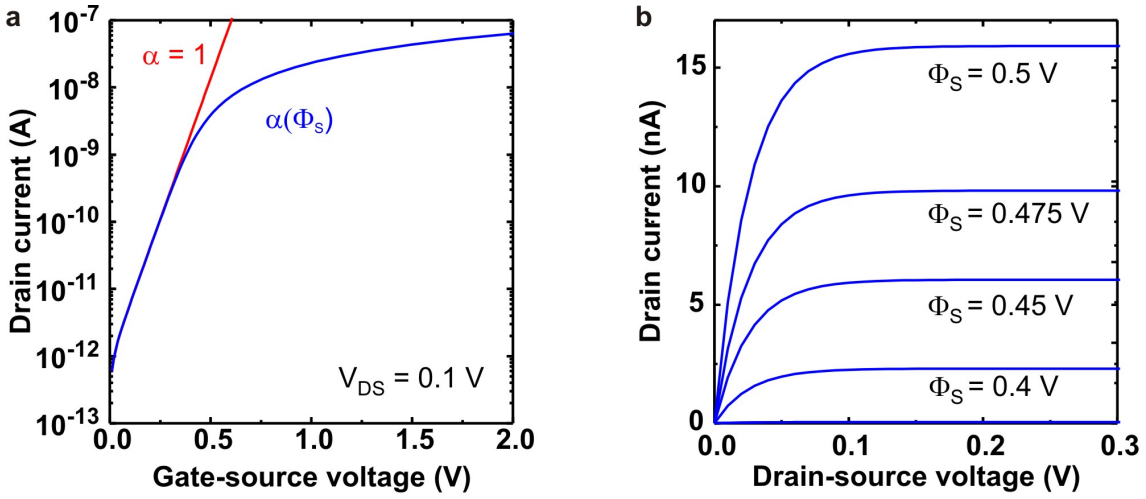


Figure 2.5: **Simulated transfer and output characteristics of an FET in the accumulation regime.**
(a) Simulated transfer characteristics for an FET in the accumulation regime based on equation 2.11 ($\mu = 50\ \frac{\mathrm{cm}^2}{\mathrm{Vs}}$, W = 50 nm, L = 1 µm, $\varepsilon_S = 9$, T = 300 K, $\mathrm{n_0} = 10^{10}\,\mathrm{cm}^{-3}$), under the assumption of a linear relationship between $\mathrm{V_{GS}}$ and $\phi_S$ (red curve, $\alpha = 1$), and after the introduction of the voltage-dependent gate-coupling factor ($\alpha(\phi_S) \sim \frac{1}{1+\exp(\phi_S/2)}$) (blue curve). (b) Simulated output characteristics for different surface potentials.

The drain current is calculated by integration of $Q_S$ according to equation 2.9:

$$\mathrm{I_D}(\mathrm{V_{DS}}, \phi_S) = \mu \frac{\mathrm{W}}{\mathrm{L}} \sqrt{2\varepsilon_S \varepsilon_0 \mathrm{k_B T} n_0} \cdot \frac{2\mathrm{k_B T}}{\mathrm{q}} \cdot \left(1 - \exp \frac{-q\mathrm{V_{DS}}}{2\mathrm{k_B T}}\right) \sqrt{\left[\left(\exp\left(\frac{q(\phi_S)}{\mathrm{k_B T}}\right) - 1\right)\right]} \tag{2.11}$$

Equation 2.11 describes the dependence of the drain current on the surface potential $\phi_S$ and $\mathrm{V_{DS}}$. As already stated above, the modulation of the surface potential $\phi_S$ in an FET is accomplished by changing $\mathrm{V_{GS}}$. However, since the coupling between the gate electrode and the semiconductor channel occurs in a capacitive manner via the gate insulator, the relationship between $\mathrm{V_{GS}}$ and $\phi_S$ can be complicated. To account for this complicated relation, the so-called gate-coupling factor $\alpha(\phi_S)$ [37] is introduced into equation 2.11 and $\phi_S \rightarrow \alpha(\phi_S) \cdot \mathrm{V_{GS}}$. The influence of the gate-coupling factor is described in the following.

### Transfer and output characteristics of an FET

A complete electrical characterization of an FET requires the measurement of the dependencies of the drain current on both, the gate-source voltage and the drain-source voltage. These dependencies are measured in the so-called **transfer** and **output** characteristics of the FET.

### Transfer characteristics: Relation between $I_D$ and $V_{GS}$ for constant $V_{DS}$

The transfer characteristics show the drain current as a function of the gate-source voltage for a constant drain-source voltage (figure 2.5a). For constant $V_{DS}$ the drain current according to equation 2.11 can be approximated as $I_D \sim \text{const}(V_{DS}) \cdot \sqrt{\left(\exp \frac{q\alpha(\phi_S)(V_{GS})}{k_B T} - 1\right)}$. Therefore, the drain current is expected to increase exponentially with increasing $V_{GS}$ for $\alpha(\phi_S) = 1$ (see red curve in figure 2.5a). In a real FET, this exponential dependency is only observed in a limited gate-source voltage range immediately after the onset of the drain current (see blue curve in figure 2.5a). The steep exponential drain-current increase transfers into a quadratic and finally a linear increase for larger $V_{GS}$. The reason for the deviation between equation 2.11 and the experiment is caused by a decrease of the previously introduced gate-coupling factor $\alpha(\phi_S)$ for larger $V_{GS}$. This decrease can be understood in the picture of the MIS capacitor introduced in section 2.2.3. Within this picture, the capacitance of the insulator $C_I$ is connected in series to the capacitance of the semiconductor $C_S$ caused by the induced charge distribution. Hence, the gate-source voltage drop across the two capacitors is described by:

$$\frac{V_{GS} - \phi_S}{\phi_S} = \frac{C_S(\phi_S)}{C_I} \rightarrow \phi_S = \frac{C_I}{C_S(\phi_S) + C_I} V_{GS} \tag{2.12}$$

Since the charge distribution within the semiconductor depends on $\phi_S$, the associated capacitance $C_S(\phi_S)$ also depends on $\phi_S$. In a simplified picture, $C_S(\phi_S)$ can be thought of as a parallel-plate capacitor with a thickness equal to the thickness of the charge sheet induced at the semiconductor surface. An estimate of this thickness is given by the Debye length of the semiconductor which gives a measure of the distance over which potential fluctuations are screened inside a semiconductor. The Debye length depends on the surface-charge density like $\sim Q_S^{-1}$. Together with equation 2.10, the relationship between the gate-coupling factor and the surface potential is then given by: $\alpha(\phi_S) \sim \frac{1}{1+\exp(\phi_S/2)}$. For larger values of $\phi_S$ , the exponential term dominates and $\alpha(\phi_S)$ decreases below unity. Consequently the increase of $\phi_S$ with $V_{GS}$ is attenuated and the drain current behaves as shown in figure 2.5a (blue curve).

### Output characteristics: Relation between $I_D$ and $V_{DS}$ for constant $V_{GS}$

The output characteristics show the drain current as a function of the drain-source voltage for a constant gate-source voltage (figure 2.5b). Two different operation regions can be identified from figure 2.5b, the linear region of operation and the saturation region of operation.

For a constant value of $V_{GS}$, the drain current obtained from equation 2.11 is given by:

$$I_D \sim \text{const}(V_{GS}) \cdot \left(1 - \exp \frac{-qV_{DS}}{2k_BT}\right). \tag{2.13}$$

For small $V_{DS}$, the exponential function can be approximated as: $\exp(\frac{-qV_{DS}}{k_BT}) \sim 1 - \frac{-qV_{DS}}{k_BT}$. As a consequence, the drain current shows a linear increase with $V_{DS}$, and this region is referred to as the **linear region of operation**.

For larger $V_{DS}$, the potential at the drain contact levels with the surface potential. Thus, no more charge carriers are accumulated at the position of the drain contact and the conducting channel from source to drain is interrupted. This effect is called pinch-off and leads to a saturation of the drain current for large $V_{DS}$. This region is referred to as the **saturation region of operation**.

### Simplified description (charge-sheet approximation)

Although equation 2.11 can be used to derive the correct transistor characteristics, the calculation of the drain current and its dependence on the material parameters ($\varepsilon_S$, $\mu$) and device parameters (W, L, $C_I$) is rather complex, especially for large charge-carrier densities. A simplified description of the relationship between $I_D$, $V_{GS}$ and $V_{DS}$ is given by the so-called charge-sheet approximation. Within this approximation, important FET parameters and their influence on the drain current can be extracted more easily.

Within the charge-sheet approximation it is assumed that the gate-source voltage drops entirely across the gate insulator. According to the considerations outlined in the previous section, this refers to the situation for large $V_{GS}$ when $C_S(\phi_S) \gg C_I$ and the gate-coupling factor $\alpha(\phi_S)$ deviates from unity. Hence, the charge-sheet model is expected to be a good approximation when the relation between the drain current and $V_{GS}$ deviates from the exponential behavior. Within the charge-sheet model, the accumulated surface-charge density in the semiconductor can be expressed by:

$$Q_S = C_i(V_{GS} - V_{FB} - \phi_{DS}), \tag{2.14}$$

with the capacitance per unit area $C_i = \frac{C_I}{L \cdot W}$. Integrating the surface-charge density according to equation 2.9 from source to drain yields the drain current:

$$I_D(V_{GS}, V_{DS}) = \frac{\mu C_I}{L^2}(V_{GS} - V_{FB} - \frac{V_{DS}}{2})V_{DS}, \tag{2.15}$$

with the flat-band voltage $V_{FB}$ which is introduced to account for a non-zero surface-charge density at $V_{GS} = 0\,V$. The charge-sheet model is capable of describing the transfer and output characteristics of an FET in the accumulation regime over a wide range of

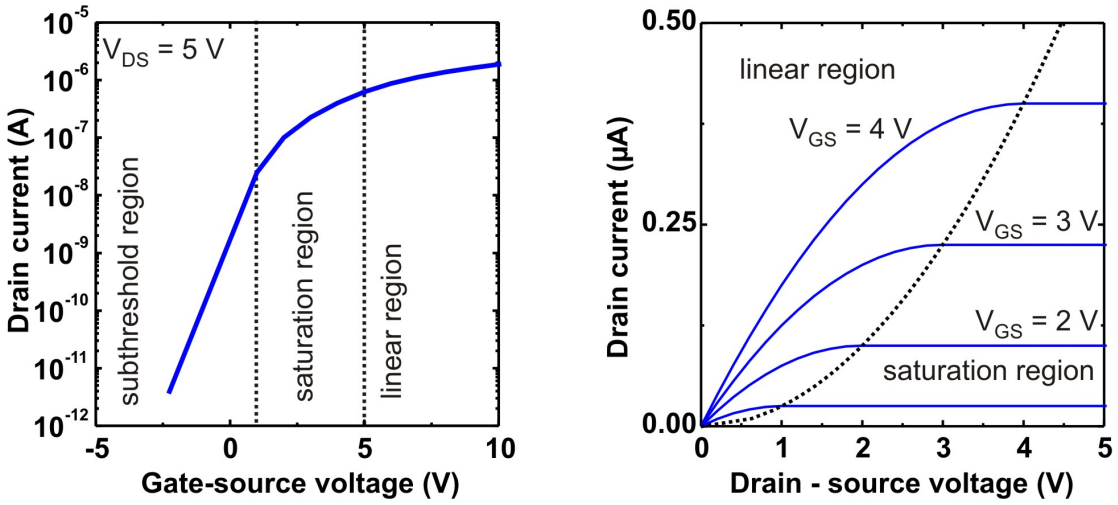


Figure 2.6: **Simulated transfer and output characteristics according to the charge-sheet approximation.**
Simulated transfer and output characteristics based on equations 2.15 and 2.16, with $\mu = 50\ \frac{\mathrm{cm}^2}{\mathrm{Vs}}$, W = 50 nm, L = 1 µm, and $C_I = 0.01\,\mathrm{fF}$. The current-voltage characteristics can be divided into different operation regions as indicated by the dotted lines. According to the equations derived from the charge-sheet approximation, the transition between the saturation and the linear region occurs for $V_{DS} = V_{DS}^{SAT} = V_{GS} - V_{FB}$. In the subthreshold region, the assumption of a charge-sheet at the semiconductor/insulator interface is not justified and a description with the charge-sheet approximation fails. The drain current in this region increases exponentially with increasing $V_{GS}$.

$V_{GS}$ and $V_{DS}$. However, some corrections have to be made for the transition between the linear and the saturation region.

Figure 2.6 shows the transfer and output characteristics according to the charge-sheet model. The dotted lines mark the transitions between the linear region, the saturation region and the subthreshold region. For constant $V_{GS}$, the drain current first increases linearly with $V_{DS}$, then gradually levels off and reaches a maximum (figure 2.6b, linear region). The drain-current maximum corresponds to $V_{DS} = V_{DS}^{SAT} = V_{GS} - V_{FB}$. For $V_{DS} > V_{GS} - V_{FB}$, equation 2.15 predicts a decreasing drain current. This drop is not physical and is only due to the fact that the approximation of a charge sheet is no longer valid at the drain end of the channel (pinch-off). To account for the constant drain current in the saturation regime, $V_{DS}$ is substituted by $V_{DS}^{SAT}$, and the drain current in the saturation region is described by (figure 2.6b saturation region):

$$I_D^{sat}(V_{GS}, V_{DS}) = \frac{\mu C_I}{2L^2}(V_{GS} - V_{FB})^2 \tag{2.16}$$

### Subthreshold region

The transfer characteristics further show the subthreshold region. This region is not described by the charge-sheet approximation, since the charge-carrier concentration in the semiconductor is small, and hence $C_S(\phi_S) \gg C_I$ is not fullfilled. Within this region, the drain current increases exponentially with increasing gate-source voltage, ($C_S(\phi_S) \leq C_I$ and $\alpha(\phi_S) \approx 1$). The slope of the drain current in this region is denoted as subthreshold swing S, which is described by [36]:

$$S = \ln(10)\frac{k_B T}{q}\left(\frac{C_I + C_S + C_{traps}}{C_I}\right), \tag{2.17}$$

and $C_{traps}$ is the capacitance associated with the presence of charge-carrier traps at the interface between semiconductor and insulator. According to equation 2.17 the theoretical minimum of the subthreshold swing at room temperature is 60 mV/decade. A steep subthreshold slope is useful to operate FETs within a small gate-source voltage range. In order to obtain a steep subthreshold swing, the capacitance contributions from interface traps and from the semiconductor need to be small compared to the capacitance of the insulator ($C_S + C_{traps} \ll C_I$). Therefore, it is beneficial to increase the capacitance of the gate insulator and to minimize the density of interface traps.

## 2.2.6 Important FET parameters

Based on the equations derived with the help of the charge-sheet approximation it is possible to extract important FET parameters from the measured current-voltage characteristics. These parameters are: the transconductance, the field-effect mobility, the subthreshold swing, the on/off current ratio, the threshold voltage, and the hysteresis. These parameters are useful to evaluate the performance of an FET compared to other FETs fabricated with different technologies.

### Transconductance

The transconductance $g_m$ describes the response of the drain current with respect to a change of the gate-source voltage and is defined as $g_m = \frac{dI_D}{dV_{GS}}$. The transconductance is especially important for the dynamic performance of an FET, since a large transconductance allows a rapid charging and discharging of the FET's capacitance (see section 9.2).

According to the equations derived from the charge-sheet model, $g_m$ is given by

$$g_m = \frac{\mu C_I}{L^2} V_{DS} \tag{2.18}$$

in the linear region and

$$g_m = \frac{\mu C_I}{2L^2}(V_{GS} - V_{FB}) \tag{2.19}$$

in the saturation region.

### Field-effect mobility

The field-effect mobility is a measure of the mobility of the charge carriers in the semiconductor and allows a comparison of different FETs independent of the device geometry:

$$\mu_{lin} = \frac{g_m L^2}{C_I V_{DS}} \quad \text{and} \quad \mu_{sat} = \frac{2L^2}{C_I}\left(\frac{d\sqrt{I_D}}{dV_{GS}}\right)^2 \tag{2.20}$$

### Subthreshold swing

See description in section 2.2.5.

### On/off current ratio

The on/off current ratio is the ratio between the drain current in the on-state (at maximum $V_{GS}$) and the minimum drain current in the off-state. A large on/off current ratio ($> 10^3$) is important for applications in digital logic, since it determines the difference between the logic levels "1" and "0".

### Threshold voltage

The threshold voltage is the minium gate-source voltage that is required to obtain an appreciable drain current. For silicon MOSFETs, the threshold voltages is defined as the gate-source voltage at the transiston between the weak inversion regime and the strong inversion regime. However, this definition is not suitable for other types of FETs, such as thin-film transistors or MESFETs, since these types of transistors are not operating in the strong inversion regime. Alternative definitions of the threshold voltage have thus been developed [38]. In the framework of this thesis, the so-called constant-current approach is employed for the definition of the threshold voltage [39]. In this approach, the threshold voltage is defined as the gate-source voltage for a certain drain current (e.g. $10^{-10}$ A):

$$V_{th} = V_{GS}@(I_D = 10^{-10}A)$$

#### Hysteresis

The hysterisis describes the difference between the drain current observed in the forward and the backward sweep of the transfer characteristics. (e.g., forward sweep from negative $V_{GS}$ to positive $V_{GS}$ and backward sweep from positive $V_{GS}$ to negative $V_{GS}$). While a large hysteresis is beneficial for non-volatile memory FETs [40], the hysteresis should be as small as possible in FETs in logic circuits, since a large hysteresis makes it difficult to obtain reproducible and reliable FET characteristics.

### 2.2.7 FET characteristics in the depletion regime

In an undoped semiconductor, the charge-carrier concentrations in the bulk ($n_0$ and $p_0$) are usually very small. Therefore, the drain current of an FET based on an undoped semiconductor will be very small when the FET is biased in the depletion regime, and the equations derived in section 2.2.5 provide an adequate description of the FET characteristics. For a doped semiconductor, however, the charge-carrier density in the bulk of the semiconductor can be substantial. Depending on the doping concentration and the geometric dimensions of the semiconductor utilized for the FET channel, the bulk conductivity can lead to a significant drain current when the FET is biased in the depletion regime and also cause a substantial contribution to the drain current when the FET is biased in the accumulation regime (see figure 2.7). In the following the equations describing the drain current of an FET based on a doped semiconductor biased in the depletion regime are derived.

As described in section 2.2.3, an FET with an n-type semiconductor operates in the depletion regime when the surface potential is negative. Mobile electrons are repelled from the interface leaving behind the immobile, ionized dopants. The surface-charge density in the depletion regime therefore stems from the charge of the ionized dopants. Hence, $Q_S$ does not contribute to the drain current in this regime and equation 2.9 needs to be reconsidered. The concentration of free charge carriers within the semiconductor bulk is given by $n = n_0 \cdot \exp\left(\frac{q \cdot \phi(\mathrm{y})}{\mathrm{k_B \cdot T}}\right)$. To obtain the potential distribution $\phi(\mathrm{y})$ and also the concentration of free charge carriers, the Poisson equation for a doped n-type semiconductor needs to be solved:

$$\frac{\partial^2 \phi(\mathrm{y})}{\partial \mathrm{y}^2} = \frac{q}{\varepsilon_s \cdot \varepsilon_0} \cdot \left(n_0 \cdot \exp\left(\frac{q \cdot \phi(\mathrm{y})}{\mathrm{k_B \cdot T}}\right) - \mathrm{N_D^+}\right). \tag{2.21}$$

In general, equation 2.21 is only numerically solvable with respective boundary conditions. However, the problem can be significantly simplified with the help of the so-called Schottky-parabola approximation.

### Schottky-parabola approximation

Due to the exponential dependence of $n$ on the potential $\phi(y)$, the Schottky-parabola approximation assumes that the concentration of free electrons in the semiconductor bulk is essentially zero up to a distance $\mathrm{W_D}$ from the interface. In this region the charge is given by the ionized dopants $\mathrm{N_D^+}$ . This distance is called depletion width. For distances larger than $\mathrm{W_D}$, the semiconductor is assumed to be neutral, i.e. all ionized donors are compensated by free electrons. Thus, the Poisson equation is given by:

$$\frac{\partial^2\phi(\mathrm{y})}{\partial \mathrm{y}^2} = \begin{cases} -\frac{q\mathrm{N_D^+}}{\varepsilon_S\varepsilon_0} & \text{for} \quad 0 < \mathrm{y} < \mathrm{W_D} \\ \\ 0 & \text{for} \quad \mathrm{y} \geq \mathrm{W_D} \end{cases} \tag{2.22}$$

By integrating the Poisson equation, the relationship between the electric field and the potential $\phi(\mathrm{y})$ can be calculated. The calculation yields a linear relationship between the electric field and the distance from the interface. Consequently, the potential follows a parabolic relationship. By introducing the boundary condition $\phi(0) = \phi_S$, the relationship between the depletion width and the surface potential can be calculated:

$$\mathrm{W_D}(\phi_S) = \sqrt{\frac{2\varepsilon_S\varepsilon_0}{q\mathrm{N_D^+}}(-\phi_S)}. \tag{2.23}$$

Using this relationship the surface-charge density in the depletion regime can also be expressed as $Q_S(\phi_S) = q\mathrm{N_D^+W_D}(\phi_S)$, which yields the familiar square-root dependence of $Q_S$ on the surface potential $\phi_S$ observed in the depletion region (see figure 2.4). The origin of the drain current in this regime is the non-depleted part of the semiconductor channel. With $\mathrm{N_D^+} = n_0$ the drain current can be calculated by:

$$\mathrm{I_D} = \mu\frac{\mathrm{W}}{\mathrm{L}}qn_0 \int_0^{\mathrm{V_{DS}}} (\mathrm{d_S} - \mathrm{W_D}(\phi_S))d\mathrm{V_{DS}}, \tag{2.24}$$

and $\mathrm{d_S}$ denotes the physical thickness of the semiconductor. By introducing the gate-coupling factor from equation 2.12, the dependence of $\mathrm{W_D}$ on $\mathrm{V_{GS}}$ and $\mathrm{V_{DS}}$ can be expressed as:

$$\mathrm{W_D}(\mathrm{V_{GS}}, \mathrm{V_{DS}}) = \sqrt{\frac{2\varepsilon_S\varepsilon_0}{q\mathrm{N_D^+}}(-\alpha\mathrm{V_{GS}})} = \sqrt{\frac{2\varepsilon_\mathrm{S}\varepsilon_0}{q\mathrm{N_D^+}}(\mathrm{V_{FB}} - \mathrm{V_{GS}} + \mathrm{V_{DS}}) + \frac{\varepsilon_\mathrm{S}^2\varepsilon_0^2}{\mathrm{C_i^2}}} - \frac{\varepsilon_\mathrm{S}\varepsilon_0}{\mathrm{C_i}}. \tag{2.25}$$

The FET is switched-off when the semiconductor is completely depleted at the source contact: $\mathrm{W_D^{source}}(\mathrm{V_{GS}}) = \mathrm{d_S}$. According to equation 2.25 the gate-source voltage necessary

to switch-off the FET ($V_{th}$) is given by:

$$V_{th} - V_{FB} = -\frac{qN_D^+ d_S^2}{2\varepsilon_S \varepsilon_0} - \frac{qN_D^+ d_S}{C_i} \tag{2.26}$$

The first term on the right-hand side of equation 2.26 describes the voltage drop across the completely depleted semiconductor (pinch-off voltage) $V_P = -\frac{qN_D^+ d_S^2}{2\varepsilon_S \varepsilon_0}$, and the second term describes the corresponding voltage drop across the insulator. By integrating equation 2.24 the drain current in the linear region ($V_{DS} < V_{DSsat}$) is given by [41]:

$$I_D^{lin} = \mu \cdot \frac{W}{L} \cdot q \cdot N_D^+ \left( d_S + \frac{\varepsilon_S \varepsilon_0}{C_i} \right) V_{DS}$$

$$-\frac{2}{3} d_S V_p \left( \left( \frac{\varepsilon_S^2 \varepsilon_0^2}{d_S^2 C_i^2} + \frac{(V_{GS} - V_{FB})}{V_p} \right)^{\frac{3}{2}} - \left( \frac{\varepsilon_S^2 \varepsilon_0^2}{d_S^2 C_i^2} + \frac{(V_{GS} - V_{FB} - V_{DS})}{V_p} \right)^{\frac{3}{2}} \right) \tag{2.27}$$

and in the saturation region ($V_{DS} \geq V_{Dsat}$) :

$$I_D^{sat} = \mu \cdot \frac{W}{L} \cdot q \cdot N_D^+ \left( d_S + \frac{\varepsilon_S \varepsilon_0}{C_i} \right) V_{DSsat}$$

$$-\frac{2}{3} d_S V_p \left( \left( \frac{\varepsilon_S^2 \varepsilon_0^2}{d_S^2 C_i^2} + \frac{(V_{GS} - V_{FB})}{V_p} \right)^{\frac{3}{2}} - \left( \frac{\varepsilon_S^2 \varepsilon_0^2}{d_S^2 C_i^2} + \frac{(V_{th} - V_{FB})}{V_p} \right)^{\frac{3}{2}} \right), \tag{2.28}$$

These equations are quite complicated, therefore only the important consequences compared to the accumulation regime will be discussed. From equation 2.23 the capacitance per unit area of the depleted part of the semiconductor is given by:

$$C_s(\phi_S) = \frac{2\varepsilon_0 \varepsilon_S}{W_D(\phi_S)}. \tag{2.29}$$

With increasingly negative $V_{GS}$, the depletion width in the semiconductor increases and consequently $C_s$ decreases. The total capacitance of the FET is given by:

$$\frac{1}{C_{tot}(V_{GS})} = \frac{1}{C_s(V_{GS})} + \frac{1}{C_i}. \tag{2.30}$$

In the accumulation regime $C_s \gg C_i$, and therefore $C_{tot}(V_{GS}) = C_i$ was used here to apply the charge-sheet approximation. However, in the depletion regime, $C_s$ and $C_i$ may be within the same order of magnitude, and thus the total capacitance is expected to be gate-bias dependent. This has important consequences on the transfer characteristics of the FET. Figure 2.7a shows the simulated transfer characteristics of an FET based on an n-doped semiconductor. For the simulation the doping concentration is set to $N_D = 5 \cdot 10^{17} cm^{-3}$ and it is estimated that the capacitance of the fully depleted semiconductor equals the capacitance of the gate insulator ($C_S/C_I = 1$). The FET is operated in the

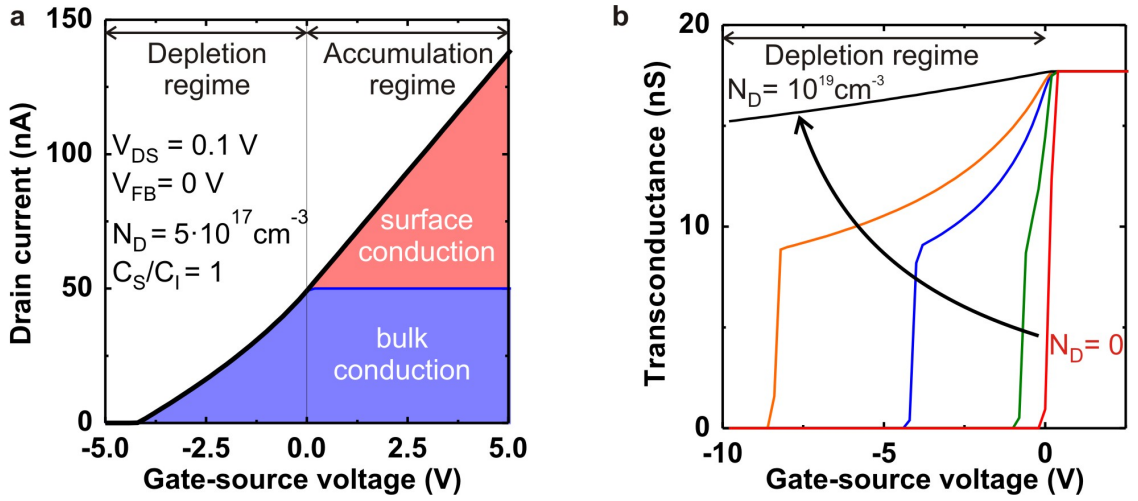


Figure 2.7: **Transfer characteristics and transconductance of an FET based on a doped semiconductor.**
(a) Simulated transfer characteristics of an FET based on an n-doped semiconductor operating in the depletion regime for $V_{GS} < 0\,V$ and operating in the accumulation regime for $V_{GS} > 0\,V$. In the depletion regime (equations 2.27 and 2.28), the slope of the drain current is smaller than in the accumulation regime, due to the contribution of the $V_{GS}$-dependent capacitance of the semiconductor $C_S$, which reduces the total gate capacitance. In the accumulation regime, the drain current consists of the constant contribution from the conductive semiconductor bulk (blue area) and the additional charge carriers accumulated at the semiconductor/insulator interface (red area). (b) Transconductance as a function of the gate-source voltage of an FET based on undoped semiconductor (red curve), and FETs based on n-doped semiconductors with a doping concentration of $N_D = 10^{17}$ cm$^{-3}$ (green curve), $N_D = 5{\cdot}10^{17}$ cm$^{-3}$ (blue curve), $N_D = 10^{18}$ cm$^{-3}$ (orange curve), and $N_D = 10^{19}$ cm$^{-3}$ (black curve). For the FETs based on doped semiconductors, the capacitance $C_S$ depends on $V_{GS}$ in the depletion regime ($V_{GS} < 0\,V$). Therefore, the transconductance in the depletion regime also depends on $V_{GS}$, but is always smaller than the transconductance in the accumulation regime ($V_{GS} > 0\,V$).

linear region with $V_{DS} = 0.1\,V$ and $V_{FB} = 0\,V$. For $V_{GS} < 0\,V$, the FET is operating in the depletion regime, and the drain current is calculated with the help of equations 2.24 and 2.25. For $V_{GS} > 0\,V$ the FET is operating in the accumulation regime. In the accumulation regime the drain current consist of the constant contribution from the doped semiconductor bulk (figure 2.7a; bulk conduction, blue area), and the contribution of the charge-carriers accumulated at the semiconductor/insulator interface, which increases linearly with increasing gate-source voltage (figure 2.7a; surface conduction, red area). Compared to the accumulation regime, the drain-current modulation in the depletion regime is reduced. This is attributed to the reduction of the total capacitance and becomes even more apparent when considering the transconductance in figure 2.7b.

For an FET based on an undoped semiconductor (figure 2.7b, red curve), the transconductance is zero in the depletion regime and constant in the accumulation regime above the

threshold voltage of the FET at ($V_{GS} \geq V_{th} = 0\,V$). For the FETs based on doped semiconductors (figure 2.7b, green, blue, orange and black curve), the transconductance is a function of the gate-source voltage above the threshold voltage given by equation 2.26 in the depletion regime ($V_{GS} < V_{FB}$) and constant in the accumulation regime ($V_{GS} > V_{FB}$). The transconductance in the depletion regime is smaller than the transconductance in the accumulation regime, due to the smaller total device capacitance determined by the depletion width of the doped semiconductor.

## 2.3 Calculation of the gate-insulator capacitance

As can be seen from the considerations in the previous section, the capacitance of the gate insulator $C_I$ is an important parameter for the calculation of the drain current of an FET. For an FET operating in the accumulation regime as well as for an FET operating in the depletion regime, $C_I$ enters the according equations (see equations 2.15 and 2.25). For FETs realized in a planar geometry, the calculation of the gate-insulator capacitance is a straight-forward task. However, in the case of a nanowire FET, the cylindrical geometry of the semiconductor complicates the calculation of the capacitance. Some of the nanowire FETs fabricated in the framework of this thesis utilize a global, planar back-gate electrode for the modulation of the drain current. To calculate the capacitance of such a global back-gate nanowire FET, the model of a "metallic cylinder on an infinite metal plate" is often used [42]. The metallic cylinder represents the surface of the semiconductor nanowire, while the metal plate represents the global back-gate electrode. The assumptions entering the model are [43]:

- The charge-carrier concentration in the semiconducting nanowire is reasonably high, so that the nanowire can be treated as metallic (i.e. the charge modulation occurs at the semiconductor surface).
- The nanowire is much longer than the thickness of the gate insulator.
- The nanowire is completely embedded in the dielectric and has a circular cross section.

The model yields an analytical equation for the gate capacitance:

$$C_{Cyl} = \frac{2\pi\varepsilon_0\varepsilon_S L}{\cosh^{-1}\left(1 + \frac{t_I}{r_{NW}}\right)}, \tag{2.31}$$

with the radius of the nanowire $r_{NW}$ and the thickness of the gate insulator $t_I$. For the ZnO nanowire FETs realized in a global back-gate configuration, the third assumption is in general not fullfilled. In a global back-gate configuration, nanowires are deposited on conducting substrates covered with a thin gate dielectric (e.g. 100 nm $SiO_2$, see section

4.2). Therefore, the gate dielectric is not homogeneous, since it consists of the ambient air around and the silicon dioxide below the nanowires. Nevertheless, the analytically derived solution can still be used to calculate the capacitance, provided the dielectric constant of the gate dielectric is substituted by an effective dielectric constant $\varepsilon_{eff}$. For a nanowire FET realized on an $SiO_2$ dielectric surrounded by air the effective gate dielectric constant is $\varepsilon_{eff} = 2.25$ [43]. Compared to the dielectric constant of $SiO_2$ ($\varepsilon_S = 3.9$), the use of the effective dielectric constant reduces the total capacitance by about 50%. The smaller capacitance accounts for the smaller dielectric constant of the ambient atmosphere surrounding the nanowire compared to the $SiO_2$ on which the nanowire is resting.

A comparison with the capacitance calculated by simply assuming a parallel-plate capacitor of length L and width $d_{NW}$ shows that $C_{Cyl}$ yields a five times higher capacitance for the nanowire FET ($t_I$ = 200 nm, $d_{NW}$= 50 nm). Hence, field-effect mobilities calculated with the simple plate-capacitor model would overestimate the actual field-effect mobility of the charge carriers in the nanowire FETs by a factor of five.

## 2.4 Metal-semiconductor contacts

The contact between a semiconductor and a metal plays an important role in the framework of this thesis. Depending on the distinct properties of the metal and semiconductor such a contact can display either symmetric, ohmic current-voltage characteristics, or asymmetric, rectifying current-voltage characteristics. In the latter case, the metal-semiconductor contact is referred to as a Schottky diode. In the following the mechanisms responsible for the asymmetric current-voltage characteristics are illustrated in the framework of the band theory.

When a semiconductor and a metal are brought into contact, an energy barrier (Schottky barrier) is formed at the interface, which has important consequences on the electric current across this interface. The origin of this energy barrier is in general a difference in the work function of the metal and the semiconductor. The work function is defined as the energy difference between the vacuum level $E_{VAC}$ and the Fermi level $E_F$ of the respective material (see figure 2.8a). When the semiconductor and the metal are electrically connected, thermal equilibrium is established and the Fermi levels of both materials align. The difference between the work functions of the semiconductor and the metal then simply represents a potential difference called the contact potential. Similar to the situation discussed in the previous section, the contact potential causes a band bending in the semiconductor. Electrons are repelled from the interface up to a distance $W_D$ (see equation 2.23) and leave behind the ionized, positively charged dopants that compensate the negative charge of the metal surface (see figure 2.8b). As a consequence, an energy barrier $\phi_B$ is formed at the interface between semiconductor and metal. In this simple

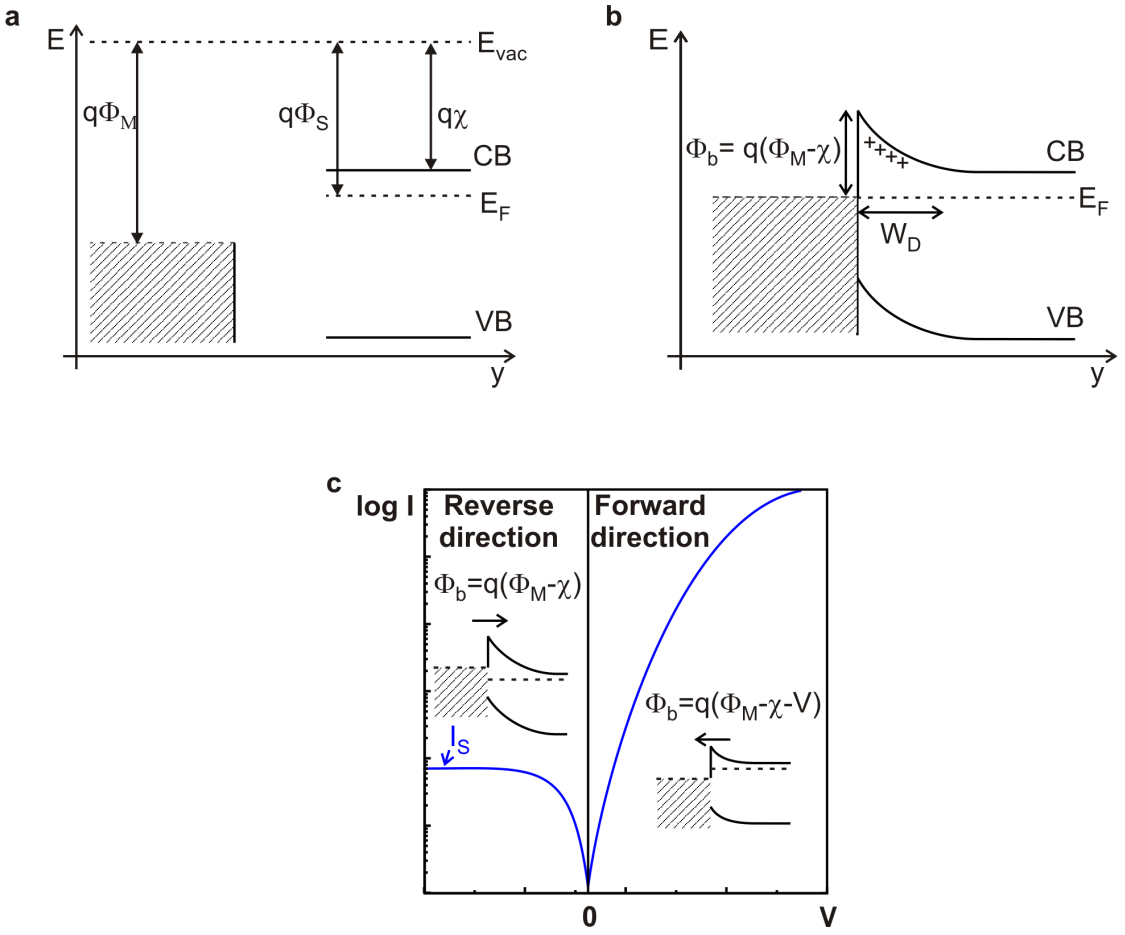


Figure 2.8: **Band diagram and current-voltage characteristics of a metal-semiconductor contact (Schottky diode).**
(a) Isolated band diagrams of a metal and a semiconductor with different work functions $\phi_M$ and $\phi_S$. The electron affinity of the semiconductor is denoted by $\chi$. (b) Band diagram after metal and semiconductor are brought into contact. Due to the work-function difference an energy barrier is formed at the interface between the semiconductor and the metal and the semiconductor surface is depleted over a width $W_D$. (c) Current-voltage characteristics of a metal-semiconductor contact (Schottky diode). For positive voltages (forward direction), the energy-barrier height is reduced (see inset) and the current increases exponentially. For negative voltages (reverse direction) the barrier for electrons traveling from the metal into the semiconductor is not affected and the current saturates at a constant value (saturation current $I_S$).

picture the barrier height is given by the difference between the work function of the metal and the electron affinity of the semiconductor $\chi$.

The current transport across such an energy barrier can be described with the help of the thermionic emission (TE) theory [36]. Within this theory, only charge carriers that are thermally excited across the energy barrier contribute to the charge transport. Hence, the resulting current only depends on the barrier height between semiconductor and metal and not on the width of the barrier ($W_D$). The resulting equation for the current transport

across the energy barrier between a semiconductor and a metal is:

$$\mathrm{I_{TE}} = \mathrm{A^*T^2} \cdot \exp(-q\phi_B/\mathrm{k_BT}) \cdot (\exp(q\mathrm{V}/\mathrm{k_BT}) - 1), \tag{2.32}$$

with the effective Richardson constant $\mathrm{A^*} = \frac{4\pi q \mathrm{m*k_B^2}}{h^3}$, the effective electron mass $\mathrm{m^*}$, and the Planck constant $h$. According to equation 2.32, the current across the energy barrier is a highly asymmetric function of the voltage (figure 2.8c). For positive voltages, the Fermi level in the semiconductor is shifted upwards with respect to the Fermi level in the metal. Consequently, the height of the energy barrier is reduced for electrons traveling from the semiconductor to the metal. Due to the exponential distribution of the energy of the electrons (Boltzmann statistics, see equation 2.2), the current across the barrier increases exponentially with positive voltage. This is called the **forward direction** of the Schottky diode. For negative voltages, the Fermi level in the semiconductor is shifted downwards with respect to the Fermi level in the metal. However, the height of the energy barrier for electrons traveling from the metal into the semiconductor is not affected by the applied voltage. Thus, a constant voltage-independent current is observed for negative voltages. This is the so-called saturation current $\mathrm{I_S} = \mathrm{A^*T^2} \cdot \exp(-q\phi_\mathrm{B}/\mathrm{k_BT})$ of the Schottky diode biased in **reverse direction**.

The situation for positive voltages resembles the situation observed in the subthreshold region of an FET, where the drain current is also limited by emission across an energy barrier. Similar to the subthreshold region of an FET, the upper limit for the current increase in forward direction of a Schottky diode is 60 mV/dec at room temperature.

However, in a real device certain deviations from the ideal TE behavior (equation 2.32) can be observed. In order to account for these deviations, the so-called ideality factor $\eta$ is introduced

$$\mathrm{I} = \mathrm{I_S} \cdot (\exp(q\mathrm{V}/\eta\mathrm{k_BT}) - 1). \tag{2.33}$$

For $\eta > 1$, the inverse slope of the current increase in forward direction is increased above 60 mV/dec. Ideality factors larger than unity can be ascribed to interface states, the presence of a thin insulator between semiconductor and metal (see section 8.2.1), contributions from other current transport mechanisms like tunneling [36], or image-force lowering of the energy barrier between semiconductor and metal [44].

The image-force lowering of the barrier, as well as a distribution of interface states a can also cause a voltage dependence of the energy barrier in the reverse direction [44]. In this situation, an exponential current increase is observed also for negative voltages. This is important for the description of the superlinear drain-current increase observed in the FETs described in section 5.

# 3 Synthesis of ZnO nanowires

## 3.1 Synthesis methods for ZnO nanowires

A wide variety of methods are available to synthesize ZnO nanowires. In general, these methods can be divided into two categories: vapor-phase growth and solution-phase growth. In the following section the methods to grow ZnO nanowires are briefly reviewed, and their advantages and disadvantages are described. In section 3.2 the growth of the ZnO nanowires utilized in the framework of this thesis is presented.

### 3.1.1 Vapor-phase growth

Vapor-phase techniques, such as chemical-vapor deposition (CVD) [10], pulsed-laser deposition (PLD) [45], and metal-organic vapor deposition (MOCVD) [46] have been utilized to grow ZnO nanowires. For all of these techniques, precursor materials are supplied from a gaseous flow and crystallize on a growth substrate at elevated temperatures ($T > 450°C$). The vapor-phase growth is usually carried out in vacuum and requires a rather expensive setup. A schematic of the growth process for standard CVD synthesis is depicted in figure 3.1. The advantages of vapor-phase methods are the precise control of the growth parameters (like gas flow rate, temperature, partial pressure) and the high purity of the source materials [47]. In general, these techniques rely on two different growth mechanisms: vapor-liquid-solid (VLS) growth and vapor-solid (VS) growth.

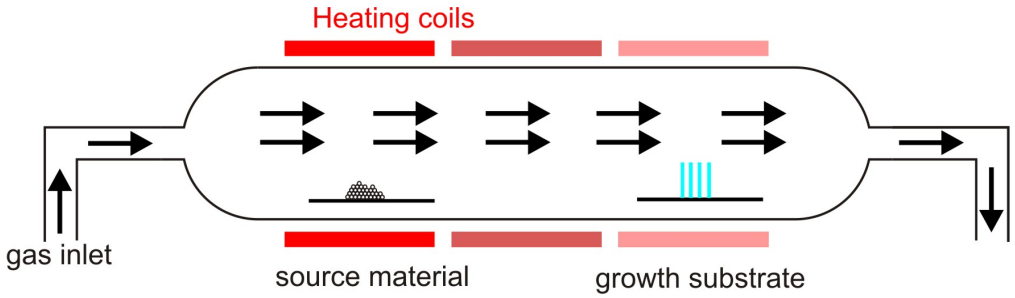


Figure 3.1: **Schematic setup for the vapor-phase growth of nanowires.** The setup consist of a tube furnace in which a well-defined temperature gradient is established with the help of heating coils. Usually the synthesis is performed under vacuum conditions. In the high-temperature region of the furnace, source material is evaporated. A carrier gas transports the evaporated source material to the growth substrate. The growth substrate is usually kept at lower temperatures, so that the gaseous source material condenses and the semiconductor crystals start to grow.

#### Vapor-liquid-solid growth (VLS)

In the VLS growth mechanism, metal-catalyst particles are distributed on the growth substrate. The particles are used as nucleation sites and to direct the growth of the nanowires. After heating-up to the growth temperature, the semiconductor material is supplied through the gas phase (evaporated source material, see figure 3.1). It dissolves in the metal-catalyst particles which leads to the formation of semiconductor-metal alloy droplets. With increasing semiconductor content, the alloy droplet becomes supersaturated and nucleation of the semiconductor crystal starts, leading to the formation of a liquid/solid interface [9] in the droplet. Further supply of semiconductor material results in an axial growth of semiconductor nanowires.

#### Vapor-solid growth (VS)

In contrast to the VLS mechanism, the VS mechanism does not require external catalyst particles and can be regarded as a self-catalytic process. The evaporated source material condenses on the growth substrate and forms seed crystals serving as nucleation sites. The directional growth of the nanostructures is thereby governed by the minimization of the surface energy [48].

### 3.1.2 Solution-phase growth

Solution-phase growth of one-dimensional nanomaterials has gained more and more attention over the last years and a large diversity of solution-based methods have been developed for the synthesis of ZnO nanowires [49]. In contrast to the vapor-phase synthesis, solution-based synthesis does not require expensive setups and high temperatures. Furthermore, solution-based synthesis provides large quantities of nanomaterial and may be scaled up more easily. However, the complex chemistry in liquids and the lower purity of the source materials make the control of the synthesis products and their properties more difficult.

The driving force for the growth of one-dimensional nanostrucutres in solution-based synthesis is the control of the growth rates of the different crystal facets which exploit different surface chemistry [49]. For example, the addition of surfactants that specifically attach to certain crystal facets can be utilized to hinder their growth and therefore promote the growth of the non-capped facets [50, 51].

The solution-based synthesis techniques can be divided into two categories: Low-temperature wet-chemical synthesis which is performed at atmospheric pressure and slightly elevated temperatures (40-80 °C), and solvothermal synthesis taking place at elevated pressure and temperatures above the boiling point of the solvent. When water is used as the solvent,

the solvothermal synthesis is referred to as hydrothermal synthesis.

The advantage of the solvothermal synthesis is the better solubility of the reactants and the faster growth compared to the low-temperature synthesis. However, solvothermal synthesis is performed in a closed vessel, making in-situ observation and process control more difficult.

## 3.2 Hydrothermal synthesis of ZnO nanowires on zinc foil

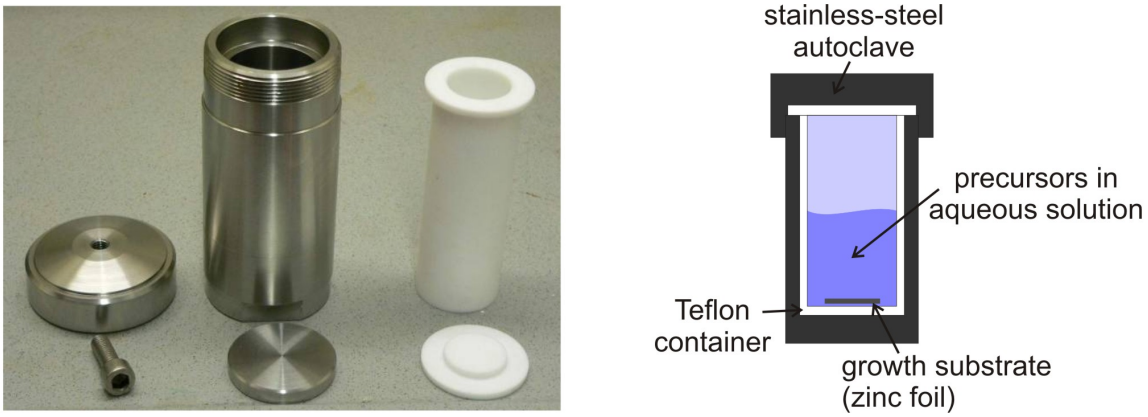


Figure 3.2: **Schematic setup for the hydrothermal growth of nanowires.** (a) Photograph of the stainless-steel autoclave and the Teflon beaker. (b) Schematic of the assembled autoclave. Precursors in aqueous solution are filled into the Teflon beaker, sealed and inserted into the stainless-steel autoclave. For the hydrothermal synthesis utilized in this thesis, a metallic zinc foil is put at the bottom of the Teflon beaker. It serves as the growth substrate and the zinc precursor for the synthesis.

For the synthesis of the ZnO nanowires used to fabricate field-effect transistors in the framework of this thesis, a hydrothermal growth method is utilized which was originally developed by Lu et al. [52]. The experimental setup for the hydrothermal synthesis consists of a home-built stainless-steel autoclave and a Teflon beaker (see figure 3.2a). A schematic cross-section of the assembled setup is depicted in figure 3.2b. The liquid and solid precursors are filled into the Teflon beaker, which is sealed and inserted into the stainless-steel autoclave. When the autoclave is heated up, the pressure within the fixed volume of the autoclave increases.

For the synthesis of the ZnO nanowires a commercially available zinc foil is used as the growth substrate and as the zinc source. The zinc foil (thickness: 0.25 mm, purity: 99.98%) is added to the autoclave containing an aqueous solution of ammonium peroxodisulfate ($(NH_4)_2S_2O_8$, purity: 99+% ) and sodium hydroxide (NaOH, purity: 98%). The overall reaction can be written as:

$$Zn + 4NaOH + (NH_4)_2S_2O_8 \rightarrow ZnO + 2Na_2SO_4 + 2NH_3 + 3H_2O. \quad (3.1)$$

In a typical synthesis, an autoclave with a volume of 40 ml is used. The autoclave is filled with 10 ml of sodium hydroxide (1 mol/l) and 10 ml of ammonium peroxodisulfate (0.2 mol/l). A 1 cm x 1 cm piece of zinc foil is added to the solution. The autoclave is sealed and put into an oven at 150 °C for 48 h hours. Under the given conditions, ammonium peroxodisulfate is acting as a strong oxidant, supplying $Zn^{2+}$ ions from the zinc foil, while the sodium hydroxide supplies $OH^-$ions for the synthesis of ZnO. After two days, the autoclave is removed from the oven and allowed to cool down to room temperature. The zinc foil is removed from the autocalve, rinsed in deionized water and blown dry with argon gas. The zinc foil is covered by a grayish film, indicating the formation of ZnO nanostructures on its surface.

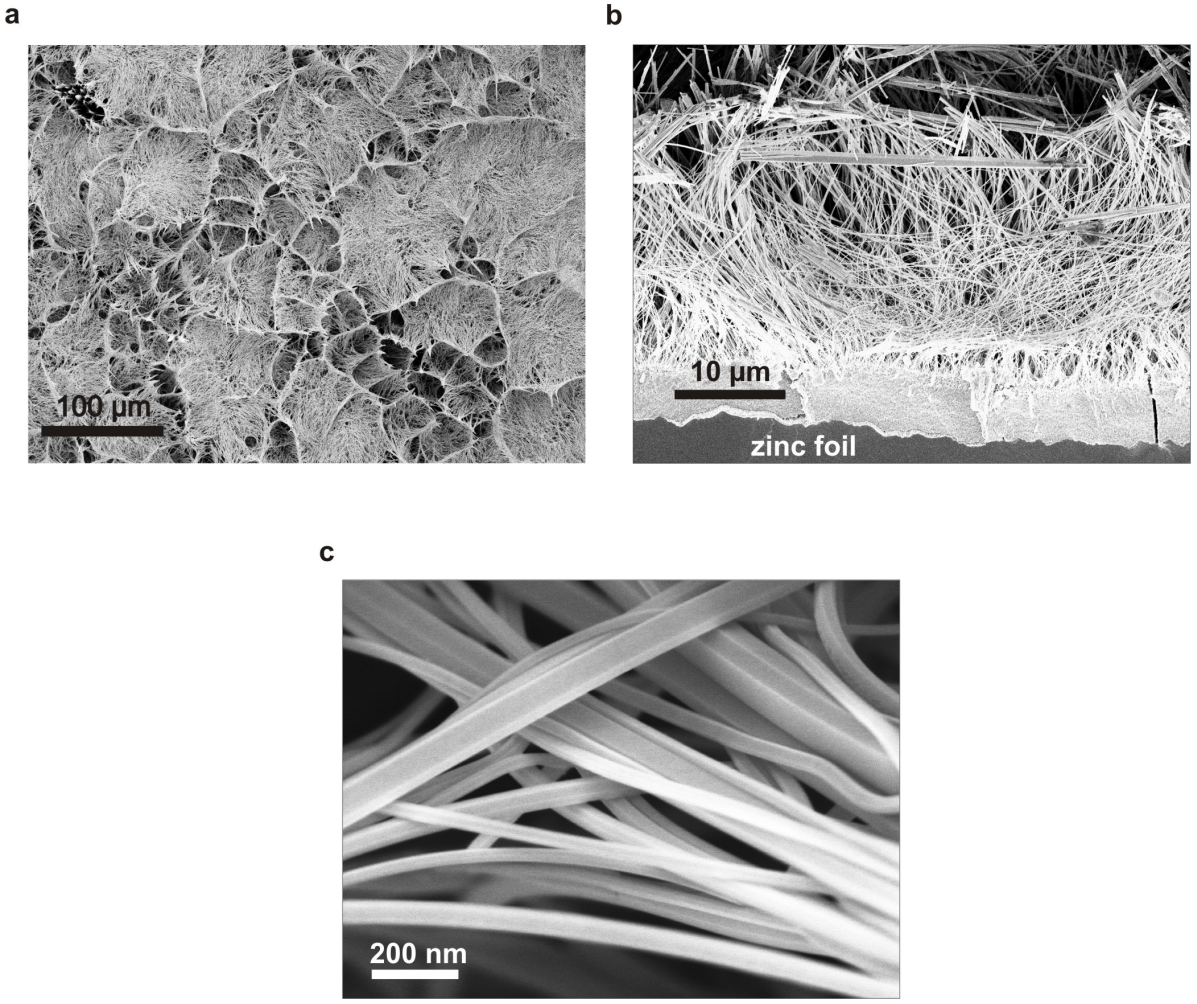


Figure 3.3: **Scanning electron microscopy images of ZnO nanowires synthesized on metallic zinc foil.**
(a) Large-area overview image. (b) The cross sectional image shows the metallic zinc foil at the bottom covered by a large density of ZnO nanowires. The ZnO nanowires are several tens of micrometers long and have aspect ratios of over 500. (c) The zoom-in shows the hexagonal structure of the nanowires expected for ZnO. The diameter of the nanowires ranges from 20 nm to more than 100 nm.

Figure 3.3 shows scanning electron microscopy (SEM) images of the surface of the zinc foil

after removing it from the autoclave. Figure 3.3a shows an overview image (480 µm x 330 µm) of the zinc foil. The whole surface of the zinc foil is covered with ZnO nanowires. The enlarged cross-sectional image of the zinc foil in figure 3.3b shows the large density of the synthesized ZnO nanowires. The nanowires are several tens of micrometers long and the nanowire diameter ranges from 20 nm to more than 100 nm, resulting in large aspect ratios of up to 500 and above. At the bottom of the image, the metallic zinc foil is seen. In a magnified image (figure 3.3c) the crystalline facets of the ZnO nanowires are recognized which indicate the hexagonal structure of the ZnO nanowires.

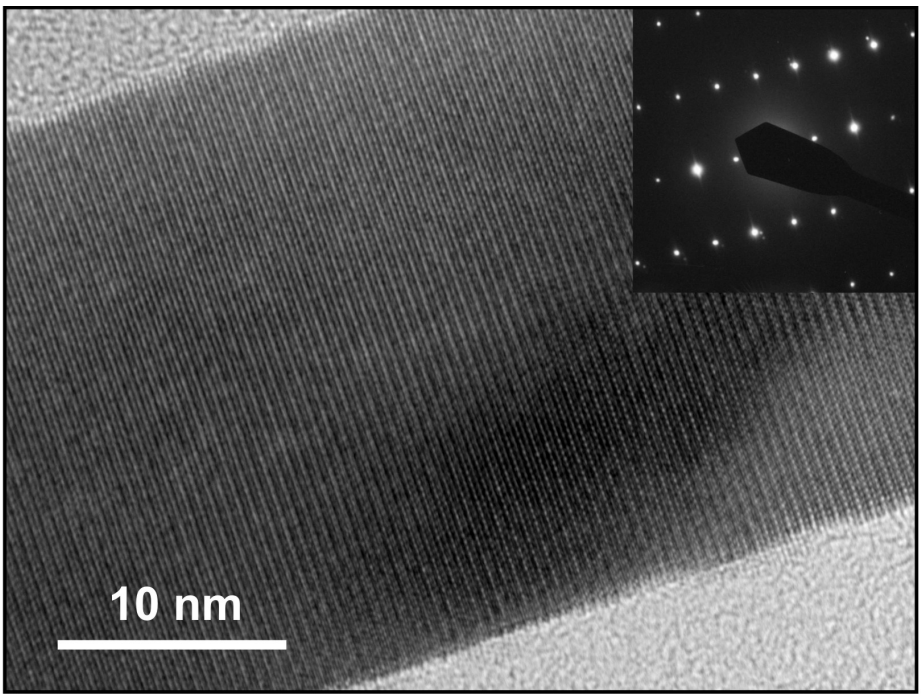


Figure 3.4: **High-resolution transmission electron microscopy image of a hydrothermally grown ZnO nanowire.**
The electron diffraction pattern (inset) reveals that the ZnO nanowires are single-crystalline. The ZnO nanowires grow along the c-axis of ZnO, and the lattice constant is estimated to 0.526 nm.

The crystalline structure of the hydrothermally grown ZnO nanowires is analyzed with a high-resolution transmission electron microscope (HRTEM). Figure 3.4 shows a HRTEM image of a single ZnO nanowire and the selected area electron diffraction (SAED) pattern. The well-defined spots in the SAED pattern show that the ZnO nanowire is single-crystalline. The distance between neighboring lattice planes estimated from the HRTEM image is 0.526 nm, which is in good agreement with the c-axis lattice constant of ZnO (0.52 nm [53]). It is therefore concluded that the nanowires grow along the (001) direction (parallel to the c-axis) of ZnO.

In summary, the hydrothermal synthesis utilized in this thesis provides a simple way to produce large amounts of ZnO nanowires with large aspect ratios exceeding 500. The

synthesized ZnO nanowires are single-crystalline and grow along the c-axis. However, it should be mentioned that the underlying mechanism of the synthesis is not understood in detail. Some attempts to reproduce the growth of the thin ZnO nanowires with large aspect ratios resulted in the formation of rather thick ZnO nanorods (d $>$ 100 nm) with small aspect ratios, although the synthesis conditions were nominally the same. A systematic analysis of the parameteres determining the shape of the ZnO nanowires is difficult, since the synthesis in an autoclave permits only a limited amount of control.

# 4 Electrical characterization of as-grown ZnO nanowires and post-growth thermal treatment

## 4.1 Introduction

To manufacture a field-effect transistor (FET) based on a semiconducting nanowire, precise patterning of the different components of the FET is required. These components are the semiconducting channel, the source and the drain contact, the gate dielectric and the gate electrode. In the following, the fabrication of the FETs will be detailed. The FETs in this chapter and in chapters 5, 6 and 7 are realized in a so-called staggered bottom-gate geometry (see figure 4.1a). This geometry offers a simple fabrication of nanowire FETs and enables the characterization of their basic properties. In section 4.3 the electrical characteristics of FETs fabricated with as-grown ZnO nanowires and their temperature-dependence are investigated. Finally the thermal treatment of the ZnO nanowires is presented in section 4.4, which is utilized to reduce the conductivity of the as-grown ZnO nanowires

## 4.2 Fabrication of ZnO-nanowire field-effect transistors based on as-grown ZnO nanowires

### Preparation of the nanowire suspension

After the synthesis of the ZnO nanowires on a zinc foil described in chapter 3, the ZnO nanowires have to be removed from the growth substrate. This can be accomplished by either scratching the zinc foil with a sharp edge, or by a short sonication (5 sec) of the zinc foil in a liquid (i.e., isopropanol). The latter method is favorable, since particularly long nanowires tend to break under the force of the edge. A short sonication of 5 sec is enough to remove a sufficient amount of ZnO nanowires from the zinc foil. After the zinc foil is removed from the bath, the ZnO nanowires are dispersed in a flask containing 10 ml of isopropanol by further sonication. A small amount (usually 10 µl) of the ZnO nanowire suspension is then dropped onto the device substrate. All measurements presented in this chapter are performed on ZnO nanowires that were dispersed onto a heavily doped silicon substrate covered with a thermally grown $SiO_2$ layer ($Si/SiO_2$ substrate). The doped silicon serves as the back-gate electrode, while the $SiO_2$ layer serves as the gate insulator. The thickness of the $SiO_2$ gate dielectric is either 100 nm or 200 nm.

### Distribution of the nanowires on the device substrate

To obtain a homogeneous distribution of ZnO nanowires across the device substrates, the substrates are heated to a temperature of 120 °C before the deposition of the nanowires. Deposition on cold substrates usually leads to aggregates of the ZnO nanowires and accumulation of ZnO nanowires at the edge of the droplet. This accumulation is due to the laminar flow in the slowly evaporating droplet. When the substrate temperature is above the boiling point of isopropanol (82 °C), the suspension droplet evaporates quickly after deposition. Due to the turbulently boiling droplet no laminar flow can be established in the droplet and a homogeneous deposition of the nanowires is achieved [54]. With the help of a darkfield microscopy image (Leica DM 4000M), the position of the individual ZnO nanowires on the substrate is determined with respect to an array of unique alignment markers previously defined on the substrates (see figure 4.1 for an atomic force microscopy (AFM) image of one of the markers together with a contacted ZnO nanowire).

### Fabrication of source/drain contacts to the ZnO nanowires

The source and drain contacts are patterned by electron-beam lithography (EBL). In general, the patterning of the contacts can also be done by photolithography or shadow-mask techniques, but the use of EBL is beneficial since it makes it possible to individually contact single nanowires of interest in arbitrary locations and orientations on the substrate, without the need of fabricating and aligning a mask for each substrate.

For the EBL process, the substrate is spin-coated with poly(methylmetacrylate) (PMMA) resist, and the areas for the source and drain contacts are exposed to the electron beam. In the exposed areas the PMMA resist is then removed by immersion of the substrate into a solution of methyl isobutyl ketone (MIBK) and isopropanol. The metalization of the contacts is performed by thermal evaporation of 80 nm thick aluminum (at a pressure of $5 \cdot 10^{-6}$ mbar). Immediately before the evaporation of the aluminum, the substrate (and therefore the contact areas of the nanowires) is exposed to a brief argon-plasma treatment. For the purpose of this plasma treatment, see subsection 5.2. Since the work function of aluminum (4.3 eV [55]) matches well with the work function of ZnO (4.2 eV), the injection barrier for the electrons is expected to be small (see chapter 2.4). After the metalization the PMMA mask is stripped in n-methyl-2-pyrrolidon (NMP) to remove the aluminum outside the contact areas. Figure 4.1 shows a schematic cross section of the finished transistor structure. L refers to the channel length defined in the EBL step and $d_{NW}$ to the nanowire diameter. Figure 4.1b shows an AFM image of a ZnO nanowire with 80 nm thick, patterned aluminum contacts on a $Si/SiO_2$ substrate.

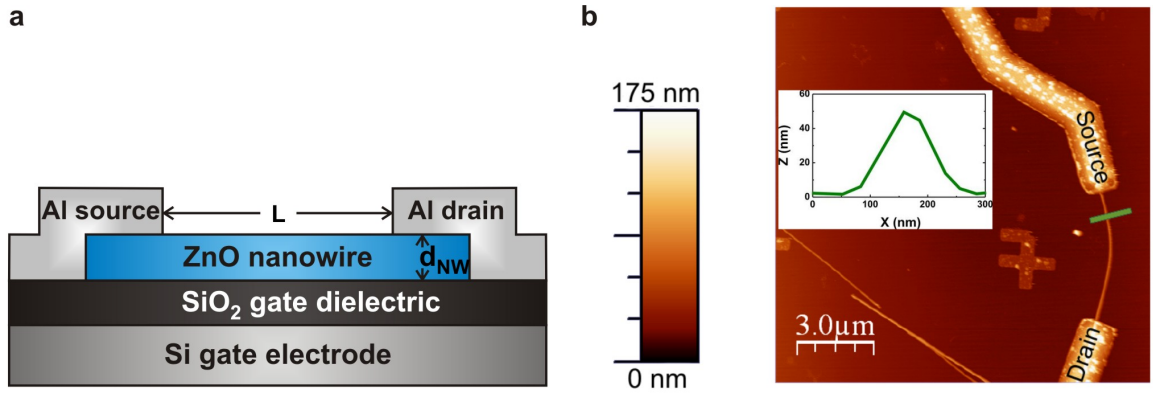


Figure 4.1: **Schematic and Atomic Force Microscopy (AFM) image of a ZnO nanowire FET realized on a Si/$SiO_2$ substrate.**
(a) Schematic cross-section of the staggered, back-gate geometry utilized in this and in the following chapters for the FET fabrication. The source and drain contacts are realized on the top surface of the ZnO nanowire. Since the silicon back-gate electrode is utilized to modulate the drain current of all FETs fabricated on the substrate, it is referred to as a global back-gate electrode. The channel length L and the source and drain contacts are defined by electron-beam lithography. (b) AFM image of a ZnO nanowire with 80 nm thick, patterned aluminum contacts on a Si/$SiO_2$ substrate next to a unique alignment marker. The inset shows the profile of the ZnO nanowire ($d_{NW}$ = 50 nm).

### Microscopic analysis of the ZnO nanowires

A major task of this thesis is the fabrication of integrated circuits on single nanowires. Therefore, the use of nanowires with a length of several micrometers suitable for the manufacturing of several FETs on the same nanowire is preferential.

As has been shown in chapter 3.2, the wet-chemically synthesized ZnO nanowires have a broad distribution concerning their diameter and length. While the channel length of the nanowire FETs is determined by EBL, the nanowire diameter cannot be modified. As can be seen from equation 2.31, the nanowire diameter influences the total device capacitance and therefore the device characteristics. This influence is even more pronounced if the nanowire is not an intrinsic semiconductor, but a doped semiconductor. As described in chapter 2.2.7 a doped semiconductor needs to be fully depleted to be switched to a non-conducting state. The depletion width of a semiconductor with a dopant concentration $N_D$ is proportional to $\sqrt{\phi_S/N_D}$. Thus, an increase of the nanowire diameter by a factor of two results in an increase of the surface potential $\phi_S$ necessary to deplete the nanowire by a factor of four. Therefore, it is important to select ZnO nanowires with approximately similar diameters in order to obtain comparable device characteristics. A precise determination of the nanowire diameter would require time-consuming AFM analysis. Alternatively, the nanowires can be located and analyzed regarding their length and

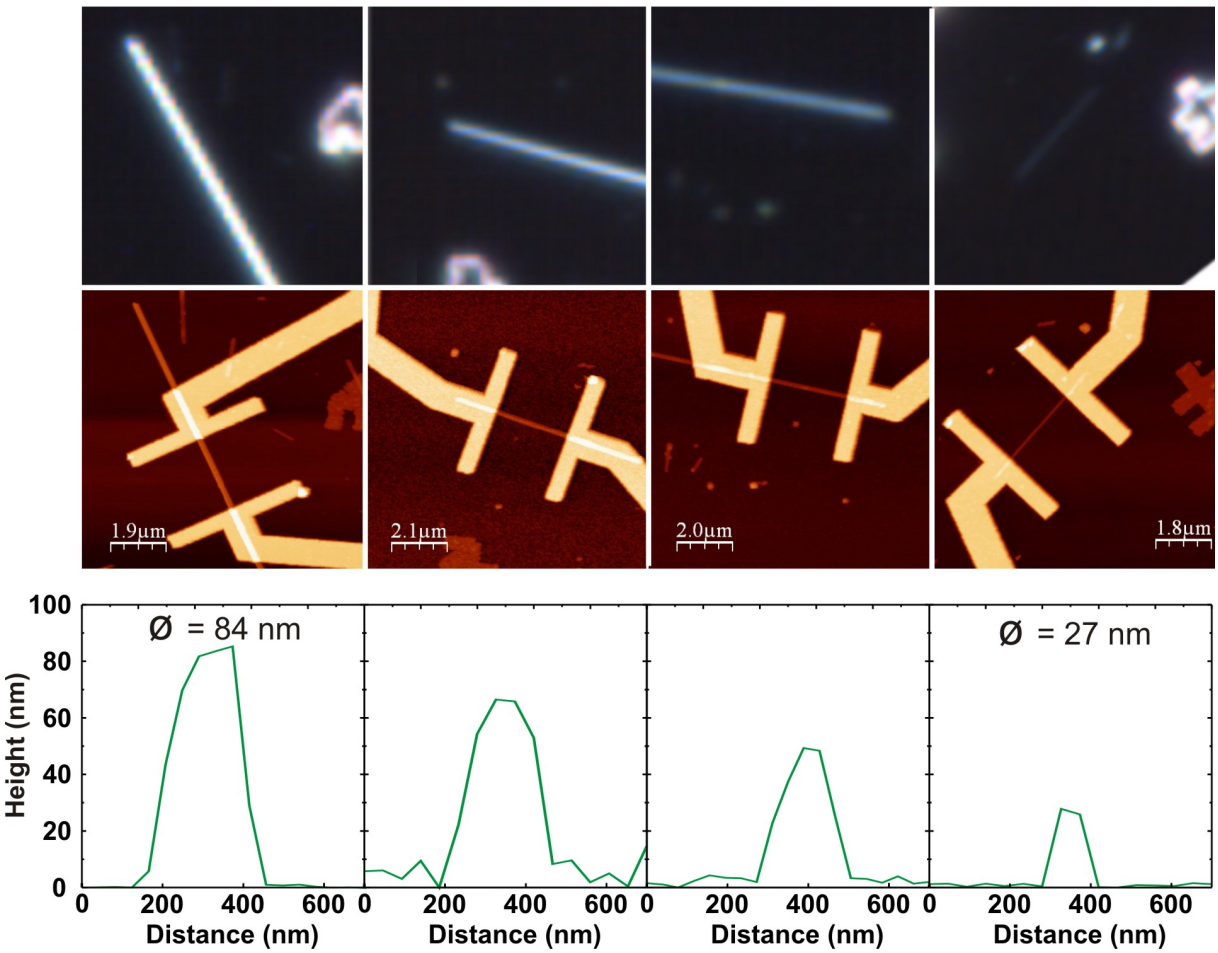


Figure 4.2: **Appearance of ZnO nanowires in darkfield microscopy and AFM images.** First row: Darkfield microscopy images of ZnO nanowires with different diameters dispersed on a $Si/SiO_2$ substrate. The $SiO_2$ gate dielectric is 100 nm thick. Second row: AFM images of the same ZnO nanowires with patterned aluminum contacts. Third row: The ZnO nanowire profile taken from the AFM images. A correlation between the intensity of the ZnO nanowires in the darkfield microscopy image and the nanowire diameter is clearly observed. The darkfield microscopy image can thus be utilized to rapidly estimate the diameter of the ZnO nanowires.

diameter by darkfield optical microscopy, which is much faster than AFM while offering an adequate precision.

The first row of figure 4.2 shows representative darkfield images of four ZnO nanowires dispersed on a heavily doped silicon substrate covered with a 100 nm thick silicon dioxide gate-dielectric layer. In the second row of figure 4.2 AFM images of the same nanowires are shown after aluminum contacts have been fabricated. The last row shows the according nanowire profiles taken from the AFM images. In order to be able to locate very thin ZnO nanowires, the exposure time of the camera attached to the optical microscope is set to its maximum of 1.5 sec. Using this exposure time, ZnO nanowires with diameters as small as 18 nm can be found on the device substrates. As can be seen, the contrast between the

nanowire and the substrate in the darkfield image becomes smaller for smaller nanowire diameters. The ZnO nanowire with maximum intensity in the darkfield image has a diameter of 84 nm, while the nanowire with the minimum intensity has a diameter of only 27 nm. The actual intensity of a ZnO nanowire in a darkfield image is of course not only dependent on its diameter. The nanowire shape (cross-section), the nanowire length, and also the type of the substrate influence the absolute value of the intensity. Therefore, the use of a darkfield microscope does not offer an absolute scale for the nanowire diameter, but it makes it possible to greatly narrow the diameter distribution of the ZnO nanowires selected for contacting. In the framework of this thesis, the investigated ZnO nanowires are intended to have a diameter of around 50 nm. According to the scale of the intensity in the darkfield microscope and taking into account the sample-to-sample variations as well as the varying diameters of the wet-chemically grown ZnO nanowires, the diameter of the nanowires which have been selected with the help of a darkfield microscopy image can be estimated to be $50 \pm 20$ nm. This approximated accuracy is consistent with AFM measurements taken from control samples.

Therefore, darkfield microscopy is a fast method to select ZnO nanowires with similar diameters.

## 4.3 Electrical characterization of as-grown ZnO nanowires

Figure 4.3 shows the current-voltage (I-V) characteristics of an as-grown ZnO nanowire with a diameter of 50 nm. The channel length as defined by electron-beam lithography is 4 µm. The I-V characteristics taken at $V_{GS} = 0\,V$ display a linear relation for $V_{DS} = \pm 0.1\,V$. This indicates that the use of aluminum as the contact metal establishes an ohmic contact to the ZnO nanowires. From the transfer characteristics it can be seen that the ZnO nanowire is an n-type conductor with a large electrical conductivity of $10^3\,S/m$. The electrical conductivity of the as-grown ZnO nanowires is due to a large charge-carrier concentration $n$ present in the as-grown nanowires. This makes it difficult to modulate the drain current with the back-gate electrode. Even for large negative $V_{GS}$ of -40 V, the nanowire cannot be switched into a non-conducting state.

The transfer characteristics of the as-grown ZnO nanowire are simulated with the help of the program MATHEMATICA. Since the as-grown ZnO nanowires are expected to have a large charge-carrier concentration, the FETs are expected to operate in the depletion regime for negative $V_{GS}$. Thus, the model introduced in section 2.2.7 is used for the simulation. The free parameters of the simulation are the charge-carrier concentration $n$ and the field-effect mobility µ. The fixed parameters that enter the model are the nanowire length ($L = 4$ µm), the nanowire diameter ($d_{NW} = 50$ nm), the drain-source voltage ($V_{DS} = 0.1\,V$), the thickness of the gate dielectric ($t_{SiO_2} = 200\,nm$), the effective

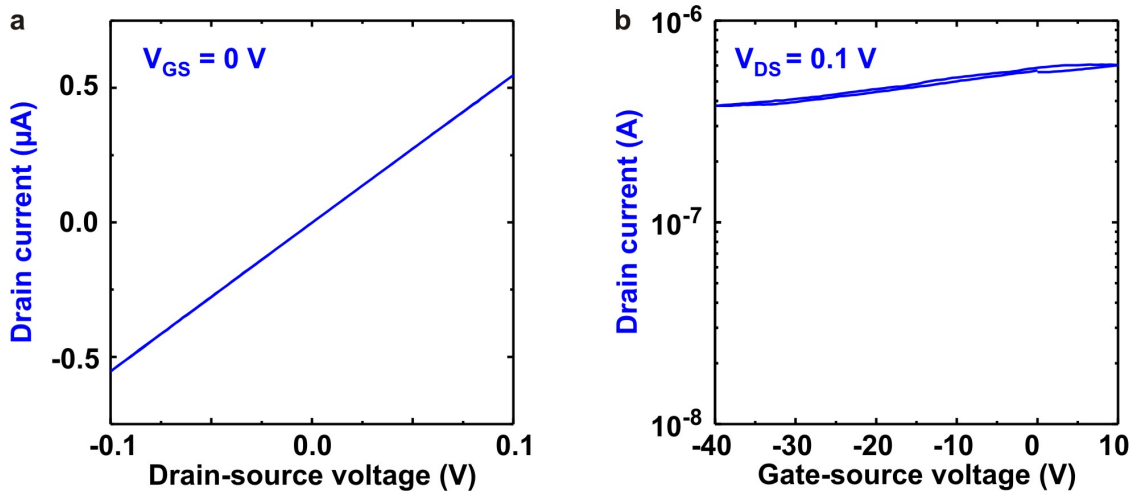


Figure 4.3: **Electrical characteristics of a wet-chemically grown ZnO nanowire**. (a) The current-voltage characteristics of an as-grown ZnO nanowire (L = 4 µm, $d_{NW}$ = 50 nm, $t_{SiO_2} = 200\,nm$) for a gate-source voltage of 0 V contacted with aluminum source/drain contacts display ohmic current-voltage characteristics. (b) The transfer characteristics measured at $V_{DS}$= 0.1 V show a large conductivity, but only very poor modulation of the drain current by the gate-source voltage. The mobility and the charge-carrier concentration is of the ZnO nanowire are estimated to 45 $\frac{cm^2}{Vs}$ and $1.5 \cdot 10^{19}\,cm^{-3}$, respectively.

dielectric constant of the gate dielectric ($\varepsilon_{SiO_2}$ = 2.5 [43]), and the permittivity of the semiconductor ($\varepsilon_{ZnO}$ = 9 [56]). The capacitance of the gate dielectric is calculated by the cylinder-on-a-parallel-plate model (section 2.3). It should be mentioned that for the sake of simplicity the charge-carrier concentration was assumed to be homogeneous over the full nanowire cross section for $V_{GS} = 0\,V$. This can lead to an underestimation of the charge-carrier concentration in the presence of a depletion layer on the ZnO nanowire surface.

The simulation of the transfer characteristics yields a field-effect mobility $\mu = 45\,\frac{cm^2}{Vs}$ and a charge-carrier concentration $n = 1.5{\cdot}10^{19}\,cm^{-3}$ for the nanowire shown in figure 4.3. The origin of the free charge carriers in the as-grown ZnO nanowires are most likely dopants unintentionally incorporated during the wet-chemical synthesis. ZnO is a material that is easily doped n-type. Among the many species that can lead to n-type doping of ZnO, the most prominent ones are aluminum, gallium, and hydrogen [26, 24]. All of these elements can be present during the hydrothermal synthesis, since the source materials used for the wet-chemical nanowire synthesis are only 98% pure and might therefore contribute to the large doping concentration. However, it is interesting to mention that during the hydrothermal growth of ZnO single-crystals also group I elements (Li, Na, K) are often incorporated in the ZnO lattice. The incorporation of group I elements on a Zn lattice site leads to the formation of deep acceptors [57] and highly-resistive ZnO [25]. In section 4.4 the different possibilities to explain the large doping concentration of the as-grown

ZnO nanowires are discussed in more detail.

### Temperature-dependent characterization of as-grown ZnO nanowires

To understand the origin of the doping, the conductivity of the as-grown ZnO nanowires is investigated at low temperatures. By reducing the temperature below the thermal activation energy of the dopants, the electrical conductivity of the ZnO nanowires is expected to decrease. The estimation of the thermal activation energy can provide an insight into the dominant dopant species incorporated into the wet-chemically grown ZnO nanowires.

Figure 4.4a shows the transfer characteristics of a ZnO-nanowire FET measured at temperatures of 303 K, 196 K and 80 K. The gate-source voltage was swept from -20 V to -10 V. All measurements shown are taken in high vacuum at a pressure of $10^{-8}$ mbar. The nanowire diameter measured by AFM is 30 nm, the channel length defined by EBL is 3 µm, and the $SiO_2$ gate dielectric on this sample is 100 nm thick. The transfer characteristics obtained from the simulation (figure 4.4a, solid lines) describe the measured data very well. The current through the ZnO nanowire decreases with decreasing temperature. This is the behavior expected for a semiconductor. The reduction in conductivity is attributed to the monotonic reduction of the charge-carrier concentration $n$ down to 80 K. Figure 4.4b shows $n$ as a function of the inverse temperature 1/T. The overall magnitude of $n$ obtained from the simulation of the as-grown ZnO nanowire under investigation is again $\sim 10^{19}\,\mathrm{cm}^{-3}$. For an n-doped, single-crystalline semiconductor with a band-gap $\mathrm{Eg} \gg \mathrm{k_B T}$, the charge-carrier concentration equals the concentration of ionized donors. The fraction of ionized dopants is dependent on the temperature and the binding energy $\mathrm{E_B}$ of the dopant atom:

$$n = \mathrm{N_D^{ionized}} = \mathrm{N_D} * \exp(-\mathrm{E_B}/\mathrm{k_B T}). \tag{4.1}$$

Therefore, the charge-carrier concentration in a doped semiconductor is expected to be independent of temperature for $\mathrm{E_B} \ll \mathrm{k_B T}$ and to decrease exponentially with temperature for $\mathrm{E_B} \gg \mathrm{k_B T}$. The measured reduction of the charge-carrier concentration with decreasing temperature is well described by equation 4.1 when an additional constant background charge-carrier concentration $n_{\mathrm{Bg}}$ is introduced. The binding energy of the dopant species responsible for the reduction of $n$ with decreasing T is $\mathrm{E_B} = 42\,\mathrm{meV}$. The dopant concentration is $\mathrm{N_D} = 2.8 \cdot 10^{18}\,\mathrm{cm}^{-3}$. The value of $n_{\mathrm{Bg}}$ obtained from the fit is $n_{\mathrm{Bg}} = 1.4 \cdot 10^{19}\,\mathrm{cm}^{-3}$. Compared to the large background charge-carrier concentration the total change of $n$ upon cooling down to 80 K is rather weak. Such weak dependency of the charge-carrier concentration on temperature and the large value of $n_{\mathrm{BG}}$ indicate that the as-grown ZnO nanowires are degenerately doped. In a degenerately doped semi-

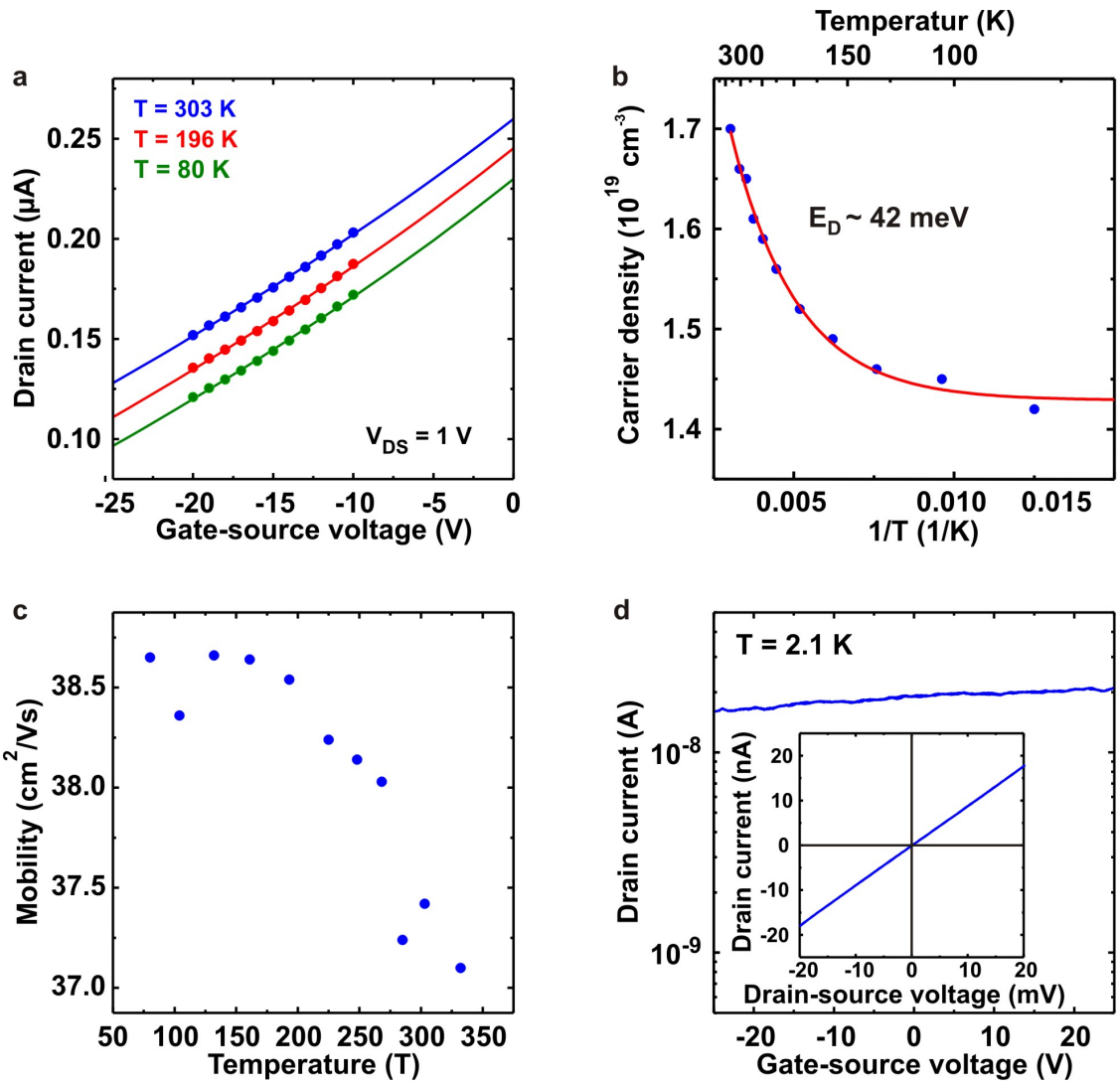


Figure 4.4: **Temperature-dependent measurements of as-grown ZnO nanowires.** (a) Simulated (solid lines, equation 2.27) and measured (dots) transfer characteristics of a ZnO nanowire FET ($L = 3\,\mu m$, $d_{NW} = 30\,nm$, $t_{SiO_2} = 100\,nm$) measured at temperatures of 303 K (blue), 196 K (red) and 80 K (green). A reduction of the drain current with decreasing temperature is observed. (b) Charge-carrier concentration obtained from the simulated transfer characteristics versus inverse temperature. The charge-carrier concentration is reduced by $2.8 \cdot 10^{18}\,cm^{-3}$ upon cooling from 300 K to 80 K. The large charge-carrier concentration of $1.4 \cdot 10^{19}\,cm^{-3}$ at 80 K indicates that the as-grown ZnO nanowire is a degenerate semiconductor. (c) Mobility obtained from modeling the transfer characteristics versus temperature. The mobility changes only slightly, in accordance with the assumption of a degenerate semiconductor. (d) Transfer and current-voltage characteristics of another ZnO nanowire FET ($L = 6.3\,\mu m$, $d_{NW} = 35\,nm$, $t_{SiO_2} = 200\,nm$) measured at 2.1 K. The nanowire is still conductive, as expected for a degenerate semiconductor.

conductor, the distance between adjacent dopant atoms is small and the wave functions of the dopants overlap. The overlapping wave functions lead to the formation of a defect band that can overlap with the conduction band. Therefore, the chemical potential

of the semiconductor will be located within the conduction band even at 0 K, and the semiconductor is highly conductive even at very low temperatures. An estimation of the charge-carrier concentration necessary to obtain a degenerate semiconductor is given by a comparison to the so-called effective density of states in the conduction band $n_{eff}$ [26]:

$$n_{eff} = 2\left(\frac{2\pi m_{eff} k_B T}{h^2}\right)^{\frac{3}{2}}. \tag{4.2}$$

In the case of ZnO, the electron effective mass $m_{eff} = 0.3\,m_0$, so the effective density of states in ZnO at room temperature is $n_{eff} = 4.2 \cdot 10^{18}\,cm^{-3}$. The calculated charge-carrier concentration of the wet-chemically grown ZnO nanowires is much larger than $n_{eff}$ and justifies the assumption of a degenerate semiconductor.

The field-effect mobility of the ZnO nanowire extracted from the simulation shows a slight increase of 5% from 37 $\frac{cm^2}{Vs}$ to 38.5 $\frac{cm^2}{Vs}$ in the temperature range from 330 K to 200 K. Below this temperature the mobility is constant down to 80 K (figure 4.4 c). For a moderately doped semiconductor, the mobility is expected to initially increase upon cooling like $T^{-3/2}$, due to reduced scattering with thermal lattice phonons. Further cooling will result in a decrease of the mobility like $T^{3/2}$, due to enhanced scattering on ionized defects. The observed temperature dependence of the mobility in the wet-chemically grown ZnO nanowires is much weaker, which coincides with the assumption of a degenerate semiconductor and the formation of a defect band [58]. Measurements performed on another ZnO nanowire ($L$ = 6.3 µm, $d_{NW}$ = 35 nm, $t_{SiO_2}$ = 200 nm, see figure 4.4d) further support this assumption. The nanowire is found to be conductive down to a temperature of 2.1 K. The charge-carrier concentration calculated from the transfer characteristics of this nanowire is $3.2 \cdot 10^{19}\,cm^{-3}$ at a temperature of $T = 2.1$ K. The resistance of the nanowire calculated from the current-voltage characteristics (see inset of figure 4.4d) is 1 MΩ.

In summary, the investigated ZnO nanowires display a mixture of semiconducting properties (increase in resistivity with decreasing temperature) and metal-like properties (low-temperature conductivity), due to the large charge-carrier concentration. Purely metal-like transport properties have been reported in the literature for degenerately doped ZnO nanobelts [59] with an even larger charge-carrier concentration of $n = 1.2 \cdot 10^{20}\,cm^{-3}$.

## 4.4 Post-growth thermal treatment

FETs in integrated logic circuits require a semiconductor that can be switched between a conducting and a non-conducting state by the gate field. The large charge-carrier concentration in the wet-chemically as-grown ZnO nanowires makes it extremely difficult to modulate the conductivity by application of an external field. As discussed in chapter

2.2.7, for a doped semiconductor the gate capacitance is a series connection of the capacitance of the insulator ($C_I$) and the capacitance of the depleted semiconductor region ($C_S$). Assuming that the capacitance of the gate dielectric is infinite, the gate-source voltage necessary to deplete the semiconducting nanowire (i.e. to switch-off the transistor) can be approximated by equation 2.23. For a ZnO nanowire with a diameter of 50 nm and a charge-carrier concentration of $10^{19}\,cm^{-3}$, a gate-source voltage of -30 V would be necessary to deplete the semiconductor. This corresponds to an immense electric field of $\sim$ 10 MV/cm that is expected to destroy the semiconductor rather than switch it into a non-conducting state in a controlled fashion. In order to manufacture useful FETs from the wet-chemically grown ZnO nanowires, the charge-carrier concentration therefore needs to be drastically reduced.

### Post-growth annealing of ZnO nanowires

In order to reduce the large charge-carrier concentration of the as-grown ZnO nanowires, the nanowires are annealed. The annealing is carried out in a quartz tube furnace which is heated to the desired annealing temperature. The sample is transferred into the hot furnace using a quartz transfer arm. This provides a rapid exposure to the intended temperature and atmosphere. The annealing is carried out after dispersing the ZnO nanowires on a $Si/SiO_2$ substrate. but before contacting the ZnO nanowires, since the high temperatures would lead to an oxidation and/or melting of the aluminum contacts. Immediately after the sample is withdrawn from the tube furnace, it is transferred to a metal plate to cool down to room temperature. After cooling-down, the sample is spin-coated with PMMA and the contacts to the ZnO nanowire are established as already described in section 4.2.

Figure 4.5a shows the transfer characteristics of three representative ZnO nanowires, the first annealed at 200 °C (red curve), the second at 400 °C (green curve), and the third at 600 °C (blue curve). All samples are annealed for 15 minutes in air and are measured at a drain-source voltage of 1 V. The transfer characteristics for the ZnO nanowires annealed at 200 °C and 400 °C resemble the transfer characteristics of the as-grown ZnO nanowires. Even for large negative gate-source voltages of -40 V the conductivity remains large and the modulation of the drain current by the back-gate electrode is poor. This indicates that the large charge-carrier concentration found in the as-grown ZnO nanowires is not significantly reduced by annealing at temperatures up to 400 °C. The situation changes dramatically when the annealing temperature is increased to 600 °C. As can be seen in figure 4.5a, the ZnO nanowire annealed at 600 °C shows strong modulation of the drain current of more than six orders of magnitude. For gate-source voltages smaller than $-10\,V$, the nanowire annealed at 600 °C is in a non-conductive state ($I_D \sim 10^{-12}$ A). The maximum drain current for $V_{GS} = 10\,V$ is 400 nA and therefore around one order of

magnitude lower than the drain current of the nanowires annealed at 200 °C and 400 °C. The dramatic change in the transfer characteristics is evidence for a strong reduction of the charge-carrier concentration in the ZnO nanowires. The unintentionally incorporated dopants are apparently passivated in a temperature range between 400 °C and 600 °C. Annealing at a temperature of 800 °C in air leads to a partial destruction of the ZnO nanowires.

In order to gain more insight into the mechanism behind the dopant passivation, the annealing is also performed in an inert argon atmosphere. Figure 4.5b shows the representative transfer curves of two ZnO nanowires annealed for 15 minutes at 600 °C in argon atmosphere (red curve) and in air (blue curve). The characteristics obtained for the ZnO nanowire annealed in air shows a strong drain current modulation in agreement with the observations from the previous experiment. In contrast, the ZnO nanowire annealed in argon atmosphere shows no change in gate dependence compared to the as-grown ZnO nanowires. This experiment indicates that ambient oxygen plays an important role in the passivation of the dopants.

### Discussion of the doping mechanism

As already discussed in section 4.3, unintentional n-type doping is often observed in ZnO, and the discussion about the origin of this doping is still ongoing in the literature. In general, n-type doping in inorganic crystals is achieved by substituting an atom of the host crystal with an atom that has an additional valence electron. For ZnO, n-type doping has been demonstrated by the substitution of zinc with group-III elements like aluminum [60], gallium [61], and indium [59]. Doping via the substitution of oxygen with group-VII elements is less investigated. Besides the substitution of an atom of the host lattice with an extrinsic atom, the generation of intrinsic defects during the growth or the incorporation of atoms onto interstitial lattice sites can also lead to n-type doping. It has been reported that hydrogen on an interstitial lattice site ($H_i$) always acts as a donor in ZnO [24, 62]. This is in contrast to many other materials in which hydrogen behaves as an amphoteric impurity counteracting the prevailing type of majority carrier [63]. Since hydrogen is always present regardless of the growth method, its presence provides a possible explanation for the observed n-type conductivity. Besides $H_i$, intrinsic defects, like zinc interstitials ($Zn_i$) and oxygen vacancies ($V_O$) are also suspected as a possible explanation of the n-type conductivity in ZnO [24]. Depending on the growth conditions, these intrinsic defects can have a small formation energy and are therefore easily incorporated into the crystal lattice. However, recent first-principle studies on ZnO showed that the formation energy of $Zn_i$ and $V_O$ are small under p-type conditions, but are rather large in n-type samples [64]. The results of these and other studies [65] indicate that the intrinsic defects are a plausible explanation for the difficulties in obtaining p-

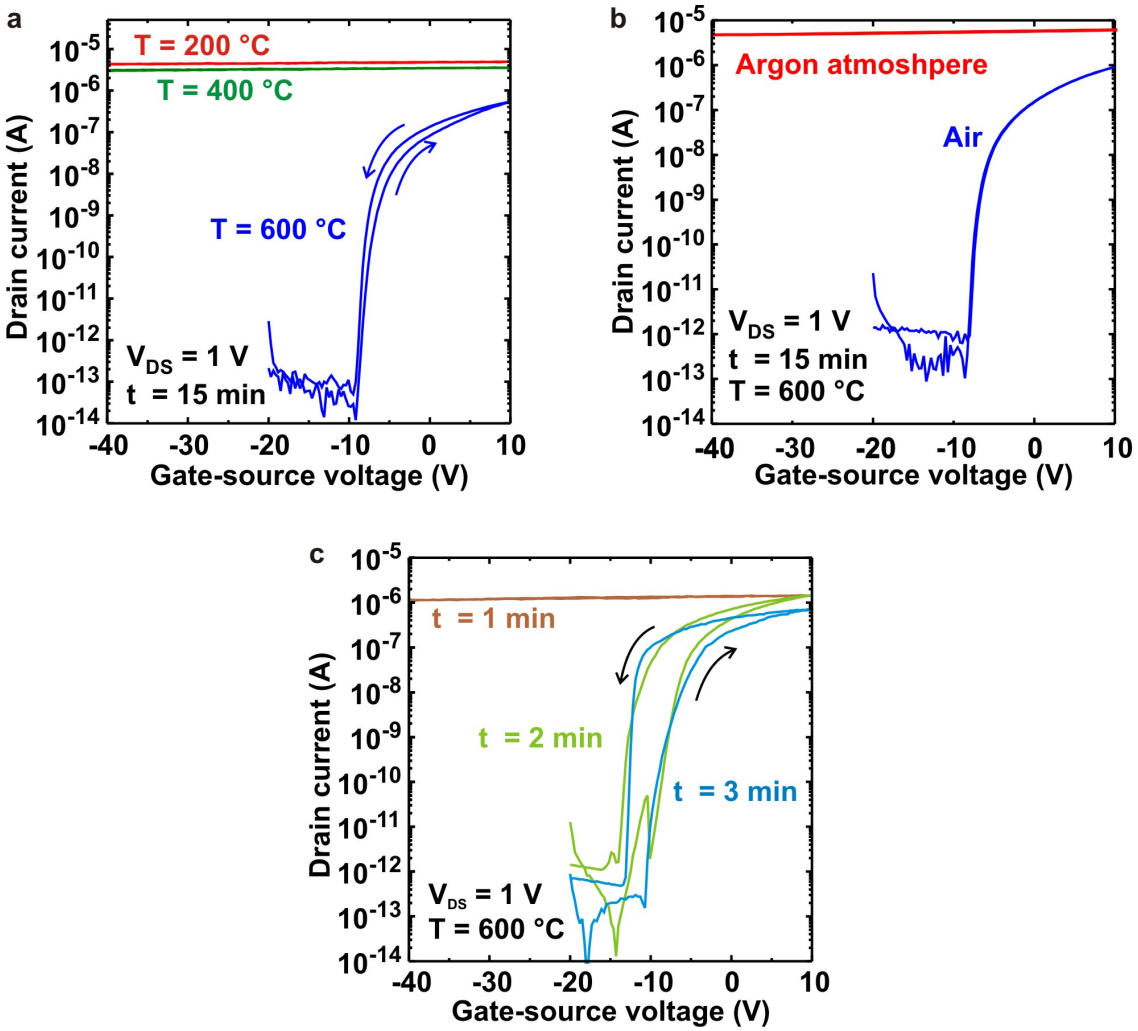


Figure 4.5: **Effect of annealing on the electrical properties of wet-chemically grown ZnO nanowires**.
(a) Transfer characteristics of three FETs based on ZnO nanowires annealed at 200 °C, 400 °C and 600 °C. The annealing is performed in ambient air for 15 minutes prior to contacting the nanowires. The FETs with ZnO nanowires annealed at 200 °C and 400 °C show no change compared to FETs based on as-grown nanowires (figure 4.3). The FET based on a ZnO nanowire annealed at 600 °C shows a dramatic increase in the gate dependence of the drain current. This increase is attributed to the passivation of the dopants incorporated unintentionally during the hydrothermal growth. (b) Transfer characteristics of two ZnO nanowires annealed at 600 °C for 15 minutes in ambient air (blue curve) and in argon atmosphere (red curve). The ZnO nanowire annealed in argon atmosphere displays no change in the transfer characteristics. This indicates the crucial role of ambient oxygen in the passivation process of the dopants. (c) Transfer characteristics of three ZnO nanowires annealed at 600 °C in ambient air for 1 minute (orange curve), 2 minutes (green curve), and 3 minutes (cyan curve). The passivation of the dopants is completed within the first two minutes of annealing at 600 °C.

type ZnO, but cannot explain the unintentional n-type doping. Another first-principle study showed that hydrogen incorporated onto an oxygen vacancy ($H_O$) can also act as

a shallow donor in ZnO [66]. The formation energy of $H_O$ is lower compared to the formation energy of a pure oxygen vacancy in n-type samples and comparable to the formation energy of $H_i$. Therefore, $H_O$ is another likely candidate to explain the n-type conductivity of ZnO. On the basis of the results obtained from the first-principle studies on hydrogen incorporation in ZnO, Bang et al. [67] simulated the thermal stability of $H_i$ and $H_O$. Their results indicate that $H_i$ is thermally much less stable than $H_O$. The simulations yield an out-diffusion temperature of 150 °C for $H_i$, while $H_O$ turns out to be stable in the ZnO lattice up to a temperature of $\sim 500$ °C.

Concerning the origin of the large doping concentration in the wet-chemically grown ZnO nanowires, several of the discussed doping mechanisms are feasible. The source materials employed in the wet-chemical growth are only about 98% pure, and therefore introduce large amounts of contaminants, like aluminum, into the ZnO nanowires. The incorporation of the contaminants into the ZnO lattice can account for the large doping concentration found in the as-grown ZnO nanowires. Besides the possible origin from contaminations, it is interesting to recognize that the temperature of 500 °C calculated for the out-diffusion of $H_O$ from the ZnO lattice [67] coincides with the experimentally observed temperature range for the reduction of the charge-carrier concentration in the ZnO nanowires (figure 4.5a). This suggests that $H_O$ is the prevailing dopant species in the wet-chemically grown ZnO nanowires (although it is not a proof). The influence of the annealing atmosphere is not discussed in the first-principle studies on $H_O$ [66, 67], but it is reasonable to assume that an oxygen vacancy created by the out-diffusion of hydrogen during annealing at 600 °C is more likely to be filled by an oxygen atom if the annealing is performed in an oxygen-rich atmosphere (air). This compensation of the oxygen vacancies can explain the observed reduction of the charge-carrier concentration upon annealing in air. In an oxygen-poor annealing atmosphere, like argon, it is not clear what happens to the created oxygen vacancy during and after the annealing. It is possible that due to the absence of oxygen in the argon atmosphere, the created oxygen vacancy might be filled again with a hydrogen atom during the cool-down of the sample. This assumption can explain the observed difference between annealing in oxygen atmosphere and annealing in argon atmosphere (figure 4.5b) and supports the proposed mechanism for the doping via hydrogen on oxygen vacancies.

In summary, the annealing experiments cannot provide an absolutely certain explanation for the large charge-carrier concentration, but give some indication that hydrogen on oxygen vacancies is the dominant doping species in the wet-chemically grown ZnO nanowires. In order to gain further insight into the doping of the ZnO nanowires, spectroscopic measurements (like UV-photoluminesence, electroluminesence, etc.) are required in combination with the electrical measurements.

In figure 4.5c the dependence of the transfer characteristics on the annealing time is

presented. The graph shows the transfer characteristics of three different ZnO nanowires annealed at 600 °C in air, for 1 minute (orange curve), 2 minutes (light green curve), and 3 minutes (cyan curve). As can be seen, the transfer characteristics of the ZnO nanowire annealed for 2 minutes and 3 minutes show similar characteristics as the ZnO nanowires annealed for 15 minutes shown in figure 4.5a and b. This is an important result for the further application of the wet-chemically grown ZnO nanowires in FETs on substrates that cannot withstand the high temperatures of the annealing (like plastic substrates). As shown in chapter 3, the growth substrate for the ZnO nanowires is a piece of zinc foil. The melting point of zinc is 420 °C and therefore lower than the temperature necessary for the annealing of the ZnO nanowires. Thus, after 15 minutes at 600 °C, the zinc foil starts to melt and the nanowires sink into the zinc foil. In contrast, a short annealing time of about 2 minutes allows the anneal to be performed on the zinc foil. Thus, the high temperatures necessary to eliminate the conductivity of the ZnO nanowires can be separated from the device substrate. In the framework of this thesis, ZnO nanowires annealed for 5 minutes on the zinc foil are used to fabricate ZnO nanowire transistors on plastic substrates (see section 9.2).

# 5 Effect of plasma treatments on ZnO nanowire field-effect transistors

Among the crucial steps in the fabrication of the FETs based on ZnO nanowires presented in this thesis are the oxygen-plasma and argon-plasma treatments. The plasma treatments greatly influence the electrical characteristics of the FETs and especially the quality of the electrical contact between ZnO and aluminum. In section 5.1 the effect of an argon-plasma treatment in the source and drain contact regions of a ZnO-nanowire FET is investigated. The influence of an argon-plasma treatment on the semiconducting channel of an FET is presented in section 5.3. Finally, the effects of an oxygen-plasma treatment in the contact regions and in the channel region are discussed in section 5.4 and 5.5, respectively.

## 5.1 Discussion of contact-resistance effects

As discussed in the preceding section 4.4, the annealing step greatly reduces the charge-carrier concentration in the as-grown ZnO nanowires. This allows the drain current to be modulated over several orders of magnitude when the annealed ZnO nanowires are utilized in FETs. However, the reduction of the charge-carrier concentration also causes problems concerning the output characteristics of the ZnO-nanowire FETs. Several of the FETs fabricated with annealed ZnO nanowires display a nonlinear increase of the drain current at small drain-source voltages in their output characteristics. An example is shown in figure 5.1.

Such a nonlinear or superlinear increase is usually attributed to the contact resistance between semiconductor and metal [68, 69, 70]. In an ideal field-effect transistor, the voltage drop across the contact resistance should be much smaller than the voltage drop across the active channel region of the device. However, this can be difficult to accomplish in a real device. As discussed in section 2.4, different work functions of the semiconductor and the contact metal lead to the formation of an energy barrier at the interface between the two materials, so the current-voltage characteristics resemble the characteristics of a Schottky diode. Under the assumption of two identical energy barriers at the source and the drain contact, the current in the FET is always limited by the voltage-independent saturation current of the reverse-biased Schottky diode at the source contact. However, due to image force lowering of the energy barrier, or due to interface states at the semiconductor/metal interface an exponential current increase can also be observed for the reverse-biased Schottky diode [71, 44]. In this situation, the current across the energy barrier at the source contact is given by:

$$\mathrm{I_{TE}} \sim \exp(-q\phi_B/\mathrm{k_B T}) \cdot \exp(q\mathrm{V}/\mathrm{k_B T}), \tag{5.1}$$

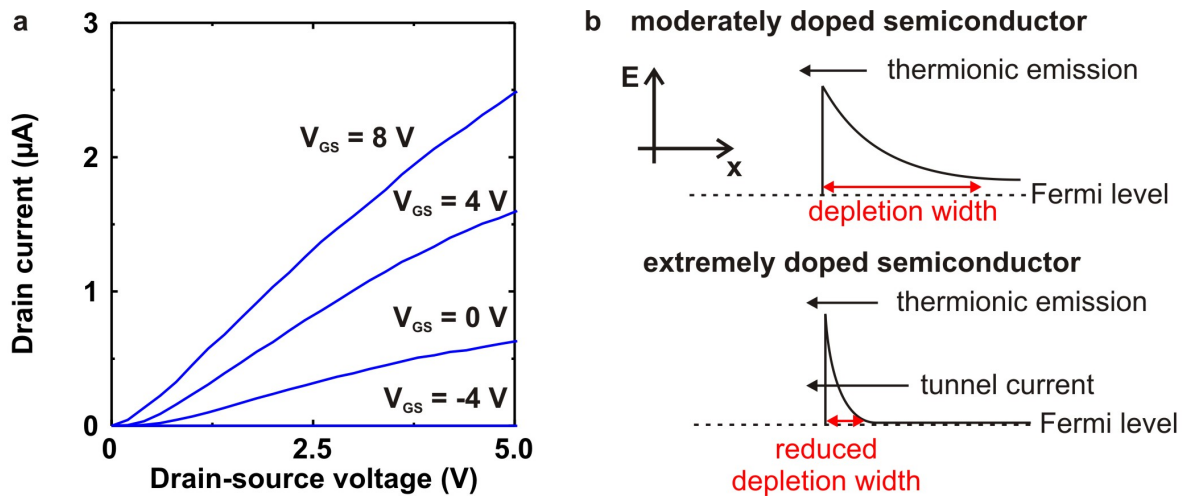


Figure 5.1: **Influence of the contact resistance on the current-voltage characteristics of ZnO-nanowire FETs.**
(a) Nonlinear output characteristics of an FET based on an annealed ZnO nanowire ($L = 3\,\mu m$, $d_{NW} = 50$ nm, $t_{SiO_2} = 200$ nm). The nonlinear current increase at small drain-source voltages indicates a significant contribution of the contact resistance between ZnO and aluminum to the overall device resistance. (b) Schematic of the band diagram of a Schottky barrier between a metal and a semiconductor. For a moderately doped semiconductor (upper graph) the depletion width is large, and therefore the current transport is dominated by thermionic emission over the barrier. In the case of a semiconductor with a large doping concentration (lower graph), the depletion width is smaller and the narrow barrier permits charge carriers to tunnel from the semiconductor to the metal.

and therefore:

$$R_C \sim \exp(q\phi_B/k_BT) \cdot \exp(-qV/k_BT) \tag{5.2}$$

with the height of the energy barrier $\phi_B$. According to equation 5.1 a superlinear (exponential) current increase as a function of voltage is expected for the contact between a semiconductor and a metal.

The more desirable linear current increase as a function of $V_{DS}$ therefore requires that the contact resistance $R_C$ introduced by the energy barrier at the metal contacts is much smaller than the overall device resistance. This can be achieved either by reducing the energy-barrier height or by increasing the charge-carrier concentration in the semiconductor by contact doping.

### Reduction of the energy-barrier height

According to equation 5.2, the contact resistance depends exponentially on the energy-barrier height $\phi_B$. A common strategy to reduce the energy barrier is the selection of a contact metal with a work function matching the work function of the semiconductor. However, the barrier height between a semiconductor and a metal is not only dependent

on the work-function difference between the semiconductor and the metal, but also on the density of interface states [36]. The selection of a metal with a matching work function is therefore beneficial, but does not necessarily lead to a small energy barrier height and a small contact resistance $R_C$.

### Contact doping

When the charge-carrier concentration in the semiconductor is large the depletion width in the semiconductor is small, according to equation 2.23, and the width of the energy barrier at the interface becomes very narrow. This can be achieved by selectively doping the contact areas of the semiconductor. For a narrow energy barrier, charge carriers may tunnel through the barrier [36] (see figure 5.1b), in addition to the thermionic emission process across the barrier. Contact doping is implemented routinely in modern silicon MOSFETs to achieve low-resistance contacts. In the presence of tunneling, equation 5.1 is modified and the contact resistance is described by

$$R_C \sim \exp\left(q\phi_B/E_{00}\right) \text{ where } E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_D}{\varepsilon_S m^*}}, \tag{5.3}$$

with the reduced Planck constant $\hbar$, the effective electron mass $m^*$ ($0.3\,m_0$ in ZnO [53]), and the dielectric constant of the semiconductor $\varepsilon_S$ (9 for ZnO [53]). $E_{00}$ is the characteristic energy [72] that determines the contribution of the tunnel current to the total current. For $E_{00} \gg kT$ the tunnel current dominates while for $E_{00} \ll kT$ the thermionic emission over the Schottky barrier dominates the current. For the as-grown ZnO nanowires ($N_D \sim 10^{19}\,cm^{-3}$), $E_{00} = 37\,meV$ is slightly larger than $k_BT = 25\,meV$. Therefore, the tunnel contribution cannot be neglected and the contact resistance is expected to be fairly small. However, the reduction of the charge-carrier concentration by annealing reduces the value of $E_{00}$ and thus the superlinear current increase given by equation 5.1 is observed for several of the annealed ZnO nanowires ($N_D \sim 10^{17} - 10^{18}\,cm^{-3}$, see section 6).

## 5.2 Effect of argon-plasma treatment in the source/drain regions of a ZnO-nanowire FET

As already mentioned above, the superlinear current increase is not observed for all FETs based on annealed ZnO nanowires. An important finding that helped to improve the transistor characteristics of the ZnO-nanowire FETs fabricated in the framework of this thesis was the observation that whenever a nonlinear current increase was measured, usually all FETs on the same substrate showed this behavior. This indicates that the contact properties are influenced by fluctuations in the fabrication process and are not an

intrinsic property of the wet-chemically grown ZnO nanowires. In the beginning of the experiments on the annealed ZnO nanowires, the least reproducible process step was the argon-plasma (Ar-plasma) treatment performed immediately prior to the evaporation of the aluminum contacts. This Ar-plasma treatment was performed in-situ in the metal evaporator. This had the advantage that the surface of the Ar-plasma-treated ZnO was not exposed to air prior to the aluminum deposition, but it had the disadvantage of offering poor control of the plasma parameters, since the electrodes of the plasma generator are always covered with various metals from the evaporations performed in the same chamber. Therefore, even though the nominal parameter settings were kept the same, the plasma treatment on different samples was not necessary identical.

To make the contacting of the annealed ZnO nanowires more reproducible, and to investigate the influence of the Ar-plasma on the FET characteristics, a stand-alone Oxford RIE plasma system is used. This has the disadvantage that the samples are exposed to the ambient atmosphere when transferred from the plasma chamber to the metal evaporator, but the Oxford RIE plasma system offers much better control and reproducibility of the plasma parameters (gas flow rate, pressure, power, time). The exposure to ambient air during the transfer is kept as short as possible and is usually about 5 minutes.

The effect of the Ar-plasma duration and power on the output characteristics of ZnO-nanowire FETs is investigated. Usually more than one FET is fabricated on the same substrate with the same plasma parameters. In order to compare the output characteristics of the FETs fabricated on the same substrate, the drain current of the individual FETs is normalized to the drain current at $V_{DS} = 1\,V$. This normalization is done to account for the different physical properties of the various nanowires (nanowire diameter, charge-carrier concentration, etc.) that affect the absolute drain currents of the nanowires. Further, the value of $V_{DS} = 1\,V$ is selected, since the influence of the contact resistance is expected to be most pronounced in the linear operation region of the transistor, i.e. at small drain-source voltages.

Figure 5.2 shows the normalized drain currents of ZnO-nanowire FETs from three samples subjected to the same Ar-plasma treatment (30 sccm Ar, 10 mTorr, 25 W) for different durations of 30 sec (b), 60 sec (c), and 180 sec (d). The curves plotted in blue (red) show the normalized drain current for $V_{GS} = 10\,V$ ($V_{GS} = 0\,V$). For positive $V_{GS}$, charge carriers are accumulated in the ZnO nanowire and the resistance of the ZnO nanowire is reduced. Consequently, the influence of the contact resistance is expected to be more pronounced at large positive gate-source voltages. However, the height of the Schottky barrier at the interface between the source and the channel can also depend on $V_{GS}$ since $V_{GS}$ modulates the Fermi level of the semiconductor and hence the work function difference between semiconductor and metal. This dependence causes higher energy barriers for smaller $V_{GS}$ and consequently a nonlinear drain current increase can be observed already

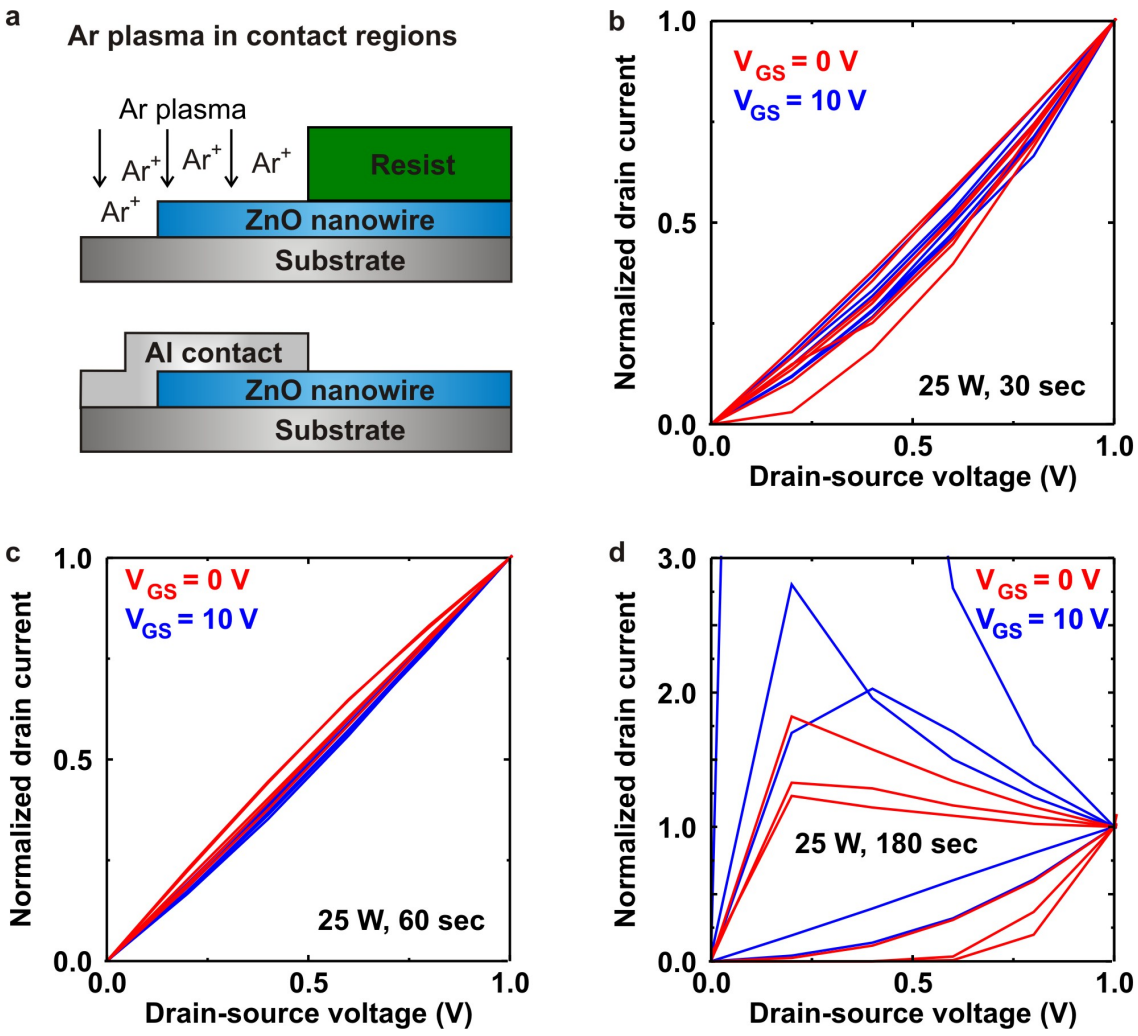


Figure 5.2: **Effect of the duration of an Ar-plasma treatment in the source/drain regions of a ZnO-nanowire FET.**
(a) Only the contact areas of the ZnO nanowires are subjected to an Ar-plasma (30 sccm Ar, 10 mTorr, 25 W) prior the evaporation of the aluminum contacts. The nanowire channel is protected by the electron-beam lithography resist. (b),(c),(d) Normalized output characteristics of ZnO-nanowire FETs measured at gate-source voltages of 0 V (red curves) and 10 V (blue curves). The output characteristics are strongly influenced by the duration of the Ar-plasma treatment. Figure (b) shows seven ZnO nanowires treated for 30 sec, figure (c) five ZnO nanowires treated for 60 sec and figure (d) six nanowires treated for 180 sec.

at smaller $V_{GS}$ (as can be seen e.g. in figure 5.1). Therefore, the normalized drain currents at $V_{GS} = 0\,V$ are also shown in figure 5.2 (red curves).

As can be seen, the output characteristics depend strongly on the Ar-plasma conditions. For a short Ar-plasma treatment (30 seconds), the drain current shows a superlinear dependence on the applied drain-source voltage. The superlinear increase is found for both gate-source voltages under investigation (red curves and blue curves). This indicates a notable contribution of the contact resistance to the output characteristics and therefore

a poor contact between the aluminum and the ZnO. For an Ar-plasma treatment of 60 seconds, the average output characteristics of the ZnO-nanowire FETs are improved. The red curves ($V_{GS} = 0\,V$) show an almost perfectly linear increase of the drain current. The blue curves measured at $V_{GS} = 10\,V$, still show a slightly superlinear increase, but less pronounced than for the ZnO nanowires treated for 30 seconds. For a longer plasma treatment (180 seconds), the current through the ZnO nanowires is strongly degraded (see table 5.1) and the output characteristics show a chaotic behavior. This indicates the onset of destruction of the ZnO nanowires by prolonged Ar-plasma treatments.

In order to compare the effect of the different plasma treatments and to quantify the superlinearities in the output characteristics, a parabolic fit to the normalized drain currents is performed. Although the thermionic emission theory predicts an exponential dependence of the drain current on the drain-source voltage, the assumption of a parabolic increase is reasonable for the small drain-source voltages under investigation. The fit was performed with the following equation:

$$I_D(V_{DS}) = A \cdot V_{DS} + B \cdot V_{DS}^2 = (1 - B) \cdot V_{DS} + B \cdot V_{DS}^2, \tag{5.4}$$

where the boundary conditions $I_D(1\,V) = 1$ and $I_D(0\,V) = 0$ are used to simplify the equation. The parameter B obtained from the fit gives a measure of the superlinearity of the drain current. For $B = 0$, the drain current is a perfectly linear function of $V_{DS}$, whereas $B = 1$ corresponds to a purely quadratic dependence on $V_{DS}$. The extracted B values for different plasma exposure times and plasma powers are summarized in table 5.1. The values obtained from the fits are compared to the values from a model nanowire FET with zero contact resistance modeled with the help of equation 2.15. The model nanowire FET is assumed to be realized in the global back-gate geometry on a 100 nm thick $SiO_2$ gate dielectric. The mobility of the model nanowire is 50 $\frac{cm^2}{Vsec}$, the channel length is 3 µm, and the flat-band voltage is -5 V. Note that the values for the parameter B obtained from the model nanowire are slightly negative instead of zero as expected for a purely linear increase. This is caused by the downward bending of the drain current due to the transition between the linear and the saturation regime (see figure 2.6 in the theory chapter). The B values presented in table 5.1 are the average values obtained from the fits to a total number of N nanowire FETs that have been fabricated with the according Ar-plasma exposure at the contacts. Depending on the plasma treatments, the B values vary form 0.7 to -0.06, which confirms the significant influence of the Ar-plasma treatment on the contact quality of the ZnO-nanowires FETs. According to table 5.1, the two plasma treatments providing the best contact performance are 60 sec / 25 W and 15 sec / 100 W. The last column in table 5.1 shows the average value of the drain current multiplied by the channel length for $V_{GS} = 10\,V$ and $V_{DS} = 1\,V$. The multiplication with the channel length is performed to compare the drain currents of FETs with different

| time / plasma power | number of ZnO nanowires N | $\overline{B}$ (@$V_{GS} = 0$ V) | $\overline{B}$ (@$V_{GS} = 10$ V) | $\overline{I_D \cdot L_{NW}}$ (@$V_{GS} = 10$V) |
|---|---|---|---|---|
| model nanowire | 1 | -0.10 | -0.03 | 6.6 µA·µm |
| 30 sec / 25 W | 7 | 0.44 | 0.40 | 3.3 µA·µm |
| **60 sec / 25 W** | 5 | **-0.06** | **0.10** | 8.5 µA·µm |
| 180 sec / 25 W | 6 | - | - | $10^{-4}$ to $10^{-1}$ µA·µm |
| 15 sec / 25W | 6 | 0.70 | 0.56 | 1.6 µA·µm |
| 15 sec / 50W | 2 | -0.01 | 0.22 | 12 µA·µm |
| **15 sec / 100W** | 7 | **-0.02** | **0.11** | 9.8 µA·µm |

Table 5.1: **Summary of the effect of Ar-plasma treatments on the quality of the contact between ZnO and aluminum.**
To quantify the superlinearity of the drain-current increase for small $V_{DS}$, the parameter B is introduced according to equation 5.4. A small value of B indicates a more linear drain current increase and a smaller contact resistance. The smallest B values are obtained for Ar-plasma treatments of 60 sec at a power of 25 W and Ar-plasma treatments of 15 sec at a power of 100 W. The latter parameters are therefore chosen to be the standard parameters for Ar-plasma treatments in the framework of this thesis.

channel lengths. Nevertheless, one should bear in mind that the individual ZnO nanowires might have different diameters, doping levels, and mobilities, which are not considered in detail. Therefore, the absolute values of the drain currents are to be treated with caution and can only give an indication whether the ZnO nanowires are damaged during the Ar-plasma exposure. This is observed for the ZnO nanowires treated for 180 sec at 25 W, which show strongly degraded drain currents. For all other plasma treatments, the average drain currents are within the same order of magnitude compared to the value predicted by the model nanowire.

On the basis of the results of these experiments, the **standard Ar-plasma parameters** selected for the contact treatment in this thesis are **30 sccm Ar, 10 mTorr, 100 W**, **and 15 sec**.

## 5.3 Effect of argon-plasma treatment in the channel region of a ZnO-nanowire FET

The initial purpose of the Ar-plasma treatment in the contact regions of the ZnO nanowires was to clean the ZnO-nanowire surface from contaminations (e.g. PMMA residue). However, the strong effect of the Ar-plasma on the contact quality between aluminum and ZnO cannot be explained by a simple cleaning of the nanowire surface alone. In order to elucidate the consequences of the Ar-plasma on the current transport in the ZnO nanowires, the channel of a ZnO-nanowire FET is exposed to an Ar-plasma. The parameters for the

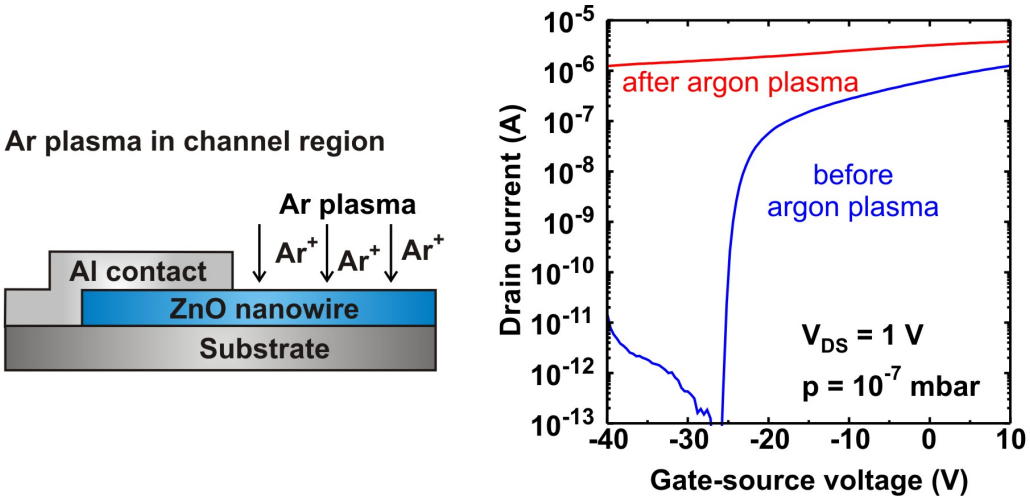


Figure 5.3: **Effect of an Ar-plasma treatment in the channel region of a ZnO-nanowire FET.**
Transfer characteristics of a ZnO-nanowire FET (L = 3 µm, $d_{NW}$ = 55 nm, $t_{SiO_2}$ = 100 nm) measured in high vacuum before (red curve) and after (blue curve) the FET channel was exposed to an Ar-plasma (30 sccm Ar, 10 mTorr, 100 W, 15 sec). The Ar-plasma treatment leads to a strong increase of the conductivity of the ZnO nanowire which is attributed to the generation of electron-donating oxygen vacancies at the nanowire surface.

plasma are the optimized values obtained in the previous section (30 sccm Ar, 10 mTorr, 100 W, 15 sec). In contrast to the Ar-plasma treatment performed in the contact regions of the ZnO nanowires (section 5.2), this time the surface of the whole substrate is exposed to the plasma. (During the plasma treatment in the S/D contact regions, the substrate was still covered with the PMMA layer and only the areas exposed to the electron beam were subjected to the plasma.) The Ar-plasma treatment renders the substrate surface of the $Si/SiO_2$ substrate highly hydrophilic and promotes the adsorption of a thin water layer. This water layer strongly affects the electrical characteristics of the FET (see section 7.2.2 of this thesis), which makes it difficult to evaluate the influence of the Ar-plasma treatment alone. To separate the effect of the water layer from the effect of the Ar-plasma treatment, the measurements presented in this section are done in high vacuum ($p = 10^{-7}$ mbar).

Figure 5.3 shows the transfer characteristics of a ZnO nanowire before the Ar-plasma treatment in the channel region (red curve) and after the Ar-plasma treatment (blue curve). The ZnO-nanowire FET has a channel length of 3 µm and the nanowire diameter is 55 nm. Both measurements are performed in high vacuum. As can be seen, the Ar-plasma treatment leads to a strong increase in the conductivity of the ZnO nanowire. While the peak transconductance $g_m$ of the plasma-treated ZnO nanowire extracted from the transfer characteristics is within an order of magnitude of that before the treatment ($g_m \sim 80$ nS at $V_{GS} = 10$ V), the charge-carrier concentration $n$ is strongly increased and the ZnO

nanowire cannot be switched into a non-conducting state. The transfer characteristics of the Ar-plasma-treated ZnO nanowire resemble the transfer characteristics of an as-grown ZnO nanowire (see figure 4.3 ). An increase of the charge-carrier concentration after an Ar-plasma treatment has been reported previously for epitaxially grown n-doped ZnO films. The increased charge-carrier concentration is believed to have its origin in the preferential sputtering of oxygen atoms from the ZnO lattice and removal of electron-capturing species from the ZnO nanowire surface [73, 74]. The atomic mass of argon (39,948 u) is larger than the atomic mass of oxygen (15,9994 u) and smaller than the atomic mass of zinc (65,409 u). Therefore, the momentum transfer from an argon atom to an oxygen atom is much larger than from an argon atom to a zinc atom, so that oxygen atoms are removed more easily. The same phenomenon of preferential sputtering of the lighter atomic compounds was also observed in GaN [75]. As discussed in section 4.4, oxygen vacancies can act as donors in ZnO and therefore can explain the observed increase of the charge-carrier concentration. Compared to the results on ZnO films from [73], the increase of $n$ by the Ar-plasma treatment is much more pronounced for the ZnO nanowires investigated in this thesis. This can be explained with the much larger surface-to-volume ratio of the ZnO nanowires compared to the ZnO films and supports the assumption of the creation of a highly doped layer at the surface of the ZnO. Comparable experiments on the effect of Ar plasma on the conductivity of ZnO nanowires performed by Ra et al. [76] also showed an increase of charge-carrier concentration from $n = 1 \cdot 10^{18}\,\mathrm{cm}^{-3}$ to $n = 4 \cdot 10^{18}\,\mathrm{cm}^{-3}$. This is in agreement with the findings of this thesis where the charge-carrier concentration of the ZnO nanowire obtained from the transfer characteristics of figure 5.3 are $n = 2 \cdot 10^{18}\,\mathrm{cm}^{-3}$ before the Ar-plasma treatment and $n = 7.1 \cdot 10^{18}\,\mathrm{cm}^{-3}$ after the plasma treatment. It should be mentioned that the calculation of a bulk charge-carrier concentration in connection with the Ar-plasma treatment is not strictly correct, since the observed increase of the charge-carrier concentration is expected to be restricted to the nanowire surface rather than to the nanowire bulk. Ra et al. also reported an increase of the mobility by over three orders of magnitude after the Ar-plasma treatment, which is not observed for the ZnO nanowires investigated in this thesis. The possible reason for this discrepancy might be that the experiments of Ra et al. are performed in ambient atmosphere which can lead to a large overestimation of the mobility due to the influence of water on the sample surface (see section 7.2.2).

## 5.4 Effect of oxygen-plasma treatment in the source/drain regions of a ZnO-nanowire FET

In the framework of this thesis the investigation of the effect of an oxygen-plasma ($O_2$ plasma) treatment is especially interesting with regard to the top-gate FETs presented in

chapter 8. The $O_2$-plasma treatment is utilized to clean and prepare the surface of the ZnO nanowires for the self-assembly of alkylphosphonic acid molecules with the purpose of covering the nanowire with a gate dielectric or a passivation layer. Although in this case the $O_2$-plasma treatment is performed only in the FET channel region, the effect of an $O_2$-plasma treatment in the source/drain regions is also investigated. It has been reported in the literature that an $O_2$-plasma treatment in the source/drain regions prior to metal deposition leads to improved performance of $In_2O_3$-nanowire FETs [68], similar to the observations made for Ar-plasma treatments in this thesis. The improved contact performance is attributed to a reduction of the Schottky-barrier height at the interface between $In_2O_3$ and aluminum.

In order to compare the effect of an Ar-plasma treatment in the source/drain regions with that of an $O_2$-plasma treatment in the source/drain regions in terms of their effect on the FET performance, ZnO nanowires are dispersed on a $Si/SiO_2$ wafer ($t_{SiO_2}$ = 100 nm). First, two contacts are patterned at the ends of a nanowire as described in section 4.2 and the source/drain regions are exposed to an Ar-plasma (30 sccm Ar, 10 mTorr, 100 W, 15 sec) prior to metal deposition (see figure 5.4a). Then, another EBL step is used to pattern a third contact in the center of the ZnO nanowire. In contrast to the previously fabricated Ar-contacts, the surface of the ZnO nanowire in the region of the third contact is exposed to an $O_2$ plasma (30 sccm $O_2$, 15 mTorr, 50 W, 20 sec) prior to the deposition of 80 nm thick aluminum. Depending on which of the three contacts are employed as source and drain, a comparison between an FET operated with two Ar-contacts and an FET operated with one Ar-contact and one $O_2$-contact is performed on the same nanowire.

Figure 5.4b shows the transfer and output characteristics of two ZnO-nanowire FETs fabricated on the same ZnO nanowire operated with two Ar-contacts (blue curve) and operated with an Ar-contact as source and an $O_2$-contact as drain (red curve). For better comparison, the drain currents are multiplied with the corresponding channel length of the FETs. Both FETs have similar threshold voltage around $-7\,V$. However, the drain current of the Ar-Ar contact FET for $V_{GS} > -1\,V$ is larger compared to the drain current of the Ar-$O_2$ contact FET. This indicates that the influence of the contact resistance is more pronounced for the Ar-$O_2$ contact FET, and this becomes even more apparent when considering the output characteristics of the two FETs. While the Ar-Ar contact FET shows a linear dependence of the drain current as expected for negligible contact resistance, the Ar-$O_2$ contact FET shows a sligthly superlinear increase and a reduced drain-current level over the entire $V_{DS}$ range. Using the parameter B introduced in section 5.3 to quantify the superlinear drain-current increase, the average value of B for three Ar-Ar contact FETs is $\overline{B}_{ArAr} = -0.03$, and for six Ar-$O_2$ contact FETs is $\overline{B}_{ArO_2} = 0.2$. Therefore, the $O_2$-plasma treatment leads to a superlinear drain-current increase, comparable to the values obtained for the 15 sec/50 W Ar-plasma treatment (see table 5.1). By systematically

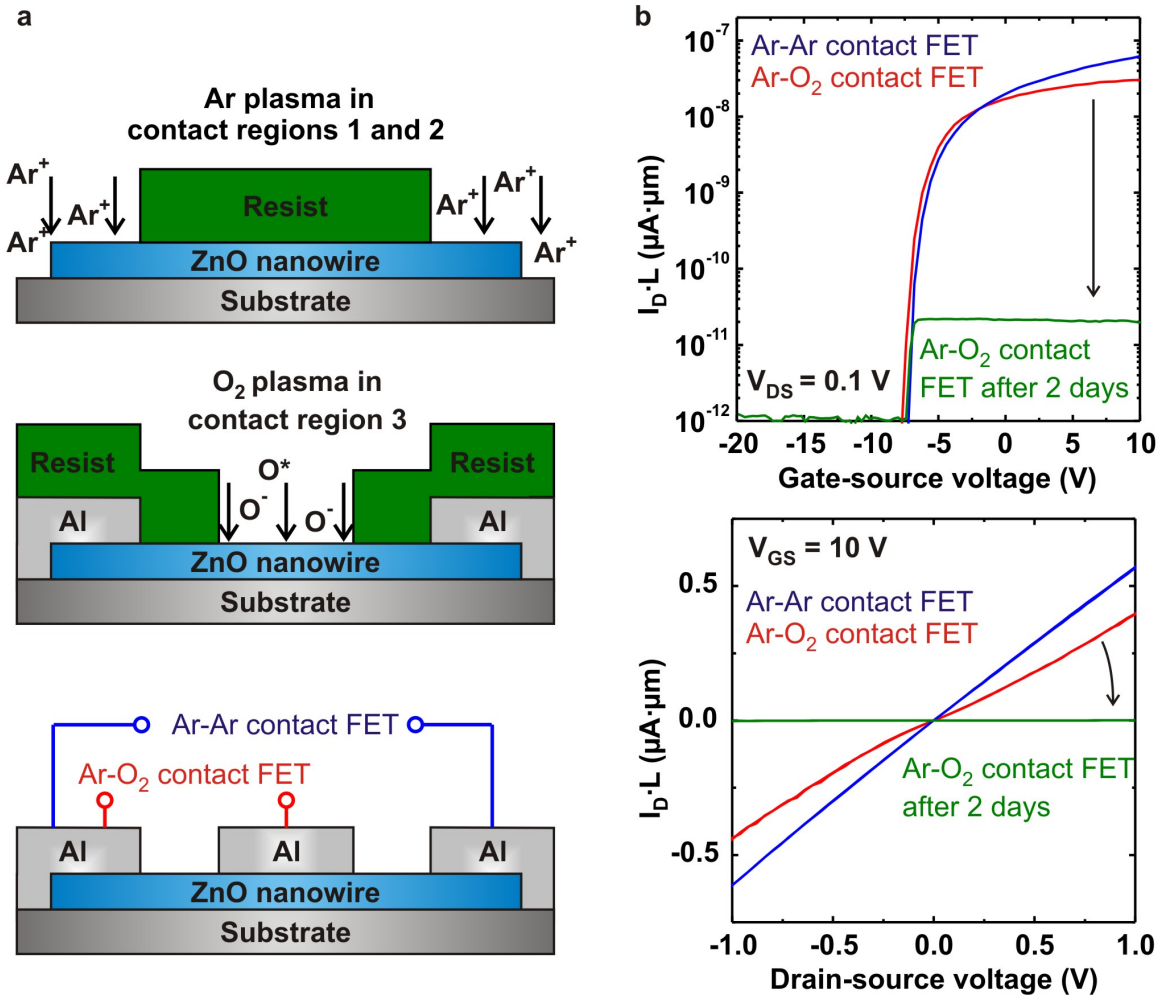


Figure 5.4: **Effect of Ar-plasma and $O_2$-plasma treatments in the source/drain contact regions of a ZnO-nanowire FET.**
(a) Schematic fabrication process for the comparison between an FET where both the source contact region and the drain contact region are exposed to an Ar plasma prior to the aluminum evaporation (Ar-Ar contact FET) and an FET where the source contact region is exposed to an Ar plasma while the drain contact region is exposed to an $O_2$ plasma prior to the aluminum evaporation (Ar-$O_2$ contact FET). (b) Transfer and output characteristics of an Ar-Ar contact FET (blue) and an Ar-$O_2$ contact FET (red) manufactured on the same ZnO nanowire. The maximum on-current of the Ar-$O_2$ contact FET is slightly reduced when measured immediately after fabrication, and strongly reduced when measured again after two days in ambient air (green curve). This indicates a strong contribution of the contact resistance on the Ar-$O_2$ contact FET.

varying the plasma parameters, it might be possible to further improve the performance of the $O_2$-contact in a similar way as observed for the Ar-plasma treatment. However, this was not investigated in the framework of this thesis, due to reasons that will be discussed in more detail in the following.

## Formation of interfacial aluminum oxide layer

After two days of storage in ambient air, the FETs are characterized again. The resulting transfer characteristics of the Ar-$O_2$ contact FET are shown in figure 5.4a (green curve). The drain current is strongly reduced by over 3 orders of magnitude compared to the red curve obtained immediately after fabrication. Although the threshold voltage of the FET is unchanged ($-7\,V$), the drain current saturates at $\sim$10 pA for $V_{GS} > -7\,V$. The observed behavior can be explained by a large contact resistance that limits the drain current and impedes the accumulation of charge carriers in the ZnO-nanowire FET. In sharp contrast, the drain current of the Ar-Ar contact FET (not shown here) is even sligthly increased (possibly due to different ambient conditions). Therefore, the origin of the large contact resistance is expected to be located at the interface between the ZnO nanowire and the aluminum of the $O_2$-contact. A possible explanation for the large contact resistance is the formation of an insulating aluminum oxide layer ($AlO_x$) in the vicinity of the $O_2$-contact interface.

In order to determine the structural composition of the $O_2$-contacts and the Ar-contacts, the contact cross section is analyzed by transmission electron microscopy (TEM). The samples for the TEM analysis are prepared with the help of a focused ion beam (FIB). In preparation for the FIB cutting, a protective layer consisting of metal-organic platinum is readily deposited on top of the structure with the help of an electron beam. Then, the FIB is used to cut a 50 nm thick lamella out of the aluminum-covered ZnO nanowire. The lamella is oriented perpendicular to the ZnO-nanowire FET channel, and shows the cross section of the ZnO nanowire contact region. In figure 5.5 the results of the TEM analysis are presented. The images and graphs in the upper row corresponds to a 50 nm thick ZnO nanowire exposed to an $O_2$ plasma prior to the aluminum evaporation, while the images in the lower row correspond to a 35 nm thick ZnO nanowire exposed to an Ar plasma prior to the metal evaporation. Both ZnO nanowires are deposited on $SiO_2$ and are covered with an 80 nm thick aluminum layer. Figure 5.5a shows the TEM bright-field images of the corresponding TEM lamellae. Since the evaporated aluminum forms a polycrystalline layer, the contrast within the aluminum fluctuates due to the different distinct orientations of individual grains. The brindle structure on top of the aluminum is the metal-organic platinum coating. Due to the hexagonal cross-section of the ZnO nanowires, only three of the six facets are covered by the aluminum, since the metal is evaporated perpendicular to the substrate. This leads to the formation of a hollow region next to the lower facets of the ZnO nanowire (bright structures in figure 5.5a).

The TEM makes it possible to identify specific elements by their characteristic x-ray radiation and to map the distribution of the elements within the lamellae. Figure 5.5b shows a zoom-in of the elemental map of oxygen around the ZnO nanowires. The oxygen signal is most pronounced in the $SiO_2$ substrate and next to the lower facets of the ZnO

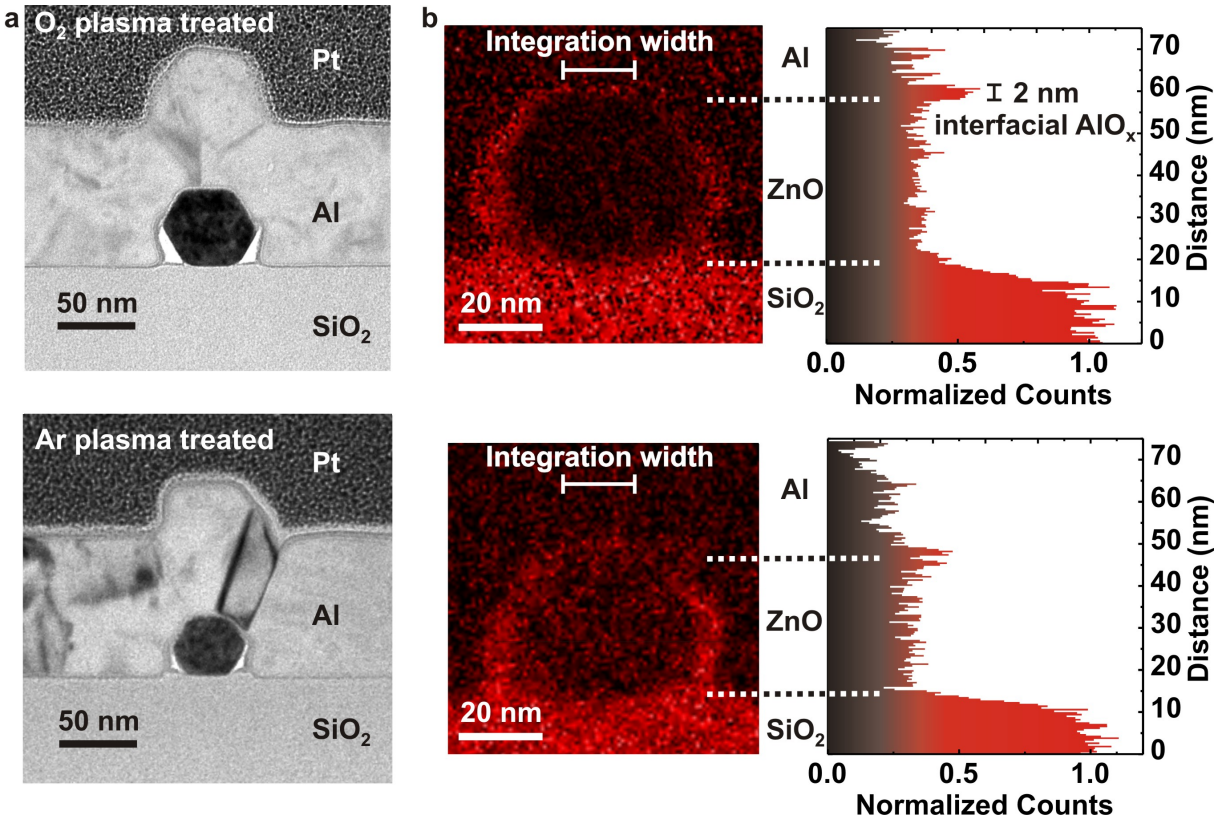


Figure 5.5: **TEM analysis of the ZnO nanowire/aluminum interface.**
The images in the upper row correspond to a ZnO nanowire exposed to an $O_2$ plasma prior to Al evaporation, and the images in the lower row to a ZnO nanowire exposed to an Ar plasma prior to aluminum evaporation. (a) Cross-section TEM bright-field image of the ZnO nanowires on a $SiO_2$ substrate. The hexagonal ZnO nanowires are covered by 80 nm thick aluminum. (b) Elemental map of oxygen taken from the cross-sectional images. The graphs on the right side show the oxygen profile obtained by integrating the elemental map of oxygen parallel to the top facet of the ZnO nanowires over the indicated integration width (16 nm). The oxygen profiles of both ZnO nanowires show an increased oxygen signal at the interface between ZnO and Al. However, the signal of the $O_2$-plasma-treated ZnO nanowire (upper profile) is more pronounced than that of the Ar-plasma-treated ZnO nanowire (lower profile), indicating the formation of an interfacial aluminum oxide layer in the case of an $O_2$ plasma. The estimated thickness of the interfacial aluminum oxide layer is 2 nm.

nanowires. For both nanowires the oxygen signal emerges from the hollow region next to the lower facets and also from the aluminum opposing the lower facets. The appearance of an oxygen signal in the aluminum indicates the formation of aluminum oxide. Since the hollow region permits oxygen to penetrate the structure, the formation of aluminum oxide is expected next to these regions and is independent of the plasma treatment.

To investigate the effect of the plasma treatment, the interface between the top facet of the ZnO nanowires and the aluminum is analyzed in more detail. The top facet of the ZnO nanowires is in intimate contact with the evaporated aluminum and therefore no

penetration of oxygen from the hollow regions is expected at this interface. Figure 5.5b also shows the profile of the oxygen signal obtained by integrating parallel to the top facet of the ZnO nanowires. The integration width (16 nm) is indicated in figure 5.5b. For a better comparison, the integrated signal was normalized to the oxygen signal of the $SiO_2$ layer. The $SiO_2$/ZnO and ZnO/Al interfaces are indicated by the dotted lines.

The oxygen profiles of both structures show an increased oxygen signal at the interface between ZnO and Al, however, the signal in case of the $O_2$-plasma treatment (figure 5.5c upper image) is more pronounced than for the Ar-plasma treatment. Together with the results obtained from the electrical characterization, the increased oxygen signal is interpreted as an indication for the formation of an interfacial aluminum oxide (IAO) layer at the interface between the $O_2$-plasma-treated ZnO nanowire and the aluminum. The aluminum oxide forms an insulating shell around the ZnO nanowire and accounts for the reduced drain-current observed for the Ar-$O_2$ contact FET compared the Ar-Ar contact FET. From the oxygen profile in figure 5.5c the thickness of this interfacial aluminum oxide layer is determined to be 2 nm. It is assumed that oxygen atoms diffuse out of the ZnO into the aluminum and lead to the formation of the IAO layer. The out-diffusion of oxygen from ZnO to aluminum has been reported previously [77] and is consistent with the smaller enthalpy of formation for $Al_2O_3$ ($\triangle H_f = -1657\,kJ/mol$ [78]) compared to ZnO ($\triangle H_f = -350\,kJ/mol$ [78]). Although the oxygen map of the Ar-plasma-treated ZnO nanowire also shows a small increase of the oxygen signal at the interface, the electrical measurements show no indication for the formation of an IAO layer. Based on the considerations of section 5.3 the absence of the IAO layer can be ascribed to the preferential sputtering of oxygen atoms from the ZnO lattice by the Ar-plasma treatment. It is believed that the oxygen-deficient surface of the Ar-plasma-treated ZnO nanowire impedes the formation of an IAO layer. In contrast, the $O_2$-plasma-treated surface is believed to be enriched with oxygen atoms (see also following section 5.4), which accelerates the interfacial reaction [79, 80, 81].

It should be mentioned that the interpretation of the oxygen profiles has to be taken with caution for the following reasons. The absolute signal amplitude obtained for the oxygen map is rather low and therefore the oxygen signal at the ZnO/Al interface is close to the noise level of the measurement (the noise level obtained from the oxygen-free aluminum layer is $\sim 0.2$ normalized counts). To increase the signal-to-noise ratio, a longer exposure of the sample to the electron beam would be required. However, this would cause a drift of the sample during the prolonged exposure and therefore a broadening of the investigated structures. Further, the absolute amplitude of the oxygen signal also depends on the relative orientation of the investigated structure to the incident electron beam, as can be seen from the contrast variations observed in the polycrystalline aluminum layer in figure 5.5a. Furthermore, one should bear in mind that the interfacial layers are very thin

compared to the lamella (50 nm). Hence, a small tilt of the sample with respect to the electron beam can also cause signal variations. To account for the multiple influences on the oxygen signal, several measurements of the TEM lamellae have been taken (also by varying the sample tilt angle) for the analysis of the IAO layer, and figure 5.5a and b shows two representative images.

Finally, it is important to note that the observed contact degradation of the $O_2$-contacts is sometimes also observed for the Ar-contacts. However, this usually happens on a much longer time scale of several weeks and may be another indication for the suppression of the oxygen diffusion from the ZnO to the aluminum as a result of the Ar-plasma treatment.

## 5.5 Effect of $O_2$-plasma treatment in the channel region of a ZnO-nanowire FET

As already mentioned in the preceding section, the primary purpose of the $O_2$-plasma treatment in the scope of this thesis is to clean and prepare the surface of the ZnO nanowires for the self-assembly of alkylphosphonic acid molecules (see chapters 7 and 8). In order to determine the consequences of an $O_2$-plasma treatment on the conductivity of the ZnO nanowires, the channel of a ZnO-nanowire FET is repeatedly exposed to an $O_2$ plasma. The parameters for the $O_2$ plasma are the same as in the preceding section (30 sccm $O_2$, 15 mTorr, 50 W, 20 sec). Similar to the Ar-plasma treatment, the $O_2$-plasma treatment increases the density of hydroxyl groups on the sample surface and renders the substrate hydrophilic. Hence the measurements presented in this section are again performed under high vacuum (pressure p = $10^{-7}$ mbar) to avoid influences from adsorbed water on the device characteristics.

Figure 5.6a shows the transfer characteristics of a ZnO-nanowire FET before exposure (blue curve), after one exposure (red curve), after two exposures (green curve), and after three exposures (orange curve) to the $O_2$ plasma. In contrast to the Ar-plasma treatment of the channel region (see figure 5.3), the $O_2$-plasma treatment of the channel region produces a large shift of the threshold voltage towards more positive values (compare blue and red curve in figure 5.6a). This indicates a reduction of the amount of free charge carriers in the ZnO nanowire after the $O_2$-plasma treatment. The positive shift is attributed to the formation of electron-capturing oxygen species on the surface of the ZnO nanowires. Ra et al. reported similar observations and found an increased concentration of $O^-$and $O_2^-$ on the ZnO nanowire surface after $O_2$-plasma exposure with the help of Secondary Ion Mass Spectroscopy [81]. These observations support the assumption made in the preceding section of an oxygen-enriched surface of the ZnO nanowire after an $O_2$-plasma treatment that promotes the formation of an interfacial aluminum oxide layer in the contact regions.

While the first $O_2$-plasma treatment produces a large positive threshold-voltage shift, the

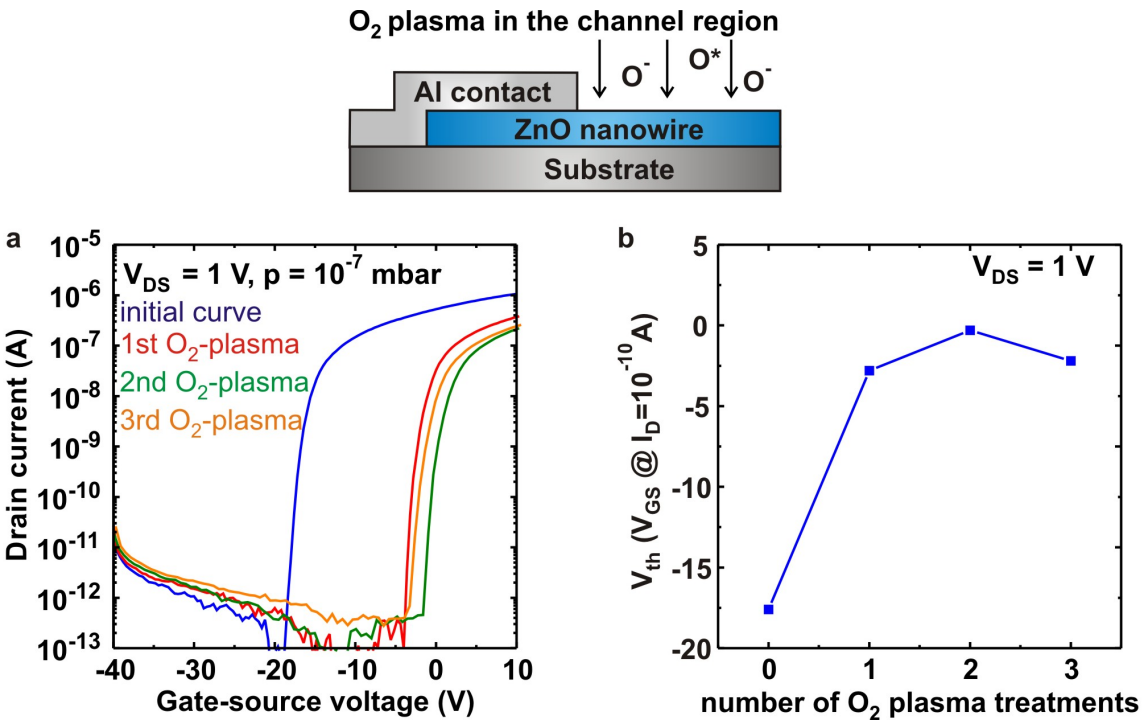


Figure 5.6: **Effect of an Ar-plasma treatment in the channel region of a ZnO-nanowire FET.**
(a) Transfer characteristics of a ZnO-nanowire FET measured in high vacuum before and after several subsequent $O_2$-plasma treatments. The first $O_2$-plasma treatment shifts the threshold voltage towards more positive values (compare blue and red curve). This indicates a reduction of the amount of free charge carriers in the ZnO nanowire and is attributed to the formation of electron-capturing species on the surface of the ZnO nanowire. Subsequent $O_2$-plasma treatments (green and orange curve) do not cause a further shift of the threshold voltage, which indicates a saturation of the surface with electron-capturing species after the first plasma treatment. (b) The threshold voltage of the FET extracted at a drain current of 0.1 nA shows a shift of 14 V towards more positive values after the first exposure to the $O_2$-plasma treatment and a saturation around ∼-2.5 V for the subsequent treatments.

effect of the second and third $O_2$-plasma treatments is insignificant. (compare red, green and orange curve in figure 5.6a). The blue curve in figure 5.6b shows the evolution of the threshold voltage (defined as the $V_{GS}$ at a drain current of 0.1 nA) versus the number of $O_2$-plasma treatments.

## 5.6 Summary of the effects of argon and oxygen-plasma treatments

| plasma type | FET region | effect |
|---|---|---|
| Ar plasma | S/D contacts | improvement of the electrical performance of the contact between aluminum and ZnO |
| Ar plasma | channel | increase of the charge-carrier concentration due to preferential sputtering of oxygen from ZnO |
| $O_2$ plasma | S/D contacts | formation of an insulating interfacial aluminum oxide layer at the interface between aluminum and ZnO |
| $O_2$ plasma | channel | reduction of charge-carrier concentration due to formation of electron-capturing species on the surface of the nanowires |

# 6 FETs based on annealed ZnO nanowires

The annealing of the as-grown ZnO nanowires and the optimization of the Ar-plasma treatment in the contact regions paves the way for the fabrication of ZnO-nanowire FETs with useful static performance. In the following section the electrical characteristics of the FETs manufactured with annealed ZnO nanowires are investigated in detail. Although the charge-carrier concentration in the ZnO nanowires is greatly reduced by the anneal, most of the annealed ZnO nanowires are conducting without external accumulation of charge carriers ($V_{GS} = 0$ V). In section 6.2 it is discussed whether this conductivity stems from the nanowire surface or the nanowire bulk. On the basis of this discussion the temperature dependence of the electrical characteristics of a ZnO-nanowire FET is investigated in section 6.3.

## 6.1 Electrical characteristics of FETs based on annealed ZnO nanowires

Figure 6.1 shows the transfer and output characteristics of an FET based on a ZnO-nanowire annealed at 600°C in air with a channel length of 5.5 µm and a nanowire diameter of 51 nm realized on a 200 nm thick $SiO_2$ gate dielectric. The measurement is performed in ambient air. From the transfer characteristics at $V_{DS} = 10$ V a peak transconductance of 300 nS, an on/off current ratio of $10^7$ and a subthreshold slope of 500 mV/decade are extracted. With the gate capacitance given by equation 2.31 the field-effect mobility in the saturation regime is calculated to 40 $\frac{cm^2}{Vs}$. The output characteristics display a linear drain-current increase for small drain-source voltages owing to the ohmic contacts obtained through the Ar-plasma treatment (see section 5.2). For larger $V_{DS}$ the drain current saturates as expected from basic transistor theory (see chapter 2). The device presented in figure 6.1 shows only a negligible hysteresis between the forward and the backward sweep. It is important to point out that this is not a common feature of the wet-chemically grown ZnO nanowires investigated in this thesis. Forward and backward hysteresis are sometimes observed in the transfer characteristics for different ZnO-nanowires FETs even when these are manufactured on the same substrate and independent of the ambient conditions. Possible origins of the hysteresis are mobile ions introduced into the ZnO nanowires during the wet-chemical growth, defects at the interface between ZnO and $SiO_2$, as well as adsorption of electron-capturing species on the surface of the nanowires during the measurements. However, the origin of the hysteresis in the wet-chemically grown ZnO nanowires is not investigated in this thesis, since the differences between the individual nanowire FETs makes a systematic analysis difficult.

The field-effect mobility of the ZnO-nanowire FET presented in figure 6.1 is representa-

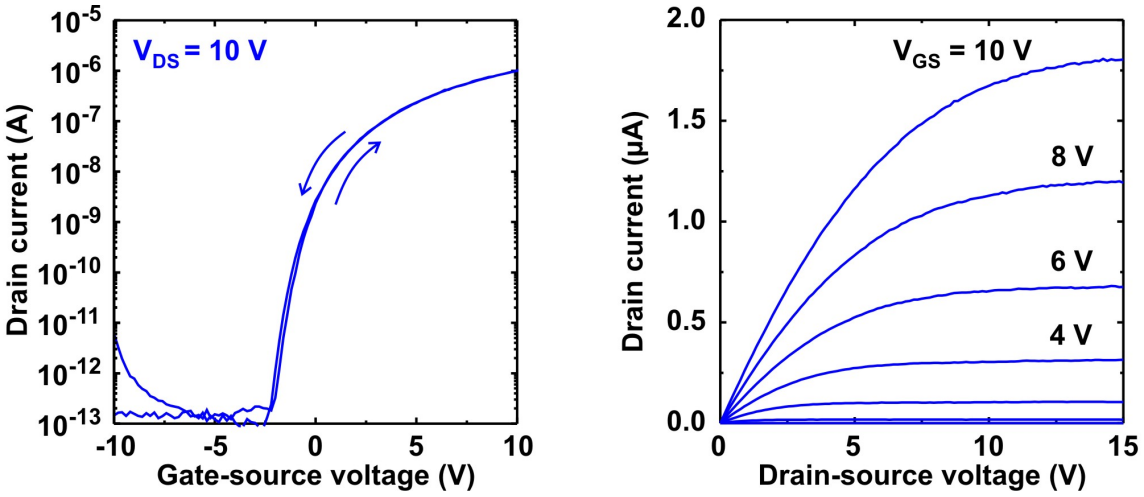


Figure 6.1: **Transfer and output characteristics of a ZnO-nanowire FET.** From the transfer characteristics at $V_{DS} = 10\,V$, a transconductance of 300 nS, an on/off drain current ratio of $10^7$ and a subthreshold slope of 500 mV/decade are extracted ($L = 5.5\,\mu m$, $d_{NW} = 51$ nm, $t_{SiO_2} = 200\,nm$). The maximum field-effect mobility of the ZnO nanowire is 40 $\frac{cm^2}{Vs}$ . Due to the Ar-plasma treatment in the contact regions, the output characteristics show a linear increase of the drain current and no indication of a contribution of the contact resistance to the overall device resistance.

tive for the wet-chemically grown ZnO nanowires. The typical values obtained for the back-gate FETs are around 20-50 $\frac{cm^2}{Vs}$. This is smaller than the room-temperature Hall mobility of single-crystalline ZnO (200 $\frac{cm^2}{Vs}$ [26]), but comparable to the field-effect mobilities reported for ZnO thin-film FETs [82] which are usually lower than the Hall mobilities due to trapping or surface scattering [83]. Field-effect mobilities of ZnO-nanowire FETs reported in the literature are spread over a wide range, from values as low as 1 $\frac{cm^2}{Vs}$ [17] to much higher values of up to 4000 $\frac{cm^2}{Vs}$ [84]. Therefore, a comparison to other results is difficult. There are several reasons for the wide range of field-effect mobilities in the literature. One reason is that there are numerous growth methods (see chapter 3) which yield ZnO nanowires with different properties (defect concentration, doping concentration, crystal quality). Further, different nanowire geometries (different diameters, different channel length) and different FET geometries (back-gate [85], top-gate [86], surrounding gate [17]) are reported in the literature. The distinct geometry of the ZnO nanowire and of the FET can greatly influence the capacitance of the FET and therefore also the extracted field-effect mobility. Finally, the ambient conditions during the measurement (UV irradiation [87], humidity [88]) affect the electrical properties of ZnO, especially at the surface of the material. Due to the large surface-to-volume ratio of nanowires these effects can be crucial and strongly influence the conductivity and mobility of the material (see also chapter 7). For ZnO-nanowire FETs realized in a global $SiO_2$ back-gate geometry (i.e. similar to the geometry utilized in this thesis) values between 6 $\frac{cm^2}{Vsec}$ and 150 $\frac{cm^2}{Vsec}$are found in the literature [85, 89, 90, 91, 92]. Therefore, the field-effect mobilities obtained

for the wet-chemically grown ZnO nanowires are well within the range of the reported values and can compete with those of ZnO-nanowires FETs grown by other methods.

## 6.2 Surface conduction versus bulk conduction

A common feature of most FETs manufactured using annealed ZnO nanowires is that the nanowires are intrinsically conducting. Negative gate-source voltages up to -15 V are sometimes required to switch the ZnO nanowires into a non-conducting state (so that $I_D < 10^{-12}$ A). The observation of a finite conductivity at zero gate bias can be explained either by a charge-accumulation layer at the semiconductor/insulator interface or by residual doping in the bulk of the annealed ZnO nanowires.

### Surface accumulation layer

In the framework of the thin-film transistor theory, the semiconductor bulk is assumed to be undoped and therefore insulating in the absence of charge accumulation induced by an external potential. Therefore, any conductivity observed at zero $V_{GS}$ must originate from a charge-accumulation layer at the semiconductor/insulator interface (or more generally at the surface of the semiconductor). This accumulation of charges is due to a non-zero surface potential at the interface (e.g. due to fixed charges in the gate dielectric or a work function difference between the semiconductor and the gate metal [36]). In the TFT theory this non-zero surface potential is accounted for by the introduction of the so-called flat-band voltage $V_{FB}$. The non-zero surface potential leads to a shift of the transfer characteristics along the $V_{GS}$ axis, but does not change the general FET operation in the accumulation regime (i.e. the conductivity is still restricted to a thin layer at the semiconductor/insulator interface and the capacitance of the FET is constant). In the following discussion this model will be referred to as **surface conduction** and a surface charge-carrier density $Q_{Surf} = q \cdot N_{Surf}\,[\frac{Cb}{cm^{-2}}]$ will be introduced. Under the assumption that the surface-charge density in different nanowires is identical at $V_{GS} = 0$ V, the threshold $V_{th}$, given by the gate-source voltage necessary to compensate the charge induced by the surface potential, is given by [41]:

$$V_{th}(d_{NW}) = Q/C = -q \cdot N_{Surf} \cdot 4 \cdot d_{NW} \cdot L_{NW}/C_i(d_{NW}). \tag{6.1}$$

For the sake of simplicity, the ZnO nanowire cross-section is assumed to be a square for the calculation of the total charge on the nanowire.

### Residual doping concentration

Another possible origin of the finite conductivity of the ZnO nanowires at $V_{GS} = 0\,V$ is the assumption of a residual bulk conductivity in the ZnO nanowires. This residual bulk conductivity is caused by dopants that are not passivated by the annealing (see section 4.4). The assumption of a residual bulk conductivity means that there will be a transition in the operation mode from accumulation to depletion when the gate-source voltage is swept from positive to negative values (see figure2.7). The transition between the two regimes occurs at $V_{GS} = V_{FB}$. In the following discussion this model will be referred to as **bulk conduction,** and a bulk charge-carrier density $Q_{Bulk} = q \cdot N_{Bulk}[\frac{Cb}{cm^{-3}}]$ will be introduced. It is expected that the bulk charge-carrier density equals the concentration of dopants $N_D$ at room temperature: $N_{Bulk} = N_D$. Again assuming that the charge density in different nanowires is equal, $V_{th}$ in the model of bulk conduction is given by (see equation 2.26) [41, 93]:

$$V_{th}(d_{NW}) = -\frac{q \cdot N_D \cdot d_{NW}^2}{2 \cdot \varepsilon_S \varepsilon_0} - \frac{q \cdot N_D \cdot d_{NW}^2 \cdot L_{NW}}{C_i(d_{NW})}. \tag{6.2}$$

The first term of equation 6.2 refers to the voltage drop across the fully depleted semiconductor (see equation 2.23), and the second term describes the voltage drop across the gate insulator.

Therefore, the models of surface conduction and bulk conduction predict different relationships for the threshold voltage as a function of the nanowire diameter.

In order to determine whether the conductivity of the wet-chemically grown ZnO nanowires is better described by surface conduction or by bulk conduction, ZnO nanowires with different diameters ranging from 25 nm up to 100 nm are characterized in an FET geometry. The threshold voltage $V_{th}$ of the ZnO-nanowire FETs is extracted from the transfer characteristics measured at $V_{DS} = 1\,V$ and is defined as the gate-source voltage at which the drain current is 1 nA. All measurements are performed in high vacuum to avoid influences of the ambient on the ZnO nanowires.

The threshold voltage $V_{th}$ extracted from the measurements are shown in figure 6.2a (black circles). The data points are fitted with the according equations 6.1 and 6.2 for $V_{th}$ derived for the different conduction mechanisms surface and bulk conduction. The free parameters of both fits are the charge-carrier concentrations $N_D$ and $N_{Surf}$. Figure 6.2a shows the resulting fits for the model of surface conduction (green curve) and for the model of bulk conduction (red curve). The charge-carrier concentrations extracted from the fits are $N_{Surf} = (2.4 \pm 0.1) \cdot 10^{12}\,cm^{-2}$ and $N_D = (4.0 \pm 0.4) \cdot 10^{17}\,cm^{-3}$. The data extracted from the transfer characteristics follow the general trend of more negative threshold voltages with increasing nanowire diameter. However, this trend is predicted by both conduction models. Due to the rather broad distribution of the extracted thresh-

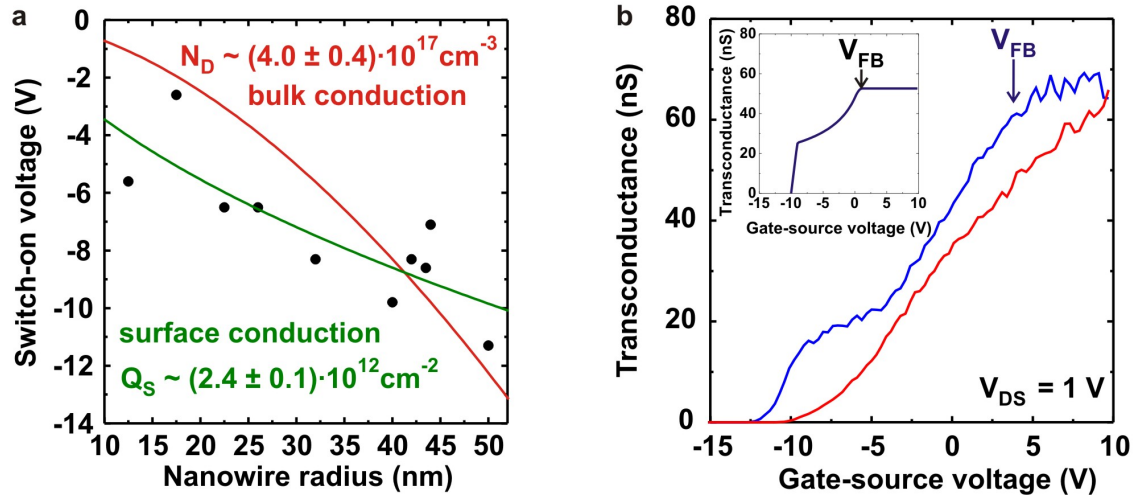


Figure 6.2: **Surface conduction versus bulk conduction.**
(a) Threshold voltages of ZnO-nanowire FETs extracted from the transfer characteristics measured in high vacuum as a function of the nanowire diameter. The green curve shows a fit of the data with the model of surface conduction and the red curve shows a fit of the data with the model of bulk conduction. Due to the broad distribution of data points, neither of the two models describes the data with sufficient accuracy. (b) Transconductance as a function of the gate-source voltage for two ZnO-nanowire FETs with a diameter of 100 nm (blue curve) and 84 nm (red curve). The blue curve, which resembles the behavior predicted for operation in the depletion regime (see inset), allows the flat-band voltage to be identified ($V_{FB} = 3$ V) and the charge-carrier concentration to be determined with useful accuracy. In contrast, the red curve does not allow the flat-band voltage to be determined.

old voltages, neither of the fitted curves describes the data with an accuracy that would justify a conclusion regarding the valid conduction mechanism. The broad distribution of the extracted threshold voltages indicates that the assumption of a constant charge-carrier concentration in the annealed ZnO nanowires is an idealization that is not observed experimentally.

Another difficulty in the analysis of the conductivity of the annealed ZnO nanowires becomes obvious from figure 6.2b. As already discussed in section 2.2.7, when an FET is operated in the depletion regime (model of bulk conduction), the capacitance and hence the transconductance of the FET are expected to be a function of the gate-source voltage (see figure 6.2 and inset of figure 6.2b). In figure 6.2b the transconductance of two ZnO nanowires measured under high-vacuum conditions at a drain-source voltage of 1 V are shown. The blue curve corresponds to a ZnO nanowire with a diameter of 100 nm and the red curve to a ZnO nanowire with a diameter of 84 nm. The curve depicted in blue resembles the behavior expected for an FET operating in the depletion regime, as can be seen by comparison to the transconductance obtained from theory (inset in figure 6.2b).

A step-like increase of the transconductance is followed by a region of superlinear increase. The superlinear increase is attributed to the reduction of the depletion width in the ZnO nanowire and the accompanied increase of the total device capacitance. For $V_{GS} > 3\,V$ the transconductance saturates, which indicates that the depletion width has become zero and no further increase of the capacitance is expected for $V_{GS} > 3\,V$. According to the theory this indicates the transition from the depletion regime to the accumulation regime and the gate-source voltage at the transition point corresponds to the flat-band voltage $V_{FB} \approx 3\,V$. A positive flat-band voltage indicates the presence of a thin depletion layer at the surface of the nanowire under equilibrium conditions.

The determination of $V_{FB}$ is crucial to determine the charge-carrier concentration $n$ with satisfying accuracy. However, the determination of $V_{FB}$ is only possible for a minority of the investigated ZnO nanowires, and for the sake of simplicity $V_{FB} = 0\,V$ was assumed for the determination of the threshold voltage data in figure 6.2a. This may introduce a substantial error in the analysis.

The red curve depicted in figure 6.2 shows an example of a ZnO nanowire where the transconductance as a function of $V_{GS}$ does not show the characteristic behavior expected for an FET operating in the depletion regime. Rather, the transconductance shows a monotonic increase over the whole range of gate-source voltages. Such a behavior is predicted by neither of the two models, which makes it difficult to determine whether the ZnO nanowire displays surface or bulk conduction.

A possible explanation for this kind of behavior is a gate-bias dependence of the field-effect mobility $\mu \rightarrow \mu(V_{GS})$ in the ZnO nanowire. Such a dependence is observed e.g. in organic transistors [94, 95], and in TFTs based on amorphous silicon [96] and can be explained by the so-called multiple trapping and release (MTR) model. The MTR model and its applicability to FETs based on ZnO nanowires will be discussed in more detail in the following section. A gate-bias dependent mobility makes it extremely difficult, if not impossible, to discriminate between surface and bulk conduction, since the characteristic features of the two models are screened, and both models can in principle be used to describe the observed characteristics under the assumption of a gate-bias dependent mobility.

## 6.3 Temperature-dependent FET characteristics

### 6.3.1 Multiple trapping and release model (MTR)

Besides the prediction of a gate-bias dependent mobility, the MTR model further predicts that the transport of the charge carriers is thermally activated, and therefore the effective mobility should decrease with decreasing temperature.

The MTR model relies on the assumption of a distribution of localized trap states inside

the band gap below the extended states of the semiconducting bands (see figure 6.3c). In the extended states, the charge carriers travel with an intrinsic mobility $\mu_0$. The model assumes that charge carriers traveling in the extended states are captured instantaneously when they arrive at an empty trap. The release of the trapped carriers is a thermally activated process. The trapping events and the time the charge carriers spend in the traps increases the transit time, and hence the effective field-effect mobility $\mu_{eff}$ of the device is smaller than the intrinsic mobility $\mu_0$. Within the MTR model the effective mobility is given by

$$\mu_{eff} = \frac{n_f}{n_f + n_t}\mu_0, \tag{6.3}$$

with the concentration of free charge carriers in the extended states $n_f$ and the concentration of trapped charge carriers $n_t$. With increasing gate-source voltage, the Fermi level in the semiconductor moves closer to the conduction-band edge, so that more and more localized trap states are filled. As a result, the maximum energy distance between the filled traps and the conduction-band edge is reduced, so the activation energy for the thermal release of trapped charge carriers decreases and consequently the effective field-effect mobility increases. The concentrations $n_f$ and $n_t$ are calculated with the help of

$$n_f = \int_{-\infty}^{\infty} f(\mathrm{E(V(y))}, \mathrm{T}) \cdot \mathrm{N_f(E)}\,\mathrm{dE} \;\text{ and }\; n_t = \int_{-\infty}^{\infty} f(\mathrm{E(V(y))}, \mathrm{T}) \cdot \mathrm{N_t(E)}\,\mathrm{dE}. \tag{6.4}$$

$f(\mathrm{E(V(y))}, \mathrm{T})$ is the Fermi-Dirac distribution and $\mathrm{N_f(E)}$ and $\mathrm{N_t(E)}$ are the densities of states in the conduction band and of the traps, respectively. From equation 6.4 it can be seen that the charge-carrier concentrations $n_f$ and $n_t$ depend on the electrostatic potential distribution V(y) (caused by the externally applied gate-source voltage) in the semiconductor and on the temperature T. In order to determine whether the mobility in the wet-chemically grown ZnO nanowires is a function of the gate-source voltage, temperature-dependent measurements of the transfer characteristics are performed. Figure 6.3a shows the transconductance of a ZnO-nanowire FET measured at T = 225 K (blue curve), 140 K (red curve) and 80 K (green curve). The transconductance displays the characteristic of operation in the depletion regime for gate-source voltages $\mathrm{V_{GS}} < 10\,\mathrm{V}$ and saturates for $\mathrm{V_{GS}} > 10$ V, which indicates the onset of the accumulation regime. The charge-carrier concentration in the ZnO nanowire is estimated to $2.5 \cdot 10^{18}\,\mathrm{cm^{-3}}$ and is therefore substantially larger than the average charge-carrier concentration of the annealed ZnO nanowires ($4{\cdot}10^{17}$ $\mathrm{cm^{-3}}$) obtained from section 6.2. When the temperature is decreased, the transconductance in the depletion regime decreases while in the accumulation regime the transconductance is constant. Since $\mu_{eff}$ is the only temperature-dependent parameter affecting the transconductance, the decrease in the transconductance can be directly associated with a decrease of $\mu_{eff}$. The MTR model predicts an exponential

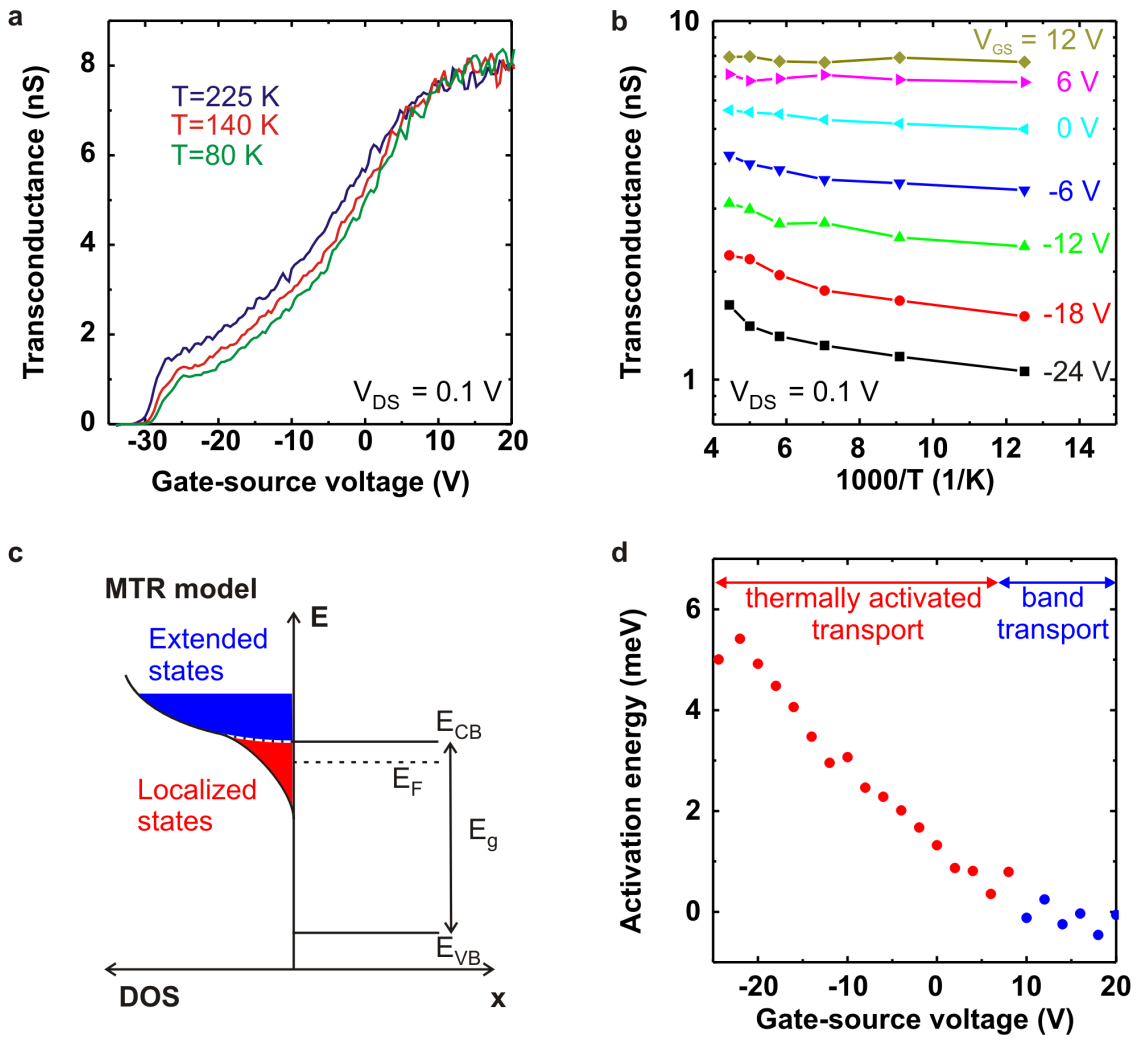


Figure 6.3: **Temperature dependence of the transfer characteristics of an FET based on an annealed ZnO nanowire.**
(a) Measured transconductance as a function of $V_{GS}$ at temperatures of 225 K (blue curve), 140 K (red curve) and 80 K (green curve). In the depletion regime $V_{GS} < 10\,V$ the transconductance decreases with decreasing temperature. (b) Transconductance as a function of the inverse temperature 1000/T for different $V_{GS}$. For positive $V_{GS}$, the transconductance is constant, while for negative $V_{GS}$, the transconductance displays a temperature-activated behavior. (c) Schematic DOS and band diagram according to the multiple trapping and release model (MTR). An exponential distribution of trap states (red) exists in the band gap below the conduction-band edge $E_{CB}$. (d) Activation energy $E_A$ as a function of $V_{GS}$ obtained by fitting the data from (b) with equation 6.5. For $V_{GS} < 10$ V, $E_A > 0$ and the transport can be described as thermally activated in this regime. Towards more negative gate-source voltages, $E_A$ increases and consequently the effective field-effect mobility decreases. Therefore, the field-effect mobility in the ZnO nanowire is a function of $V_{GS}$, as predicted by the MTR model.

dependence of the effective field-effect mobility on the inverse temperature [96, 97]:

$$\mu_{eff} \sim \mu_0 \cdot \exp\left(-\frac{E_A}{k_B T}\right) \tag{6.5}$$

with the activation energy $E_A$ necessary for the thermal release of an electron from a trap. Figure 6.3b shows the transconductance of the ZnO-nanowire FET as a function of the inverse temperature for different gate-source voltages. While for positive $V_{GS}$ the transconductance is independent of the temperature, the data shows an increasingly negative slope for more negative $V_{GS}$. Figure 6.3d shows the activation energy versus the gate-source voltage obtained by fitting the data shown in figure 6.3b with the help of equation 6.5. Two different transport regimes are recognized from the graph. For $V_{GS} > 10\,V$, $E_A$ is zero or even slightly negative. This indicates that all traps in the semiconductor are filled and the transport can be described as band transport [97]. For $V_{GS} < 10\,V$, $E_A > 0$ and the transport can be described as thermally activated in this regime. The fact that $E_A$ increases for more negative $V_{GS}$ shows that the mobility is indeed gate-bias dependent in this regime, as predicted by the MTR model. The temperature-dependent and gate-bias-dependent mobility indicates the presence of a trap distribution below the conduction band of the ZnO nanowires. For the investigated ZnO nanowire, the maximum activation energy of 6 meV corresponds to a mobility degradation of 20% at room temperature when sweeping $V_{GS}$ from 10 V to -24 V. Compared to organic or amorphous silicon FETs the activation energy is rather small [96, 94]. This can be explained with the smaller defect density expected for single-crystalline materials compared to polycrystalline or amorphous semiconductors.

Although the results from the temperature-dependent measurements coincide well with the predictions of the MTR model, the results need to be treated with caution. It is important to recognize that the MTR model was developed in the framework of TFT theory and assumes that the gate-induced charge carriers are located in a thin charge sheet at the semiconductor/insulator interface (surface conduction; see section 6.2). This assumption is not valid in the case of bulk conduction where the potential drops over the whole semiconductor body. An estimation of the applicability of the MTR model in the case of bulk conduction can be found in the appendix.

In conclusion, the analysis of the annealed ZnO nanowires revealed that it is difficult to estimate whether the finite conductivity at zero gate-bias is caused by surface conduction or bulk conduction, in part because of the poor uniformity of the physical parameters (diameters, doping concentration) and electrical parameters (capacitance, mobility, flat-band voltage) of the wet-chemically grown ZnO nanowires. The temperature-dependent transport measurements reveal that also the field-effect mobility in the wet-chemically grown ZnO nanowires depends on the applied gate-source voltage. This makes the analysis extremely complicated, since in the case of bulk conduction this causes both the capacitance and the field-effect mobility to depend on the gate-source voltage.

Nevertheless, some of the investigated ZnO nanowires clearly display the behavior expected for bulk conduction. As will be shown in chapter 8 it is further possible to fabricate

metal-semiconductor FETs (MESFETs) using the annealed ZnO nanowires. The general operation principle of a MESFET relies on the controlled depletion of a semiconductor bulk, and therefore requires a doped semiconductor. It is therefore concluded that the intrinsic conductivity of the post-growth annealed ZnO nanowires originates from residual unintentional bulk doping.

# 7 Passivation of ZnO-nanowire FETs using self-assembled monolayers

## 7.1 Characterization of phosphonic acid self-assembled monolayers on ZnO

Self-assembled monolayers (SAMs) are organized arrangements of organic molecules that form spontaneously on the surface of a solid. Molecules that form self-assembled monolayers usually consist of an anchor group that chemisorbes on the surface of the solid, and a tail that is responsible for the organization of the molecules on the surfaces with respect to each other. The interaction between adjacent molecules is promoted by van-der-Waals forces. Under ideal conditions, the molecules form a densely packed monolayer with crystalline quality. Depending on the choice of the anchor group, self-assembled monolayers can be formed on a large variety of different materials. For example, thiol anchor groups can be used to form self-assembled monolayers on metals like gold and silver [98, 99], while silane anchor groups form dense monolayers on silicon dioxide [100, 101]. A detailed overview of different substrate/anchor group combinations is given in [102, 103]. The molecules utilized in the framework of this thesis consist of a phosphonic-acid anchor group and a tail consisting of an octadecyl chain (chemical formula: $CH_3(CH_2)_{17}P(O)(OH)_2$). Self-assembled monolayers based on phosphonic-acid molecules are known to form densely packed monolayers on metal oxides, like aluminum oxide [102, 104] or titanium dioxide [105]. For the formation of SAMs based on phosphonic-acid anchor groups on ZnO controversial reports can be found in the literature. While Taratula et al. [106] have found no evidence for the chemisorption of the phosphonic-acid anchor group on the surface of ZnO, Perkins [107] reported the formation of SAMs on ZnO with excellent quality based on phosphonic-acid molecules.

### 7.1.1 Water contact angle measurements

In order to investigate whether phosphonic acids form SAMs on ZnO, static water contact angle measurements are performed on large-area (3x2 $cm^2$) ZnO single-crystals. The contact angle between a water droplet and the surface of a solid depends on the energetic interaction of the liquid and the solid. A hydrophilic surface will promote wetting of the solid surface, since the interaction between the water and the surface is large. Consequently, a small water contact angle is measured on a hydrophilic surface, while a large water contact angle is measured on a hydrophobic surface. Since the molecules for the formation of the SAM have a hydrophobic, methyl-terminated tail, the surface is expected to be very hydrophobic when the molecules form a well-ordered SAM on the surface. The

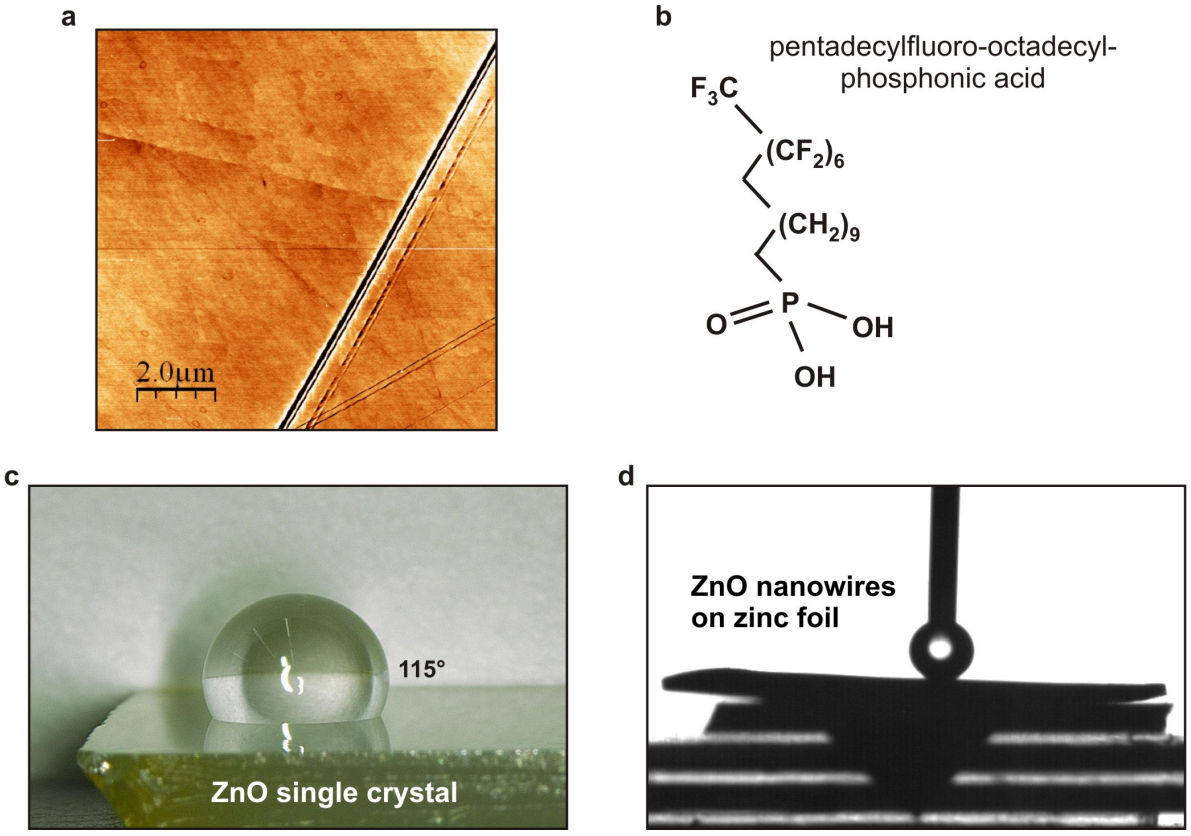


Figure 7.1: **SAMs of fluoroalkylphosphonic acids on ZnO**.
(a) Atomic force microscopy image of the polished surface of a ZnO single-crystal. The surface of the crystal is very smooth, but also shows some scratches caused by the polishing procedure. The surface roughness in the smooth areas is as low as 0.4 nm. (b) Pentadecylfluoro-octadecylphosphonic acid molecule (c) Water droplet on a polished ZnO single-crystal covered with a self-assembled monolayer (SAM) of pentadecylfluoro-octadecylphosphonic acid. The crystal surface is polished parallel to the (1010) direction of ZnO. The water contact angle of 115° confirms the formation of a hydrophobic SAM on the surface of the ZnO crystal. (d) Water droplet on the surface of a zinc foil covered with ZnO nanowires grown by the hydrothermal synthesis (see figure 3.3). The ZnO nanowires are coated with a hydrophobic SAM. Due to the large surface area and the hydrophobic SAM, the surface is superhydrophobic (water contact angle $> 150°$).

measurement of the water contact angle can therefore indicate the quality of the SAM.

Single-crystalline, c-axis oriented ZnO samples are purchased from the company Topgeo. The crystals are cut into 0.5 mm thick slices, oriented parallel to the (1010) plane of zinc oxide. The (1010) plane of the ZnO single-crystal is expected to beidentical to the side facets of the hexagonal ZnO nanowires. The purchased crystals show a sligthly red coloration, indicating a non-stoichometric structure. After annealing the crystals for 24 h at 1000 °C in an oxygen atmosphere, the coloration vanishes and the crystals become transparent, as expected for stoichometric ZnO. The slices are then ground and polished to provide a smooth surface for the formation of the SAM. Figure 7.1a shows an atomic

force microscopy image (size 10 µm x 10 µm) of the surface of the ZnO single-crystal after polishing. As can be seen, large areas of the crystal are very smooth after the polishing procedure, but there are also some unavoidable scratches distributed across the sample surface. The root-mean-square roughness of the smooth area is determined to be 0.4 nm. The (1010) orientation of the surface was confirmed by Laue diffraction.

In order to prepare the surface for the formation of the self-assembled monolayer, the ZnO single-crystal is briefly exposed to an oxygen plasma (30 sccm $O_2$, 15 mTorr, 50 W, 20 sec). The purpose of the oxygen plasma is to clean the crystal surface from organic adsorbants and to increase the density of hydroxyl groups on the surface of the ZnO, which is beneficial for the formation of a high-quality alkylphosphonic acid self-assembled monolayer [104]. After the plasma treatment, the surface of ZnO is expected to be very hydrophilic. This is confirmed by a water contact angle smaller than 20° measured directly after the plasma treatment. The formation of the self-assembled monolayer is then performed from solution. For the experiments presented in this chapter, the self-assembling molecules consist of a phosphonic-acid anchor group and a partially fluorinated alkyl chain (pentadecylfluoro-octadecylphosphonic acid; see figure 7.1b). Immediately after the plasma treatment, the crystal is immersed in an isopropanol solution containing 5 mMol of pentadecylfluoro-octadecylphosphonic acid. After 3 h in the solution, the crystal is rinsed with pure isopropanol, blown dry with nitrogen gas, and briefly baked on a hot plate (10 min, 100 °C).

Figure 7.1c shows a photograph of a water droplet on the ZnO single-crystal after the SAM treatment. The water-contact angle measured on a fluoroalkylphosphonic acid SAM is 115°. This confirms the formation of a high-quality, hydrophobic, self-assembled monolayer on the surface of the ZnO single-crystal. In addition to the measurements on the single-crystalline ZnO surface, water contact angle measurements are also performed on the zinc foil covered with hydrothermally grown ZnO nanowires (see figure 3.3). The high density of ZnO nanowires on the zinc foil provides a very large surface area compared to the atomically flat surface of the ZnO single-crystal. The combination of the large surface area and the hydrophobic coverage by the fluoroalkylphosphonic acid molecules causes the zinc foil to be superhydrophobic after the adsorption of the phosphonic acid molecules. Figure 7.1d shows a photograph of a water droplet brought down onto the zinc foil after the SAM treatment. As can be seen, the water droplet does not wet the superhydrophobic surface and keeps its ideal spherical shape. An exact determination of the water-contact angle is therefore difficult, but the experiment clearly shows that the ZnO nanowires are covered by the SAM (before the SAM treatment, the water droplet wet nearly the complete nanowire surface). Superhydrophobicity of ZnO nanowires covered with fatty acids [108] and octadecanethiol molecules [109] have been previously reported.

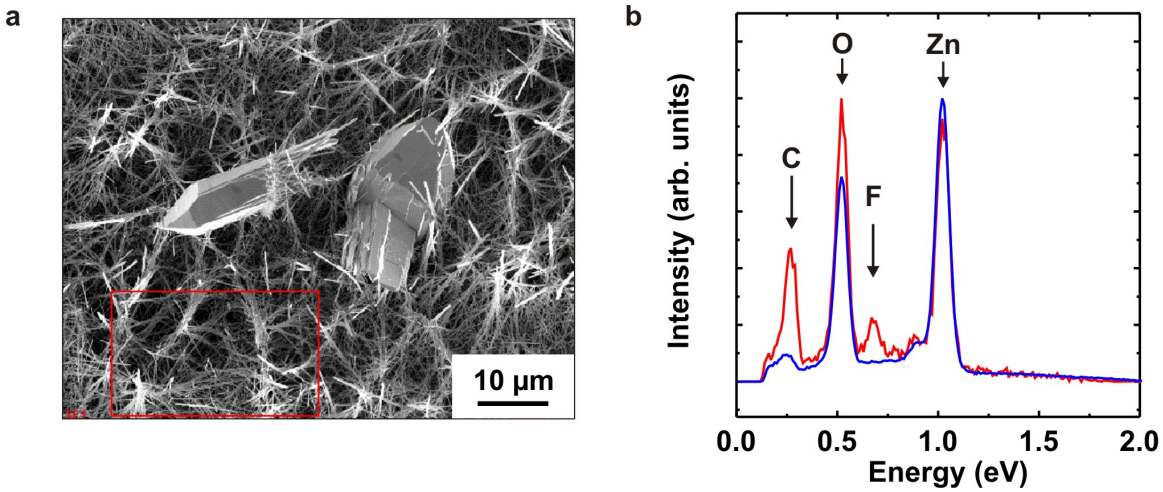


Figure 7.2: **Energy-dispersive x-ray spectrum of ZnO nanowires on zinc foil before and after SAM treatment.**
(a) Scanning electron microscopy image of the SAM-covered ZnO nanowires on the zinc foil growth substrate. (b) Energy-dispersive X-ray spectra of the ZnO nanowires on the zinc foil before the SAM treatment (blue curve) and after the SAM treatment (red curve). Due to the coverage of the ZnO nanowires with the fluoroalkylphosphonic-acid molecules, the fluoro peak emerges in the spectrum.

### 7.1.2 Energy-dispersive x-ray spectroscopy

In order to investigate the attachment of the fluoroalkylphosphonic-acid molecules on the ZnO nanowires, energy-dispersive x-ray spectroscopy (EDX) is performed on a piece of zinc foil covered with a dense layer of hydrothermally grown ZnO nanowires. Figure 7.2a shows a representative scanning electron microscopy image of the investigated zinc foil. In order to obtain a high surface sensitivity, the energy of the incident electrons is set to 2 keV. This low energy leads to a small penetration depth of the electrons into the ZnO and therefore to a higher probability for x-ray emission from the fluoroalkylphosphonic-acid molecules attached to the ZnO-nanowire surface. Figure 7.2b shows a comparison of the EDX spectra obtained before the SAM treatment (blue curve) and after the SAM treatment (red curve). For a better comparison, the spectra have been normalized to their maximum. After the treatment with the fluoroalkylphosphonic-acid molecules, the fluorine clearly emerges in the EDX spectrum. This indicates the attachment of the fluoroalkylphosphonic-acid molecules to the surface of the ZnO nanowires.

## 7.2 Effect of different atmospheres on ZnO-nanowire FETs

The rich surface chemistry of ZnO causes atmospheric species, like $O_2$ [110] and $H_2O$ [88], to easily adsorb on the surface of ZnO. Due to the large surface-to-volume ratio of the nanowires, these adsorbates greatly affect the electrical conductivity of the material.

While this is beneficial for nanowire transistors that are utilized as sensors, it is a drawback for nanowire transistors integrated into circuits, since the performance of the circuits depends critically on the stability of the FET parameters.

To analyze the specific effects of the atmosphere on the device characteristics, ZnO-nanowire FETs are investigated in ambient air, in vacuum ($p < 10^{-6}$ mbar) and in water vapor. The device substrate is a heavily doped silicon wafer covered with a 30 nm thick layer of aluminum oxide ($Al_2O_3$) grown by atomic layer deposition at T = 250 °C. Hydrothermally grown ZnO nanowires are annealed at 600 °C for 5 min in air on the zinc foil and afterwards dispersed in isopropanol. The annealed ZnO nanowires are solution-deposited onto the $Si/Al_2O_3$ substrate, and aluminum source and drain contacts are defined by e-beam lithography, argon-plasma treatment (30 sccm Ar, 10 mTorr, 100 W, 15 sec) and metal evaporation as described in chapter 4.2. The sample is glued into a chip carrier and thin metal wires are carefully bonded to the contact pads to establish reliable contacts between the device terminals and the chip carrier.

### 7.2.1 Effect of ambient air on ZnO-nanowire FETs

#### Comparison between ambient air and high vacuum

To study the effect of ambient air and high vacuum on the electrical characteristics, the sample was transferred into a home-built high-vacuum chamber. The red curve in figure 7.3 a shows the initial transfer characteristics of a ZnO-nanowire FET measured in ambient air (42% relative humidity, T = 20 °C, L = 2 µm, $d_{NW}$ = 54 nm, $t_{Al_2O_3}$ = 30 nm). The FET has an on/off current ratio of $10^6$ (at $V_{DS}$ = 1 V) and a transconductance of 0.2 µS (at $V_{GS} = 5\,V$ and $V_{DS} = 1\,V$). Owing to the small thickness of the gate dielectric (30 nm) the FET is operated with a relatively small gate-source voltage of 5 V.

The blue curve in figure 7.3b shows the transfer characteristics of the same FET after evacuating the vacuum chamber to a background pressure of $10^{-7}$ mbar. A shift towards more negative gate-source voltages is observed when comparing the red and the blue curve. To quantify this shift, the threshold voltage $V_{th}$ of the transistor is defined as the gate-source voltage at a drain current level of 0.1 nA:

$$I_D(V_{th}) > 10^{-10}\,A$$

The left part of figure 7.3b shows the observed shift of the threshold voltage $\Delta V_{th}$ as a function of the time in vacuum with respect to the value of $V_{th}$ in ambient air. Over a period of 90 minutes in high vacuum, the threshold voltage of the FET shifts by about 2 V towards more negative values. The observed shift of $V_{th}$ can be attributed to the desorption of electron-capturing species (like $O_2$, $NO_2$ [111]) from the nanowire surface

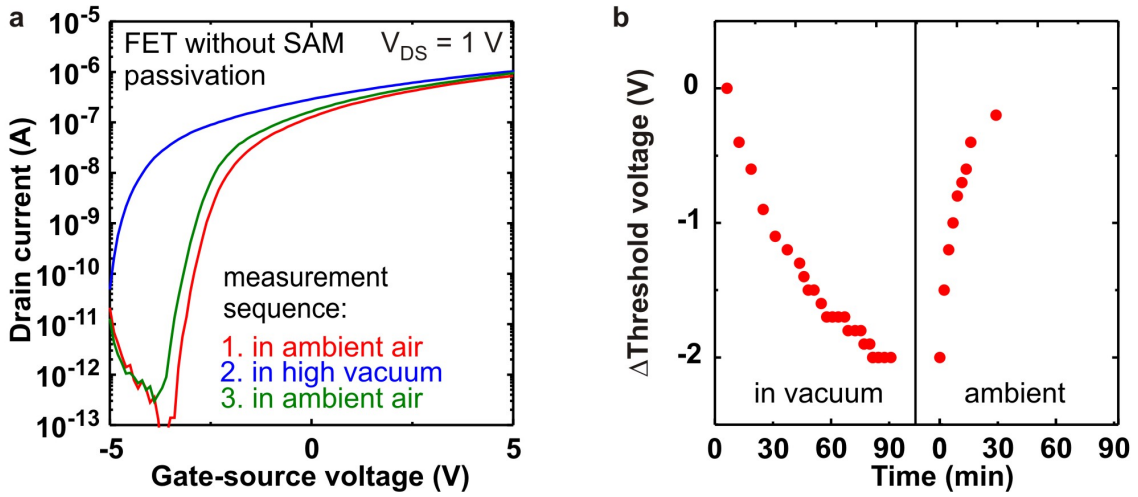


Figure 7.3: **Effect of ambient air on the transfer characteristics of a ZnO-nanowire FET.**
(a) Transfer characteristics of a ZnO-nanowire FET (L = 2 µm, $d_{NW}$ = 54 nm, $t_{Al_2O_3}$ = 30 nm). First measurement in ambient air (red curve), second measurement in high vacuum (blue curve) and third measurement again in ambient air (green curve). The threshold voltage shifts towards more negative values when the FET is placed in high vacuum (compare red and blue curve). This shift can be attributed to the desorption of electron-capturing species from the nanowire surface in vacuum. Venting the chamber with ambient air causes the threshold voltage to recover to nearly its initial value (compare blue and green curve). (b) Evolution of the threshold voltage over time when the device is kept in vacuum (left part) and when the chamber is vented with ambient air (right part).

under high-vacuum conditions. Venting the chamber with ambient air results in a recovery of the initial threshold voltage (compare blue and green curve in figure 7.3a and red data points in the right part of figure 7.3b). Among the many different possible surface adsorbents on ZnO, oxygen and water are believed to have the biggest impact on the conductivity of ZnO nanowires. The impact of oxygen on the conductivity of ZnO has been investigated in great detail in the literature. Adsorbed oxygen molecules from the ambient air capture electrons close to the nanowire surface and become oxygen ions in the form of $O^-$, $O^{2-}$, $O_2^-$ [110, 112, 113, 114]. This leads to a reduction of the charge-carrier concentration at the ZnO nanowire surface and a shift of the threshold voltage towards more positive values.

### 7.2.2 Effect of water vapor on ZnO-nanowire FETs

The role of water on the electrical characteristics of ZnO has been investigated in much less detail. In general, an increase of the conductivity of ZnO is observed with increasing relative humidity. Humidity sensors based on ZnO nanowire and nanobelt films [88, 115] and individual ZnO nanofeathers [116] have been demonstrated. A monotonic increase

in the electrical conductivity over up to five orders of magnitude with increasing relative humidity was observed [115] in these reports. The strong variation of the conductivity was explained by the large surface area of the nanostructured films and feathers available for water adsorption. Measurements on individual $SnO_2$ nanowires showed a much weaker, but still strong increase of the conductivity by a factor of 32 when comparing measurements in dry air and 85% relative humidity [117]. The mechanism behind the increase in conductivity upon water exposure is not completely understood. It is believed that water molecules adsorb on the surface of metal oxides and substitute previously adsorbed electron-capturing species. Therefore, a previously captured electron is released and the conductivity of the material increases [118, 119, 120, 121].

To investigate the effect of water on the electrical characteristics of the ZnO nanowires used in the framework of this thesis, the vacuum chamber is flooded with pure water vapor. To provide pure water vapor, an Erlenmeyer flask containing 100 ml of deionized (DI) water is connected to the vacuum chamber via a needle valve. Via a second valve, the flask is further connected to a vacuum pump that makes it possible to evacuate the flask to a pressure of $10^{-1}$ mbar. The low pressure causes the DI water to boil in the flask. When the valve between the vacuum pump and the flask is closed the pressure in the flask increases to 23 mbar due to the boiling water. This corresponds to the water vapor pressure at room temperature and is comparable to 100% relative humidity. When the needle valve to the vacuum chamber is opened, the chamber ($10^{-2}$ mbar) is flooded with the pure water vapor atmosphere from the Erlenmeyer flask.

In the course of the experiments presented in this section, it was found that there are two different effects on the electrical characteristics of the ZnO-nanowire FETs associated with the water vapor. These effects are liquid gating and the donor effect, and both are explained in more detail in the following.

### Liquid gating

Figure 7.4a shows the transfer characteristics of a ZnO-nanowire FET measured first in high vacuum (red curve) and measured again in water vapor (23 mbar, blue curve). When the chamber is flooded with water vapor and the FET is characterized in water vapor, the transfer characteristics change dramatically. The on-state current of the transistor at $V_{DS} = 1\,V$ and $V_{GS} = 5\,V$ increases form $0.87\,\mu A$ to $5.3\,\mu A$. Further, the threshold voltage of the FET shifts by about 1.4 V towards more positive values. To compare the transconductance of the FET in the different environments, it is important to account for the different threshold voltages. Therefore, the so-called overdrive voltage is introduced, which is defined as: $V_{OD} = V_{GS} - V_{th}$. For an overdrive voltage of 4 V, the transconductance of the transistor increases by an order of magnitude from 90 nS to 900 nS upon

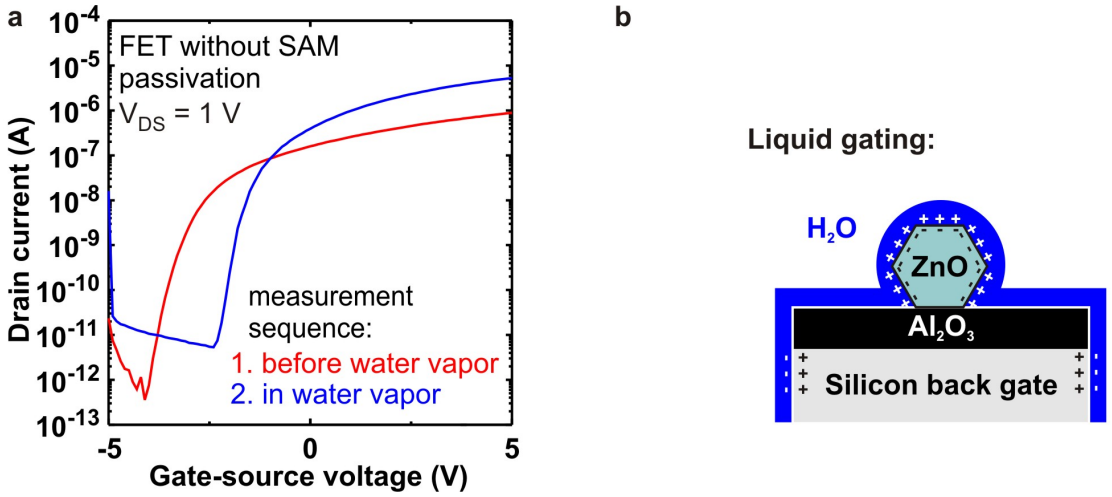


Figure 7.4: **Effect of water vapor on the transfer characteristics of a ZnO-nanowire FET without SAM passivation I: Liquid gating.**
(a) Transfer characteristics of an FET measured in high vacuum (red curve) and in 23 mbar water vapor (blue curve). In water vapor, the threshold voltage is shifted towards more positive values, and the current through the ZnO nanowire at $V_{GS} = 5\,V$ is increased by an order of magnitude. The observed behavior is believed to be caused by an increased capacitance due to liquid gating. (b) Schematic cross-section of the device covered with a thin water layer. The water layer establishes an ionically conducting connection between the silicon back-gate electrode and the nanowire surface. The formation of an electrochemical double layer on the surface of the ZnO introduces a large capacitance and causes the liquid gating.

flooding the chamber with water vapor. The observed increase of the transconductance and the shift of the threshold voltage towards more positive values can be explained by an increase of the device capacitance upon exposure to water vapor. In high-humidity environments, a thin water layer condensates on the sample surface. This water layer establishes an ionically conducting path between the nanowire surface and the back-gate electrode of the substrate. Figure 7.4b shows a schematic of the situation in water vapor. When a gate-source voltage is applied, the water layer is believed to act as an electrolyte, leading to the formation of an electrochemical double layer (Helmholtz layer) at the water/ZnO interface. The capacitance of the electrochemical double layer, which is connected in parallel to the capacitance of the $Al_2O_3$ gate dielectric, can be calculated as follows [122]:

$$C_{water} = \frac{2 \cdot \pi \cdot \varepsilon_{Water} \cdot \varepsilon_0 \cdot L}{\ln(1 + \lambda_D / r_{NW})} \sim 7 \cdot 10^{-14}\,F, \tag{7.1}$$

with the dielectric constant of water $\varepsilon_{water} = 80$, the radius of the nanowire $r_{NW} = 27\,nm$ and the thickness of the electrochemical double layer $\lambda_D = 4 - 5\,nm$ [123]. The calculated value of $C_{water}$ is therefore more than one order of magnitude larger than the capacitance of the back gate ($C_{Al_2O_3} \sim 10^{-15}\,F$) calculated with the cylinder-on-a-parallel-plate model (see equation2.31). Considering the geometry of the sample (4 mm x 4 mm) and the

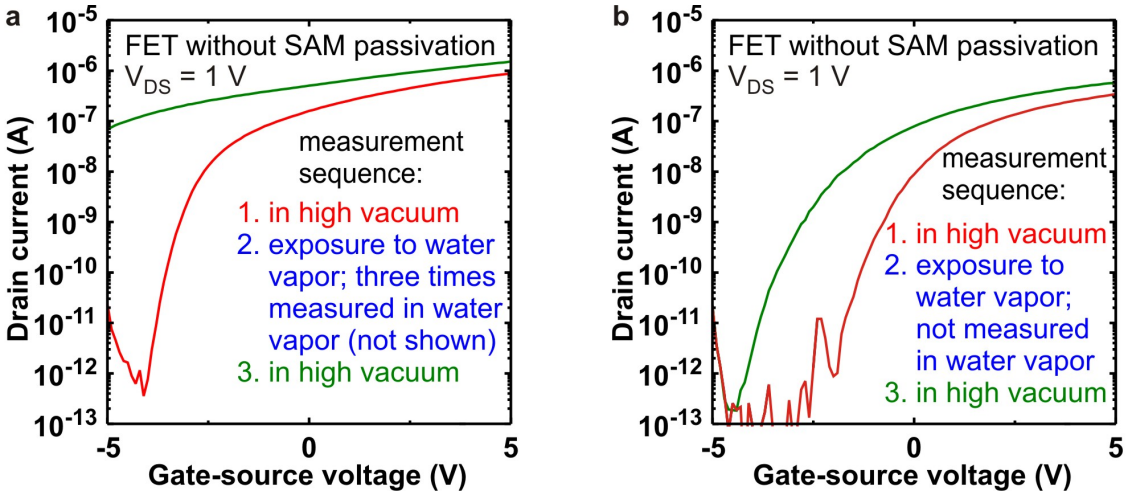


Figure 7.5: **Effect of water vapor on transfer characteristics of a ZnO-nanowire FET without SAM passivation II: Donor-effect**
Transfer characteristics of ZnO nanowire transistors measured in high vacuum before (red curves) and after (green curves) exposure to water vapor for a device measured during the exposure in water vapor atmosphere (a) and a device not measured during the exposure to water vapor atmosphere (b). Both graphs show a shift of the transfer characteristics towards more negative values which indicates an increase of the charge-carrier concentration by water vapor. The more pronounced shift of the device in the left graph is believed to be caused from electrochemical effects occurring during the measurement in water vapor.

nanowire (50 nm x 2000 nm), the resistivity of deionized water (18.2 MΩcm) and the thickness of the water layer of 3 nm at 100% RH [124], the resistance of the water layer is estimated to $R_{water} \sim 10^{13}\,\Omega$. Together with the calculated capacitance of the electrochemical double-layer, the time constant for the charging of the capacitance is estimated to $\tau = R_{water} \cdot C_{water} \sim 1\,\text{sec}$. Taking into account the patterned metal lines on the substrate surface (contact pads and lines), the actual resistance and time constant will be even shorter. Therefore, the liquid gating is sufficiently fast to affect the measurement of the transfer characteristics of the FET. The large capacitance of the "liquid gate" dominates the electrical characteristics of the device in water vapor, leading to the observed increase in the transconductance.

### Donor effect

A second effect of the water vapor on the FET characteristics is revealed when the chamber is evacuated again after the exposure to water vapor. Figure 7.5a shows the transfer characteristics of the FET from 7.4a measured in high vacuum before the chamber was flooded with water vapor (red curve), and measured again in high vacuum after the chamber had been flooded with water vapor for 15 minutes and then been evacuated from the water vapor (green curve). During the time in the water vapor the FET was

measured three times (curves not shown). As can be seen, the threshold voltage is shifted substantially towards more negative values after the FETs were operated in water vapor. The threshold-voltage shift is so large that it is not possible anymore to modulate the drain current to a value of $10^{-10}$ A. (This would require a more negative gate-source voltage which leads to increasing gate current $I_G > 10^{-10}$ A.) Therefore, to quantify the shift of the transfer characteristics, the gate-source voltage at a drain current level of 0.1 µA was compared. Using this criterion the transfer characteristics of the FET shown in figure 7.5a is shifted 4 V towards more negative values after operating the FETs in water vapor (see green curve in figure 7.4a).

As already mentioned above, the FET in figure 7.5a was measured three times during the exposure to water vapor. The sample is expected to be covered with a thin water film when exposed to the water vapor. Under these conditions, the sample can be thought off as an electrochemical cell. Under application of voltages larger than ±1 V electrochemical reactions are expected to start on the surface of the ZnO, which makes it difficult to isolate the physical effect of the water vapor on the ZnO from electrochemical effects. Figure 7.5b shows the transfer characteristics of an FET measured in high vacuum before (red curve) and after (green curve) exposure to water vapor. In order to exclude electrochemical effects, no measurements were performed on the FET during the exposure to water vapor. Similarly to the FET measured during the exposure to water vapor (figure 7.5a), the FET of figure 7.5b shows a shift of the threshold voltage towards more negative values. This confirms that exposure to water vapor leads to an increase of the conductivity that is attributed to an increase of the charge-carrier concentration in the ZnO nanowire (so-called "donor-effect" of water [120]). Compared to the device shown in figure 7.5a, the shift is less pronounced (about 2 V). The observation that the threshold-voltage shift is larger when the device is measured during exposure to water vapor, is therefore attributed to electrochemical reactions, which apparently introduce additional charge carriers in the ZnO nanowire. A possible explanation is the formation of oxygen vacancies under application of a negative gate bias that can act as donors in ZnO (see section 5.3).

Independent of the measurement sequence, the observed shift of the threshold voltage is reversed when the device is exposed again to ambient air. As already stated above, the detailed mechanism behind the donor effect of water is not understood. However, the reversal of the threshold voltage upon exposure to ambient air can be explained with the assumption that water molecules replace previously adsorbed electron-capturing species on the surface of ZnO. The electron-capturing species simply adsorb again on the ZnO surface when the device is exposed again to ambient air.

## 7.3 Effect of different atmospheres on ZnO-nanowire FETs with SAM passivation

The results presented in the previous section demonstrate the large sensitivity of ZnO nanowires to the ambient. The competitive effects between water and electron-capturing species on the surface of the ZnO nanowires make it difficult to obtain reproducible and reliable FET characteristics. Therefore, ZnO-nanowire FETs for integrated circuits require a passivation layer. Passivation of ZnO-nanowire FETs has been demonstrated in the literature, with the help of a spin-coated organic passivation layer [85, 125, 110] and with the help of an inorganic passivation layer (e.g. $SiO_2$ [126] or $Si_3N_4$ [84]). The passivation of ZnO nanowires usually leads to much more stable device characteristics and even improved device performance. In the following, the passivation of ZnO nanowires is demonstrated by the use of a self-assembled monolayer.

To passivate the ZnO-nanowire FETs, the substrate is first exposed to an oxygen plasma. The plasma parameters are the same as those used for the SAM preparation on the ZnO single crystals presented in subsection 7.1.1 (30 sccm $O_2$, 15 mTorr, 50 W, 20 sec). After the plasma treatment the sample is immersed in an isopropanol solution of pentadecylfluoro-octadecylphosphonic acid molecules for 1 h. This leads to the formation of a hydrophobic SAM on the $Al_2O_3$ gate dielectric, on the aluminum source and drain contacts, and on the ZnO nanowires.

### 7.3.1 Effect of ambient air on ZnO-nanowire FETs with SAM passivation

Figure 7.6 shows the transfer characteristics of the nanowire FET presented in chapter 7.2.1 before the SAM passivation (figure 7.6a) and after the SAM passivation (figure 7.6b). Compared to the unpassivated device, the threshold voltage of the nanowire FET after the SAM passivation is shifted towards more positive values from $-3\,\mathrm{V}$ to $1\,\mathrm{V}$ (compare red curves in figure 7.6a and b). The positive shift of $V_{th}$ indicates a reduction of the density of free charge carriers in the ZnO nanowire as a consequence of the surface passivation. The change of the surface-charge density is related to $\Delta V_{th}$ like

$$\Delta Q_S = \frac{\Delta V_{th} \cdot C_{Al_2O_3}}{L_{NW} \cdot \pi \cdot d_{NW}}. \tag{7.2}$$

A shift of $\Delta V_{th} = 4\,\mathrm{V}$ therefore corresponds to a reduction of the surface-charge density of $5.3 \cdot 10^{12}\,\mathrm{cm}^{-2}$. A comparable shift towards more positive values was already observed in section 5.5, when the channel of a ZnO-nanowire FET was exposed to an oxygen plasma. The FET in chapter 5.5 has been fabricated on a 100 nm thick $SiO_2$ gate dielectric. The observed shift of $\Delta V_{SO} = 14\,\mathrm{V}$ therefore corresponds to a reduction of the surface-charge density of $\Delta Q_S^{SiO_2} = 3 \cdot 10^{12}\,\mathrm{cm}^{-2}$. Therefore, the observed $V_{th}$ shift is mainly attributed

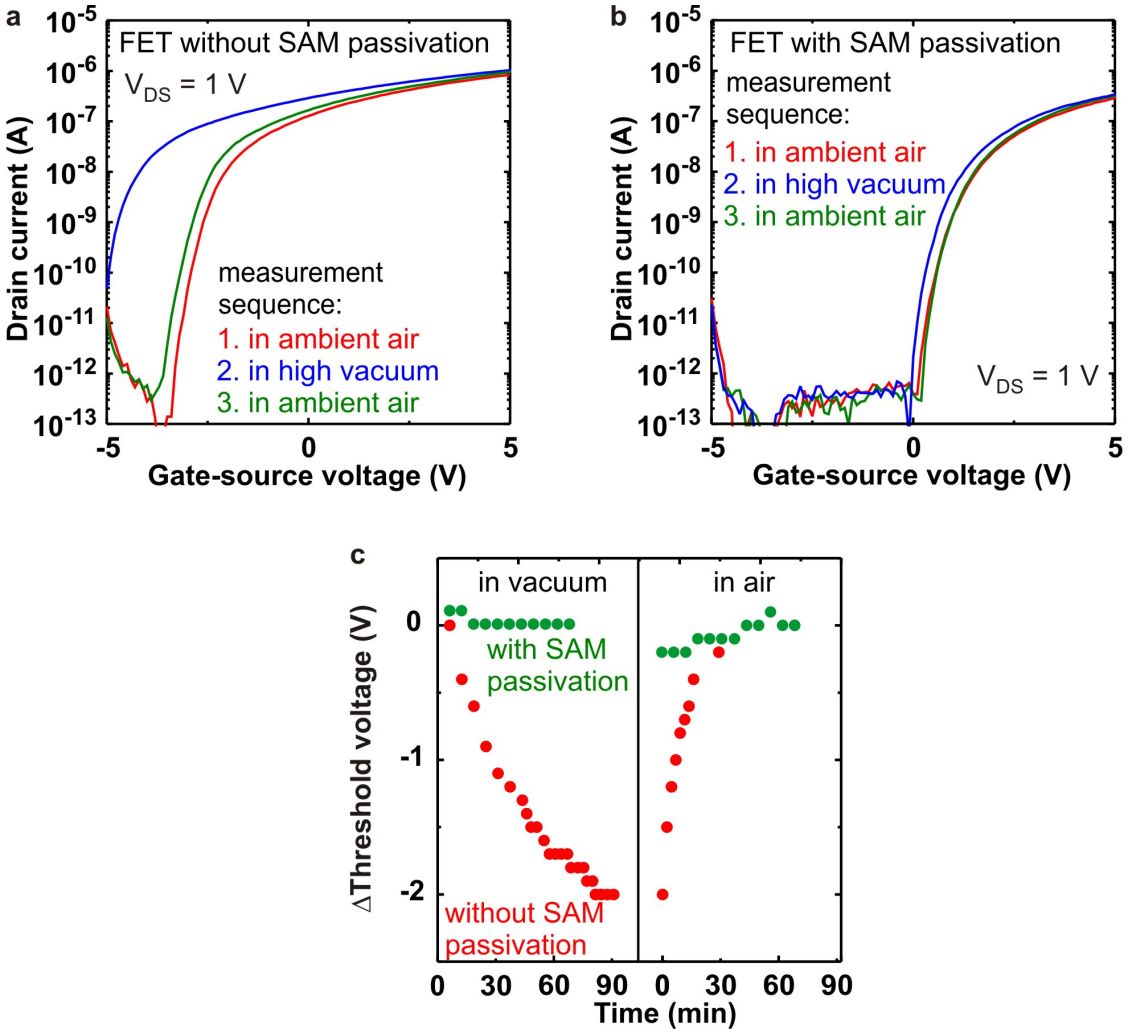


Figure 7.6: **Effect of ambient air on the transfer characteristics of ZnO-nanowire FET with and without SAM passivation.**
(a) Transfer characteristics of the unpassivated FET (left graph) and (b) the SAM-passivated FET (right graph), in ambient air (red curve), after 90 minutes in high vacuum (blue curve) and after venting again to ambient air (green curve). The transfer characteristics are much more stable against the influence of the ambient air after the SAM passivation. (c) Shift of the threshold voltage $\Delta V_{th}$. Compared to the shift of the unpassivated FET (red symbols), the shift of the SAM-passivated FET (green symbols) is reduced by a factor of 10.

to the oxygen-plasma treatment. However, the treatment with the SAM might also affect the surface-charge density of the ZnO nanowire and lead to an additional shift of $V_{th}$.

Similar to the experiments presented in the preceding section, the FET is again measured in high vacuum and in ambient conditions (figure 7.6b). As can be seen by comparing with the unpassivated FET (figure 7.6a), the SAM-passivated FET is much more stable against the influence of the atmosphere. The transfer characteristics measured in ambient air (red and green curve in figure 7.6b) are almost identical to the transfer characteristics measured in high vacuum (blue curve in 7.6b). The shift of the threshold voltage between

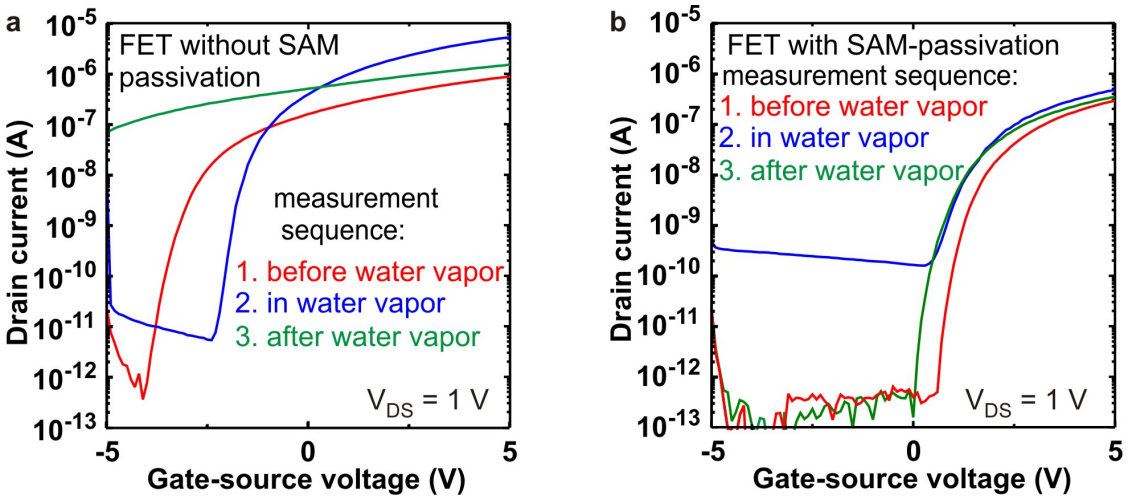


Figure 7.7: **Effect of water vapor on the transfer characteristics of a ZnO-nanowire FET with and without SAM passivation.**
(a) Transfer characteristics of the unpassivated FET (left graph) and the SAM-passivated FET (right graph), measured before exposure to water vapor (red curve), during exposure to water vapor (blue curve) and after exposure to water vapor (green curve). (b) As can be seen, the maximum drain current as well as the threshold voltage are much more stable after the SAM treatment.

the measurements in high vacuum and in ambient air is reduced to 0.2 V and therefore a factor of 10 smaller compared to the FET without SAM passivation (7.6c).

### 7.3.2 Effect of water vapor on ZnO-nanowire FETs with SAM passivation

To analyze the benefit of the SAM passivation in suppressing the undesirable reactions with water, the SAM-passivated FET is exposed to water vapor (23 mbar). Figure 7.7a shows a summary of the effect of water vapor on the transfer characteristics of the unpassivated FET already presented in the section 7.2.1. The same measurement sequence was repeated for the SAM-passivated FET (figure 7.7b).

As for the measurements in ambient air and high vacuum (figure 7.6), the stability of the ZnO nanowire FET is greatly improved by the SAM passivation. The transfer characteristics measured in water vapor (blue curve in figure 7.7b) show no indication of liquid gating. Compared to the transfer characteristics of the unpassivated FET, the transconductance of the SAM-passivated device increases only slightly (about 25 %) when the FET is exposed to water vapor (see table 7.1). The absence of liquid gating is attributed to the presence of a hydrophobic monolayer on the $Al_2O_3$ gate dielectric, which suppresses the formation of a conducting water layer that would connect the back-gate electrode to the ZnO-nanowire surface. The observed increase in the off-state drain current of the transistor during the exposure to water vapor ($V_{GS} < 0\,V$, blue curve) is caused by an increase in the gate current of the device after the oxygen-plasma treatment. The oxygen-plasma

| Transconductance (nS) (@ $V_{GS} - V_{th} = 4\,V$) | before water vapor (high vacuum) | in water vapor | after water vapor (high vacuum) |
|---|---|---|---|
| unpassivated FET (measured in water vapor) | 93 | 890 | 99 |
| unpassivated FET (not measured in water vapor) | 80 | - | 80 |
| SAM-passivated FET | 122 | 168 | 121 |

| Voltage shift (V) ($\Delta V_{th}$) (@ $I_D = 0.1\,\mu A$) | in water vapor | after water vapor (high vacuum) |
|---|---|---|
| unpassivated FET (measured in water vapor) | -0.2 | -4 |
| unpassivated FET (not measured in water vapor) | - | -1.8 |
| SAM-passivated FET, measured in water vapor | -0.7 | -0.4 |

Table 7.1: **Summary of the FET parameters for the experiments in water vapor.** Upper table: Transconductance estimated at an overdrive voltage of 4 V. Due to liquid gating, the transconductance of the unpassivated FET is increased by an order of magnitude when measured in water vapor atmosphere. Lower table: Shift of the threshold voltage with respect to the transfer curve obtained before exposure to water vapor. As a consequence of the SAM passivation the FET performance is greatly stabilized.

treatment renders the whole sample hydrophilic and therefore promotes the adsorption of a conductive water layer which can connect the back-gate electrode and the source and drain terminals on the chip carrier. The green curves in figure 7.7 show the corresponding transfer characteristics measured in high vacuum after the exposure to water vapor. The transfer characteristics of the SAM-passivated FET shows only a small shift of $\Delta V_{th} = -0.4\,V$ towards more negative values. Compared to the unpassivated devices ($\Delta V_{th} = -4\,V$ and $-1.8\,V$, see table 7.1), $V_{th}$ is therefore greatly stabilized by the SAM treatment.

The shift of $V_{th}$ observed for the unpassivated FETs was attributed to the so-called donor effect of water adsorbed on the ZnO-nanowire surface. The stabilization of $V_{th}$ therefore indicates that the adsorption of water on the ZnO-nanowire surface is greatly suppressed, as expected if the ZnO nanowire is covered with a hydrophobic SAM.

Finally, it should be mentioned that the experiments reported here for ZnO-nanowire FETs with $Al_2O_3$ gate dielectric have also been performed for ZnO-nanowire FETs manufactured on an $SiO_2$ gate dielectric. In contrast to the observations for FETs with $Al_2O_3$ gate dielectric, the FETs measured with $SiO_2$ gate dielectric did not show improvements

in the device stability after the SAM treatment. A possible reason for the observed differences is that pentadecylfluoro-octadecylphosphonic acid does not from a hydrophobic monolayer on $SiO_2$, as has been confirmed by a water contact angle of only 20° after the SAM treatment. The influence of the hydrophilic $SiO_2$ gate dielectric therefore seems to dominate over the hydrophobic passivation of the ZnO-nanowire channel. It is therefore concluded that the passivation of both, the gate dielectric and the ZnO nanowire channel is necessary to stabilize the FET performance against the influence of the ambient. For a more detailed understanding of the distinct influences, further experiments are necessary.

# 8 Low-voltage top-gate ZnO-nanowire transistors with self-assembled monolayer gate dielectric

To fabricate low-voltage FETs and integrated circuits based on individual ZnO nanowires, the global back-gate FET fabrication process described in section 4.2 is not suitable, since a global gate does not permit all the FETs on the substrate to be addressed individually. Therefore, local (i.e. patterned) gate electrodes are required. The studies in conjunction with the passivation of ZnO-nanowire transistors presented in chapter 7 showed that alkylphosphonic-acid molecules adsorb on the surface of ZnO and self-assemble into dense, hydrophobic monolayers. On the basis of these results, the use of a SAM as the gate dielectric in top-gate FETs is investigated in this chapter. The utilization of a SAM as a gate dielectric is widely used in the field of organic thin-film transistors [127, 128, 129, 104, 130, 131, 103] and has also been demonstrated for nanowire FETs [90, 132, 133, 20, 134] and carbon-nanotube FETs [135, 136, 137]. However, in all of these reports the SAM gate dielectric was utilized in a bottom-gate FET geometry. Thus, the SAM is anchored to the gate electrode or is part of an inorganic hybrid gate dielectric and the semiconductor is placed on top of the SAM. The top-gate approach investigated in this thesis is different, since the SAM is anchored directly on the active semiconductor channel of the FET and the metal gate electrode is placed on top of the SAM. The utilization of a SAM gate dielectric in a top-gate geometry is much less investigated in the literature. A common difficulty for the application of a SAM gate dielectric in a top-gate geometry is the polycrystalline or amorphous structure of many semiconductors utilized for FET fabrication. Such semiconductors usually have a large surface roughness, which makes the formation of a closed, defect-free SAM difficult. In contrast, the single-crystalline ZnO nanowires employed in this thesis are expected to provide a much smoother surface and therefore permit the formation of a dense SAM on the semiconductor surface. The use of a 22 nm thick gate dielectric based on the self-assembly of several molecular layers in a top-gate FET geometry was demonstrated for TFTs based on sputter-deposited ZnO [138, 139]. However, these self-assembled multilayer gate dielectrics are much thicker than the SAM gate dielectric developed in the framework of this thesis. The large thickness of the multilayer gate dielectric that was chosen for these reports might be related to the previously discussed problematic influence of the surface roughness.

## 8.1 Fabrication of top-gate ZnO-nanowire FETs with self-assembled monolayer gate dielectric

In contrast to the experiments presented in chapter 7, phosphonic-acid molecules with a hydrogen-terminated (rather than fluorine-terminated) alkyl chain are utilized in this sec-

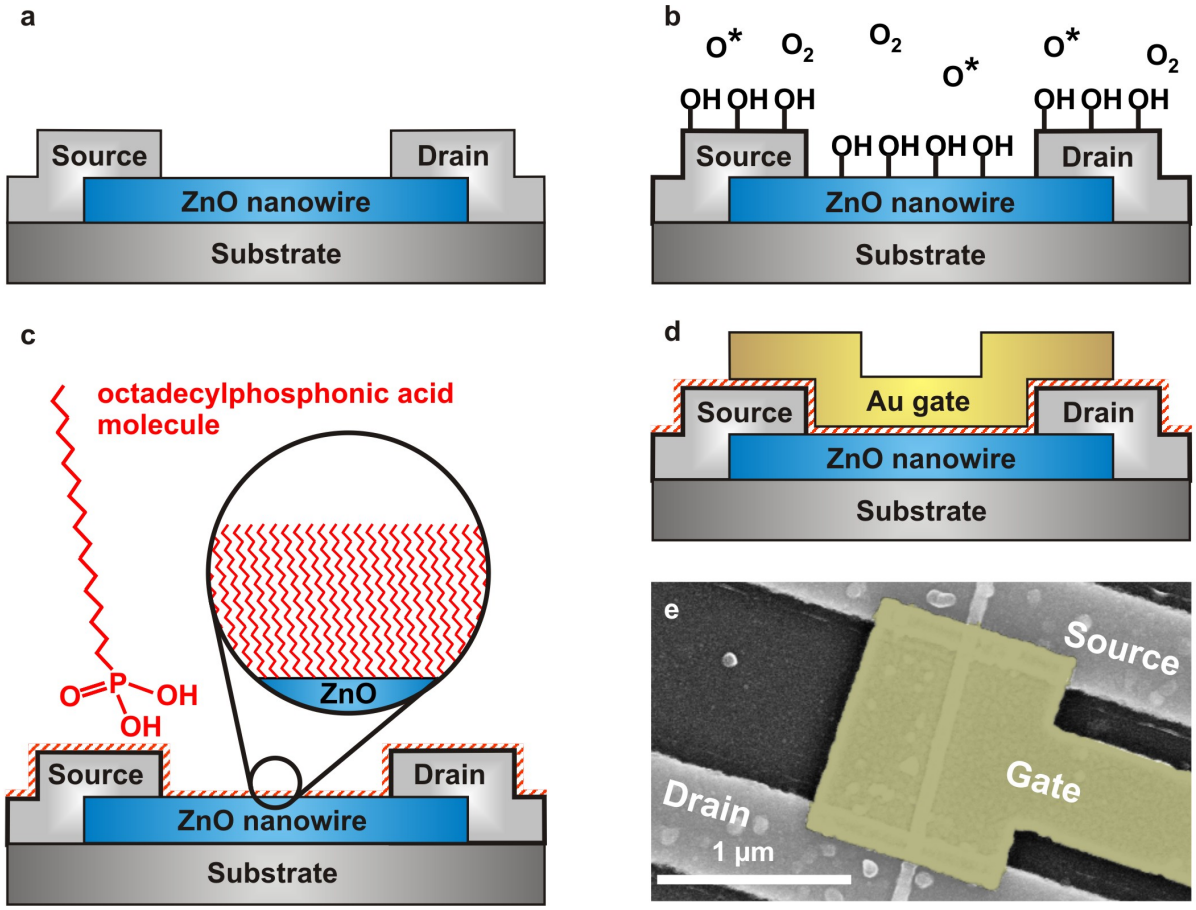


Figure 8.1: **Top-gate nanowire FET fabrication process.**
(a) ZnO nanowire with patterned source and drain contacts. (b) Oxygen-plasma treatment (30 sccm $O_2$, 10 mTorr, 50 W, 30 s) to increase the density of hydroxyl groups on the surface of the ZnO nanowire and on the aluminum source and drain contacts. (c) Immersion in a solution of isopropanol and octadecylphosphonic acid. The phosphonic-acid molecules adsorb on the ZnO nanowire and the aluminum source and drain contacts and form a densely packed self-assembled monolayer. The octadecylphosphonic-acid molecule is also depicted. (d) Top-gate electrodes are patterned by electron-beam lithography, metal evaporation and lift-off. (e) Scanning electron microscopy image of a completed top-gate ZnO-nanowire FET. The top-gate electrode of this FET consists of 80 nm thick gold.

tion. The formation of a high-quality, hydrophobic SAM based on hydrogen-terminated octadecylphosphonic acid molecules is confirmed by water contact angle measurements on a ZnO single-crystal. The obtained water contact angle of 104° is slightly smaller than the water contact angle obtained for the fluoroalkylphosphonic-acid molecules (115°, see section 7.1.1). The trend of slightly smaller contact angles for SAMs based on alkylphosphonic acids compared with fluoroalkylphosphonic acids was also observed for SAMs on vacuum-evaporated, plasma-oxidized aluminum films and can be attributed to the different surface energies of the hydrogen-terminated and fluorine-terminated SAMs [140].

The fabrication process for the top-gate FETs is outlined in figure 8.1. In the first step

aluminum source and drain (S/D) contacts are defined on the randomly dispersed and annealed ZnO nanowires by electron-beam lithography, Ar-plasma treatment of the nanowire surface in the contact regions, aluminum evaporation (80 nm thick), and lift off; this step is similar to the fabrication of the back-gate FETs in chapter 4.3 (figure 8.1a). In preparation for the self-assembly of the organic monolayer gate dielectric, the ZnO nanowire and the aluminum source and drain contacts are briefly exposed to a low-power oxygen plasma (30 sccm $O_2$, 10 mTorr, 50 W, 30 s; figure 8.1b). Immediately after the oxygen-plasma treatment, the substrate is immersed in an isopropanol solution of 1 mMol octadecylphosphonic acid. The molecules (figure 8.1c) adsorb on the hydroxyl-terminated ZnO and aluminum surfaces and form a densely packed self-assembled monolayer. Finally, top-gate electrodes are fabricated on the SAM gate dielectric using electron-beam lithography, metal evaporation (80 nm thick) and lift-off (figure 8.1d).

A scanning electron microscopy image of a ZnO-nanowire FET with a gold top-gate electrode and a channel length of 1 µm is shown in figure 8.1e. Because the SAM gate dielectric covers not only the ZnO nanowire, but also the plasma-oxidized aluminum S/D contacts, the gate electrode is allowed to overlap the S/D contacts. This permits the top-gate electrode to control the charge accumulation along the entire nanowire channel from source to drain, which is an advantage compared to FETs with top-gate electrodes that do not overlap the entire semiconductor channel (see section 8.3.1). FETs with gate electrodes that only partially overlap the semiconductor channel require additional doping or gating of the uncovered channel regions in order to achieve a usefully large transconductance [135]. The precise patterning of the top-gate electrode by electron-beam lithography makes it possible to realize overlaps as short as 100 nm in a reproducible manner.

It is important to emphasize that the top-gate fabrication process does not require high temperatures. The annealing of the ZnO nanowires can be performed on the growth substrate (see section 4.4) and is therefore separated from the device substrate. The maximum process temperature for the top-gate FETs is 160 °C which is required to bake the electron-beam resist. Therefore, the top-gate fabrication process reported here makes it possible to fabricate individually addressable FETs on a variety of substrates, such as glass and flexible plastics, that do not tolerate the use of elevated temperatures ($T < 200$ °C).

In the framework of this thesis, two different metals were investigated for the top-gate electrodes, namely gold and aluminum. The choice of the top-gate metal greatly affects the device characteristics and especially the gate current of the FETs, as will be shown in the following sections. First, the electrical characteristics of gold top-gate FETs are presented in section 8.2. The insulating properties of the SAM gate dielectric are investigated in comparison to ZnO-nanowire metal-semiconductor FETs with gold top-gate electrodes. In

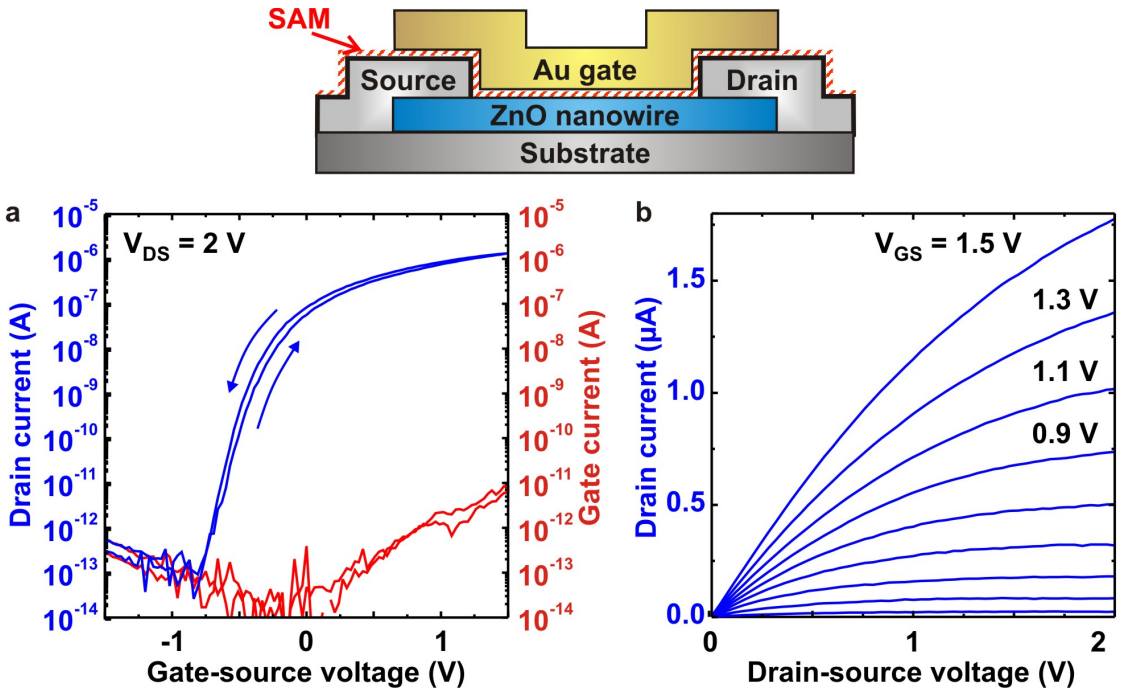


Figure 8.2: **Transfer and output characteristics of a gold top-gate ZnO-nanowire FET with SAM gate dielectric.**
The FET has a channel length of 2 µm and a nanowire diameter of 38 nm. From the transfer characteristics, a transconductance of 1 µS, an on/off current ratio of $10^7$, and a subthreshold slope of 90 mV/decade are extracted. The gate current through the SAM gate dielectric is below 10 pA.

section 8.3 the use of aluminum for the top-gate electrodes is presented and the structure of the gate dielectric layer is investigated by Transmission Electron Microscopy (TEM).

## 8.2 Gold top gates for ZnO-nanowire FETs

### 8.2.1 Electrical characteristics of gold top-gate ZnO-nanowire FETs with and without SAM gate dielectric

Figure 8.2 shows the transfer and output characteristics of a gold top-gate FET with a channel length of 2 µm based on a ZnO nanowire with a diameter of 38 nm. Due to the small thickness and large capacitance of the SAM gate dielectric the FET can be operated with small voltages. For $V_{DS} = 2\,V$ the FET has an on/off ratio of $10^7$, a subthreshold slope of 90 mV per decade, a transconductance of 1 µS, and negligible hysteresis. The gate current of the FET is below 10 pA even at the largest gate-source voltage of 1.5 V. The fact that the gate current is so small is remarkable considering that the expected thickness of the SAM gate dielectric layer is only about 2 nm. The possible contributions to the gate current are investigated in more detail in the following paragraphs.

The two contributions to the gate current are (1) the current between the gate electrode

and the source and drain contacts and (2) the current between the gate electrode and the ZnO nanowire. In those regions where the gate electrode overlaps the S/D contacts, the gate dielectric is a stack of the oxygen-plasma-grown $AlO_x$ and the 2 nm thick alkylphosphonic acid SAM. In those areas where the gate electrode overlaps the ZnO nanowire, the gate dielectric only consists of the alkylphosphonic acid SAM.

The overlap area between the gate electrode and the source and drain contacts is only about $10^{-9}\,cm^2$ (see figure 8.1e). Based on measurements of the current density through the $AlO_x$/SAM dielectric [104] which yield an upper limit of $10^{-5}\,A/cm^2$ at 3 V, the absolute current flowing between the gate electrode and the S/D contacts is expected to be at most 10 fA. Therefore, its contribution to the total gate current can be safely neglected, and in the following the focus is placed on the overlap between the gate electrode and the ZnO nanowire.

The different work functions of the top-gate electrode (5.1 eV for Au [55]) and the nanowire ($\sim$4.2 eV for n-type ZnO) lead to the formation of a Schottky barrier along the FET channel, and therefore to a depletion of the ZnO nanowire according to equation 2.23. In principle, FETs can be implemented without a gate dielectric in the form of a metal-semiconductor FET (MESFET). In a MESFET the density of free charge carriers and therefore the conductivity of the semiconductor are controlled by the modulation of the depletion width created by the Schottky barrier between the metal gate electrode and the semiconductor [36]. MESFETs based on semiconducting nanostrucutres have been demonstrated for ZnO nanorods [141], CdSe nanowires and nanobelts [142, 143], and GaAs nanowires [144]. This implies that the alkylphosphonic acid SAM gate dielectric is not strictly necessary for transistor operation when a gold top-gate electrode is utilized on a ZnO nanowire. In order to investigate the influence of the SAM gate dielectric on the transistor characteristics, a comparison between ZnO-nanowire devices with a gold top-gate electrode and either with a SAM gate dielectric (MISFET) or without a SAM gate dielectric (MESFET) is performed.

Figure 8.3a and b show the transfer characteristics of a MESFET (without SAM gate dielectric) and of a MISFET (with SAM gate dielectric). Both FETs have a channel length of $L = 1.5\,\mu m$. As expected, the gate current of the MESFET shows the characteristics of charge transport across a Schottky barrier described by thermionic-emission theory (see section 2.4). For negative gate-source voltages, the Schottky barrier between the gold gate electrode and the ZnO nanowire is biased in reverse direction. The gate current of 5 pA therefore corresponds to the voltage-dependent saturation current across the Schottky barrier. Positive gate-source voltages result in an exponential increase of the gate current due to the increasing charge transport across the built-in Schottky barrier, as expected from thermionic-emission theory (equation 2.32). In comparison to the MESFET, the gate current in the MISFET (figure 8.3b) is smaller by several orders of magnitude, both for

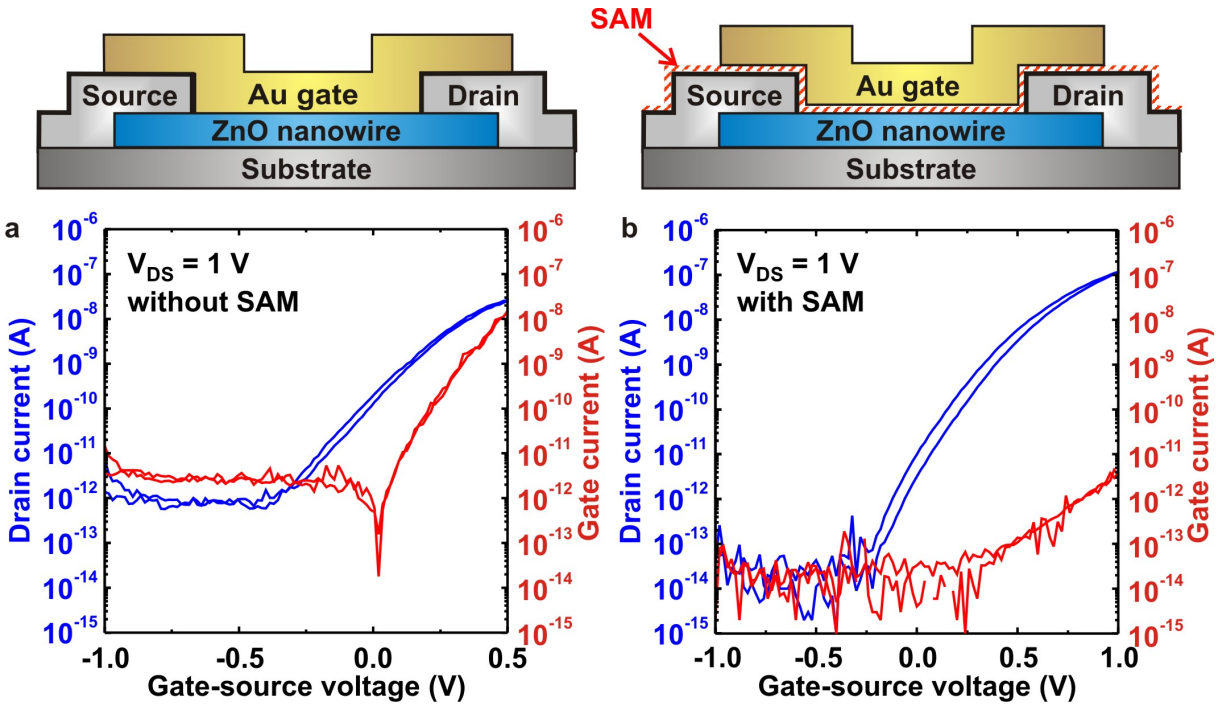


Figure 8.3: **Comparison between ZnO-nanowire MESFET and MISFET.** (a) Top-gate ZnO-nanowire FET without SAM gate dielectric (MESFET) and (b) with SAM gate dielectric (MISFET). The gate current in the MESFET displays the characteristic behavior of a Schottky diode, with a large exponential increase for positive gate-source voltages. In contrast, the gate current in the MISFET is below 0.1 pA for $V_{GS} < 0.5\,V$ and shows a far less pronounced increase for $V_{GS} > 0.5\,V$.

negative and especially for positive gate-source voltages. For $V_{GS} < 0.5\,V$ the gate current is near the resolution limit of the measurement system (0.1 pA). For $V_{GS} > 0.5\,V$ the gate current increases approximately exponentially with $V_{GS}$, but the slope is significantly smaller than in the MESFET. The comparison of the gate currents in the MESFET and the MISFET clearly demonstrates the insulating properties of the SAM on the ZnO nanowires. In the following section, the gate currents of 16 MESFETs and 25 MISFETs are compared, and a more detailed analysis of the gate currents of the MESFETs and the MISFETs is performed.

### 8.2.2 Statistical investigation of the gate currents of ZnO-nanowire MESFETs and MISFETs

In order to quantify and better understand the reduction of the gate current as a consequence of the presence of the SAM gate dielectric, 16 MESFETs and 25 MISFETs are manufactured and the gate currents of the devices are compared.

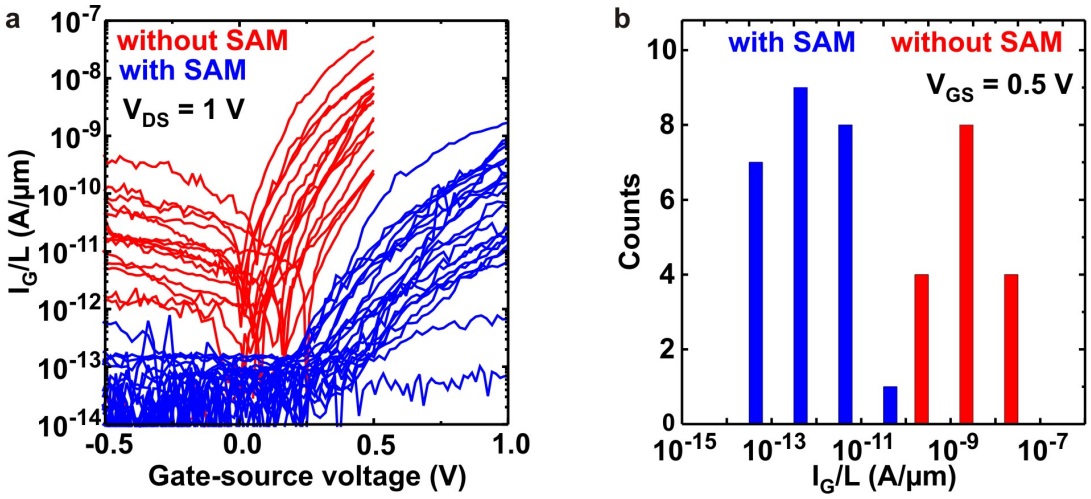


Figure 8.4: **Comparison of the gate currents of 16 MESFETs and 25 MISFETs.** (a) Gate currents $I_G$ normalized by the FET channel length L. The gate currents of the MISFETs (blue curves) and the MESFETs (red curves) are subject to considerable fluctuations and are spread over two orders of magnitude. The fluctuations are most probably caused by variations in the electrical properties of the wet-chemical grown ZnO nanowires. (b) Distribution of the normalized gate currents obtained for $V_{GS}$= 0.5 V. In consequence of the SAM gate dielectric, the gate currents of the MISFETs are reduced by three orders of magnitude compared to the gate currents of the MESFETs.

### Comparison of gate currents of MESFETs and MISFETs

Figure 8.4a shows the gate currents of the 16 MESFETs in red and the 25 MISFETs in blue. All gate currents are measured for a drain-source voltage of 1 V. Since the absolute current across a Schottky barrier is proportional to the overlap area of the gate electrode and the ZnO nanowire, the gate currents are normalized to the channel length for better comparison. For the same reason, the gate current should also be normalized to the nanowire diameter. However, since the diameter of the nanowires chosen for this study varies by only about 30% (50 nm±20 nm, see section 4.2) this was not done here. As can be seen, gate currents for both the MESFETs and the MISFETs are subject to considerable fluctuations and vary over two orders of magnitude. The observed fluctuations between the individual FETs are not surprising, considering the large fluctuations of the electrical properties of the individual wet-chemically grown ZnO nanowires (section 6.2). Independent of the fluctuations, the substantial difference between the gate currents of the MESFETs and the MISFETs is apparent. Over the whole gate-bias range, the gate currents of the investigated MISFETs are much smaller compared to the gate currents of the MESFETs. Figure 8.4b shows the distribution of the normalized gate currents for a gate-source voltage of 0.5 V. The peak of the distribution for the MESFETs is in the range of $10^{-9}$ A/µm to $10^{-8}$ A/µm. This corresponds to a current density of J $\sim 10^0$ to $10^1$ A/cm$^2$, assuming a nanowire diameter of 50 nm. The gate current distri-

bution of the MISFETs peaks at $10^{-13}$ A/µm to $10^{-12}$ A/µm, corresponding to a current density J $\sim 10^{-4}$ A/cm$^2$ to $10^{-3}$ A/cm$^2$. The average gate current at $V_{GS} = 0.5$ V for the MISFETs is therefore more than three orders of magnitude smaller compared to the MESFETs. In the following the statistical distributions of the gate currents of the MESFETs and the MISFETs are analyzed.

### Gate-current analysis: MESFET statistics

The gate currents of the 16 MESFETs resemble the characteristics of a Schottky diode and are therefore described by thermionic-emission (TE) theory. In order to account for deviations from the pure TE theory, the dimensionless ideality factor $\eta$ is introduced (see section 2.4). Figure 8.5 shows the statistical distribution of the barrier heights $\phi_b$ and the ideality factors $\eta$ extracted by fitting the gate currents of the MESFETs to equation 2.33.

Although the individual MESFET gate currents vary over two orders of magnitude, the distribution of the barrier heights and ideality factors is rather narrow. The average built-in potential barrier height is $\overline{\phi}_b = 0.55$ eV and therefore significantly smaller than the maximum possible value $\phi_{ms} = 0.9$ eV that is given by the difference between the work functions of gold and ZnO. Further, for most of the Schottky diodes, $\eta$ is above two, which indicates gate-current contributions from mechanisms other than TE [145]. Large ideality factors $\eta$ and built-in potential barrier heights $\phi_b$ smaller than the work-function difference are commonly observed for Schottky diodes on gold and ZnO [24, 146, 147], and various explanations for this observation are found in the literature.

One possible explanation is a Gaussian distribution of $\phi_b$ along the length of the nanowire [82, 148]. In such a situation, the gate current will flow mostly across the regions with low $\phi_b$ and therefore reduce the extracted effective $\phi_b$. A second explanation is the assumption of an interfacial layer between gold and ZnO that introduces a distribution of interface states. This situation is depicted in figure 8.5c. The interfacial layer is assumed to be transparent to electrons, but due to the charging of the interface states, $\phi_{ms}$ partially drops across the interfacial layer [36]. Under forward bias most of the applied voltage may be compensated for by the charging of the interface states. Hence, the gate-current increase will be smaller than expected, and consequently the ideality factor of the junction is increased (figure 8.5d).

### Gate-current analysis: MISFET statistics

As can be seen from figure 8.4a (blue curves), the gate currents of the MISFETs are asymmetric with respect to $V_{GS} = 0$ V. For most of the MISFETs the gate current starts to increase for $V_{GS} > 0.3$ V. This asymmetry is attributed to the Schottky diode connected

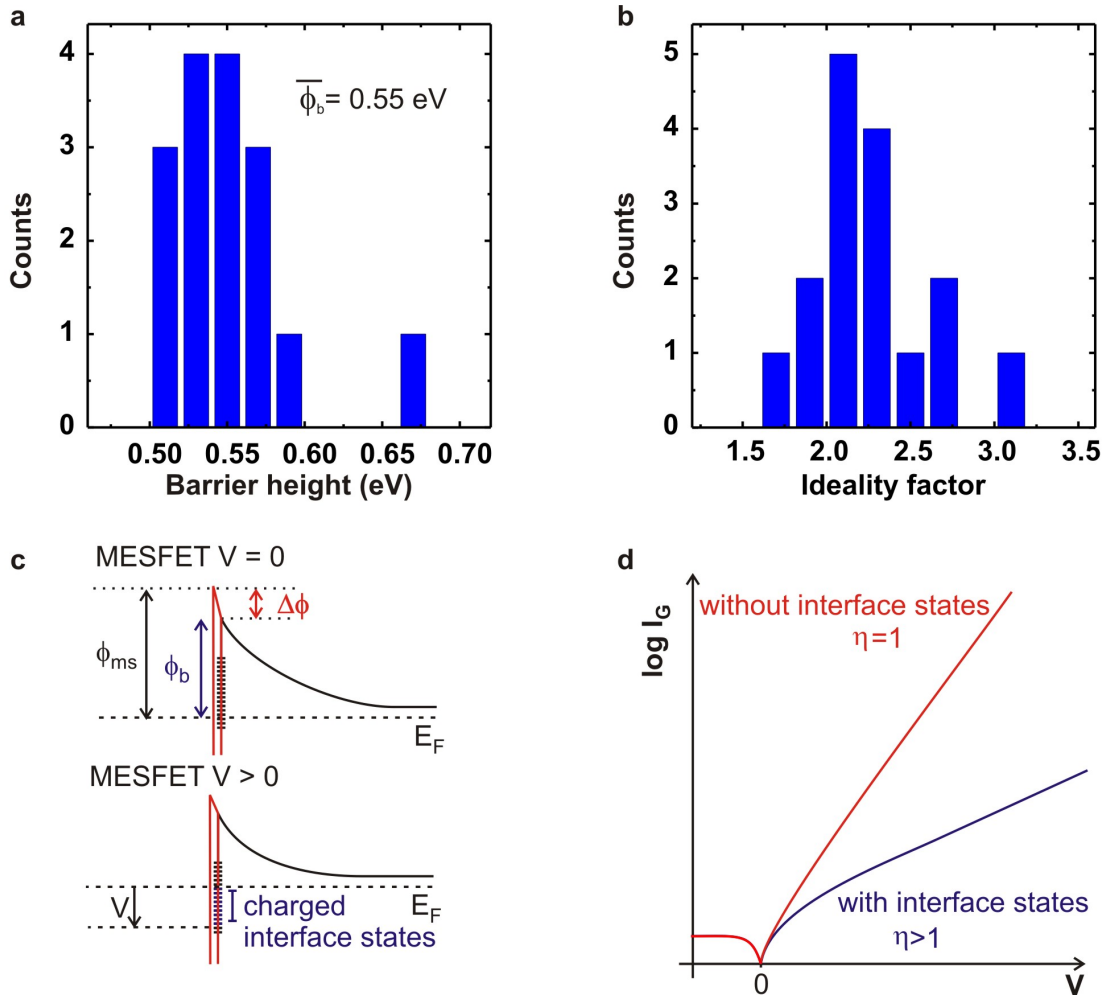


Figure 8.5: **Statistical analysis of MESFET devices.**
(a) Distribution of the Schottky-barrier heights $\phi_b$ and (b) ideality factors $\eta$ for the 16 MESFETs of figure 8.4a. The average barrier height is smaller than expected from the work-function difference between gold and ZnO ($\phi_{ms} = 0.9\,\mathrm{eV}$). (c) Schematic band diagram of the metal/semiconductor interface in the presence of a distribution of interface states. The interface states cause a lowering of the effective barrier height $\phi_b$ and an increase of the ideality factor $\eta$. (d) Effect of an increased ideality factor (blue curve, with interface states) on the gate current.

in series to the insulating SAM gate dielectric. As already mentioned before, the expected thickness of the SAM gate dielectric is only about 2 nm, so that electrons can tunnel through the dielectric. The series connection of a Schottky diode with a thin insulating layer is described by the so-called MIS Schottky-diode model [149]. A schematic band diagram for V = 0 V is depicted in figure 8.6a. According to the MIS Schottky-diode model, the insulating tunnel barrier modifies the current-voltage characteristics of an ideal Schottky diode by introducing a voltage dependence of the ideality factor $\boldsymbol{\eta(V)}$ and by lowering the overall current magnitude described by a tunnel correction factor $\mathbf{exp(\sqrt{\phi_t} \cdot d_t)}$ :

$$\mathrm{I_{MIS}} = \mathrm{I_S}(\phi_b) \cdot \left( \exp\left( \frac{q\mathrm{V}}{\boldsymbol{\eta(V)} \mathrm{k_B T}} \right) - 1 \right) \cdot \mathbf{exp}(\sqrt{\boldsymbol{\phi_t}} \cdot \mathbf{d_t}), \tag{8.1}$$

with the built-in potential barrier height in the semiconductor $\phi_b$, the tunnel-barrier height $\phi_t$, the tunnel-barrier thickness $\mathrm{d_t}$, and the saturation current of the Schottky diode $\mathrm{I_S}(\phi_b)$.

**Gate-voltage-dependent ideality factor:** Due to the introduction of a tunnel barrier, the potential difference between semiconductor and metal $\phi_{ms}$ drops in part across the insulating layer, and the potential at the semiconductor surface is reduced compared to the situation in an ideal Schottky diode. The ideality factor $\eta$ is then given by:

$$\eta(V) = 1 + \frac{\mathrm{d_t} \cdot \varepsilon_S}{\mathrm{W_D(V)} \cdot \varepsilon_I}, \tag{8.2}$$

with the voltage-dependent semiconductor depletion width $\mathrm{W_D(V)}$, the permittivity of the semiconductor $\varepsilon_s$ and the permittivity of the insulator $\varepsilon_i$. Under forward bias, the depletion width is expected to decrease and therefore $\eta(V)$ increases. This leads to a reduction of the gate-current increase under forward bias (see figure 8.6b).

**Tunnel attenuation factor:** Due to the insulating tunnel barrier, the overall current magnitude is decreased. The decrease of the current is described by the introduction of a tunnel correction factor, which depends exponentially on the square root of the tunnel-barrier height $\phi_\mathrm{t}$ and the thickness of the tunnel barrier $\mathrm{d_t}$. The tunnel correction simply shifts the current-voltage characteristics of the ideal Schottky diode towards lower currents (see figure8.6b). Therefore, a larger "apparent" barrier height is evaluated when the current-voltage characteristics of the MIS Schottky diode are modeled with the TE equation. The term "apparent" thereby refers to the fact that the evaluated barrier height is an effective value describing the influence of the insulating layer in connection with the Schottky barrier. The Schottky-barrier height $\phi_b$ at the semiconductor/insulator interface will in general be lower than the apparent barrier height extracted from the current-voltage characteristics. This was confirmed by capacitance-voltage measurements on $\mathrm{Si/SiO_2}$ MIS Schottky diodes [149] and Si/SAM MIS Schottky diodes [150, 151], which yield a smaller $\phi_b$ compared to the barrier height extracted from current-voltage measurements.

As can be seen from the MISFET gate currents plotted in figure 8.4a, the gate current is indeed greatly reduced over the full range of $\mathrm{V_{GS}}$ compared to the gate currents of the MESFETs. This is in accordance with the described tunnel correction to the common TE equation.

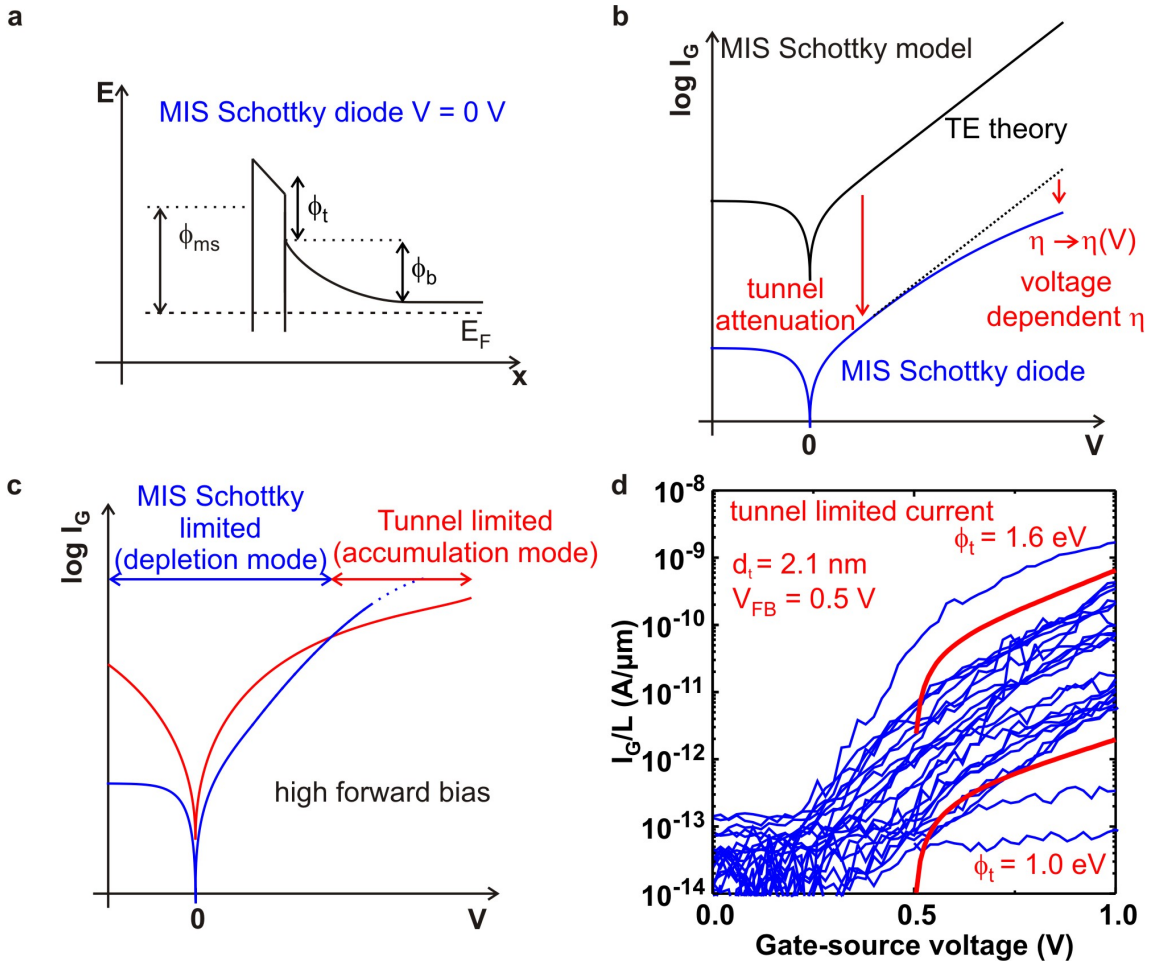


Figure 8.6: **MIS Schottky-diode model and effect of a tunnel barrier on the gate current.**
(a) Schematic band diagram of the MIS Schottky-diode model. The insulator introduces an additional tunnel barrier $\phi_t$ connected in series to the Schottky-barrier height $\phi_b$. (b) Modification of the current expected from thermionic emission (TE) theory by the introduction of the tunnel barrier (MIS Schottky diode). The overall current is attenuated by the presence of the tunnel barrier, and the current increase for higher voltages is decreased due to the voltage dependence of the ideality factor $\eta$(V). (c) Possible gate-current limitations for higher voltages. When the external voltage V compensates the Schottky barrier $\phi_b$, the operation mode of the FET changes from depletion regime to accumulation regime. In the accumulation regime the tunnel barrier is expected to limit the gate current (red curve). The voltage at which the transition to the accumulation regime occurs depends on $\phi_b$. (d) Gate currents of 25 MISFETs (blue curves). The red curves show the computed gate currents according to tunnel-limited transport. The gate currents follow the general trend expected for tunnel-limited transport and are found for a tunnel-barrier height ranging from 1 to 1.6 eV.

### Gate-current increase for $V_{GS} > 0.3\,V$

The observed increase in gate current for $V_{GS} > 0.3\,V$ (figure 8.4a) can be described by the MIS Schottky-diode model introduced in the previous paragraph, as long as the

semiconductor depletion width $W_D$ is larger than zero. According to this model, the gate current is the attenuated forward current across the gold/ZnO Schottky diode. However, depending on the height of the Schottky barrier $\phi_b$, the depletion width inside the semiconductor is expected to drop to zero for more positive $V_{GS}$. This situation corresponds to the so-called flat-band condition, where $V_{GS}$ compensates the built-in potential barrier $\phi_b$ and the device operation changes from the depletion regime to the accumulation regime (i.e. charge carriers are accumulated at the semiconductor/insulator interface). For $W_D = 0$, the MIS Schottky-diode model predicts $\eta \to \infty$ (see equation 8.2), and therefore a physically irrelevant reduction of the gate current. In a real device, the gate current in the accumulation regime is limited by the tunnel barrier and increases with increasing voltage according to the Simmons tunnel equation [152]:

$$I_t \sim \phi_t \cdot \exp\left(-\sqrt{\phi_t - \frac{V}{2}} \cdot d_t\right) \tag{8.3}$$

The transition between charge transport limited by the MIS Schottky diode and charge transport limited by tunneling has been experimentally observed for MIS Schottky diodes based on SAMs on n-type silicon [153] and is depicted in figure 8.6c.

Figure 8.6d shows the measured gate currents of the 25 MISFETs in blue and gate currents computed with the help of equation 8.3 in red. For the computation, the thickness of the tunnel barrier $\phi_t$ is set to 2.1 nm (the estimated thickness of the SAM), and a flat-band voltage $V_{FB} = 0.5\,V$ is introduced to account for the Schottky-barrier height $\phi_b$. The measured MISFET gate currents are well described by equation 8.3 and yield a tunnel-barrier height ranging from 1 eV to 1.6 eV for the given parameters.

The estimated tunnel-barrier heights of 1 eV to 1.6 eV are much smaller than the band gaps reported for molecules similar to the alkylphosphonic acid utilized here ($E_{gap}^{mol} = 9 - 10\,eV$ for alkane chains [154]). However, tunnel-barrier heights very similar to those extracted for the devices in this thesis have been reported for tunnel junctions based on SAMs on Si [153, 155] and GaAs [156, 157] ($\phi_t = 0.8\,eV - 1.5\,eV$). The reduction of the tunnel barriers for the condensed molecules is attributed to the close packing of the molecules in the self-assembled monolayer and to the interaction of the monolayer with the substrate [155].

In summary, the charge transport through the SAM gate dielectric is well described by the MIS Schottky-diode model. The presence of the SAM decreases the gate current by several orders of magnitude over the entire range of $V_{GS}$ compared to MESFETs without SAM. Depending on the Schottky-barrier height $\phi_b$ of the MIS Schottky diodes, the increase of the gate current observed for $V_{GS} > 0.3$ V is either due to an increase in the forward current across the MIS Schottky diode (depletion regime) or due to an increase in the

tunnel current through the SAM gate dielectric (accumulation regime). However, since the gate current is below the resolution limit of the measurement setup for $V_{GS} < 0.3\,V$, it is not possible to estimate the Schottky-barrier height $\phi_b$ of the MISFETs and distinguish which of the current contributions dominates the gate current in this regime.

## 8.3 Aluminum top gates for ZnO-nanowire FETs

In this section the use of aluminum as the gate metal for top-gate ZnO-nanowire FETs is investigated. Two different gate dielectrics are utilized. In section 8.3.1, the insulating properties of the interfacial aluminum oxide layer that forms spontaneously at the interface between the oxygen-plasma-treated ZnO nanowire and the aluminum top gate are examined. Subsequently, the use of a SAM gate dielectric with an aluminum top-gate electrode is investigated in section 8.3.2.

### 8.3.1 Interfacial aluminum oxide as a gate dielectric for aluminum top-gate FETs

In chapter 5 the effects of different plasma treatments on the properties of the electrical contact between ZnO and aluminum were investigated. It was shown that an insulating interfacial aluminum oxide layer is formed at the interface between ZnO and aluminum, when the ZnO nanowire is exposed to an $O_2$ plasma immediately prior to the aluminum deposition. In the following it is investigated whether the ability to tune the ZnO/Al interface from ohmic (Ar-plasma treatment) to insulating ($O_2$-plasma treatment) permits the fabrication of top-gate ZnO-nanowire FETs which utilize the interfacial aluminum oxide layer as the gate dielectric.

To prepare ZnO-nanowires FET with interfacial aluminum oxide gate dielectric, ZnO nanowires are dispersed on a $Si/SiO_2$ substrate and annealed at 600°C. The source and drain contacts are fabricated by EBL, Ar-plasma treatment, and thermal evaporation of 80 nm thick aluminum (Ar-contacts; see section 5.2). Next, the top gate is defined in the center of the nanowire by EBL, oxygen-plasma treatment (30 sccm $O_2$, 10 mTorr, 50 W, 15 sec), and aluminum evaporation ($O_2$-contact;, see section 5.4). A schematic of the FET is shown in figure 8.7a. In order to allow time for the formation of the interfacial aluminum oxide layer, the devices are characterized after two days of storage in ambient air. Since the FETs are realized on a $Si/SiO_2$ substrate, the charge-carrier concentration in the ZnO nanowire can be modulated either by the global silicon back gate or by the local aluminum top gate. This so-called dual-gate configuration makes it possible to compare the characteristics of the Al top-gate FET to the characteristics of the same ZnO nanowire in a global back-gate geometry.

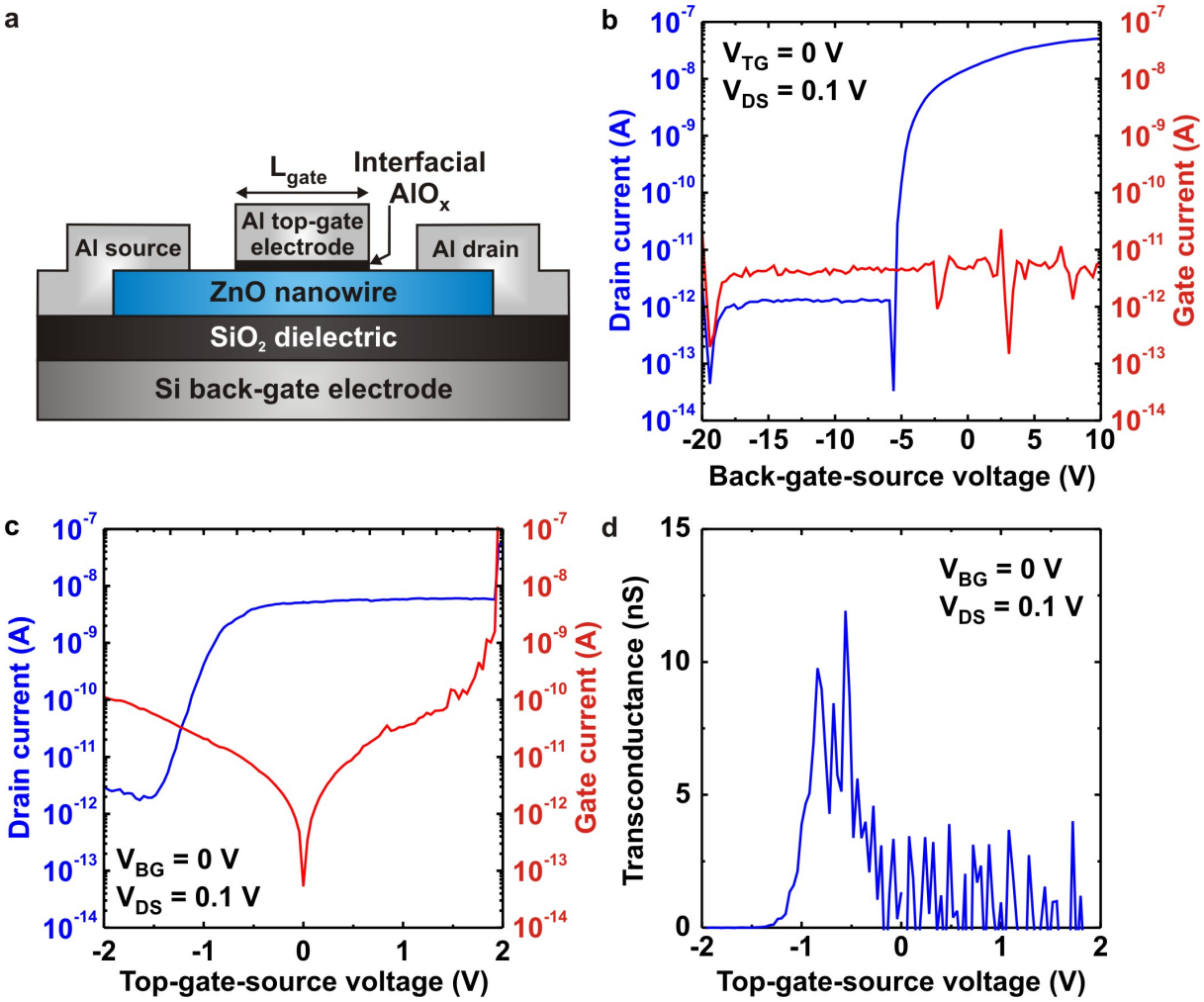


Figure 8.7: **ZnO-nanowire FET in a dual-gate configuration with a global back gate and a non-overlapping Al top gate.**
(a) Schematic device structure of a dual-gate ZnO-nanowire FET (L = 3 µm, $d_{NW}$ = 40 nm, $t_{SiO_2}$ = 100 nm). The conductivity of the ZnO nanowire can be modulated either by the global back gate or by the local top gate. The gate dielectric for the top gate consists of the thin aluminum oxide layer that forms spontaneously at the interface between the $O_2$-plasma-treated ZnO and the deposited Al top gate. (b) Back-gate transfer characteristics for $V_{DS} = 0.1\,V$ and a top-gate voltage $V_{TG} = 0\,V$. (c) Top-gate transfer characteristics for $V_{DS} = 0.1\,V$ and a back-gate voltage $V_{BG} = 0\,V$. The gate current increases symmetrically, as expected for charge carriers tunneling through a thin barrier (see figure 8.6c). At $V_{TG} = 2\,V$ the gate dielectric breaks down. (d) Transconductance as a function of the top-gate voltage. Due to the fact that the top gate does not overlap the source and drain contacts, the transconductance is near zero for $V_{TG} > 0\,V$.

Figure 8.7b shows the transfer characteristics of a dual-gate ZnO-nanowire FET obtained by sweeping the back-gate voltage ($V_{BG}$) from -20 V to 10 V. The drain-source voltage is 0.1 V and the top-gate voltage ($V_{TG}$) is 0 V. The FET has a channel length L = 3 µm and the nanowire diameter is $d_{NW}$ = 40 nm. The gate current is shown in red. Figure 8.7c shows the transfer characteristics of the same device when the drain current is

modulated by sweeping the top-gate voltage $V_{TG}$ ($V_{DS} = 0.1\,V$ and $V_{BG} = 0\,V$). Because the interfacial aluminum oxide top-gate dielectric is thinner and has a larger capacitance than the $SiO_2$ back-gate dielectric, the voltage necessary to modulate the charge-carrier concentration is much smaller ($V_{TG} = \pm 2\,V$). Again, the gate current is plotted in red. In contrast to the gold top-gate devices presented in section 8.2.1, the top gate does not overlap the source and drain contacts. Therefore, the gate current shown in figure 8.7c is a measure of the leakage current through the interfacial aluminum oxide layer at the interface between the $O_2$-plasma-treated ZnO nanowire and the aluminum top gate.

### Gate-current analysis

The behavior of the gate current can be well understood with the model introduced in the previous section for gold top gates with SAM gate dielectric. Similar to the SAM gate dielectric, the thin interfacial aluminum oxide layer acts as a tunnel barrier. For top-gate voltages $V_{TG}$ between -1 V and 1 V, the gate current shows a symmetric increase around 0 V as expected for current limited by tunneling (see equation 8.3 and figure 8.6c, red curve). A fit of the gate current with equation 8.3 yields a tunnel-barrier thickness of $d_t = 1.5\,nm$ and a tunnel-barrier height of $\phi_t = 2.8$ eV. The extracted thickness of the tunnel barrier is in accordance with the estimated thickness of the interfacial aluminum oxide layer in section 5.4. For larger $V_{TG}$, the gate-current increase becomes asymmetric. While for $V_{TG} < -1\,V$, the slope of the gate current slightly decreases, the gate current starts to fluctuate for $V_{TG} > 1\,V$ and finally the gate dielectric breaks down at $V_{TG} \sim 2\,V$. The asymmetry of the gate current in this regime indicates the presence of a Schottky barrier connected in series to the tunnel junction. For increasingly negative $V_{TG}$, the depletion width in the ZnO increases and $V_{TG}$ drops across the depleted part of the ZnO nanowire and the interfacial aluminum oxide. For increasingly positive $V_{TG}$, the depletion width in the ZnO nanowire is reduced. Hence, the voltage drop across the interfacial aluminum oxide increases and approaches the breakdown voltage. In summary, the gate-dielectric stack (Schottky barrier + tunnel barrier, see figure 8.6c) of the aluminum top-gate FETs with interfacial aluminum oxide gate dielectric therefore resembles the gate-dielectric stack of the gold top-gate FETs with a SAM gate dielectric. However, in contrast to the gold top-gate FETs where the Schottky barrier limits the gate current over a wide range of $V_{GS}$, the gate current in the aluminum top-gate FETs with interfacial aluminum oxide gate dielectric is limited by the tunnel barrier over the whole range of gate-bias. This indicates that the height of the Schottky barrier between ZnO and Al is small, as expected from the small difference between the work function of Al (4.3 eV [55]) and ZnO ($\phi_{ms} \approx 0.1\,eV$). As a consequence of the breakdown of the dielectric, the use of the top-gate FETs with interfacial aluminum oxide gate dielectric is limited to relatively small gate-source voltages between -2 V to 1 V.

### Transconductance analysis

As mentioned in section 8.1, a gate electrode that only partially overlaps the semiconductor channel along a length $L_{Gate}$ (see figure 8.7a) is unfavorable since this requires additional electrostatic or chemical doping of the channel areas not controlled by the gate. This becomes apparent when the relationship between the transconductance and the top-gate voltage is considered (see figure 8.7d). For positive top-gate-source voltages the transconductance drops to near to zero. This is due to the fact that parts of the nanowire channel are not controlled by the gate, so that increasing the gate bias beyond 0 V does not lead to a larger drain current. This clearly shows the necessity of a gate electrode that overlaps the S/D contacts and thus controls the entire channel.

In summary, the spontaneous formation of an $AlO_x$ layer at the interface between ZnO nanowire and Al top gate can be exploited to fabricate top-gate ZnO-nanowire FETs. However, the low quality of the interfacial aluminum oxide and the need for a gate electrode overlapping the entire nanowire channel and the S/D contacts limit the applicability of the interfacial aluminum oxide as a gate dielectric.

## 8.3.2 Aluminum top-gate ZnO-nanowire FETs with SAM gate dielectric

In subsection 8.2 it has been shown that the gate current of a gold top-gate ZnO-nanowire FET can be significantly reduced when the ZnO nanowire is covered with a SAM that acts as a gate dielectric layer. Based on these results, the influence of a SAM on the gate currents of aluminum top-gate FETs is investigated. Since the insulating SAM based on alkylphosphonic acid molecules covers the ZnO nanowire and also the aluminum S/D contacts, the use of the SAM permits the gate electrode to overlap the S/D contacts.

### Investigation of Al/$AlO_x$/SAM/Al leakage current

In order to quantify the insulating properties of the SAM in the regions where the Al gate electrode and the plasma-oxidized Al S/D contacts overlap, leakage-current-test junctions are fabricated with the help of polyimide shadow masks. Figure 8.8a shows a photograph and a schematic cross section of the test junctions. The test junctions consist of an 80 nm thick, $O_2$-plasma-oxidized aluminum bottom electrode, coated with a SAM based on pentadecylfluoro-octadecylphosphonic acid ($FC_{18}$-SAM, see inset figure 8.8b), and an 80 nm thick aluminum top electrode. The test-junction area is 60 µm x 60 µm. The thickness of the plasma-grown aluminum oxide is expected to be around 3-4 nm [104]. Figure 8.8b shows the current density through 14 leakage-test junctions (blue curves, Al/$AlO_x$/$FC_{18}$-SAM/Al) as a function of the applied voltage. For comparison, the red curve shows the leakage current density of a test junction without $FC_{18}$-SAM, in which

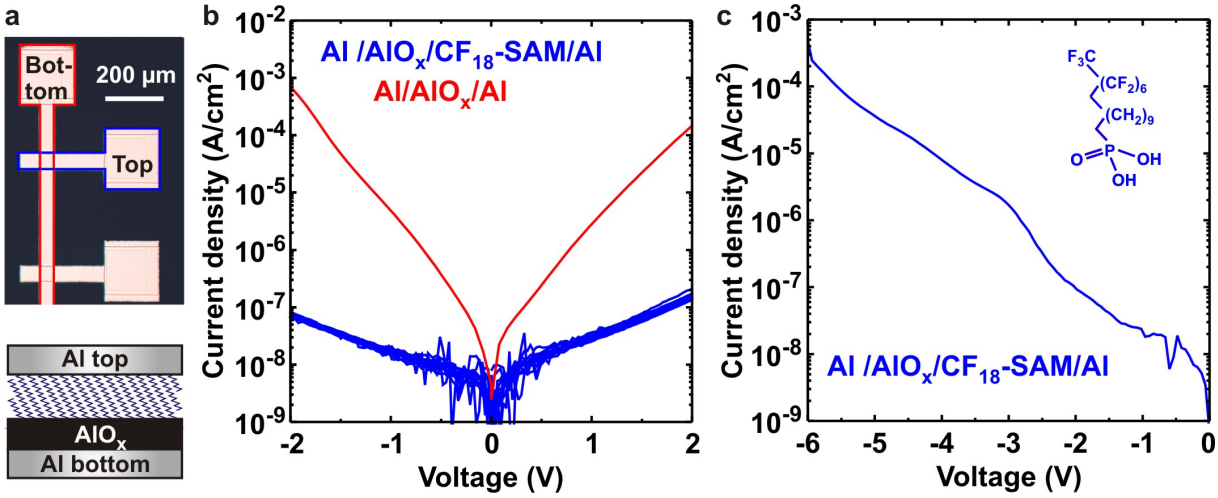


Figure 8.8: **Leakage current density through Al/AlO$_x$/FC$_{18}$-SAM/Al junctions.** (a) Optical microscopy image and schematic cross section of the leakage-current-test junctions. The Al/AlO$_x$/FC$_{18}$-SAM/Al junction is defined in the overlap areas between the metal bottom electrode (framed red) and the metal top electrodes (framed blue). (b) Leakage current density through 14 Al/AlO$_x$/FC$_{18}$-SAM/Al junctions (blue curves). The insignificant variation of the leakage current confirms the junction uniformity. The red curve corresponds to the leakage current density of similar test junctions without FC$_{18}$-SAM. The FC$_{18}$-SAM reduces the leakage current density by more than three orders of magnitude. (c) Leakage current density through an Al/AlO$_x$/FC$_{18}$-SAM/Al junction under application of higher voltages. Up to -6 V, the junction shows no indication of a dielectric breakdown.

the dielectric layer consist only of the plasma-grown aluminum oxide (Al/AlO$_x$/Al). The addition of the SAM leads to a reduction of the current density by more than three orders of magnitude at a voltage of 2 V. The fact that the current fluctuations observed for the 14 Al/AlO$_x$/FC$_{18}$-SAM/Al junctions are extremely small indicates that the junctions are very uniform. Figure 8.8c shows the leakage current density through an Al/AlO$_x$/FC$_{18}$-SAM/Al junction for voltages between 0 V and -6 V. This voltage range corresponds to the voltage drops observed across the overlap areas in the FETs presented later in this chapter (see e.g. figure 8.11). Up to a voltage of -6 V the junctions show no indication of a dielectric breakdown. The experiments therefore clearly demonstrate the insulating properties of the FC$_{18}$-SAM sandwiched between a plasma-oxidized aluminum bottom electrode and an evaporated aluminum top electrode.

### Electrical characteristics of aluminum top-gate ZnO-nanowire FETs with SAM gate dielectric

The small current leakage and the large breakdown voltage of the Al/AlO$_x$/FC$_{18}$-SAM dielectric with Al top electrode suggests that aluminum top-gate ZnO-nanowire FETs with gate electrodes overlapping the entire SAM-covered semiconductor channel and the

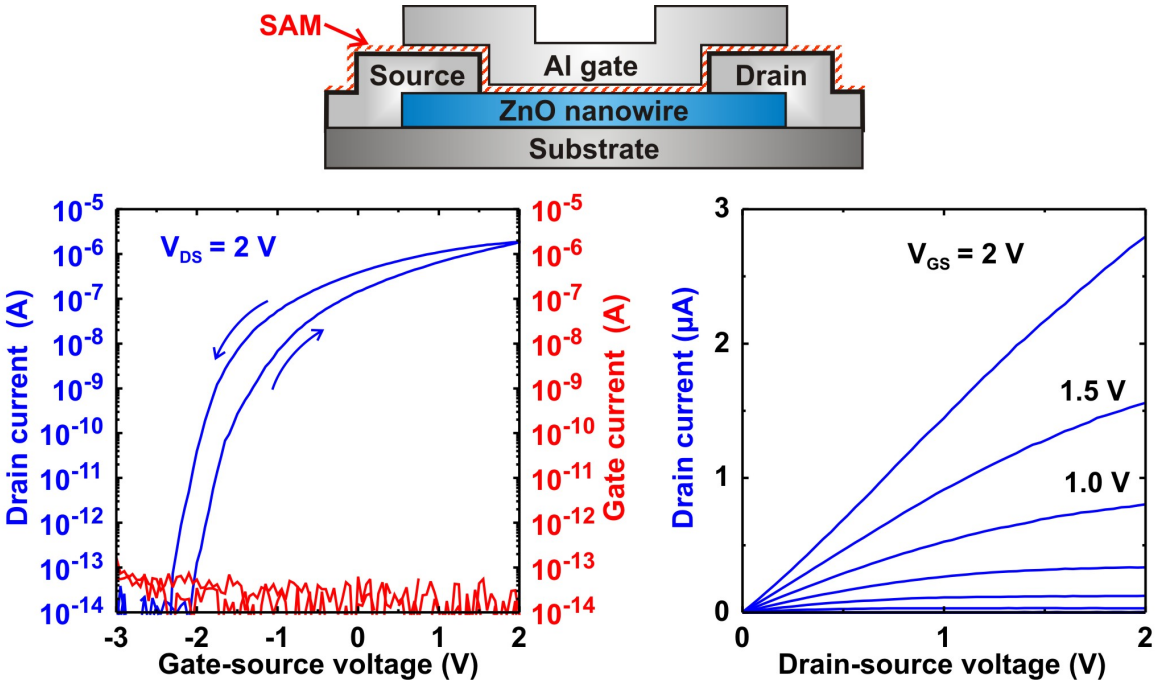


Figure 8.9: **Transfer and output characteristics of an aluminum top-gate ZnO-nanowire FET with SAM gate dielectric.**
The FET has a channel length of 1.5 µm and the nanowire diameter is 60 nm. From the transfer characteristics a transconductance of 1 µS, an on/off drain current ratio of $10^7$, and a subthreshold slope of 120 mV/decade are extracted.

SAM-covered aluminum S/D contacts can be fabricated with good yield and performance. The fabrication procedure for the aluminum top-gate FETs with SAM gate dielectric is similar to the fabrication of the gold top-gate FETs described in section 8.1.

Figure 8.9 shows the transfer and output characteristics of an aluminum top-gate FET with SAM gate dielectric (L = 1.5 µm, $d_{NW}$ = 60 nm). The FET has a transconductance of 1 µS, an on/off ratio of $10^7$, a subthreshold slope of 120 mV/decade, and a small hysteresis of 0.4 V. It is especially remarkable that the gate current is close to the resolution limit (0.1 pA) over the whole range of gate-source voltages. For $V_{GS} < 0$ V, the gate-current is expected to be small in accordance with the observations from the gold top-gate FETs. However, even for $V_{GS} > 0$ V, the gate current stays below 0.1 pA up to a gate-source voltage of 2 V. This is in contrast to the observations of the gold top-gate FETs and is especially surprising with regard to the expected lower height of the Schottky barrier between aluminum and ZnO compared to gold and ZnO ($\phi_{ms}^{Al-ZnO} \approx 0.1$ eV, $\phi_{ms}^{Au-ZnO} \approx 0.9$ eV). For a lower Schottky barrier height, the leakage current is expected to be dominated by the tunneling current, as was previously observed for the top-gate FETs with interfacial aluminum oxide gate dielectric in section 8.3.1. However, the gate current of the aluminum top-gate FETs with SAM gate dielectric is more than four orders of magnitude lower than the gate current of the top-gate FETs with interfacial aluminum oxide gate dielectric for $V_{GS} = 2$ V.

Thus, the observation that the gate current is so small is neither in accordance with the MIS Schottky-diode model, nor with the assumption of a tunnel-limited gate current. It is important to mention that the observation of the small gate current is made independent of whether the SAM has a fluorine-terminated or hydrogen-terminated alkyl chain. The gate current is below 0.1 pA even when the $O_2$-plasma treatment in preparation for the formation of the SAM is replaced by an Ar-plasma treatment. (Note that the formation of a densely packed, hydrophobic SAM is independent of whether the surface is treated with an Ar plasma or an $O_2$ plasma prior to the immersion in the (fluoro)alkylphosphonic acid solution, as was confirmed by a water contact angle of 104° (115°) for both plasma treatments.) This gives another indication that the insulating quality of the gate dielectric layer does not depend on the Schottky-barrier height between ZnO and aluminum, since based on the experiments of chapter 5, a lower Schottky-barrier height is expected for the Ar-plasma-treated ZnO compared to the $O_2$-plasma-treated ZnO.

### Structural composition of the gate dielectric in the channel region

In order to investigate the structural composition of the aluminum top-gate FETs with SAM gate dielectric, the cross section of the gate stack is investigated by transmission electron microscopy (TEM). Similar to the experiments presented in chapter 5, a gallium ion beam is used to prepare a nominally 50 nm thick lamella of a ZnO nanowire covered with $FC_{18}$-SAM prior to the deposition of 80 nm thick aluminum. The surface of the ZnO nanowire was exposed to an Ar plasma prior to the immersion into the fluoroalkylphosphonic acid solution.

Figure 8.10b shows the bright-field TEM image of the SAM-covered ZnO nanowire (right image) and for comparison a TEM image of a ZnO nanowire also exposed to an Ar-plasma but without SAM (see also section 5.4). Apparently the SAM coverage of the ZnO nanowire strongly affects the interface between the aluminum top-gate and the ZnO nanowire. In the TEM image of the SAM-covered nanowire, a bright shell is recognized around the ZnO nanowire. A darker region is found at the bottom interface of the aluminum near the nanowire.

Figure 8.10c shows the bright-field image, superimposed with the elemental map of oxygen obtained from the structure. For clarity, the elemental map of oxygen has been colored red. As can be seen, the oxygen signal (red) is found in the dark regions at the bottom interface of the aluminum, which indicates the formation of an aluminum oxide layer. The measured thickness of the aluminum oxide is 3-4 nm (see figure 8.10d). This indicates that atmospheric oxygen can diffuse into the SAM/Al interface. Similar observations have recently been reported for the interface between graphene and aluminum deposited on top of the graphene [158].

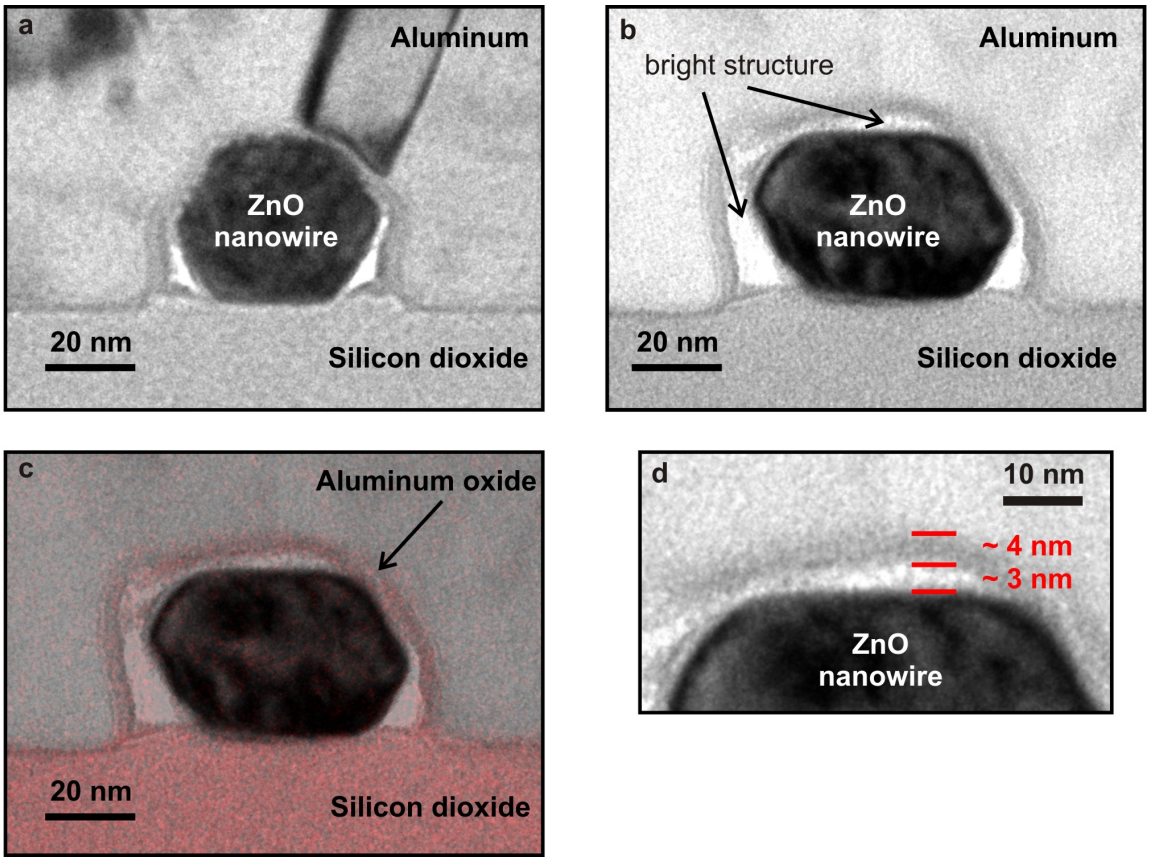


Figure 8.10: **TEM and elemental analysis of the channel cross-section of an aluminum top-gate ZnO-nanowire FET with SAM gate dielectric.**
(a) Cross section TEM image of a ZnO nanowire, exposed to an Ar plasma and covered with aluminum, and (b) cross section TEM image of a ZnO nanowire exposed to an Ar plasma, and covered with $FC_{18}$-SAM and aluminum. A bright structure is seen around the SAM-covered ZnO nanowire which may stem from the SAM itself and/or indicate the formation of hollow regions at the interface between aluminum and SAM-treated ZnO caused by a poor wetting of the aluminum on the SAM-covered ZnO nanowire. (c) TEM image of the SAM-covered ZnO nanowire superimposed with the elemental map of oxygen (colored red). An oxygen signal is found in the darker regions at the bottom interface of the aluminum near the nanowire, indicating the formation of aluminum oxide. (d) Zoom-in of the upper facet of the SAM-covered ZnO nanowire. The thickness of the bright structure at the upper facet is about 3.5 nm, and the thickness of the aluminum oxide is 4 nm.

Interestingly, the distance between the aluminum oxide layer and the surface of the ZnO nanowire appears to vary around the nanowire. The thickness of the bright structure (see figure 8.10b) separating the aluminum oxide from the ZnO nanowire varies between 2 and 6 nm. The interpretation of this bright layer on the basis of the TEM image is difficult. A straight-forward assumption is to conclude that the bright structure represents the self-assembled monolayer. However, the thickness of the SAM should be no more than 2.1 nm and is expected to be constant around the surface of the nanowire [159]. It is therefore believed that the variation in thickness of the bright structure indicates that

the aluminum is not in intimate contact with the SAM covered ZnO nanowire. With this assumption, the bright structures are interpreted as hollow regions at the interface between the aluminum and the SAM. The hollow regions are possibly caused by a poor surface wetting of the aluminum on the SAM covered surface. The surface wetting of aluminum depends not only on the specific surface, but also on the temperature [160], so poor wetting might be related to the specific conditions during the deposition of the aluminum.

In summary, the TEM images reveal that the gate dielectric in the channel region of the aluminum top-gate FETs consist of a 3-4 nm thick aluminum oxide layer in addition to the self-assembled monolayer and possibly an additional hollow region. The total thickness of the hybrid dielectric is 5-11 nm around the circumference of the nanowire and therefore much thicker than in the case of the gold top-gate FETs where the gate dielectric in the channel region consists only of the self-assembled monolayer. The observation of the rather thick dielectric explains the small gate current observed for the aluminum top-gate FETs with SAM gate dielectric.

### Aluminum top-gate FET with SAM gate dielectric as drive transistor for an organic light-emitting diode (OLED)

The small gate current and large breakdown voltage of the gate dielectric of the aluminum top-gate ZnO-nanowire FETs with SAM gate dielectric allow these FETs to be operated with much larger overdrive voltages compared to the gold top-gate FETs. As a result of the large overdrive voltages, larger drain currents and transconductances are achieved. Figure 8.11 shows the transfer and output characteristics of an aluminum top-gate ZnO-nanowire FET with a channel length of 1 µm. To maximize the drive current and transconductance, the source and drain contacts were designed in a comb-like pattern with a total of eight contact fingers (see inset in figure 8.11). The device has an on/off ratio of $10^8$, a subthreshold slope of 100 mV/decade, a peak transconductance of 50 µS and a maximum gate current below 1 pA at a gate-source voltage of 3 V. The maximum drain current obtained at $V_{DS} = 2\,V$ and $V_{GS} = 3\,V$ is as large as 85 µA.

The large drain current of the FET can be used to drive an organic light-emitting diode (OLED) to a brightness sufficiently high for practical display applications. The FET is connected to the OLED as depicted in the circuit diagram (figure 8.12). The OLED is a bottom-emitting fluorescent device manufactured by the company Novaled and has an active area of 0.067 $cm^2$. Figure 8.12 shows three photographs of the OLED driven by the nanowire FET at a drain potential of 5 V and gate potentials of 0 V, 4.5 V and 5.5 V. As expected, the brightness of the OLED and the current increase with increasing gate potential. The luminous efficiency of the OLED is 7 cd/A. For a gate potential of

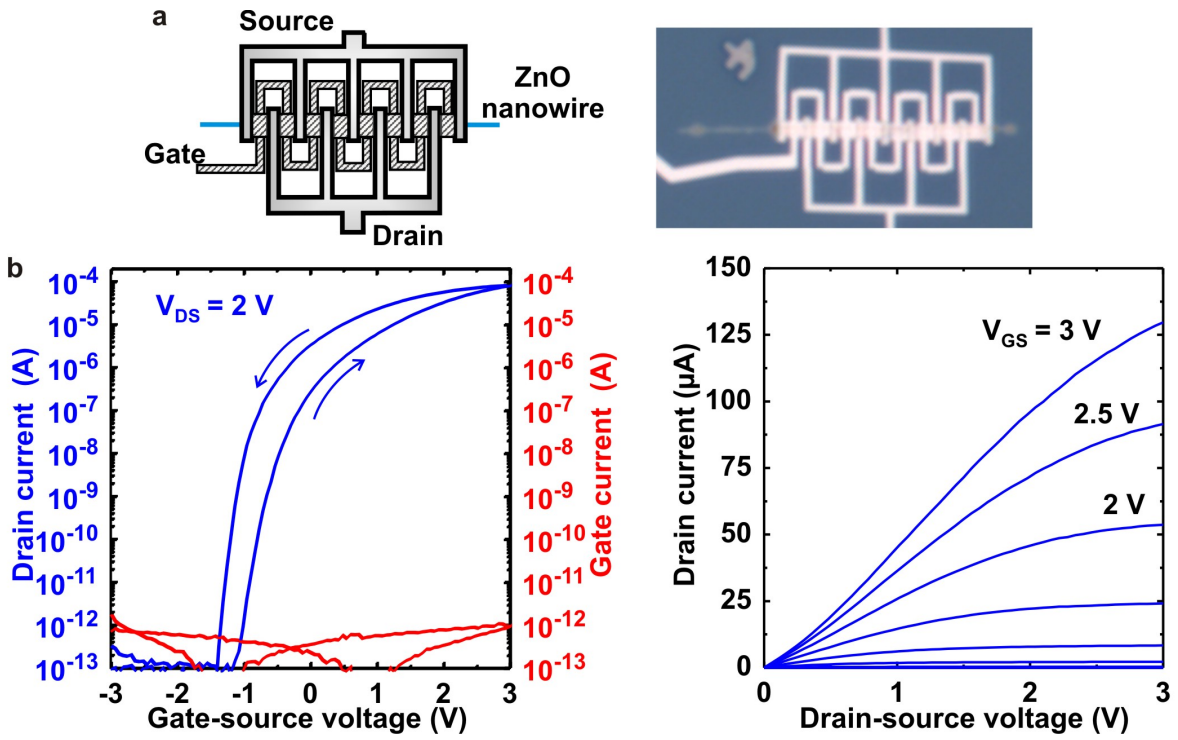


Figure 8.11: **Aluminum top-gate ZnO-nanowire FET with a comb-like pattern of the S/D contacts.**
(a) Schematic and photograph of an FET with a channel length of 1 µm, a nanowire diameter of 75 nm, and a total of eight contact fingers. (b) Transfer and output characteristics of the FET. Due to the comb-like pattern of the S/D contacts, the drain current and the transconductance are greatly increased compared to the FET from figure 8.9. The FET shows a peak transconductance of 50 µS, an on/off current ratio of $10^8$, and a subthreshold slope of 100 mV/decade.

5.5 V and a drain potential of 5 V, a current of 85 µA is driven through the OLED, which corresponds to a current density of 1.26 mA/cm$^2$. The OLED therefore produces a brightness of 88 cd/m$^2$.

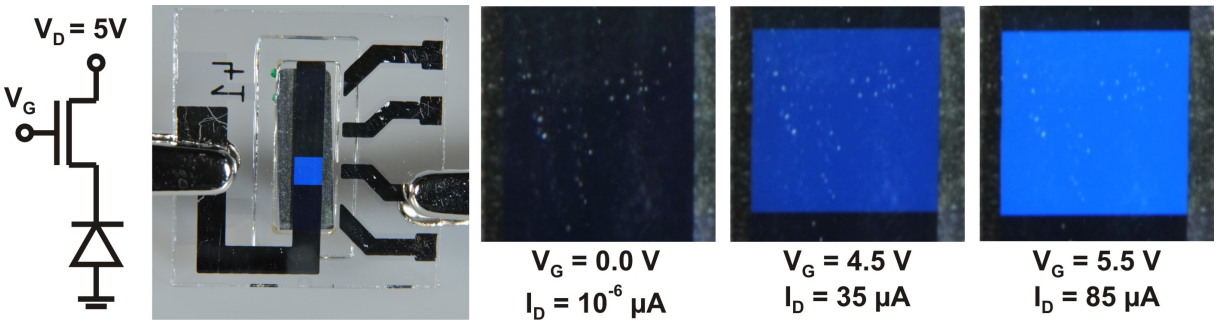


Figure 8.12: **Blue organic light-emitting diode driven by a ZnO-nanowire FET.**
Schematic circuit diagram and photograph of a large-area (0.067 cm$^2$) organic LED, connected to the FET of figure 8.11. The brightness of the OLED increases monotonically with increasing gate potential. At a potential of 5.5 V, the OLED brightness reaches 88 cd/m$^2$.

# 9 Integrated circuits realized on single ZnO nanowires and their dynamic characteristics

In chapter 8 it was demonstrated how gate dielectrics based on phosphonic acid self-assembled monolayers can be used to fabricate top-gate FETs on ZnO nanowires. Since most of the wet-chemically grown ZnO nanowires are several tens of micrometers long, it is even possible to manufacture several FETs on the same nanowire, which in turn allows the realization of integrated circuits on single ZnO nanowires. In this chapter, the experimental results on the realization of such integrated circuits on single ZnO nanowires and their dynamic performance will be presented.

## 9.1 Inverters on single ZnO nanowires

The simplest integrated circuit and the fundamental building block of binary logic is the inverter. An inverter is a four-terminal circuit with an input node, output node, supply node, and ground node (figure 9.1). It consists of a drive and a load element and can be realized either in a complementary or unipolar design.

State-of-the-art silicon-based microprocessors are based on complementary logic. A complementary inverter consists of an n-channel and a p-channel FET which alternately work as the drive and the load element (figure 9.1a). Compared to unipolar inverters, the complementary inverter has several advantages, like a low static power consumption and a large noise immunity. However, since the ZnO in general and especially the ZnO nanowires investigated in this thesis are natural n-type conductors, it is difficult to realize p-channel FETs with ZnO. Hence, only unipolar inverters are fabricated with the ZnO nanowires.

In contrast to a complementary inverter, in a uniploar inverter only n-channel or only p-channel FETs are required. The working principle of a unipolar inverter will be briefly discussed in the following. The simplest realization of a uniploar inverter is depicted in figure 9.1b (resistive load). The FET represents the drive element of the inverter which is connected in series to the load element which is an ohmic resistor. When the input node of the inverter is at high potential, the FET is in its on-state. Consequently, the resistance of the FET is much smaller than the resistance of the load resistor, and the supply voltage $V_{DD}$ drops entirely across the load resistor. Hence the output node is at ground potential ($V_{OUT} \sim 0\,V$). When the input node is at low potential, the FET is switched into its off-state. Therefore, the resistance of the FET is strongly increased and exceeds the resistance of the load resistor. Hence the supply voltage mainly drops across the drive FET and $V_{OUT} \sim V_{DD}$.

From the discussion of the working principle, it is obvious that the absolute value of the

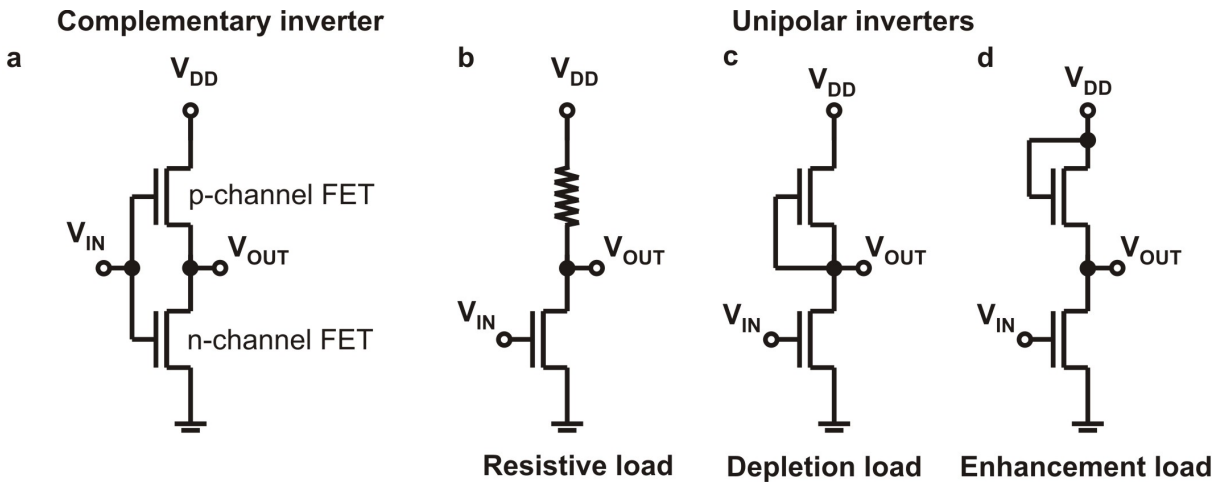


Figure 9.1: **Circuit schematics of various inverters.**
(a) Complementary inverter using n-channel and p-channel FETs. (b,c and d) Different types of unipolar inverters. The load resistor can be realized as an ohmic resistor (b), an FET operated at constant gate-source voltage (c), or an FET at constant gate-drain voltage (d).

resistance of the load resistor is crucial for the functionality of the unipolar inverter. The resistance needs to be much smaller than the off-state resistance of the drive FET and much larger than the on-state resistance of the drive FET. The integration of a resistor with an adequate resistance is a non-trivial task, and may need additional processing steps and materials [161, 162]. An alternative approach to the realization of the load element is depicted in figure 9.1c and d, where a second FET is utilized as the load element. Depending on the FET characteristics, the gate can be connected to the output node (depletion load) or to the supply node (enhancement load) of the inverter. Both these architectures have been utilized to fabricate inverters based on single ZnO nanowires in the framework of this thesis.

### Unipolar inverters on single ZnO nanowires

Figure 9.2a shows the circuit schematic and a scanning electron microscopy image of an enhancement-load inverter fabricated on a ZnO nanowire. The FETs are realized in the gold top-gate architecture with a self-assembled monolayer gate dielectric as described in section 8.2. The drive FET has a channel length of 1 µm and the load FET has a channel length of 4 µm. Figure 9.2b shows the static transfer characteristics of the inverter obtained for supply voltages of 0.5 V, 1 V and 1.5 V. As can be seen from the transfer characteristics, the output voltage ($V_{OUT}$) does not reach 0 V for positive input voltages. This is often observed for unipolar inverters and is ascribed to the finite resistance of the load FET. The resistance of the load FET is still within the same order of magnitude as the resistance of the drive FET for positive input voltages. Therefore, the supply voltage

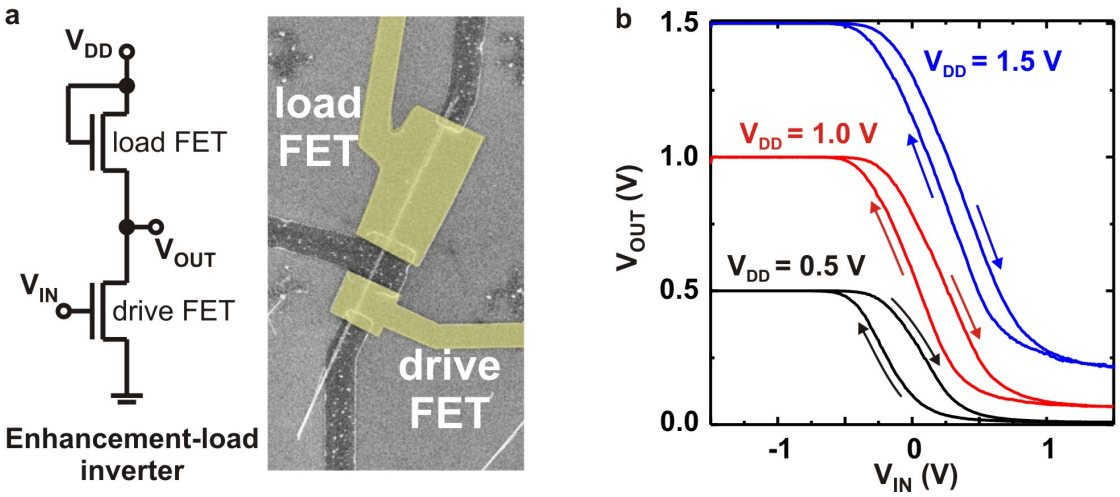


Figure 9.2: **Enhancement-load inverter realized on a single ZnO nanowire.** (a) Circuit schematic and scanning electron microscopy image of an enhancement-load inverter realized on a single ZnO nanowire. The drive FET has a channel length of 1 µm and the load FET a channel length of 4 µm. (b) Static transfer characteristics of the inverter for supply voltages of 0.5 V, 1 V and 1.5 V. The maximum small-signal gain of the inverter is 1.5.

partially drops across the load FET causing the non-zero output voltage. The maximum small-signal gain extracted from the derivative of the static transfer characteristics is 1.5. The maximum small-signal gain of an enhancement-load inverter is determined by the channel width W and channel length L of the two FETs and can be calculated according to [163]:

$$\text{gain} < \sqrt{\frac{W_{Drive} L_{Load}}{W_{Load} L_{Drive}}}. \tag{9.1}$$

Since both FETs are realized on the same ZnO nanowire, the width of the FETs is the same and can be omitted in equation 9.1. Thus, the maximum small-signal gain is given by

$$\text{gain} < \sqrt{\frac{L_{Load}}{L_{Drive}}}. \tag{9.2}$$

The measured small-signal gain of 1.5 is therefore close to the expected value of 2, calculated for the geometry given for the device of figure 9.2.

Since the threshold voltage $V_{th}$ of the gold top-gate FETs is sligthly negative (see section 8.2.1), the resulting inverters need a negative input voltage in order to obtain a clean positive output signal (see figure 9.2). This means that the input and output levels of the inverters do not match and therefore these inverters cannot be cascaded.

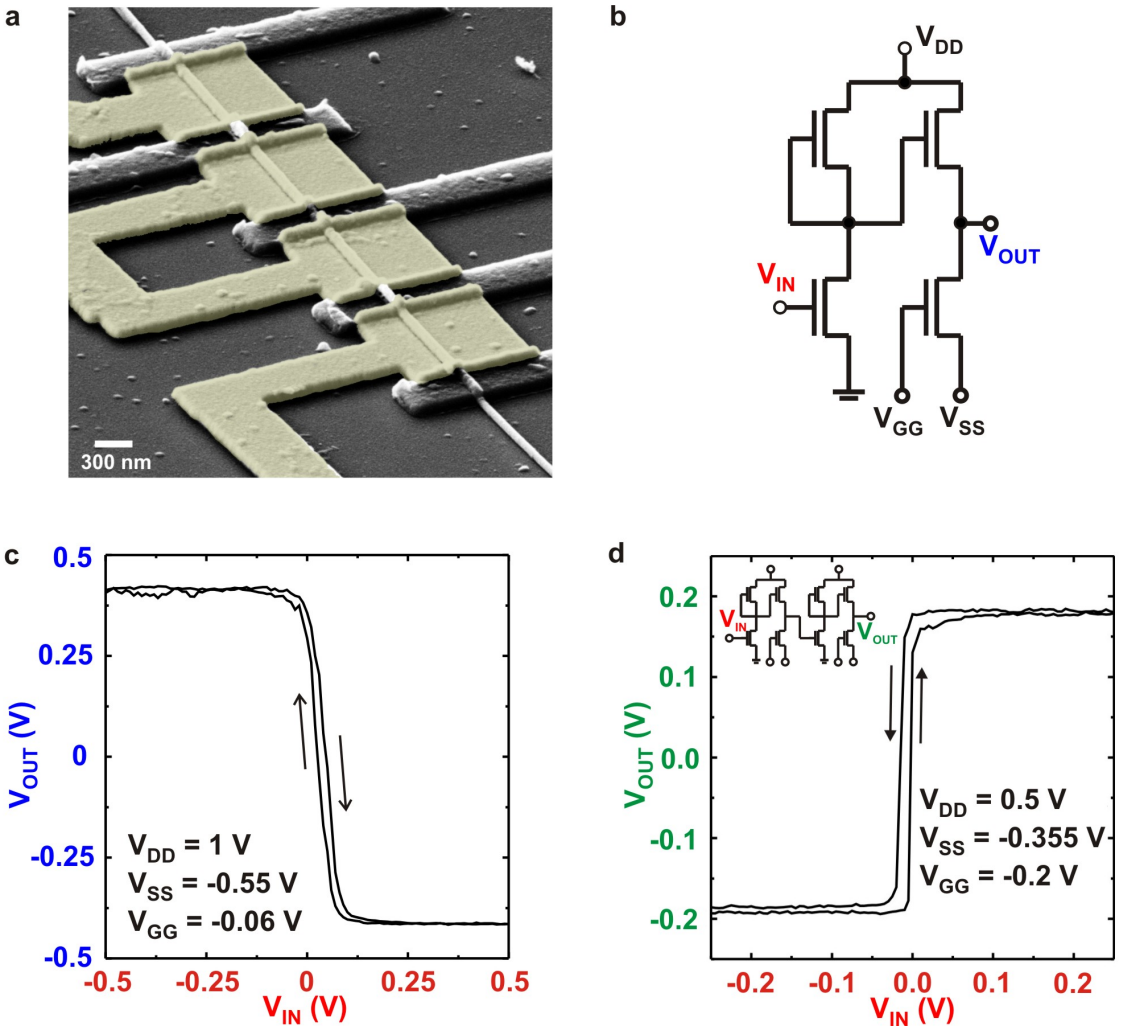


Figure 9.3: **Inverters with integrated level-shift stage on a single ZnO nanowire.** (a) Tilted SEM image of an inverter with integrated level-shift stage. Four FETs with a channel length of 1 µm are fabricated on the same ZnO nanowire. (b) Circuit schematic of an inverter with integrated level-shift stage. Additional supply voltages $V_{SS}$ and $V_{GG}$ are introduced to adjust the output levels of the inverter. (c) Static transfer characteristics of the inverter. Due to the level-shift stage, the inverter shows matching input and output levels. The small-signal gain reaches 12. (d) Transfer characteristics of two cascaded inverters with level-shift stage.

### Inverters with integrated level-shift stage

In order to allow cascading and to increase the small-signal gain, inverters with an integrated level-shift stage have been manufactured. Figure 9.3a shows a tilted SEM image of an inverter with an integrated level-shift stage on a 12 µm long ZnO nanowire. The circuit consists of four FETs, each having a channel length of 1.5 µm. A circuit schematic of the inverter with integrated level-shift stage is depicted in figure 9.3b. With the additional supply voltages $V_{GG}$ and $V_{SS}$ the output levels of the inverter are shifted towards more negative values to make them compatible with the input levels [164]. Figure 9.3c shows the static transfer characteristics of the inverter with level-shift stage. For supply voltages

of $V_{DD} = 1\,V$, $V_{GG} = -0.06\,V$, and $V_{SS} = -0.55\,V$ the inverter shows symmetric switching around 0 V for input voltages between 0.4 V to -0.4 V. The maximum small-signal gain is 12. Due to the level-shift stage, the input levels match the output levels of the inverters, which makes it possible to cascade these inverters. Figure 9.3d shows the static transfer characteristics when two inverters with level-shift stage are cascaded. Clearly, the input signal of the first inverter is recovered at the output voltage node of the second inverter. For the inverter cascade a maximum small-signal gain of 35 is obtained.

## 9.2 Dynamic characteristics of integrated circuits on single ZnO nanowires

Fast switching is an essential requirement of the FETs and circuits with regard to their implementation in practical applications, such as active-matrix displays. An estimation of the maximum switching frequency of an FET is given by the so-called cutoff frequency $f_T$.

When an alternating voltage is applied to the gate electrode of an FET, the gate capacitor is charged and discharged during every period of the alternating voltage. The charging and discharging of the gate capacitor requires a charge flow (displacement current) at the gate of the FET. With increasing frequency, more and more charge needs to be transported to the FET gate and consequently the gate current increases with frequency [165]. In contrast, the drain current is independent of the frequency. The cutoff frequency is defined as the frequency at which the gate current becomes as large as the drain current and the FET can no longer be operated in a useful manner:

$$f_T = f(I_G \equiv I_D) = \frac{g_m}{2\pi C_G} = \frac{g_m}{2\pi(C_{chan} + C_{con} + C_{par})}, \tag{9.3}$$

with the transconductance $g_m = \frac{dI_D}{dV_{GS}}$ and the gate capacitance $C_G$. The gate capacitance is the sum of the capacitance from the overlap between the gate electrode and the semiconducting channel $C_{chan}$, the capacitance from the overlap between the gate electrode and the source and drain contacts $C_{con}$, and additional parasitic capacitances $C_{par}$.

$C_{chan}$ depends on the overlap area between the gate electrode and the semiconducting ZnO-nanowire channel. An upper limit for the channel capacitance of the top-gate FETs with SAM gate dielectric can be calculated under the assumption that the device is operating in the accumulation regime. Under this assumption, only the SAM gate dielectric layer contributes to the capacitance and

$$C_{Chan} = \frac{\varepsilon_0 \varepsilon_{SAM} L \pi r_{NW}}{d_{SAM}} \sim 1\,fF, \tag{9.4}$$

with the SAM thickness $d_{SAM} = 2.1$ nm and the SAM permittivity $\varepsilon_{SAM} = 2.5$ [166]. The capacitance between the gate and the S/D contacts $C_{con}$ can be estimated from the capacitance per unit area of the $AlO_x$/SAM gate dielectric ($C_{AlO_x/SAM} = 700$ nF/cm$^2$ [104]) and the overlap area defined by electron-beam lithography. If further parasitic capacitances are neglected, the total gate capacitance of the gold top-gate FET is calculated to $C_G = 2$ fF. For a transconductance of 1 µS, equation 9.3 yields $f_{cut-off} \sim 80$ MHz as an upper limit for the switching frequency of the gold top-gate FETs with SAM gate dielectric.

The measurement of the cutoff frequency of an FET can be realized by the dynamic characterization of the output signal of an inverter. For this purpose, the enhancement-load inverters fabricated in the previous section are used. However, the small total capacitance of the FET makes this measurement a non-trivial task, since it is extremely important to avoid contributions of parasitic capacitances. When the inverters are fabricated on a conducting substrate like Si/$SiO_2$, the overlap area between the output probe pad and the conducting Si back-gate introduces a large parasitic capacitance ($C_{par} \sim 10$ pF) that is much larger than the device capacitance. Indeed, cutoff frequencies of only 10 kHz are measured for inverters realized on conducting Si substrates.

### FETs and inverters on insulating substrates

An accurate measurement of the cutoff frequency of the gold top-gate FETs requires the use of an insulating substrate. As mentioned in chapter 8.1, the top-gate fabrication process does not require high temperatures during the fabrication. Therefore it is possible to implement gold top-gate FETs on unconventional and insulating substrates, such as glass and plastics.

Figure 9.4a and b shows the transfer characteristics of two gold top-gate FETs, one realized on glass, the other on polyethylene naphthalate (PEN). Both FETs have a channel length of 1 µm and are utilized as the drive FET of an enhancement-load inverter ($L_{Load} = 4$ µm). The FETs have an on/off current ratio of more than $10^6$ and a subthreshold slope below 110 mV/decade. Owing to the more negative threshold voltage, the maximum transconductance of the transistor on the glass substrate ($g_m = 1$ µS at $V_{GS} = 1$ V) is slightly larger than the transconductance of the FET on PEN ($g_m = 0.6$ µS at $V_{GS} = 1$ V).

While the parasitic capacitances associated with the insulating substrates are negligible, the capacitances introduced by the measurement setup are still large compared to the device capacitance. In order to perform the dynamic characterization of the respective inverters, a high-impedance active probe needle Picoprobe® purchased from the company GGB Industries is utilized. The active probe needle is specially designed to record AC signals from low-capacitance circuits. However, even though the input capacitance of the

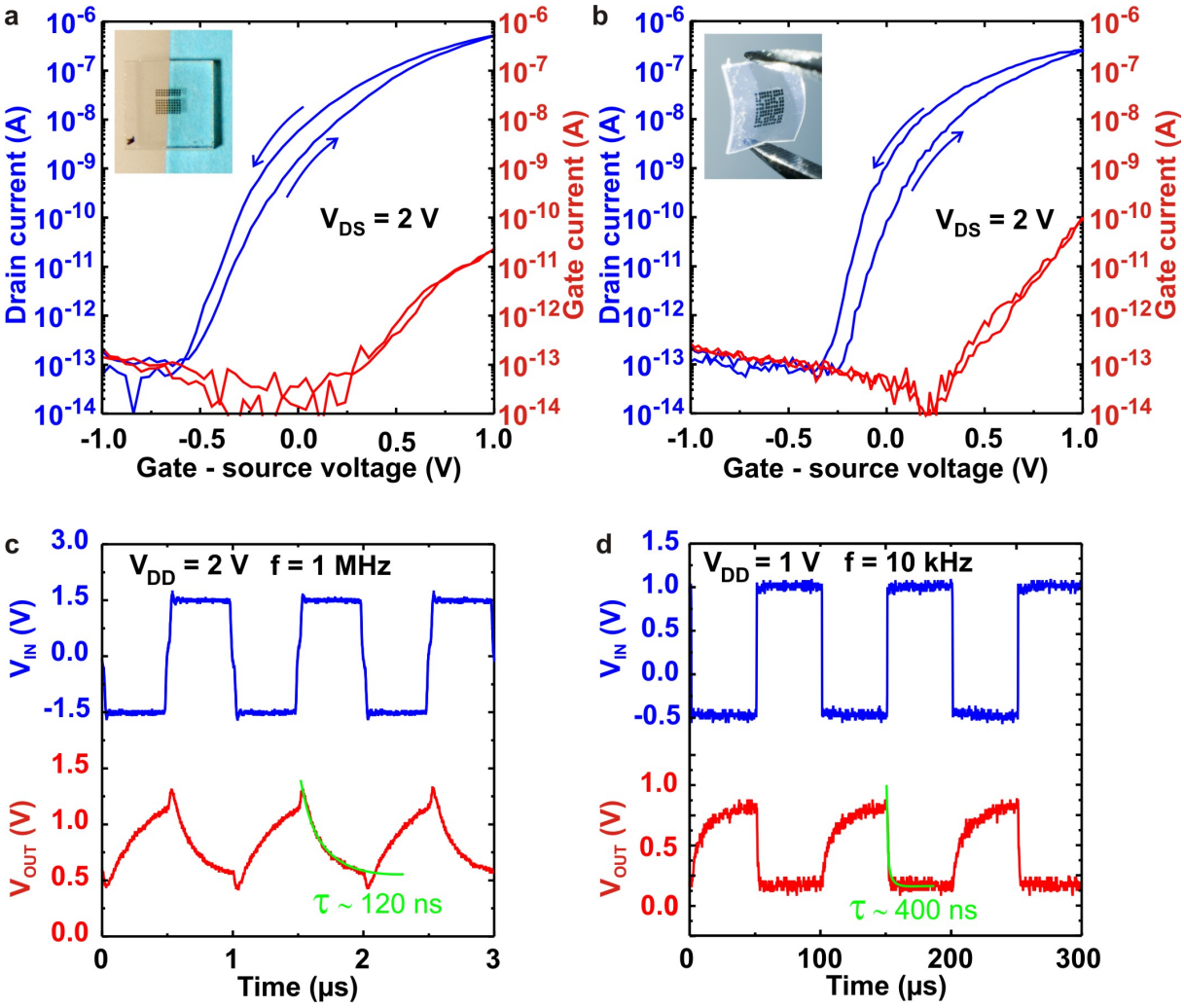


Figure 9.4: **Dynamic performance of inverters on insulating glass and plastic substrates**

(a) Transfer characteristics of a gold top-gate FET realized on a glass substrate. (b) Transfer characteristics of a gold top-gate FET realized on a plastic substrate. The FETs have an on/off current ratio of more than $10^6$ and a subthreshold slope steeper than 110 mV/decade. The transconductance at $V_{GS} = 1\,V$ is 1 µS and 0.6 µS, respectively. Both FETs have a channel length of 1 µm and are utilized as the drive FET in enhancement-load inverters. (c) and (d): Input and output voltages of the enhancement-load inverters realized on insulating substrates. For the inverter on a glass substrate (c) the output voltage follows the input voltage up to a frequency of 1 MHz. The inverter on a plastic substrate (d) is limited to a frequency of 10 kHz by the slow RC time constant of the load FET. The time constants of the drive FETs are estimated to 120 ns on glass and 400 ns on plastic, corresponding to switching frequencies between 2 and 8 MHz.

probe needle is as low as 20 fF, it is still approximately one order of magnitude larger than the capacitance of the ZnO-nanowire FETs.

The active probe needle is connected to the output node of the inverter and conducts the signal to an oscilloscope for signal recording. Figure 9.4c and d show the respective

AC input and output signals of the inverters fabricated on glass and on a flexible PEN substrate. For a supply voltage of $V_{DD} = 2\,V$, the output signal of the inverter on glass follows the input signal up to a frequency of 1 MHz (figure 9.4c). To the best of our knowledge, this is the highest frequency reported for an inverter based on a single metal-oxide nanowire so far.

For a unipolar inverter the output node is charged to the high potential via the load FET and discharged to the low level via the drive FET. Therefore, the charging time of the output node depends the RC time constant of the load FET, which will in general be larger than the time constant of the drive FET and thus limit the dynamic performance of the inverter. This is apparent for the inverter fabricated on the PEN substrate. For a frequency of 10 kHz, the load FET starts to limit the dynamic performance of the inverter, while the discharging via the drive FET still occurs nearly instantaneously at this frequency. By assuming a simple exponential decay for the discharging of the output node,

$$V(t) \sim \exp\left(-\frac{t}{\tau}\right) \tag{9.5}$$

the time constant $\tau$ provides an estimate of the dynamic performance of the drive FET. A fit of the output signal (Figure 9.4c and d, green curves) yields $\tau_{FET}^{glass} = 120\,ns$ for the inverter on glass and $\tau_{FET}^{PEN} = 400\,ns$ for the inverter on PEN. Therefore, the performance of the drive FETs is within an order of magnitude on both types of insulating substrates.

The estimated time constants correspond to a maximum switching frequency of 2-8 MHz and are therefore around an order of magnitude smaller than the estimated cutoff frequency (80 MHz). Since the capacitance of the active probe needle (20 fF) is around an order of magnitude larger than the calculated device capacitance (2 fF), the measured cutoff frequencies are in good agreement with the calculated values.

# 10 Summary and outlook

High-performance, low-voltage field-effect transistors (FETs) based on hydrothermally grown ZnO nanowires have been fabricated and investigated in this thesis. Starting from the synthesis of the nanowires, their electrical properties have been analyzed and progressively improved with regard to their application in FETs. To be potentially useful for large-area electronic applications on flexible substrates, FETs based on semiconducting nanowires require local gating and a low-temperature ($T < 200°C$) fabrication process. For this purpose, the potential of self-assembled monolayers (SAM) on the surface of ZnO nanowires utilized as an ultra-thin (2 nm) gate dielectric in a locally addressable top-gate FET geometry has been studied.

The ZnO nanowires investigated in this thesis have been grown by a hydrothermal synthesis on a zinc foil as previously reported by Lu et al. [52]. Large amounts of single-crystalline, hexagonal ZnO nanowires with aspect ratios as large as 500 have been synthesized. To investigate the electrical characteristics of the wet-chemically grown ZnO nanowires in a global back-gate FET geometry, nanowires have been dispersed on $Si/SiO_2$ substrates and aluminum source and drain contacts have been patterned on the nanowires. The as-grown ZnO nanowires have a large n-type conductivity that stems from dopants that have been incorporated unintentionally during the synthesis. The doping concentration has been estimated to be larger than $10^{19}$ $cm^{-3}$ which indicates that the as-grown ZnO nanowires are degenerately doped. This has been confirmed by temperature dependent measurements, which show that the field-effect mobility as well as the charge-carrier concentration is only weakly dependent on the temperature. The large charge-carrier concentration in the wet-chemically as-grown ZnO nanowires makes it extremely difficult to modulate the conductivity by application of an external field and makes the fabrication of FETs impractical.

In order to reduce the charge-carrier concentration of the wet-chemically grown ZnO nanowires, a post-growth annealing has been performed. While annealing at 200 °C and 400 °C does not affect the conductivity of the ZnO nanowires, annealing at 600°C in ambient air results in a dramatic reduction of the charge-carrier concentration. It has been demonstrated that an anneal of only two minutes is sufficient to achieve the reduction of the charge-carrier concentration. Due to the large effect of the annealing temperature and the important role of oxygen in the reduction of the charge-carrier concentration it is believed that hydrogen incorporated onto an oxygen vacancy provides a possible explanation for the large dopant concentration in the as-grown ZnO nanowires [66, 67]. However, other doping mechanisms can also account for the doping, since the source materials for the synthesis are only about 98% pure and can introduce significant amounts of contaminations in the ZnO nanowires that can cause n-type doping [60]. To elucidate

the mechanisms responsible for the doping of the wet-chemically grown ZnO nanowires it would be interesting for future experiments to combine the annealing experiments with spectroscopic measurements, such as UV-photoluminesence or electroluminesence, since these techniques provide a powerful tool to identify dopants in ZnO.

After annealing at 600 °C in ambient air, the wet-chemically grown ZnO nanowires are suitable for the fabrication of FETs with excellent electrical performance. The reduced charge-carrier concentration makes it possible to modulate the drain current of FETs based on annealed ZnO nanowires over seven orders of magnitude. The field-effect mobilities extracted from FETs fabricated on silicon substrates with a 200 nm thick, thermally grown silicon dioxide gate dielectric are around 20-50 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$ and therefore comparable to mobilities reported for ZnO-nanowire FETs with nanowires grown by other methods [41, 85, 89, 90].

Although the charge-carrier concentration in the wet-chemically grown ZnO nanowires is greatly reduced after the annealing, the annealed ZnO nanowires are conductive without application of an external electric field and substantially negative gate-source voltages are often required to switch the nanowires into a non-conducting state. It has been concluded that the conductivity of the annealed ZnO nanowires originates from a residual bulk doping present in the nanowires even after the annealing at 600 °C and that the ZnO-nanowire FETs are operated in the depletion regime for negative gate-source voltages. Furthermore, it has been shown that the field-effect mobility in the depletion regime is a function of the temperature and of the gate bias. To better understand the temperature and gate-bias dependence of the field-effect mobility, it would be interesting in future experiments to investigate the transfer characteristics of ZnO-nanowires FETs over a broader temperature range. The observed gate-bias dependence of the field-effect mobility resembles the behavior expected from the so-called multiple trapping and release model (MTR) [95, 96]. However, this model was developed for thin-film transistors that operate in the accumulation regime. In order to examine the applicability of the MTR model to an FET operating in the depletion regime, an accurate modeling will be required.

The effects of argon- and oxygen-plasma treatments on the electrical characteristics of FETs based on annealed ZnO nanowires have been investigated. In agreement with other reports [81, 80, 76] it has been concluded that an argon-plasma treatment increases the charge-carrier concentration in the ZnO nanowires, while an oxygen-plasma treatment decreases the charge-carrier concentration in the ZnO nanowires. It has been demonstrated that the plasma treatment greatly affects the electrical performance of the contact between ZnO and aluminum when the plasma treatment is performed exclusively in the source and drain contact regions prior to the aluminum evaporation. While the doping effect of an argon-plasma treatment has been shown to reduce the contact resistance and improve the FET characteristics, an oxygen-plasma treatment in the contact regions results in the formation of an insulating aluminum oxide layer at the interface between ZnO

and aluminum and therefore causes a strong increase of the contact resistance. These findings are important with regard to the fabrication of high-performance FETs based on ZnO nanowires and lead to a method to fabricate reliable, low-resistance contacts to ZnO. The possibility to tune the conductivity of the ZnO nanowires by a plasma treatment may provide an interesting tool to improve the performance of top-gate ZnO-nanowire FETs with a gate electrode that only partially overlaps the semiconductor channel. The argon-plasma treatment could be used to increase the conductivity of the channel areas not controlled by the gate electrode and therefore increase the transconductance.However, in order to be useful for these kind of experiments, it will be necessary to study whether the plasma-induced doping is stable under ambient conditions or if a passivation is required to maintain the doping.

To study the effect of the ambient atmosphere on the electrical characteristics, ZnO-nanowire FETs have been characterized in ambient air, in high vacuum and in water vapor. The electrical characteristics of a ZnO-nanowire FET have been found to be strongly affected by the distinct atmospheric conditions. In ambient air, the adsorption of electron-capturing species (such as oxygen [110, 112, 113, 114]) on the surface of the ZnO nanowires reduces the electrical conductivity. In contrast, the exposure to water vapor causes an increase of the conductivity of the ZnO nanowire FETs, possibly attributed to water molecules that replace previously adsorbed electron-capturing species on the surface of the ZnO nanowires [118]. The competitive effects between water and electron-capturing species on the surface of the ZnO nanowires make it difficult to obtain reproducible and reliable FET characteristics. Therefore, the potential of a self-assembled monolayer (SAM) based on (fluoro)alkylphosphonic-acid molecules has been investigated for the passivation of ZnO-nanowire FETs fabricated on a global aluminum oxide ($AlO_x$) gate dielectric layer. By means of static water contact angle measurements, it has been shown that (fluoro)alkylphosphonic acids form densely packed, hydrophobic monolayers on ZnO and $AlO_x$ [102], while on silicon dioxide no formation of a hydrophobic monolayer has been observed. The coverage of the ZnO-nanowire-FET channel as well as the aluminum oxide gate dielectric with the hydrophobic SAM has been shown to greatly stabilize the electrical characteristics of the FET against the effects of the ambient conditions. However, attempts to improve the stability of ZnO-nanowire FETs fabricated on a global silicon dioxide gate dielectric with the help of a SAM based on (fluoro)alkylphosphonic acids have not been successful so far. It has therefore been concluded that both, a passivation of the gate dielectric layer and a passivation of the ZnO nanowire are necessary to achieve a stabilization of the FET's electrical characteristics. With regard to these experiments, it is necessary to put further effort into the analysis of the importance of passivating the semiconducting channel and/or the surface of the gate dielectric. This could be achieved e.g. by selectively passivating only the gate dielectric by a proper choice of the anchor group of the molecules used for the formation of the SAM.

A novel top-gate fabrication process based on the use of a phosphonic acid SAM as an ultrathin gate dielectric in a top-gate ZnO-nanowire FET geometry has been developed in this thesis. Because the SAM gate dielectric covers not only the ZnO nanowire, but also the aluminum S/D contacts, the top-gate electrode is allowed to overlap the S/D contacts and control the charge-carrier concentration in the entire FET channel. The insulating properties of the SAM on the surface of the ZnO nanowires have been investigated for ZnO-nanowire FETs with gold top-gate electrodes and aluminum top-gate electrodes.

For the gold top-gate FETs the SAM gate dielectric reduces the gate current by more than three orders of magnitude compared to gold top-gate ZnO-nanowire FETs that have been fabricated without a SAM gate dielectric layer (MESFETs). The observed reduction of the gate current is well described in the framework of the MIS Schottky-diode model which assumes that the 2 nm thick SAM acts as a tunnel barrier connected in series to the built-in Schottky barrier between ZnO and gold. Gold top-gate ZnO nanowire FETs with a SAM gate dielectric show excellent electrical characteristics with a transconductance of 1 µS, on/off current ratios of $10^7$, and steep subthreshold slope of 90 mV/decade. Due to the thin gate dielectric, the gold top-gate FETs operate at low voltages of 1 V. The gate current for the gold top-gate FETs is below 1 pA for gate-source voltages between -1 V and 0.5 V, but increases approximately exponentially for more positive gate-source voltages. This makes it impossible to apply voltages larger than about 1-2 V in order to produce drain currents larger than a few microamps and a transconductance of more than a few microsiemens.

When aluminum is used for the top-gate electrode on the SAM-covered ZnO nanowires, it has been demonstrated that the gate dielectric consists of the SAM and an additional layer of aluminum oxide that spontaneously forms at the interface between the aluminum top-gate electrode and the SAM-covered ZnO nanowire. The formation of the aluminum oxide layer indicates that atmospheric oxygen diffuses to the SAM/Al interface. It is believed that due to a poor surface-wetting of the aluminum on the SAM-covered ZnO nanowire, hollow regions have been formed at the SAM/Al interface which may lead to the diffusion of oxygen to the SAM/Al interface and thereby promote the formation of the aluminum oxide. The hybrid gate dielectric of the aluminum top-gate FETs was found to have a total thickness of 5-11 nm. As a result, the aluminum top-gate FETs operate with gate currents below 1 pA for voltages up to 3 V. The low gate current makes it possible to apply larger overdrive voltages compared to the gold top-gate FETs and therefore the aluminum top-gate FETs show larger drain current and larger transconductance. An aluminum top-gate FET with a peak transconductance of 50 µS, an on/off current ratio of $10^8$, and a subthreshold slope of 100 mV/decade has been demonstrated.

The formation of a hybrid gate dielectric consisting of aluminum oxide and the SAM is an interesting observation and should be examined in more detail in further experiments.

If the assumption of hollow regions caused by a poor wetting of aluminum on the SAM-covered ZnO nanowire is correct, it will be of particular interest to investigate the gate stack of aluminum top-gate FETs when the ZnO nanowire is covered with a SAM of larger surface energy. The wetting of the SAM-covered nanowire by the aluminum and hence the formation of the hollow regions and/or the aluminum oxide layer may strongly depend on the surface energy. Therefore, the thickness as well as the stack of the gate dielectric might be altered by the SAM that covers the ZnO nanowire. This may provide a larger capacitance and a further improvement of the FET characteristics.

The developed top-gate fabrication process makes it possible to fabricate several FETs on a single ZnO nanowire and to connect them into circuits. Enhancement-load inverters and inverters with an integrated level-shift stage consisting of up to four FETs on a single ZnO nanowire have been demonstrated. Since the top-gate fabrication process does not require high temperatures it is possible to fabricate FETs and circuits on substrates that do not tolerate elevated temperatures, such as flexible plastics. Enhancement-load inverters have been successfully fabricated on glass and plastic substrates and their dynamic performance has been investigated. For the inverters on a glass substrate a maximum switching frequency of 1 MHz has been achieved.

So far only integrated circuits based on gold-top gate FETs have been fabricated and dynamically characterized. Future experiments should focus on the fabrication and dynamic characterization of integrated circuits with aluminum top-gate FETs. The larger transconductance of the aluminum top-gate FETs compared to the gold top-gate FETs hold promise for the realization of higher switching frequencies. Further, the increased electrical stability of the gate dielectric for the aluminum top-gate FETs may allow the realization of more complex integrated circuits, such as ring oscillators.

# Appendix

## Multiple trapping and release model for a depletion-mode FET

Although the results from the temperature-dependent measurements coincide well with the predictions of the MTR model, the results need to be treated with caution. It is important to recognize that the MTR model was developed in the framework of TFT theory and assumes that the gate-induced charge carriers in the semiconductor are located in a thin charge sheet at the semiconductor/insulator interface (surface conduction; see section 6.2). Hence, the potential drop in the semiconductor V(y) is also restricted to a narrow region next to the semiconductor/insulator interface (see figure 10.1a). This assumption is not valid in the case of bulk conduction where the potential drops over the whole semiconductor body (see figure 10.1b). The different potential distributions have important consequences on the applicability of the MTR model and the interpretation of the measurement data.

According to Fermi-Dirac statistics (equation 6.4), the charge-carrier concentrations $n_t$ and $n_f$ in the semiconductor depend exponentially on the potential V(y):

$$n_{f/t}(\mathrm{x}) = \int_{-\infty}^{\infty} f(\mathrm{E(V(y))}, \mathrm{T}) \cdot \mathrm{N_{f/t}(E)}\,\mathrm{dE} = \int_{-\infty}^{\infty} \left(1 + \exp\left(\frac{\mathrm{E_f + V(y) + E}}{\mathrm{k_B \cdot T}}\right)\right)^{-1} \mathrm{N_{f/t}(E)}\,\mathrm{dE} \tag{10.1}$$

Within the framework of the original MTR model, the potential distribution is narrow so that V(y) can be substituted by the potential $\mathrm{V_S}$ at the semiconductor/insulator interface, which substantially simplifies the calculations of $n_f$ and $n_t$ [94]. With increasingly positive $\mathrm{V_{GS}}$, the surface potential $\mathrm{V_S}$ increases and the energetic distance between the Fermi level and the conduction band edge is decreases continuously (see figure 10.1a). The ratio between the density of free charges $n_f$ and the density of trapped charges $n_t$ at the surface therefore changes continuously, leading to a continuous variation of the effective field-effect mobility (see equation 6.3).

The situation in the case of bulk conduction is depicted in figure 10.1b. Under the assumption that the nanowire is doped and the semiconductor bulk is conducting, a negative $\mathrm{V_{GS}} = \mathrm{V_{th}}$ is required in order to deplete the nanowire from free charge carriers, leaving behind the ionized dopants. According to the Schottky-parabola approximation (see section 2.2.7) the charge of the ionized dopants causes a parabolic potential distribution across the channel cross section in the off-state of the nanowire FET (figure 10.1b, upper schematic). When $\mathrm{V_{GS}}$ is increased, the potential drop is reduced, and the energetic distance between the Fermi level and the conduction band is decreased. As a consequence,

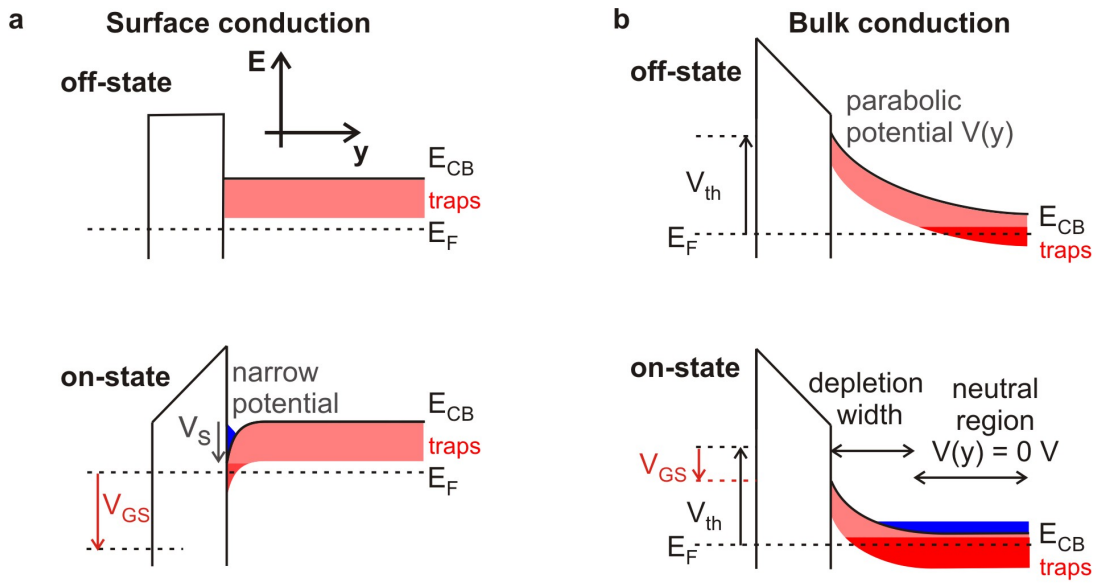


Figure 10.1: **Schematic band diagram of the FET channel cross-section according to the MTR model.**
(a) Schematic band diagram of an FET operating in the accumulation regime (surface conduction). The potential in the semiconductor drops across a narrow region close to the semiconductor/insulator interface. With increasing $V_{GS}$, the bands in the semiconductor are bent downwards and the ratio between the number of free charges $n_f$ and the number of trapped charges $n_t$ at the surface changes continuously. Therefore, the field-effect mobility is expected to be a function of $V_{GS}$. (b) Schematic band diagram of an FET in the depletion regime (bulk conduction). A negative potential $V_{th}$ is required to deplete the doped semiconductor of free charge carriers. This causes a parabolic potential distribution V(y) across the channel cross-section in the off-state. With increasing $V_{GS}$ the potential distribution across the channel cross-section can be divided into a neutral region (V(y) = 0 V) and a parabolic region.

electrons populate the trap states and the extended states in the nanowire and compensate the charge of the ionized dopants.

However, in contrast to the previously discussed surface conduction model, the Fermi level moves towards the conduction band only until the induced electronic charge equalizes the charge of the ionized dopants ($V(y) = 0\,V$, neutral region). A further increase of $V_{GS}$ decreases the depletion width and extends the neutral region closer towards the semiconductor/insulator interface (figure 10.1b). Since the Fermi level does not move towards the conduction band in the neutral region, the effective field-effect mobility is expected to be constant in this region (since $n_t$ and $n_f$ are constant). Therefore, it is questionable whether the mobility will show a gate-bias dependence in this situation.

In order to investigate whether the effective field-effect mobility is gate-bias dependent or not in the case of bulk conduction, the transfer characteristics of a ZnO nanowire operating in the depletion regime are simulated using an exponential distribution of trap

states below the conduction band (section 2.2.7). Within the simulation it is assumed for simplicity that the electronic charge introduced by the dopants is constant in the investigated temperature range from 273 K to 80 K. Therefore, the potential distribution V(y) across the nanowire channel is independent of the temperature. The influence of the temperature is restricted to the distribution of the electronic charges between the extended states and the trap states governed by Fermi-Dirac statistics (see equation 10.1). The distribution of $n_f$(y) and $n_t$(y) along the nanowire channel cross-section is then calculated for different $V_{GS}$ and different T according to equation 10.1. From this the effective mobility $\mu_{eff}$(y) is calculated using equation 6.3. Due to the spatial variation of the distribution of $n_f$(y) and $n_t$(y), the effective field-effect mobility is also dependent on y. The average value of $\mu_{eff}$ for given $V_{GS}$ and T can therefore be computed by:

$$\overline{\mu}_{eff}(\mathrm{V_{GS}, T}) = \frac{\int_0^{\mathrm{d_{NW}}} \mu_{eff}(\mathrm{y, V_{GS}, T}) \cdot n_f(\mathrm{y, V_{GS}, T})\mathrm{dy}}{\int_0^{\mathrm{d_{NW}}} n_f(\mathrm{y, V_{GS}, T})\mathrm{dy}} \tag{10.2}$$

The doping concentration of the simulated ZnO nanowire is set to $N_D = 2.5{\cdot}10^{18}$ cm$^{-3}$ in order to compare the results to the ZnO nanowire investigated in in section 6.3.1.

In figure 10.2, the results of the simulation are shown. As can be seen, the simulation predicts a gate-bias dependent mobility also in the case of bulk conduction (figure 10.2a). The mobility strongly increases above the switch-on of the FET between $-35\,\mathrm{V} < V_{GS} < -25\,\mathrm{V}$, but is nearly constant for larger $V_{GS}$. An explanation for the observed gate-bias dependence becomes obvious from figure 10.2b. In a simplified picture, the mobility across the ZnO nanowire channel can be divided into two regimes, $\mu_1$ and $\mu_2$. In the neutral region of the nanowire (V(y) = 0) the ratio of $n_f$ and $n_t$ is constant and therefore the mobility is also constant ($\mu = \mu_1$). In the depletion region of the nanowire, the parabolic potential V(y) produces a monotonic reduction of the $n_f/n_t$ ratio towards the semiconductor/insulator interface. Since the density of trap states extends into the band gap, the number of electrons captured in traps is reduced less strongly towards the semiconductor/insulator interfaces than the number of electrons in the extended states (figure 10.2b, blue and red curve). Therefore, the mobility in this regime $\mu_2$ will be smaller than $\mu_1$. With increasing $V_{GS}$, the regime of $\mu_1$ extends more and more towards the gate dielectric. Therefore the influence of regime $\mu_1$ more and more dominates for larger $V_{GS}$ and the total mobility increases. However, since the number of free charge carriers in regime $\mu_1$ is usually much bigger than the number of free charge carriers in regime $\mu_2$, the overall variation in the simulation is only about 2% for $V_{GS} > -25\,\mathrm{V}$ (figure 10.2c), and therefore substantially lower than the experimentally observed 20% variation.

Nevertheless, the simulation reveals that also for the case of bulk conduction, a gate-bias dependent mobility can be observed in the presence of a trap distribution within the nanowire. The crucial factor for the observation of a gate-dependent mobility is the

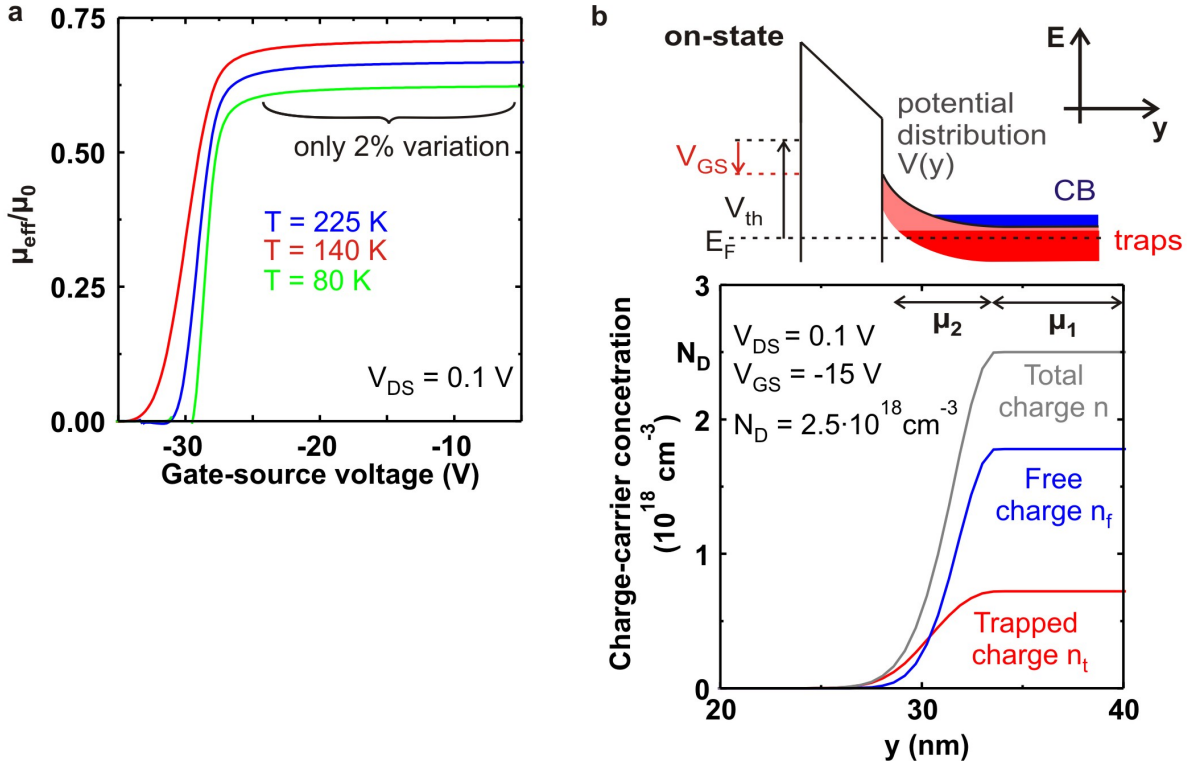


Figure 10.2: **Simulation of the effect of trap states on the mobility of an FET operating in the depletion regime.**
(a) Simulated normalized mobility versus $V_{GS}$ for temperatures of 225 K (red curve), 140 K (blue curve), and 80 K (green curve). A ZnO nanowire with a doping concentration of $N_D = 2.5 \cdot 10^{18}\,cm^{-3}$ and an exponential distribution of trap states below the conduction band was assumed for the simulation. The mobility shows a strong dependence on $V_{GS}$ above the switch-on of the FET ($-35\,V < V_{GS} < -25\,V$). For $V_{GS}$ > -25 V the mobility is only weakly dependent on $V_{GS}$. (b) Schematic band diagram of the channel cross-section and simulated charge distribution across the channel for $V_{GS} = -15\,V$. The field-effect mobility across the channel can be divided into two regions: In the neutral region (V(y) = 0) the ratio between the free charges $n_f$ (blue curve) and the trapped charges $n_f$ (red curve) is constant, causing a constant mobility $\mu_1$. The total electronic charge (gray curve) in this region equals the number of ionized dopants $Q_{tot} = qN_D^+$. In the depletion region ($V(y) \neq 0$) the ratio between $n_f$ and $n_t$ reduces monotonically towards the semiconductor/insulator interface and the effective mobility $\mu_2$ is smaller than $\mu_1$. With increasing $V_{GS}$, the neutral region ($\mu = \mu_1$) extends towards the semiconductor/insulator interface. Therefore the influence of region $\mu_1$ increases with increasing $V_{GS}$ and the overall effective mobility also increases with $V_{GS}$.

regime $\mu_2$ in figure 10.2b . The extension of regime $\mu_2$ in comparison with the regime of constant mobility $\mu_1$ thereby determines the magnitude of the gate-bias dependence. Within the model of the Schottky-parabola approximation, the charge distribution across the nanowire channel is assumed to be constant (and equal to the amount of ionized dopants $Q_{tot} = qN_D^+$) in the depleted area of the nanowire, and zero in the neutral region

($Q_{tot} = 0$). This leads to the parabolic potential drop V(y). In the presence of traps this approximation might be too simple. The important mobility regime $\mu_2$ (that determines the gate-bias dependence of the effective mobility) corresponds to the region were the total charge is $0 < Q_{tot} < qN_D^+$ (figure 10.2c, gray curve). Therefore, the utilized Schottky parabola approximation may underestimate the extension of the regime $\mu_2$ and therefore also underestimate the gate-bias dependence of the mobility. Furthermore, the situation in a real nanowire might also involve spatially varying densities of trap states and dopants, which further complicates the calculation of the real potential drop in the nanowire and an accurate modeling of the gate-voltage dependence of the mobility.

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# Publications

- R.T. Weitz, U. Zschieschang, A. Forment-Aliaga, D. Kaelblein, M. Burghard, K. Kern, and H. Klauk. Highly Reliable Carbon Nanotube Transistors with Patterned Gates and Molecular Gate Dielectric. *Nano Letters*, 9(4):13351340, 2009.
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- R. Noriega, J. Rivnay, L. Goris, D. Kaelblein, H. Klauk, K. Kern, L.M. Thompson, A.C. Palke, J.F. Stebbins, J.R. Jokisaari, et al. Probing the electrical properties of highly-doped Al: ZnO nanowire ensembles. *Journal of Applied Physics*, 107(7):074312074312, 2010.
- D. Kaelblein, H.J. Boettcher, R.T. Weitz, U. Zschieschang, K. Kern, and H. Klauk. Integrated circuits using top-gate ZnO nanowire transistors with ultrathin organic gate dielectric. *International Electron Devices Meeting (IEDM)*, 2009.
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- H. Ryu, D. Kaelblein, R.T. Weitz, F. Ante, U. Zschieschang, K. Kern, O.G. Schmidt, and H. Klauk. Logic circuits based on individual semiconducting and metallic carbon-nanotube devices. *Nanotechnology*, 21:475207, 2010.
- F. Ante, D. Kaelblein, U. Zschieschang, T. W. Canzler, A. Werner, K. Takimiya, M. Ikeda, T. Sekitani, T. Someya, and H. Klauk. Contact doping and ultrathin gate dielectrics for nanoscale organic thin-film transistors, *Small*, pages n/a-n/a, 2011.
- D.Kaelblein, H.J. Boettcher, R.T. Weitz, U. Zschieschang, K. Kern, and H. Klauk, Top-Gate ZnO Nanowire Transistors with Ultrathin Organic Gate Dielectric, *in preparation.*
- H. Ryu, D. Kaelblein, O.G. Schmidt, and H. Klauk, Sequential Circuits with Transistors based on Individual Carbon Nanotubes and Thin-Film Carbon Resistors, *in preparation.*

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