# Graphene-based Field-effect Transistors

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by

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# Abstract

With transistors set to reach their smallest possible size in the next decade, the silicon chip is likely to change dramatically, or be replaced entirely. The transistor industry's path which has been largely shaped by Gordon Moore's famous prediction that the number of transistors on a silicon chip would double approximately every eighteen months, predicts a size of transistor which silicon technology cannot sustain, thereby ushering in a post-silicon age in semiconductors soon.

In this scenario, graphene-derived nanomaterials are emerging as promising candidates for post-silicon electronics devices, with potential applications as atomically thin transistors and other nanoelectronic devices which incorporate quantum size effects. However, such claims still require a few important issues to be addressed first.

This thesis focuses on demonstrating and studying field effect behaviour in graphene- and graphite-based devices. It describes the differences between the two types of graphene bilayers and the effect of their stacking order when placed in an electric field. The differences are studied using Scanning Photocurrent Microscopy, leading to the conclusion that the bottom layer in a misoriented bilayer effectively screens the charge carrier modulation when used in a back-gated FET configuration. A polymer electrolyte gate was employed on top to ultilise the enhanced carrier mobility within the top layer.

The study is extended from bilayer graphene to multilayer graphene (graphite) while addressing a possibility of fabricating a field effect transistor on such a material. The thesis comments on the differences between each of these and their prospects in future applications.

While emphasizing the effect of the substrate in such FETs, an intrinsic gain in a graphene-based FET of over one is shown at room temperature. The importance of both these aspects in the devices is also elucidated. Furthermore, the misoriented bilayer transistors were incorporated into phase-shift detectors, to exhibit their functioning in logical circuits.

On the technical side, a novel method for fabricating graphene-based transistors on a lab-scale has been demonstrated which uses fluorescence quenching to distinguish the number of layers in a graphene stack.

**Keywords:** Graphene, Graphite, Field Effect Transistors, Lithography, Scanning Photocurrent Microscopy.

# Zusammenfassung

Die zunehmende Verkleinerung von Halbleiter-Transistoren wird voraussichtlich innerhalb der nächsten 10 Jahre an ihre Grenzen sto$\beta$en. Dadurch wird eine grundlegende Veränderung des herkömmlichen Siliziumchips oder gar dessen Ersetzung erforderlich. Die bisherige Entwicklung der Chipindustrie erfolgte in guter Übereinstimmung mit Gordon Moore's berühmter Vorhersage, dass sich die Zahl der Transistoren auf einem Siliziumchip etwa alle 18 Monate verdoppelt. Mittlerweile nähern sich Transistoren einer Grö$\beta$e an, die sich mittels Siliziumtechnologie nicht länger verwirklichen lässt, womit das Post-Silizium-Zeitalter in greifbäre Nähe gerückt ist.

Vor diesem Hintergrund rücken Kohlenstoff-Nanostrukturen wie Graphen als vielversprechende Kandidaten für nicht-siliziumbasierte elektronische Bauelemente in den Vordergrund. Von diesen verspricht man sich Transistorkanäle mit atomarer Dicke oder nanoelektronische Bauelemente, in welchen Quanteneffekte eine Rolle spielen. Deren praktische Realisierung bedarf allerdings noch der Überwindung etlicher technologischer Hürden.

Diese Doktorarbeit befasst sich mit dem Nachweis und der Untersuchung von elektrischen Feldeffekten in Graphen- und Graphit-basierten Bauelementen. Ein Thema ist hierbei der Vergleich von Graphen-Doppellagen, die sich in der Stapelanordnung der Lagen unterscheiden. Mittels Rasterphotostrommikroskopie wurde festgestellt, dass die untere Graphenlage in einer nicht-kommensurablen Doppelschicht die andere Lage effektiv gegenüber dem Backgate abschirmt. Mit Hilfe eines Topgates bestehend aus einem Polymerelektrolyten gelang es, den Ladungstransport durch die obere Graphenlage unter Bewahrung einer hohen Ladungsträgermobilität zu steuern. Zusätzlich zu den Doppellagen wurde auch der Einsatz von mehrlagigem Graphen (Graphit) als Transistorkanal untersucht. In diesem Zusammenhang werden die kritischen Faktoren, welche den zukünftigen Einsatz solcher Transistoren begrenzen, diskutiert.

Darüber hinaus gelang es, eine intrinsische Verstärkung grö$\beta$er eins in einem Graphen-basierten Feldeffekttransistor bei Raumtemperatur zu erzielen. Hierbei kommt dem Effekt des Substrats eine wichtige Rolle zu. Weiterhin wurde aus einem Transistor, dessen Kanal aus einer nicht kommensurablen Graphendoppellage besteht, ein Phasenverschiebungsdetektor gewonnen, und dessen Funktionsweise in einem logischen Schaltkreis demonstriert.

Schlie$\beta$lich wurde ein neuartiges Verfahren zur schnellen und effizienten Herstellung von Graphen-basierten Transistoren im Laborma$\beta$stab entwickelt. Dieses macht sich die

Abhängigkeit der Fluoreszenzlöschung eines adsorbierten Farbstoffs von der Anzahl an Lagen in einem Graphenstapel zunutze.

**Schlüsselbegriffe**: Graphen, Graphit, Feldeffekttransistoren, Lithografie, Lokale Photostrommessungen.

# Contents

# Abbreviations

| | |
|---|---|
| 1D, 2D, 3D | one-, two-, three-dimensional |
| AFM | atomic force microscope |
| ALD | atomic layer deposition |
| BLG | bilayer graphene |
| CMOS | complementary metal-oxide semiconductor |
| CNP | charge neutrality point |
| CNT | carbon nanotube |
| DOS | density of states |
| FET | field effect transistor |
| HEMT | high electron mobility transistor |
| HOPG | highly ordered pyrolitic graphite |
| IC | integrated circuit |
| ITRS | international technology roadmap for semiconductors |
| JFET | junction field effect transistor |
| MESFET | metal-semiconductor field effect transistor |
| MIBK | methyl iso-butyl ketone |
| MOSFET | metal-oxide-semiconductor field effect transistor |
| PCB | printed circuit board |
| PMMA | poly-methyl methacrylate |
| SPCM | scanning photocurrent microscopy |
| XOR | exclusive-OR |

# Chapter 1

# Introduction

George Beylerian says, "the world seems to expect a never-ending supply of new material options" [1]. Mr. Beylerian is the founder and current Head of *Material ConneXion*, a global materials supplier to designers and industry alike, and which hosts one of the largest physical libraries of advanced materials in the world. Whether or not the whole world is really expectant could be arguable, but the evolution of material science over the years fuels this expectancy at least amongst those who have a vision that projects into the future. New materials have their genesis in the laboratories of universities, governments and industry. The technologies developed here are spun-off into start-ups or are adopted by existing firms into their production line-ups.

An example of the expectancy for novel materials can be found in the semiconductor industry where new forms of carbon have been vying to substitute silicon. The International Technology Roadmap for Semiconductors (ITRS) which is sponsored by the world's top chip manufacturing companies, has forecasted the end of CMOS-based technology by the year 2022 [2]. ITRS has the objective of ensuring cost efficient advancements in IC manufacturing, and thus the reasons for the CMOS demise is both economical and practical. Silicon has the physical limitation of not being able to exist below 10 nm as a crystalline solid, as the thermal fluctations due to the generated heat (in microcircuitry) in that range makes it turn amorphous. The continually downsizing channel widths in modern circuitry thus has a deadend in less than a decade. To continue the advancements in this field, one must indulge in a suitable substitute. Carbon has been widely tipped as this substitute. The reasons for the candidature is its impressive allotropes, and its similiarity with silicon on the VI-A column on the periodic table. Interestingly, silicon's predecessor, germanium also hails from the same column. Although, both silicon and

carbon have the same number of electrons in the outermost electronic shell, and hence similar chemical properties, the size of the electronic wave functions and their energy vary significantly. (This difference can be seen in the Coulomb intereactions of the respective electron systems. Silicon's larger electron cloud shields these interactions amongst its electrons.) Carbon also has the highest melting of all elements, around $3500^oC$ (while silicon melts at $1700^oC$). Considering these properties, swapping silicon for one of carbon's allotropes seems a logical choice, so the research community has been searching for an ideal allotrope which matches the needs.

In the recent past, two carbon allotropes had become prominent contenders to replace silicon - nanotubes and graphene. Graphene is a two-dimensional honeycomb lattice of carbon rings just one atom thick, while nanotubes can be considered as rolled-up graphene sheets. They both have equally impressive mechanical and electronic properties. Carbon nanotubes (CNTs) had dominated research news in the 90's with their widespread potential in various fields of applications ranging from medicene to electronics. However, they have been facing unresolved challenges involving their controlled growth with desired chirality, purity and dispersion. In the electronic world, inspite of their first claim to fame - charge carrier mobilities of more than 100,000 $cm^2/Vs$ at room temperature - the unpredictability of their electronic nature (metallic or semiconducting) on production, has dented their chances of replacing silicon. Though younger, graphene has leapfrogged nanotubes in this scene, primarily due to the seemingly simpler methods of production and consistent electronic behaviour (semi-metallic) which can be modified according to use. Graphene's charge carrier mobilities are measured to be over 200,000 $cm^2/Vs$ at room temperature. But unlike CNTs, which require a different set of processing techniques from silicon, graphene shares a similar set of processing techniques currently used for silicon. Graphene is also the thinnest known material, which enables it to be transparent, thereby providing an attractive offer for the usage in optoelectronic devices like photovoltaics. The competition between the two allotropes is gradually also extending to other fields like chemical and bio-sensors, mechanical resonators etc. But to go from lab scale to mass scale, engineers still need to devise methods to make industrial quantities of large, uniform sheets of pure, single-planed graphene.

This thesis concentrates on the electronic properties of graphene and elucidates its stance in post-silicon electronics (or nanoelectronics due to the current dimensions of operation) from a material point of view. It investigates prototype field effect transistors (FETs) with graphene and graphite as conducting channels. This work aims to study

these materials' electronic properties for potential applications, as there are some pertinent challenges remaining about graphene, including its low (intrinsic) on-off ratios, voltage gain, substrate effects and scalability.

The thesis is organized in the following manner:

Chapter 2 provides an introduction to the theoretical aspects of graphene and a brief literature survey to make the reader aware of the existent work on graphene.

Chapter 3 introduces the major technological aspects of the thesis, where the various characterization techniques and fabrication methods employed in this work are discussed.

Chapter 4 describes a novel fabrication procedure for graphene transistors and a fluorescence-quenching based technique used to distinguish graphene layers of varying thicknesses.

Chapter 5 is devoted to the analysis of two different types of bilayers and the effect of a misorientation in the stacking order of the two layers. It also discusses the effect of the substrate and decoupling in layers.

Chapter 6 takes a look at the relevance of mono- and bilayer graphene in real world nanoelectronics, and discusses the intrinsic gain measurements of over 1 in decoupled bilayer devices.

Chapter 7 describes field effect in multi-layered graphene (graphite) and its relavence in comparision to few-layer bilayers.

Chapter 8 rounds up the thesis with a summary and an outlook as to where graphene-based electronics is heading.

# Chapter 2

# General Concepts

## 2.1 Graphene

**What is graphene?**

Graphene is a one-atom thick layer of carbon atoms arranged in a hexagonal lattice. It can be considered as a conceptual building block for other carbon allotropes like nanotubes, buckyballs or graphite. In fact, many of the electronic and structural properties of the latter can be derived from graphene. Interestingly though, graphene was the last allotrope to be discovered. Until about a few years ago, this two-dimensional form of carbon was known only in the three-dimensional stack of graphite or tightly bound to the surface until scientists from Manchester University, Andrei Geim and Kostya Novoselev famously cleaved it from the former (a graphitic stack) in 2004 and studied the electronic properties of their samples. This subsequently resulted in the popularisation of the material especially amongst condensed-matter physicists and their pioneering efforts bagged Geim and Novoselev the 2010 Nobel Prize in Physics. Surface scientists had previously been familiar with its occurence as "mono-layer graphite" and as an undesirable impurity on metal or semiconductor surfaces [3]. Its origin can be traced back to the 1950s, when Linus Pauling in his work "The Nature of Chemical Bond" described the only known carbon allotrope at that time, i.e., graphite as a layered structure made up of several "giant molecules". Those giant molecules were also found by a German chemist, Hann-Peter Boehm in 1962, when he described them as single layer carbon foils [4] which can be obtained by reducing or delaminating graphite oxide. Since then much progress has been made in understanding these monolayers which are called *graphene* today, while many more of its fascinating aspects still continue to be discovered.

The original paper which triggered off the recent enthusiasm [6] reported that graphene could be obtained by rubbing a freshly cleaved piece of highly ordered pyrolitic graphite (HOPG) on a tape, and then transferred onto a silicon substrate with a native oxide. This method is termed as "mechanical exfoliation" and was also used in the experiments involved in this thesis. Identifying such a sheet of carbon atoms, is where this group pipped other scientists. They found that graphene is visible in an optical microscope, due to the contrast exhibited when placed on a Si substrate with 300 nm thick $SiO_2$ owing to the interference in the optical path upon reflection. Such recognition and identification of graphene layers is explained more elaborately in Chapter 3.

**What is special about graphene?**

Early experiments on graphene showed its field-effect transistor behaviour, with the underlying silicon substrate acting as a back-gate. The electrical properties impressed [6], with an intrinsic charge carrier mobility of 200,000 $cm^2/Vs$ at room temperature, highest known in any material. In a perpendicular magnetic field, electrons in a conventional two-dimensional electron gas are quantised in equidistant Landau levels leading to the quantum Hall effect. But the conducting electrons moving in the graphene lattice are described by the Dirac equation, rather than the usual Schroedinger's equation [5]. These Dirac electrons are also quantised in Landau levels when subjected to a perpendicular magnetic field. However, the Landau levels are not equally spaced but follow a square root dependence on the magnetic field. The most interesting feature is the existence of a zero energy Landau level. As a result, the Hall conductance in graphene is quantised in values that are half-integer multiples of $4e^2/h$ i.e. $2e^2/h$, $6e^2/h$, $10e^2/h$ etc. Philip Kim and colleagues [14] at Columbia University showed the quantum Hall effect (QHE)in mechanically exfoliated graphene. This effect was previously only seen in carefully prepared semiconductor heterostructures. The QHE in graphene can be observed even at room temperature. Later, the observation of anamolous half-integer quantization of the Hall conductance proved the massless chiral nature of charge carriers in graphene.

The relation between energy and momentum in graphene is different from any other material due to this honeycomb lattice structure. For non-relativistic electrons moving in free space, the energy $E$ is related to the momentum $p$ by the classical relation: $E = p^2/(2m)$, where $m$ is the electron mass. This relation holds in many materials, even in the presence of the interactions between electrons and lattice (ions) and among electrons themselves, where the electron mass $m$ is replaced with an effective electron mass $m^*$

which reflects the change in the inertia of the electron due to its environment. In the honeycomb lattice, this energy-momentum relation changes into $E = +- \nu|p|$, where $\nu$ is the so-called Fermi-Dirac velocity that depends on the material properties. The +- signs refer to the two cones in the energy-dispersion relation of graphene, unlike the single energy band in metals. This modified energy relation corresponds to massless relativistic particles with the speed of light being substituted by $\nu$, which is about 300 times less than the speed of light. Thus, this difference in the energy-momentum relation makes graphene unique and has significant consequences in the physics of graphene.

## 2.2 Electronic Structure of Graphene

Graphene consists of a honeycomb lattice of carbon atoms, in which 2s, $2p_x$ and $2p_y$ orbitals hybridize such that each carbon atom is bonded to its three neighbours by strong $sp^2$ or $\sigma$ bonds. The remaining $p_z$ orbital is perpendicular to the lattice and overlaps with other $p_z$ orbitals to form a $\pi$ bond. The $p_z$ electrons are delocalized throughout the crystal and govern the electronic transport. Figure 2.1(a) shows a schematic of the graphene lattice. The dotted structure represents the unit cell of the crystal, where two carbon atoms are represented in two different colours, with lattice vectors $a_1$ and $a_2$.

Figure 2.1(b) shows the $\pi$ bands of the ideal monolayer in the vicitinity of the K-point, as calculated from a tight binding approach. The two cones seen in its electronic structure are a consequence of particles and anti-particles, which are also termed electrons and holes (collectively called charge carriers). For undoped graphene, the two cones which represent the conduction and valence bands, respectively, intersect at a single point called the Dirac point. This feature distinguishes graphene from conventional semiconductors which exhibit a bandgap. Hence, graphene is a hybrid between a metal and semiconductor, and hence dubbed a "semimetal". The absence of a gap has a practial relevance in electronics, which will be discussed later. The following paragraphs meanwhile, explain the origin of its electronic structure.

For graphene, the tight binding Hamiltonian with only nearest neighbour hopping can be written as

$$H = -t(\sum_{<jk>} |j><k|) \tag{2.1}$$

where $t > 0$ is the hopping integral, $|j>$ ($|k>$) is an atomic wavefunction centred around atomic sites $r_j$ ($r_k$), and the $\sum$ sums all over neighbouring sites $j$ and $k$. The

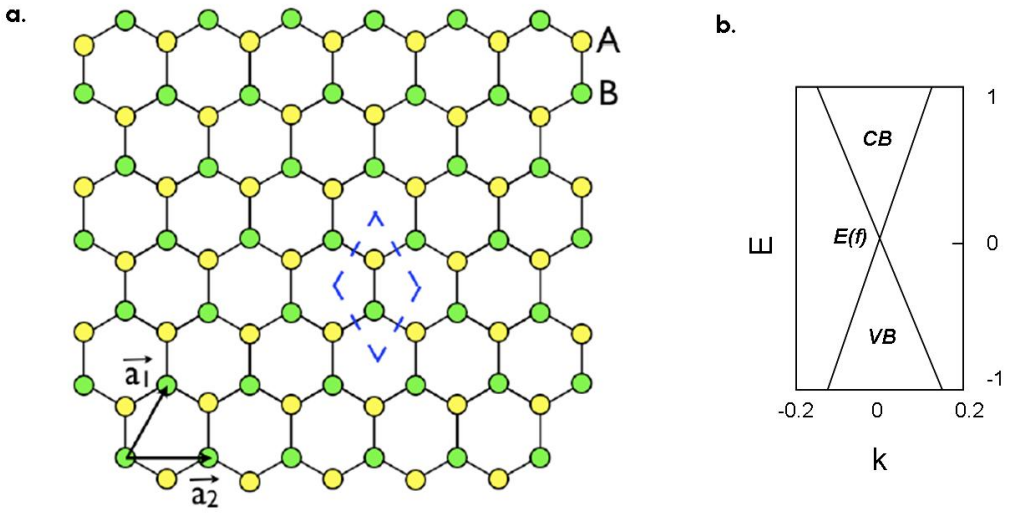


Figure 2.1: (a) Schematic representing the hexagonal graphene lattice, which is formed by two sublattices of inequivalent carbon atoms A and B. The dotted rhombus corresponds to the unit cell, whereas $a_1$ and $a_2$ are unit vectors. (b) Electronic band structure depicting the $\pi$ bands of an ideal monolayer in the vicitinity of K-point. (CB and VB are conduction and valence bands respectively).

minus sign is because the electron lowers its energy by hopping to the neighbouring site. From the lattice structure, it is evident that all atoms from sublattice A (see Fig.2.1) have atoms B as nearest neighbour. In graphene, the hopping integral t has been found to be 2.7 eV [7, 8].

The solution to this Hamiltonian is a Bloch wave and can be written in terms of sublattice A and B as:

$$|\psi_k >= b_1 \sum_A exp(ik.R_n)|n >_A + b_2 \sum_B exp(ik.R_n)|n >_B \tag{2.2}$$

where $R_n$ represent lattice vectors, $|n >_A$ are atomic wave functions of A and $|n >_B$ are atomic wave functions of B, while $\sum$ sums over the entire A or B sublattice.

To solve for the eigenvalues we project $|\psi_k >$ to two wavefunctions $|l >_A$ and $|l >_B$ and obtain the following

$$_A < l|H|\psi_k >= -tb_2 \sum_{j=1,2,3} exp(-ik.\rho_j) = b_1 E_k \tag{2.3}$$

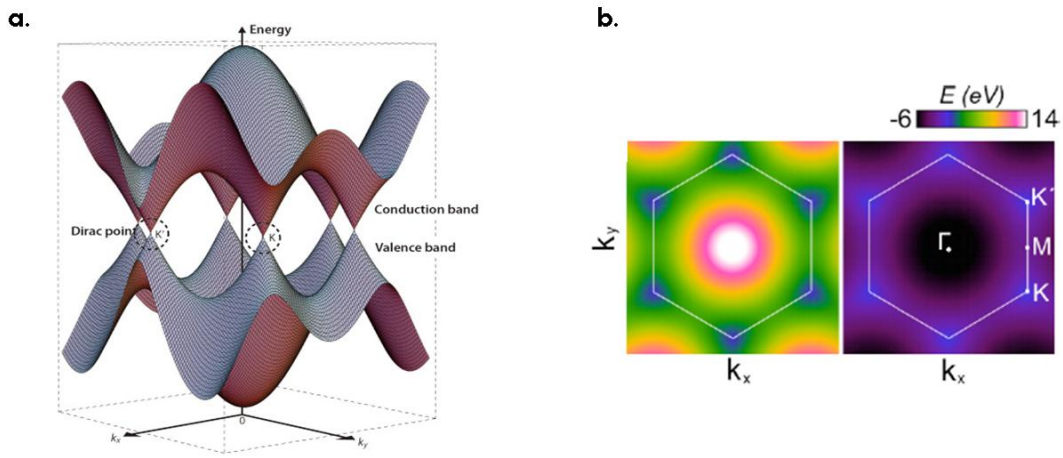


Figure 2.2: (a) Tight-binding 2D energy dispersion plot of graphene. It can be seen that the bands are approximately linear in the vicinity of Fermi level (E=0). (b) Contour plots of the energy dispersion of th $\pi^*$ and $\pi$ bands. The white lines depict the boundary of the Brillouin zone.

$$_B < l|H|\psi_k >= -tb_1 \sum_{j=1,2,3} exp(ik.\rho_j) = b_2 E_k \tag{2.4}$$

where $\rho_i$ are vectors that connect one lattice site to its three neighbouring lattice sites as indicated in the Fig.2.1. The energy dispersion $E_k$ is obtained after eliminating $b_1$ and $b_2$,

$$E_k = +/-t|(\sum_{j=1,2,3} exp(ik.\rho_j)| \tag{2.5}$$

Fig. 2.2(a) shows a plot of the Eq.2.5. As there are two atoms per unit cell, there are two bands, i.e. the conduction band and the valence band, which touch each other at six points in the reciprocal space. These six points are called K points, which coincide with the boundary of the first Brillouin zone. The Fermi energy lies exactly at the K points for undoped graphene since each atom contributes one electron. The Fermi surface of graphene therefore consists of these six *points*, thereby no "gap". This is the reason why graphene is also sometimes called a "zero band-gap semiconductor".
These six points at the Fermi surface are independent, since every next nearest neigh-

bouring points are related to each other by a reciprocal lattice vector b. They are thus reduced to only two independent K points : K and $K' = -K$ as shown in Fig. 2.2 (b). The two independent K points or valleys are sometimes referred to as the iso-spin. The K and K' points are degenerate, because they are related to each other by time reversal symmetry. This is often called valley degeneracy. This physics is important to understand the nature of Fermions in graphene.

The charge carrier density and the density of states (DOS) are critical for understanding the experimental results related to electronic devices. For conventional electron gases, the number of electrons at Fermi level, $E_F$ for $T = 0$ is given by dividing the k-space volume $V_k$ of all states by the k-space volume $\Omega_k$ of one state [9]. Further, the valley and spin degeneracy each contribute with a factor of 2. Also, the two-dimensionality of graphene's electron system and the linear dispersion relation $E(q) = \hbar v_F q$ have to be taken into account. The concentration of electrons at the Fermi energy $E_F$ (per volume V) is given by

$$n = \frac{4V_k}{V\Omega_k} \tag{2.6}$$

$$n = \frac{4q_k^2\pi}{2(4\pi^2/V)} \tag{2.7}$$

$$n = \frac{q_F^2}{\pi} \tag{2.8}$$

$$n = \frac{E_F^2}{\hbar^2 v_F^2 \pi} \tag{2.9}$$

Here $q_F$ denotes the electron momentum with respect to the K-point at $E_F$. The density of states as the derivative of the energy dependent concentration n(E), i.e. $\frac{dn}{dE}$ consequently amounts to

$$\rho(E) = \frac{2E}{h^2 v_F^2 \pi} \tag{2.10}$$

The DOS in graphene thus exhibits a linear behaviour.

The initial transport experiments on graphene revealed its ambipolar behaviour, i.e. the charge carrier concentration can be tuned by modulating the voltage in the backgate upto $10^{13} cm^{-2}$ for electrons as well as holes. The variation of the cyclotron mass with charge carrier concentration had provided the first evidence of fermions in graphene [10, 14].

Another interesting feature of graphene is that its conductance remains finite even when the charge carrier concentration tends towards zero. Many explanations have been put forth for this. One of them being a phenomenon known as "Zitterbewegung" which describes jittery movements of a relativistic electron due to interference between parts of its wavepacket belonging to positive (electron) and negative (positron) energy states [13]. Theory suggests a minimum conductivity of $4e^2/(h\pi)$, but the experimental data showed $4e^2/h$. The so-called "missing $\pi$" was addressed by Adam et al. [15], who analysed graphene devices from a semiconductor physics perspective and attributed the factor $\pi$ as a consequence of charge impurities. Their model assumes that charge impurities trapped between the substrate and the graphene layer induce charges within the graphene flake, thus leading to the formation of puddles of electrons and holes. Therefore, the electrical transport in the low charge carrier density regime around the Dirac point is governed by percolating paths along these electron-hole puddles. Experimental support for this model is provided by a scanning single electron transistor study, wherein the electron and hole rich regions were directly observed [16]. However further experiments on suspended graphene [26] have shown that the minimum conductivity approaches the theoretical value of $4e^2/(h\pi)$. This finding underlines the need to address the substrate influence in more detail.

**Bandgap**

As mentioned, monolayer graphene is a zero-band semiconductor. As a consequence, graphene devices cannot be switched off, and hence cannot be used for logic applications. However, the bandstructure of graphene can be modified to open a gap in the following ways: (1) by fabricating narrow graphene structures (nanoribbons) [17, 18] within the 2D plane, (2) by biasing bilayer graphene with an external field [19], and (3) by applying strain on graphene [20, 21].

To open a bandgap useful for conventional FET devices, very narrow nanoribbons (less than 20 nm in width) with well-defined edges are needed. This is a serious challenge at a mass-scale considering there is no technology to cut such edges in a controlled manner yet. Even a perfectly defined nanoribbon is not perfect for electronic applications. In general, the larger the bandgap that opens in a nanoribbon, the more the valence and

conduction become parabolic, thus decreasing the curvature around the K point and thereby increasing the effective mass of the charge carriers [17]. This would decrease the mobility, which is the prime lure of graphene based electronics.

Bilayer graphene inherently is without a gap too, and its valence and conduction bands have a parabolic shape near the K point. However, if an electric field is applied perpendicular to the bilayer, a gap opens [22, 23] and the bands near the K point take on the so-called Mexican hat shape. Such a band gap opening has been verified both theoretically and experimentally. Theoretical predictions [24] show that the bandgap size depends on the field strength and could reach values of 200 to 250 meV for very high field strengths (3x$10^7$ V/cm).

Strain has been reported as another method to open a bandgap in large-area graphene, and the effect of uniaxial strain on the band structure has been simulated. The theoretical prediction to induce a gap would require a global uniaxial strain exceeding 20 percent which will be difficult to achieve in practice. However, the effect of biaxial strain and local strain has yet to be investigated.

As this thesis concentrates primarily on employing graphene as field effect transistors (FETs), the following section introduces the corresponding basic principles.

## 2.3 Transistors

Initial reports about transistors date back to 1938 when Hilsch and Pohl presented one of the first transistor models [46]. Later Bardeen, Brattain and Shokley discovered their bipolar transistor in 1947 [47], which was the first three-terminal device to be realised. It consists of two p-n junctions back to back, i.e., a p-n-p structure. One terminal is connected to each of the sections. The current flowing between the two p-type parts of the device can be tuned by the application of a voltage to the n-type terminal. Since this discovery, however, the electronics industry has come a long way, and the FETs we commonly find now are called MOSFETs. Any transistor based on an alternative material (other than silicon) must compete with a 50-odd year history of MOSFETs. (The first metal-oxide-semiconductor FET (MOSFET) was realized in 1960 by Kahng and Atalla [48]). The schematic structure of a MOSFET is shown in Figure 2.3.

The semiconducting channel is connected to two terminals labeled source (S) and drain (D) that are used to apply a voltage along the channel, whereas the third terminal labeled

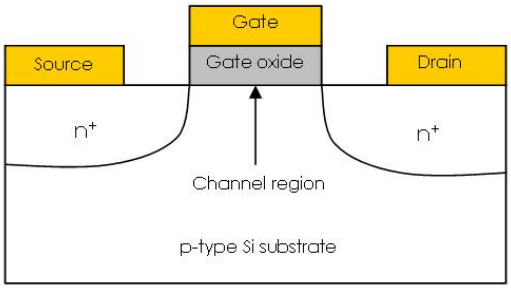


Figure 2.3: Cross section of a n-doped Si MOSFET.

gate (G) is electrically insulated from the semiconducting channel. It serves to control the electrostatic potential at the semiconductor/insulator interface. There are different types of FETs that can be distinguished by the way the gate is coupled to the channel. At present, the most commonly used type is the MOSFET in which the gate capacitor is formed by an insulator, for example $SiO_2$ between the metallic gate electrode and the semiconducting channel. Other types of FETs are the junction FET (JFET) and the metal-semiconductor FET (MESFET) in which the gate capacitor is formed by a depletion layer. In MOSFETs, the charge carriers in the conducting channel are electrons, but the semiconducting channel is slightly p-doped (termed inversion mode). Doping stems from the incorporation of chemical impurities into a crystal that do not have the same valency as the host crystal. The FETs usually rely on a heavily doped silicon wafer that is used as back-gate electrode and as the substrate. The substrate is coated with an insulating layer called gate dielectric. In contrast, the graphene FETs that are being addressed in this thesis are not deliberately doped, and the channel is formed by the accumulation of holes or electrons, with the underlying $Si/SiO_2$ substrate acting as the back-gate.

For high-speed applications, FETs should respond quickly to variations in gate voltage, which requires short gates and highly mobile carriers in the channel. Unfortunately, FETs with short gates suffer from degraded electrostatics and other problems (collectively known as short-channel effects), such as threshold-voltage roll-off, drain-induced barrier lowering, and impaired drain-current saturation [53]. Scaling theory predicts that a FET with a thin barrier and a thin gate-controlled region (measured in the vertical direction in Fig. 2.3) will be robust against short-channel effects down to very short gate lengths (measured in the horizontal direction in Fig. 2.3 [49]). The possibility of having channels that are

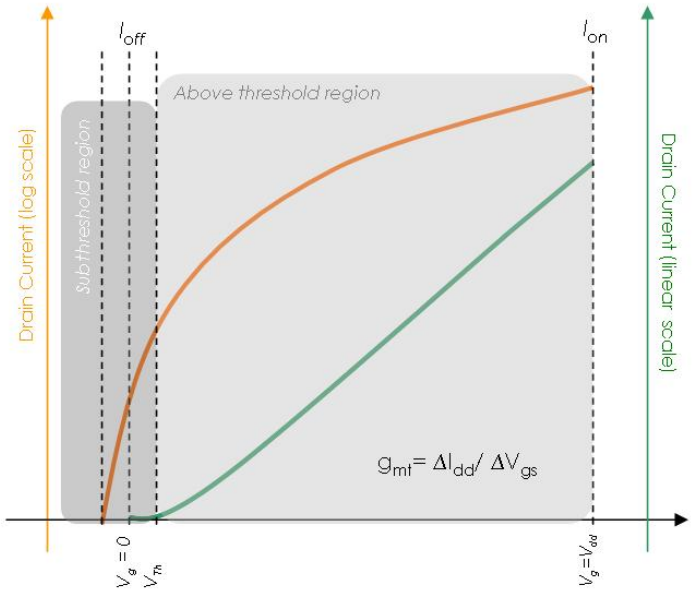


Figure 2.4: FET transfer characteristics showing drain current (on a logarithmic scale on the left and a linear scale on the right) versus the gate-source voltage [53, 54].

just one atomic layer thick is perhaps the most attractive feature of graphene for use in transistors. Mobility, which is often considered to be graphene's most useful property for applications in nanoelectronics, is discussed later. By comparison, the channels in $III-V$ group High Electron Mobility Transistors (HEMTs) are typically 10 to 15 nm thick, and although silicon-on-insulator MOSFETs with channel (that is, silicon body) thicknesses of less than 2 nm have been reported [51], rough interfaces caused their mobility to deteriorate. More importantly, the body of these MOSFETs showed thickness fluctuations that lead to unacceptably large threshold-voltage variations (and similar problems are expected to occur when the thickness of the channel in a $III-V$ HEMT is reduced to only a few nanometers). These problems occur at thicknesses that are many times greater than the thickness of graphene.

The series resistances between the channel and the source and drain terminals are also important, and their adverse impact on the FET becomes more pronounced as the gate length decreases [50]. As a result, device engineers devote considerable effort to developing transistor designs in which short-channel effects are suppressed and series resistances are minimized.

Current digital logic is based on silicon complementary metal oxide semiconductor (CMOS) technology, which includes gates consisting of both n- and p-channel MOSFETs that can be switched between the on-state (i.e. with a large on-current, $I_{on}$ , and $V_{gs} = +-V_{dd}$ , where $V_{dd}$ is the maximum voltage supplied to the device) and the off-state (with a small off-current, $I_{off}$, and $V_g = 0$). In other words, the gate terminal is involved in the logical operation. The value of $V_{gs}$ at which the FET is just on the verge of switching on is known as the threshold voltage, $V_{Th}$. Figure 2.4 shows the transfer characteristics of an n-channel FET indicating the on-state and the off-state. Useful measures with which to assess the switching behaviour are the subthreshold swing, S (relevant to the subthreshold region), and the transconductance, $g_{mt}$ (relevant to the above-threshold region) are shown in Table 1.

| | |
|---|---|
| *Terminal transconductance* | $g_{mt} = \left.\frac{dI_D}{dV_{GS}}\right\|_{V_{DS}=\text{const}}$ |
| *Intrinsic transconductance* | $g_m = \left.\frac{dI_D}{dV_{GSi}}\right\|_{V_{DSi}=\text{const}}$ |
| *Drain conductance* | $g_{ds} = \frac{1}{r_{ds}} = \left.\frac{dI_D}{dV_{DSi}}\right\|_{V_{GSi}=\text{const}}$ |
| *Gate-source capacitance* | $C_{GS} = -\left.\frac{dQ_{ch}}{dV_{GSi}}\right\|_{V_{DSi}=\text{const}}$ |
| *Gate-drain capacitance* | $C_{GD} = -\left.\frac{dQ_{ch}}{dV_{DSi}}\right\|_{V_{GSi}=\text{const}}$ |
| *Cut-off frequency* | $f_T \approx \frac{g_m}{2\pi} \frac{1}{(C_{GS}+C_{GD})[1+g_{ds}(R_S+R_D)]+C_{GD}g_m(R_S+R_D)}$ |
| *Field-effect mobility* | $\mu_{FE} = \frac{L_{ch}g_m}{W_{ch}C_G V_{DS}}$ |

Table 1: Relevant Formulae.

Power dissipation is another key issue in CMOS technology. The ability to switch off silicon MOSFETs enables extremely low static power dissipation. In the steady state, a certain number of the MOSFETs in a CMOS logic gate are always switched off so that no current, except the small $I_{off}$ flows through the gate [52]. Thus, according to ITRS, any successor to the silicon MOSFET that is to be used in CMOS-like logic must have excellent switching capabilities, as well as an on/off ratio, $I_{on}/I_{off}$, of between $10^4$ and

$10^7$ [2]. In a conventional FET, this would require semiconducting channels with a sizeable bandgap, preferably 0.4 eV or more. Moreover, n- and p-channel FETs with symmetrical threshold voltages, that is, with $V_{Th,n}$ = -$V_{Th,p}$, are needed for proper CMOS operation.

In radiofrequency (RF) applications, however, such a switch-off is not required. In small-signal amplifiers, for example, the transistor is operated in the on-state and small radiofrequency signals that are to be amplified are superimposed onto the d.c. gate/source voltage. The cut-off frequency ($f_T$) is the frequency at which the magnitude of the small-signal current gain rolls off to unity. The cut-off frequency is the most widely used figure of merit for radiofrequency devices and is, in effect, the highest frequency at which a FET is useful in radiofrequency applications.

As can be seen from the expression for $f_T$ [53, 54] in Table 1, the cut-off frequency can be maximized by making the intrinsic transconductance, $g_m$, as large as possible, and making the drain conductance, $g_{ds}$, and all the capacitances and resistances in the equivalent circuit as small as possible. However, the values of all these quantities vary with the applied d.c. gate source voltage, $V_{gs}$, and the applied d.c. drain−source voltage, $V_{ds}$. As shown previously for GaAs HEMTs [55, 56], $V_{ds}$, has a pronounced effect on the FET performance. Typically in such transistors, $f_T$ peaks around $V_{ds}$ = 1 V, that is, deep in the region of drain-current saturation, where g$m$ is near its peak and $g_{ds}$ has decreased sufficiently. For lower values of $V_{ds}$, the device operates in the linear regime and the cut-off frequency is low because $g_m$ is small and $g_{ds}$ is large.

The critical issue for radiofrequency performance is that although shorter gates, faster carriers and lower series resistances all lead to higher cut-off frequencies, saturation of the drain current is essential to reach the maximum possible operating speeds. Drain-current saturation is also necessary to maximize the **intrinsic gain**, $G_{int} = g_m/g_{ds}$, which has become a valuable figure of merit for mixed-signal circuits.

## 2.4 Other properties of Graphene

Graphene's non-electronic properties are very impressive. It is a robust material in 2D with a breaking strength of 40 N/m [27], which is at the theoretical limit. Moreover, its Young's modulus is close to 1 TPa [27]. Graphene displays a room-temperature thermal conductivity of 5000 W/mK [28], and the unique property of expanding on decreasing the temperature. It can also be (theoretically) stretched elastically by 20 percent more than any other crystal [20, 21, 27]. Graphene is also found to be impermeable to gases [29]

and can be useful for sensing applications.

# Chapter 3

# Fabrication and Characterisation of Graphene

## 3.1 Fabricating graphene

Methods for obtaining graphene can be classified as physical and chemical techniques. Physical methods include micromechanical cleavage (exfoliation) of highly ordered pyrolitic graphite (HOPG) crystal and epitaxial growth on silicon carbide [30, 31]. Other methods to obtain large area graphene include chemical vapour deposition on thin (Ni) metal films. [32, 33] Chemical methods involve the reduction of graphene oxide obtained from graphitic particles [34, 35]. While chemical methods show great promise for obtaining graphene flakes with higher throughput, the high electrical resistance of such flakes is still a matter of concern.

In this work, the graphene flakes were prepared by mechanical exfoliation of HOPG.

**Mechanical exfoliation**

Mechanical exfoliation is a method of cleaving layer(s) of graphene off a HOPG crystal, which consists of layers of graphene sheets. Within each layer, atoms are strongly bound to each other by sigma and pi bonds with bond length 1.42 Angstroms. The interlayer bonds, by contrast, are much weaker and the bond length is of the order 3.4 Angstroms. Therefore, the layers can be separated tranversally by cleaving, either chemically or physically. The latter can be realised using a sticky tape, and that is the method employed in this thesis. The HOPG crystal used in our research group is a ZYA grade (from Momentive Performance Materials Quartz, Inc.) crystal. Alternatives include Kish graphite and natural graphite.

The exfoliation method consists of three basic steps: (i) Repeated peeling of HOPG using a tape, (ii) cleaning the substrate and (iii) transfer of the peeled graphene onto the clean substrate. The repeated peeling is to ensure the cleavage of the layers upto a single layer. Clean substrates are critical, as trapped impurities between the substrate and the graphene flake modify the electrical characteristics that are to be measured. The surfaces of silicon wafers often have a thermally grown oxide which behaves hydrophobically, contrary to the general concept of hydrophilic $SiO_2$. This is due to contamination of the oxide layer. In other instances, prior lithography steps (for markers) induce the same kind of contamination. Accordingly, the substrates must be cleaned in acetone whilst ultrasonicating. Other cleaning methods can be employed provided they do not compromise the surface roughness of the substrate, as this would reduce the charge carrier mobility in the graphene. There have been successful reports of pre-treating the substrate specifically to improve these mobilities and avoid hysterisis [58].

**Visualisation and identification of layers**

After isolating graphene flakes, one of the initial challenges in graphene research was to differentiate a single and bilayer, and later on to identify the number of layers in a few-layer graphene stack. The pioneering works which used exfoliation method to make these graphene layers, proposed the use of 300 nm of native $SiO_2$ on the silicon substrate so that the graphene flakes could be identified under a optical microscope by the optical contrast exhibited due to interference phenomenon [11, 12].

This achievement stimulated groups around the world to conduct similar research, and more importantly to make and identify graphene on a substrate. However, as it was later learned, optical contrast alone is usually not sufficent to distinguish between one and two layers (or three layers even). Figure 3.1(b) shows an optical image of a typical graphene flake that is found on the substrate, after exfoliation. To take a closer look at the same flake, an Atomic Force Microscope (AFM) is used.

## 3.2 Atomic Force Microscopy

Atomic force microscopy (AFM) makes use of the interaction forces between a sharp silicon tip and a sample surface in order to define a constant distance to the surface and thus to obtain a topographic image of the sample surface. The tip with a radius of about 20 nm is mounted at the end of a cantilever. The interaction between the tip and the surface

leads to an attraction or repulsion of the tip and thus to a deviation of the cantilever. This deviation is detected with a laser which is directed on the cantilever and reflected on a photodiode. In the tapping mode the tip has a distance of 1 to 10 nm to the sample and oscillates close to its resonance frequency. If the tip comes closer to the surface weak attractive forces (van der Waals forces) modify the resonance frequency. By keeping a constant frequency the distance between tip and sample is kept constant which is used to obtain the topography. In this work, all AFM images were taken in tapping mode with a *Digital Instruments Nanoscope IIIa Multimode AFM*.

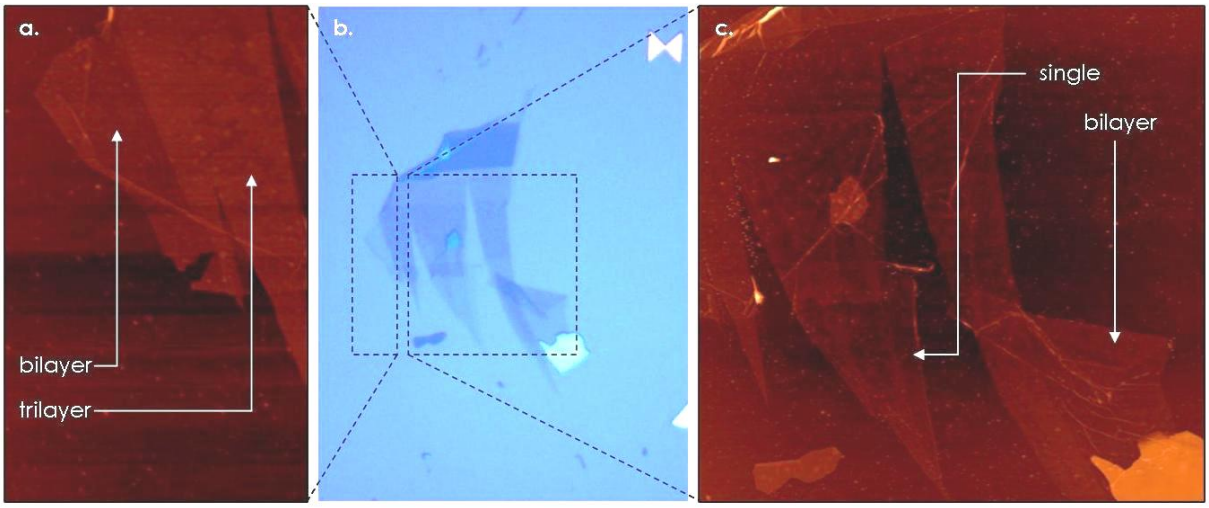


Figure 3.1: (a) (c) AFM images of a selected region. (b) Optical image of the same region.

The AFM image of the flake observed under an optical microscope in Fig 3.1(b) is shown in Figures 3.1(a,c). It can be seen that this particular flake comprises more than one layer of graphene, either folded on top of each other, or stacked together to form a few layer graphene. This can be verified by measuring the height of the flake. A single layer usually exhibits a height of 1 nm, under ambient conditions. Bilayers and trilayers exhibit heights of around 2 and 3 nm, respectively, though with certain inconsistency.

While AFM is helpful to a certain extent in estimating the sheet height, it is difficult to assert the number of layers with confidence using this technique due to the influence of substrate inhomogeneities and adsorbates [57]. A more reliable technique for identifying the number of layers is Raman spectroscopy.

## 3.3 Raman Spectroscopy

Raman spectroscopy gives information about the vibrational properties of a system by detecting and analyzing inelastically scattered light. The difference in energy of the illuminated monochromatic light and the scattered light stems from the excitation of phonon modes in the sample. Raman spectroscopy is a powerful tool to characterize carbon-based materials. Signature spectra of graphene have been reported both on mechanically exfoliated flakes and epitaxially grown graphene (see Fig. 3.2).

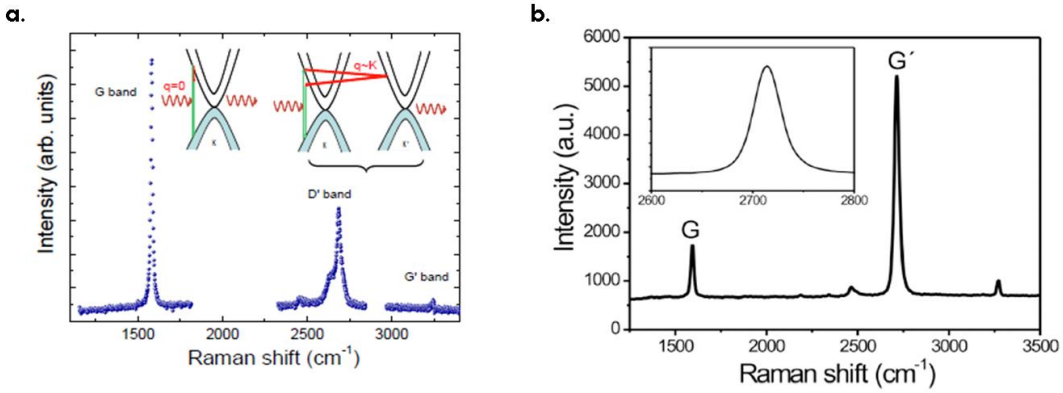


Figure 3.2: (a) Raman spectrum of a bilayer graphene and a schematic to show the scattering processes (b) Raman spectrum of a monolayer graphene.

As shown in the previous chapter, the unit cell of graphene contains two carbon atoms and hence there are six phonon dispersion bands, three of which are acoustic branches and the other three are optical phonon branches [25]. However, only a few of these modes are actually Raman active and responsible for the features in the Raman spectra. The most prominent features are found around 1580 $cm^{-1}$ and 2700 $cm^{-1}$, which are the G band and 2D (or G') band, respectively, when using a 488 nm laser excitation wavelength. The disorder band or D band is positioned at half of the frequency of the 2D band, i.e., around 1350 $cm^{-1}$.

The physical origin of these bands originates from the scattering mechanisms in the electronic band structure, when excited by the laser. Electrons with appropriate binding energy are available only in the $\pi$ bands around the K points. After excitation, the electron is inelastically scattered by a phonon of energy $E_{phonon}$. For the G band, a phonon which

is located at the Γ point of the phonon dispersion, is scattered along with the electron, so that the electron momentum remains unchanged. The electron-hole is then annihilated accompanied by the emission of the energy $E_{laser} - E_{phonon}$. This is a first-order Raman scattering process. The type of vibration of the graphene lattice is defined by the phonon dispersion. The G band is due to the doubly degenerate phonon mode and represents an in-plane vibration of the graphene lattice. The 2D and the D bands originate from second order scattering, involving the graphene phonons near the K point for the 2D band, or one graphene phonon and one defect for the D band. Both the 2D and D modes are dependent on the laser energies. Their frequencies shift upwards with increasing laser energies, though with dissimilar slopes. As shown in Fig 3.2(a), the double resonance process in case of the D and the 2D begins with the electron wave vector k around the K point, which is excited by the photon of energy $E_{laser}$. This electron is then scattered by a phonon of vector q to a point belonging to a circle around the K point. It now has a wavevector k + q. Hence, this process is termed intervalley scattering. In the next step, the electron is scattered back to a k-state and emits a photon by recombining with the hole in the k-state. In case of the D band, the two scattering events consist of one elastic scattering process by defects and one inelastic scattering event by emitting or absorbing a phonon. For the 2D band, both the processes are inelastic scattering events and two photons are involved.

Raman spectra obtained on individual graphene flakes have helped in unambiguously identifying the number of layers. The shape and distribution of the sub-peaks in the 2D band and the position of the G-band are used for performing this analysis [36]. For monolayers, the 2D peak can be fitted to a single Lorentzian, while the multiple bands in the few-layers require fitting to more Lorentzians. For bilayers in particular, the two pi bands allow for four different double resonance scattering processes. Correspondingly, the shape and distribution of the sub-peaks in the Raman 2D band, as well as the position of the Raman G-band, can be used to distinguish mono- and bilayers. [36]

The combination of AFM and Raman spectroscopy, provide reliable information about the number of layers in a graphene stack. This is required to determine the exact character of the graphene one is investigating, for its electrical character would differ accordingly. It must be noted that both these characterization tools are complementary, as AFM is notorious for unreliable height profiles when performed under ambient conditions, due to the presence of adsorbates on the tip or the surface being probed [57]. The error could be of the order of a few nanometers, thereby giving unreliable information.

After characterizing and selecting suitable graphene flakes, one then procedes to fabricate field effect transistors (FET) with graphene as conducting channel.

## 3.4 Marker-assisted electron beam lithography (EBL)

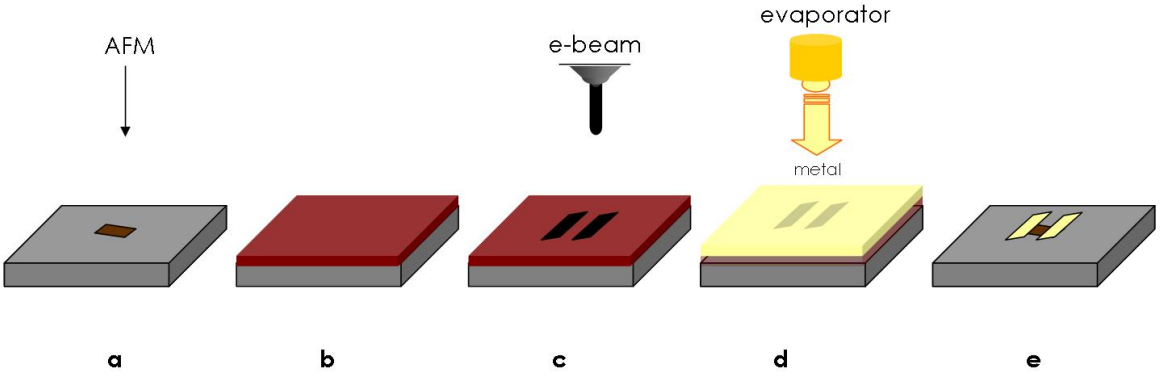


Figure 3.3: The EBL procedure represented in a schematic fashion, step-wise. (a) Characterization with AFM, (b) spincoating PMMA, (c), ebeam lithography, (d-e) evaporation and lift-off.

The FET fabrication process usually involves a marker-based electron beam lithography technique. Its application is to prepare suitable masks on the substrate, onto which desired metal is evaporated as an electrode. In this process, electron beam sensitive resist poly-methyl methacrylate (PMMA) is spin-coated onto the substrate. PMMA is a positive resist, and when exposed to an electron beam, the polymer chains would break in the exposed areas. The regions to be exposed to the electron beam are identified by using the co-ordinates of the pre-written markers on the substrate. The marker based regions, which were hitherto identified using optical and AFM techniques, help in the alignment between the electrode layout and the sample during the e-beam writing. These exposed regions can be preferentially dissolved in a suitable solvent like methyl iso-butyl ketone (MIBK). The sample is then put in a vaccuum chamber to evaporate contact metals. One could evaporate a variety of metals, but only a select few would match the purpose of near-ohmic contacts. After the evaporation of metal contacts, the PMMA is removed in a

solution of 1-methyl-2-pyrrolidone ($55^0$C, 3 hours). The procedure is summarised in Figure 3.3 and a finished graphene-based FET can be seen in Figure 3.4(a). The source and drain contacts lead to larger contact pads ( 150 micron x 150 micron) which provide the interface to external electrical probes during electrical measurements. Since the silicon on the bottom acts as gating device, this configuration is termed as "back-gated FET".

Obviously, the entire fabrication process of a graphene-based FET is a discontinuous and complementary procedure which involves various steps and instruments. In the next chapter, a novel method to fabricate such graphene devices is introduced, which involves only a single instrument. A more detailed description of lithography is also provided in that chapter.

## 3.5 Electrical Transport Measurements

The fabricated FETs are then electrically characterized in a home-made electrical transport setup. The experimental setup used for the measurements comprises a voltage source (Keithley 2400) that supplies the source-drain bias ($V_{ds}$). A home-built current-to-voltage converter is used to amplify the drain current ($I_d$) signal, before it is recorded by a multimeter (Keithley 2000). A second voltage source (Keithley 2400) is used to supply the gate-source voltage ($V_{gs}$), and to measure the leakage current ($I_g$) through the gate oxide. The current-voltage (I -V) characteristics of the samples were measured by recording $I_d$ as a function of the applied drain-source voltage. Typically, linear responses were observed at low-bias ( 1mV), where the inverse slope corresponded to the device resistance (R = 1/G, where G is conductance). By repeating this procedure at different $V_{gs}$, resistance vs. gate voltage, (R $\times$ $I_{gs}$) plots were obtained. It is important to note that, by using a two-probe configuration, the measured resistance comprises both the intrinsic resistance of the nanostructure and the contact resistance. Although four-probe measurements constitute the adequate approach to determine the intrinsic resistance of a material, they are not able to completely exclude the contact resistance in graphene devices, due to the invasiveness of metal contacts on graphene [72].

A typical two-probe backgate dependence of the graphene's resistance is shown in Fig. 3.4(b). The plot shows the typical ambipolar behaviour, with the holes contributing to the conduction in the negative voltage regime, and electrons in the positive regime. This is distinguished from most conventional semiconductors, in which the transport is exclusively due to either n-doping or p-doping. In ambient conditions, the gate dependent electrical

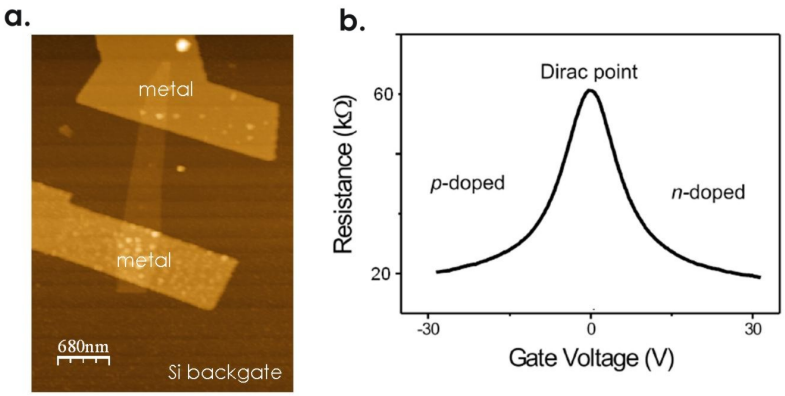


Figure 3.4: (a) AFM image of a graphene-based FET(b) The back-gate dependence plot of the FET.

response of the devices sometimes exhibits a hysteresis, whose origin has been attributed to water molecules that are bound to the $SiO_2$ surface and act as charge traps [58]. This is a typical "substrate effect" in graphene transport measurements, as discussed in section 3.1.

## 3.6 Scanning Photocurrent Microscopy

Photoconductivity can be described as a process where current is generated by the dissociation of photoexcited electron-hole pairs in a semiconductor. Experimentally, photoconductivity is usually detected by observing changes in the drain current, under applied $V_{ds}$, upon photoexcitation of a semiconducting device with a wide-field light source.

In the present spatially resolved measurements, the FET is irradiated with a diffraction-limited laser spot, while measuring the drain current as a function of the (x; y) coordinates, as shown in Figure 3.5. A commercial confocal optical microscope (Leica TCS SP2), which contains Helium−Neon (HeNe operating at 633 nm and GreNe at 543 nm) and Argon (Ar with 458 nm, 488 nm and 514.5 nm lines) lasers, was employed to provide photoexcitation. A photodiode was used to detect the reflected light, and the photocurrent signal was measured by a multimeter (Keithley 2000), after being amplified by a current-to-voltage converter. The drain current, on the other hand, was detected by a similar electrical transport system as that described in section 3.5. Two-dimensional photocurrent maps were obtained by raster-scanning the samples through the laser spot, by

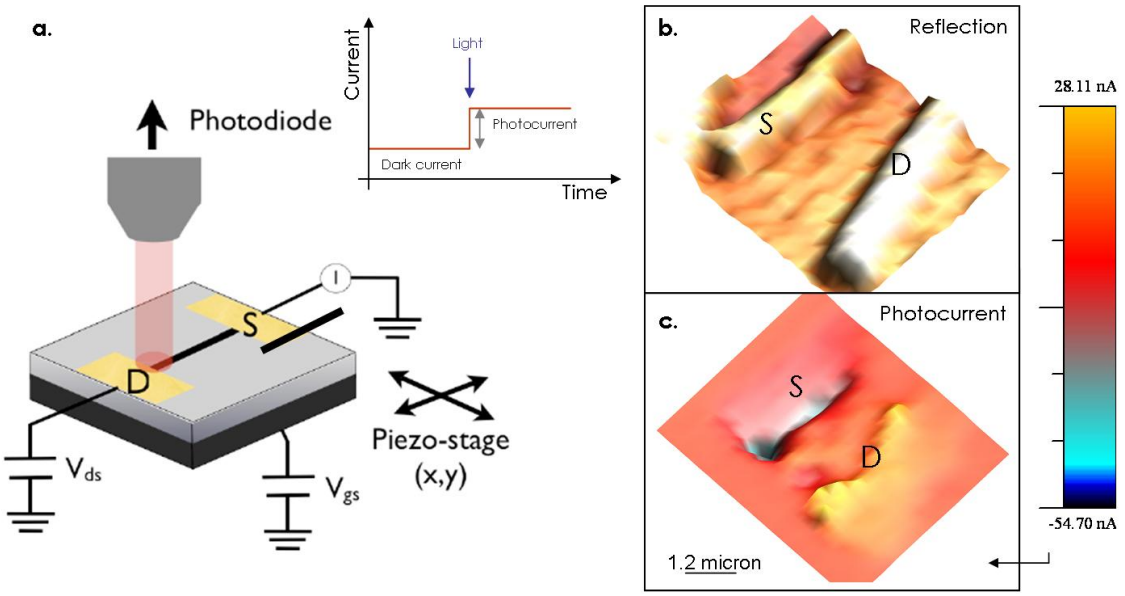


Figure 3.5: (a) Schematic representing the SPCM set-up. (b) The reflection image of a graphene-based FET. (c) The photocurrent image of the same FET recorded simultaneously.

means of a piezoelectric stage. Simultaneously acquired optical reflection images (measured at the photodiode) served to assign the photoresponses to actual positions within the devices. All measurements were performed under ambient conditions.

Fig. 3.5 (b,c) show the reflection and photocurrent images taken simultaneously on a graphene device taken at zero drain-source bias at Dirac point. As can be seen, the photocurrent signal on the sheet is weaker than at the contacts. This is due to the contacts doping the graphene sheet under them. It has been shown theoretically [75] and experimentally [72] that the difference in the work functions of the metal and the graphene leads to a charge transfer at the contact interface and pronounced interface dipole layers. Such metal-induced doping has been shown on many graphene samples - both exfoliated [72] and on SiC [80].

The photocurrent image in Fig. 3.5(c) belongs to the graphene state at charge neutrality point; it is also possible to vary the back-gate voltage and measure the photocurrent responses in different charge carrier regimes.

This technique has been previously used to probe local charge transport barriers that

arise from charge transfer at the interface to attached electrodes or from defects along the nanotubes such as intramolecular junctions [70]. Moreover, it has enabled the estimation of the electrostatic potential distribution along CNT channels in field-effect transistors [71]. More recently, this technique was applied to evaluate the impact of the electrical contacts and the sheet edges on the properties of graphene devices [72].

All the images obtained were plotted using the WSxM software [73].

# Chapter 4

# Marker-free Lithography

## 4.1 Existing Technology

Modern electronics exemplified in Fig. 4.1 contains three distinct components. The main base of the assembly is a printed circuit board (PCB), and other devices are mounted onto it. The two subassemblies include integrated circuits (ICs) and hybrid circuits. These three - PCBs, ICs and hybrid circuits are principally distinguished by the choice of substrate and by radical differences in construction methods. Recently, the individual functions of each of these have begun to blur. Designing a circuit board is one of the critical points in the industry and many companies spend considerable time designing these circuits for optimal spacial efficiency. Computer-aided design techniques are used to reduce sophisticated electronic designs (of interconnected devices) into a suite of surface processing sequences which build the structure required. Each stage requires some areas of the surface to be exposed to particle fluxes while other areas are protected. One protective medium widely used is $SiO_2$ in MOSFETs and integrated resistors are made in this method, for example.

The ICs are manufactured through a critical process known as lithography. Lithography was originally introduced in 1958 when ICs were invented, and consists of three basic parts: (1) the IC layout printer (2) photoresist tenchology and (3) the mask fabrication.

The IC layout printer can print out a desired layout of the circuitry based on the semiconductor devices available on the base. The photoresist technology involves organic polymer resists which change their solubility in specific solvents after being exposed to either photons or electrons. Mask fabrication is one of the techniques to plane out the required circuit. For example, optical images are used to define electrical circuit patterns

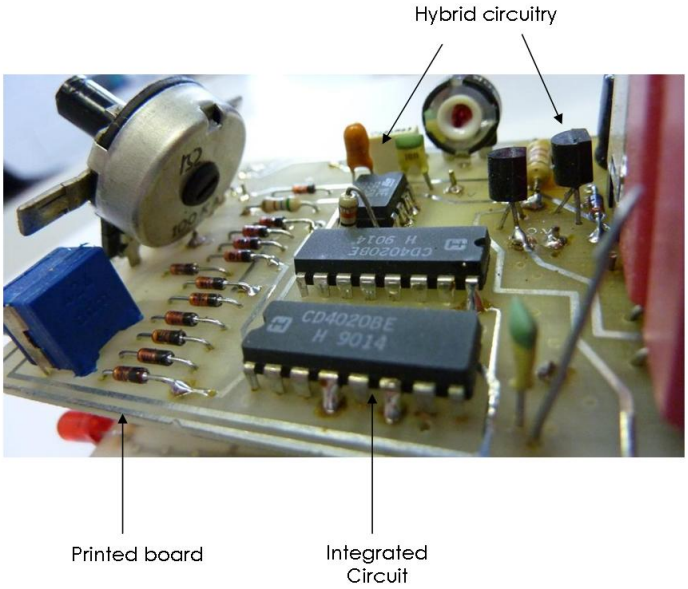


Figure 4.1: A photograph of a commonly found electronic assembly.

for printed circuit boards and screen-printed inks to define patterns of thick conducting films.

Initially, lithography used light of the visible G-line (436 nm) and the ultraviolet I-line (365 nm) from a mercury arc lamp. With the evolution of this technology and fast reducing circuit sizes, the wavelength of the exposure light had to be reduced dramatically. In the case of microtechnology, it is inherently the size of the (ultra-violet) photon which limits the lithographic capability.

**Types of Lithographies**

The polymeric photoresist material is dropped in an organic solvent at the center of the wafer. A fast spinning motion is then used to spread the droplet uniformly across the surface. A baking stage follows, to remove solvent. The surface is then illuminated with ultra-violet light through a shadow mask on, or very close to, the surface. Alternatively, the desired pattern may be projected onto the surface with UV light.

The pattern is developed in the resist by dissolving unwanted material (like uncrosslinked material in a negative resist). The same pattern is transferred into underlying $SiO_2$ by using the photoresist to protect from the etchant areas which are to remain.

Lithography can also be performed using beams of electrons or X-rays to *write* onto

the resist. Electrons can be steered using an e-beam machine (as was briefly described in the previous chapter), but X-rays are simply shaded by an absorbing mask analogous to the UV optical method.

Electron-beam resists use similar principles to photoresists, exploiting the fact that a low-molecular-weight-polymer dissolves more readily than a high-molecular-mass material. The electron beam is used to break up long chains (in case of positive resist) or else to promote cross-linking between short ones (in negative resists). In the latter case, however, the material which remains behind will take up some solvent into any regions which are incompletely cross-linked and this can lead to swelling, to the detriment of resolution.

X-ray absorption by a material kicks electrons out of atoms so "electron beam resists" can also be activated by electrons internally liberated during exposure to X-rays. Thus X-ray resists are no different.

This is the general fabrication procedure for making microstructures on the the printed board and ICs. A collective set of structures contribute towards various materials on the circuit board which act as resistors, semiconductors, amplifiers and logical components, which need to be assembled. The dream though is to have an all-carbon circuit board, where graphene, amorphous carbon or graphite could each play an independent role. This is still a far-off vision, but scientists have started to approach this goal.

A major boost to such a vision has been the recent invention of mass-scale graphene production technique [32]. Hong and co-workers grew their graphene by chemical vapour deposition (CVD) of carbon atoms (supplied by decomposing $CH_4$ at high temperature) onto copper foils, and used a roll-to-roll technique similar to a newspaper printing press to transfer the graphene between different substrates. They also performed a comprehensive characterization to demonstrate the excellent quality of their graphene, particularly as a transparent conductor that is also ultrathin and highly flexible.

## 4.2 Photolithography on Graphene

In order to develop graphene into an application-relevant material, it is important to realize the capability of large scale production of graphene devices. Until now, e-beam lithography (EBL) has been the main method used for the fabrication of prototype graphene devices. However, since EBL is not easily scalable and a sequential process, graphene devices like many other nanoscale devices suffer from limitated industrial acceptability.

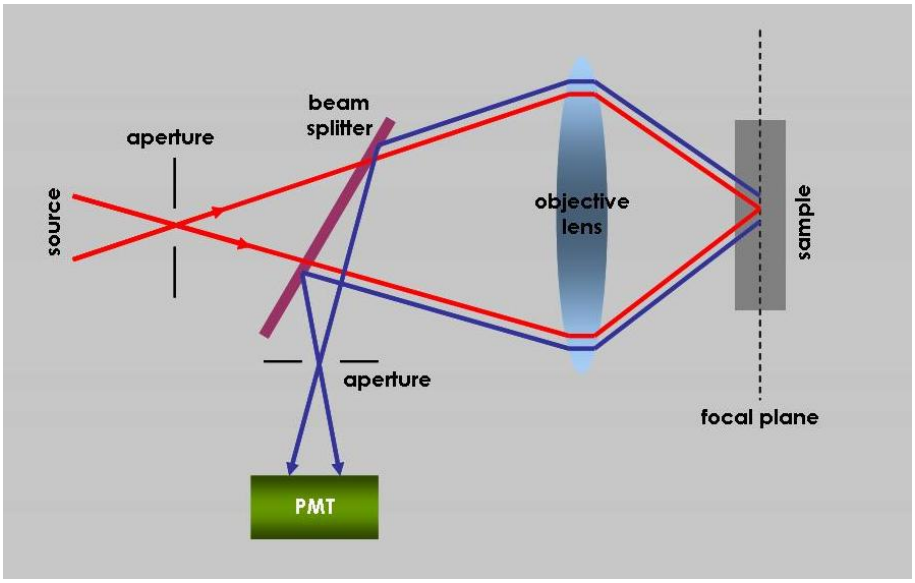


Figure 4.2: A schematic depiction of components of a Confocal Microscope.

Current methods described in the previous chapter, require the identification of graphene with the help of markers on a substrate, followed by subsequent deposition of electrodes, thereby requiring at least two steps of EBL, one of which involves a manual alignment procedure. The identification is performed using an optical microscope and a specified oxide thickness is necessary for obtaining the optimal contrast. Here, we demonstrate a novel strategy involving just a single process step, without the use of markers. The graphene flakes are identified and the devices are fabricated on-the-fly using a confocal laser scanning microscope.

**How does confocal microscopy work?**

In conventional optical microscopes, a global light source is used to illuminate the specimen, and hence the resulting image contains information of both the in-focus and out-of-focus regions. Confocal microscopy emerged as an alternative method, where the out-of-focus reflected light is suppressed, thus leading to a degree of enhancement in the optical resolution. Figure 4.2 schematically illustrates the principle of a confocal microscope. Specimen illumination is provided by a diffraction-limited laser spot, which is focused onto the sample by a high numerical aperture objective lens. The reflected light is recollected by the objective lens, before it is redirected by a beam splitter through a pinhole aperture and to a photodetector, such as a photomultiplier tube (PMT). The detector (pinhole) aperture leads to the filtering of out-of-focus information, by obstructing

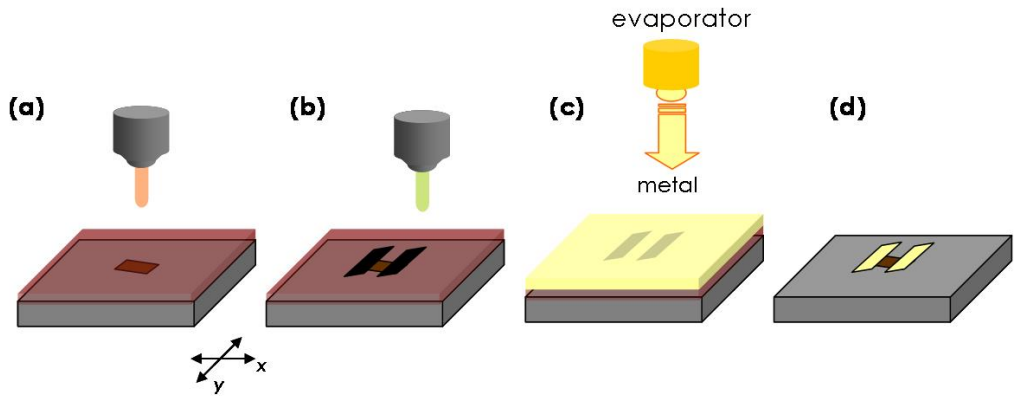


Figure 4.3: A schematic describing the steps involved in our fabrication process of a graphen-FET using photolithography.

light that does not come from the focal point. Since the signal detected at the PMT corresponds to light reflected from the small volume of the laser spot, complete images are only obtained by scanning the sample with respect to the light source. This can be achieved by either (i) moving the laser spot with scanning mirrors, or (ii) raster-scanning the sample via a piezoelectric stage. In this work, we used a confocal microscope to perform lithography.

### *in-situ* Lithography

The graphene flakes were prepared by exfoliation of HOPG and then transferred onto a silicon wafer (highly p-doped) with a thermally grown 300 nm $SiO_2$ serving as the insulating gate dielectric. Such transfer can also be performed with sheets grown from silicon carbide [37], or chemically derived graphene sheets [35]. Hence, the procedure outlined here can be adopted to all sources of graphene sheets, *fabricated in any manner and on any substrate.*

Figure 4.3 shows a schematic describing the steps involved in our fabrication process starting from an exfoliated graphene sheet on the $Si/SiO_2$ substrate (Figure 4.2(a)). The substrate is spin-coated with a photoresist (ma-P1215, micro resist technology GmbH) and baked to obtain a 1.5 mm thick film. ma-P1215 is a G- or I-line photoresist [38] with absorption maxima close to 436 nm or 365 nm. Illumination by UV light induces chemical changes in the resist increasing the solubility of the exposed areas [39], which

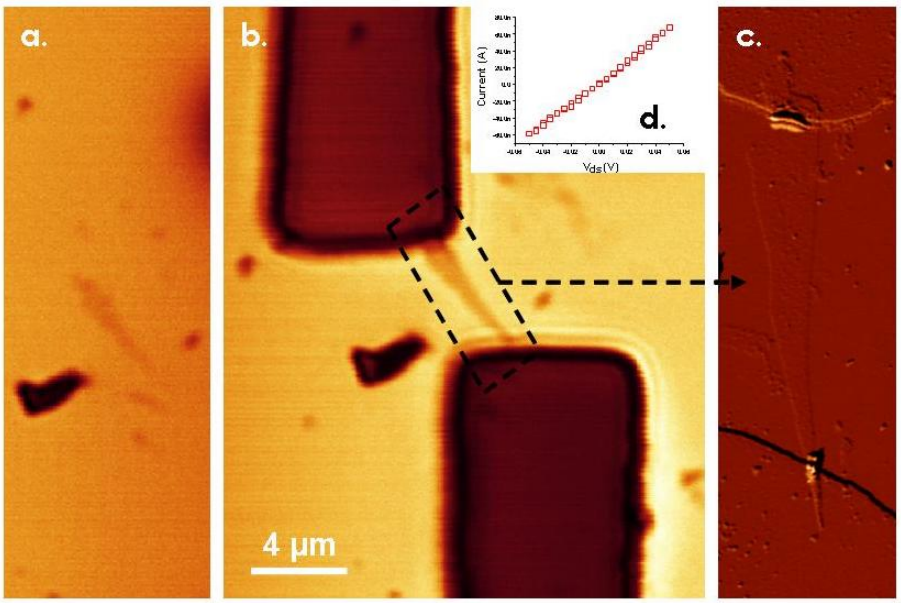


Figure 4.4: Confocal reflection images during various steps of fabrication. The I-V curve shows a linear behaviour, indicating good Ohmic behaviour.

can be preferentially stripped off by dissolution in an appropriate developer solution (ma-D331, micro resist GmbH). A subsequent metal evaporation step and a lift-off procedure finalize the device fabrication providing metal regions only in the exposed areas. Usually, a mask is used to specify the layout of the electrodes. Although m-aP1215 is designed for UV exposure, we have observed that the coated resist still possesses a sizeable molar absorption coefficient up to visible wavelengths of around 580 nm. Chemical modifications can still be induced by irradiating with low energy laser sources. We exploit this property to devise a fabrication protocol, wherein the exposure is performed at a wavelength of 476 nm (write laser) instead of UV light. On the other hand, at a wavelength of 633 nm (imaging laser), the sample can be imaged without chemically modifiying the photoresist. Thus obtained confocal images enable identifying the flakes as depicted in Figure 4.3b. After the flake is identified, the write laser is utilized to perform the exposure. The desired layout is obtained by scanning the piezo stage using a computer controlled interface, avoiding the need for a separate mask. After a development step the desired metal is evaporated onto the sample (Figure 4.3(c)). The procedure is completed (Figure 4.3(d)) by removing the residual photoresist by lift-off in 1-methyl-2-pyrrolidone ($55^oC$ for 3 hours), thus yielding a graphene-based transistor.

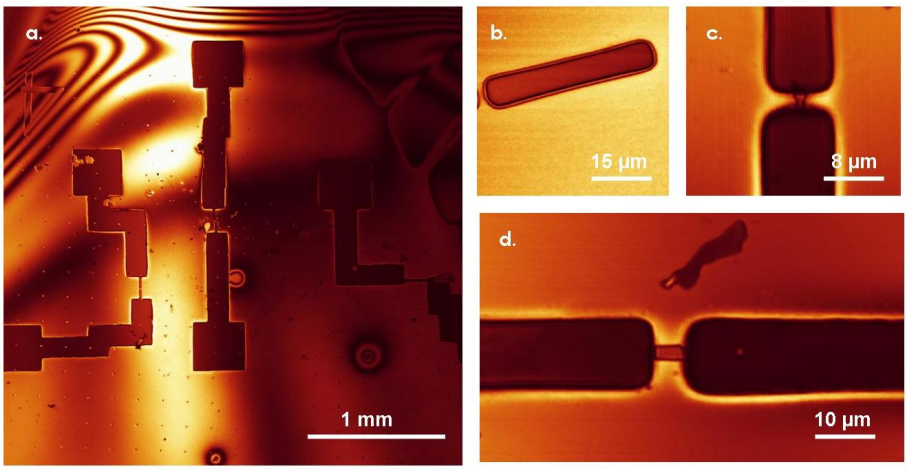


Figure 4.5: Confocal reflection images showing different sizes of exposure.

Figure 4.4 shows a representative sample prepared using the fabrication procedure described above. Figure 4.4a depicts a confocal image (recorded using the imaging laser) of the sample after deposition of the photoresist, where the graphene flake to be contacted is identified. After imprinting the desired structure using the write laser, the sample is developed in a ma-D331 solution. The etched areas are distinctly seen in Figure 4.4b. Figure 4.4c displays an atomic force microscope (AFM) image of the final graphene device after the deposition of metal (1 nm Ti / 10 nm Au) and by lift-off. The gap between the electrodes is around 4 micrometer, which can be adjusted according to the required transport channel. Although this would suffice for most common applications, some of the more demanding applications require sub-micron gaps between electrodes. This may easily be obtained by optimizing the fabrication procedure and using an appropriate high resolution photoresist [38]. In addition, the chemical structure of the resist can be optimized for the wavelength of the write laser. Alternative scanning techniques such as near field microscopy promise a resolution below the diffraction limit as low as 50 nm, with some compromise for speed [40].

Fig.4.5(a-d) show confocal reflection images of the windows of varying sizes opened in the photoresist, before metallization. The graphene flakes are clearly visible in Fig.4.5(c) and Fig.4.5(d).

**Fluorescence quenching based identification of graphene layers**

While we have demonstrated the convenient one-step device fabrication using just the

confocal microscope and without the employment of markers, there is another important task. The majority of the graphene preparation methods reported until now yield a distribution of sheets with varying number of layers. This holds also for the well-cited roll-to-roll production technique [32] has exhibited the propensity to have a distribution of layer thicknesses. Hence, before contacting it is important to identify the number of layers in the graphene flake of interest. While AFM is helpful to a certain extent in estimating the height as shown in the profile in Figure 4.6(c), it is difficult to assert the number of layers using this technique due to the influence of substrate inhomogeneities and adsorbates [57]. A more reliable technique is local Raman spectroscopy (described in Chapter 3), which however requires additional equipment, and the recording of Raman spectrum is a time consuming step. Here, we propose an alternative simple method for identification that does not require any additional equipment.

This method is based on the observation that the fluorescence from the photoresist is quenched in the presence of graphene [42], analogous to observations made on carbon nanotubes [43]. This is already apparent in the confocal images shown in Figure 4.6. The extent of fluorescence quenching is found to be proportional to the number of layers in the graphene flake. This is clear from the confocal image shown in Figure 4.7a, where it can be seen that the recorded fluorescence intensity is lower on the flakes with respect to the background. Three regions of interest have been identified as monolayer, bilayer and multilayer flakes with the help of Raman spectra recorded independently (Figure 4.7(b)). Figure 4.7(c) shows a histogram of the fluorescence intensities from the three regions in addition to the background intensity. It can be seen that the intensity is maximum on the substrate and goes down sequentially for single, bi and multi layers. From this a normalized calibration plot can be derived as shown in Figure 4.7(d), which can be used to determine the number of layers in any flake.

Based on the foregoing discussions and the presented results, we propose a strategy for the fabrication of graphene devices on a wafer-scale. This is summarized in Figure 4.8, where we start with a $Si/SiO_2$ wafer containing graphene flakes obtained by any production method of choice. Following this, the wafer is coated with a photoresist and loaded into the confocal microscope. The whole wafer or a sub-region is then scanned using the imaging laser (633 nm) and graphene flakes identified by image segmentation techniques [44]. With the help of calibration plots as shown in Figure 4.7c, the number of layers in every flake is estimated. The identification of the flakes and the estimation of the number of layers can be easily automated with standard image processing algorithms [45].

At this stage, a standard or a user-specified layout can be produced by using the write laser (488 nm). Subsequently, the exposed wafer is developed, metal is evaporated and the resist lifted-off to obtain the final wafer with the desired devices or circuits with minimal user intervention. This whole procedure can be carried out in a closed sequence. At a lab scale, we conservatively estimated that within an hour, up to 20 flakes can be detected (accounting for a 1:100 probability of finding the desired flake) and the associated layout could be prepared. In comparison to current procedures which require elaborate search, alignment and verification of the number of layers, this technique provides an improvement in throughput of at least one order of magnitude.

Although the substrate used in this specific case was $Si/SiO_2$, it can be replaced with more flexible substrates like Kapton, a polymide film used in flexible electronics. Figure

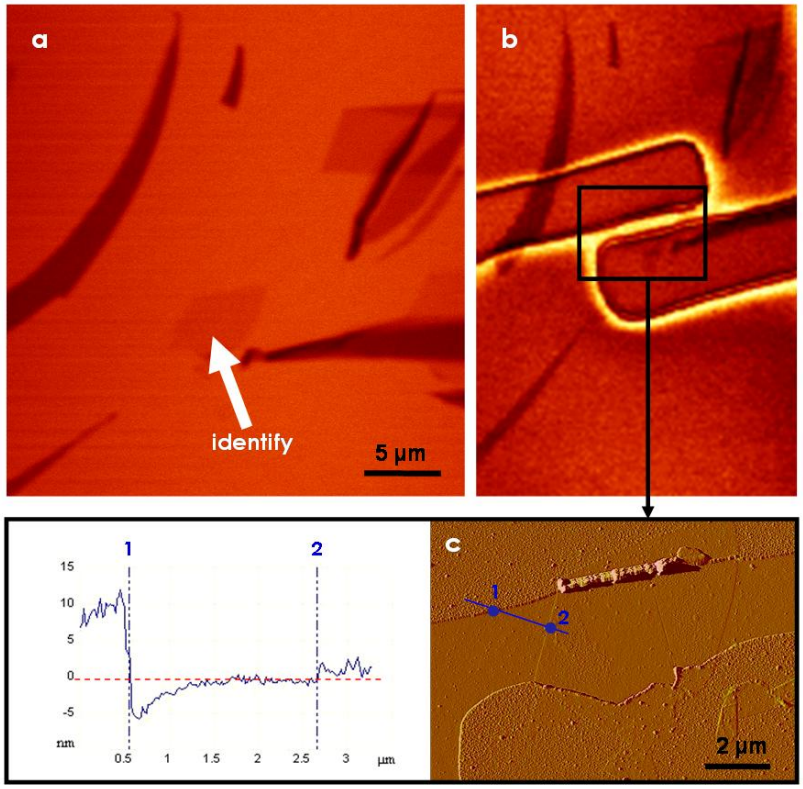


Figure 4.6: Confocal reflection images exhibiting varied height distribution of graphene flakes. Here a monolayer graphene is (a) identified by read laser, (b) exposed by write laser, and subsequently fabricated into a FET. (c) AFM image of the graphene FET, with the height profile.

4.9 shows the confocal images of exfoliated graphene on Kapton. It should be remarked that exfoliation was found to be much more difficult on Kapton owing to its charged surface, and additional functionalisation was required. (The substrate was silanized in 2 weight percent di-amino silane.) Due to the concerns expressed regarding the "substrate effect" in the previous chapter (and the next), we did not do extensive fabrication on Kapton substrates during this period. CVD grown graphene films would serve as a better alternative in our opinion.

In Table 2, a comparison is made between the proposed method of fabrication and the existing e-beam lithography technique (which has yielded hundreds of samples to our group in the last few years).

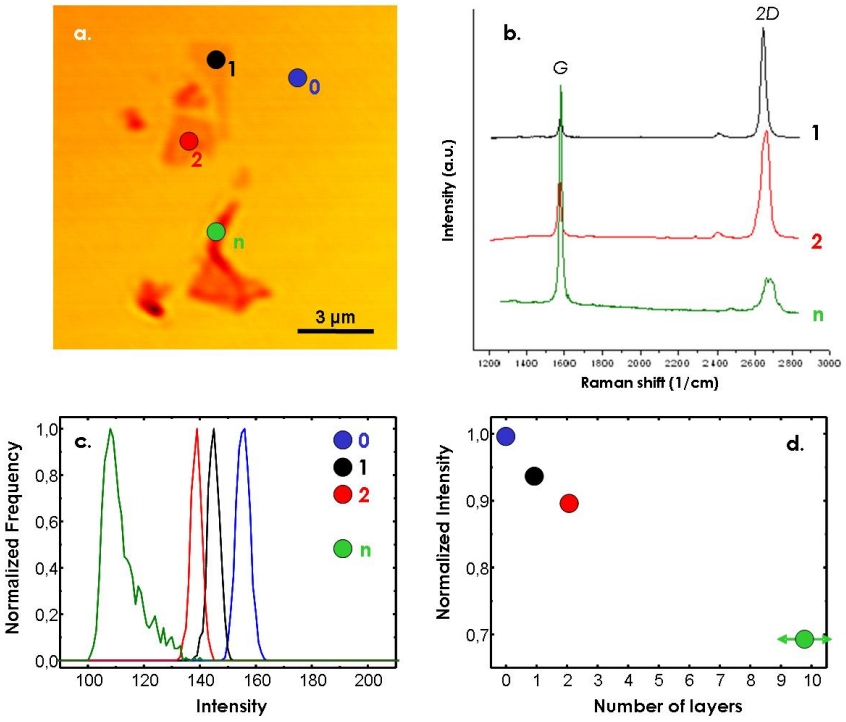


Figure 4.7: Identification of heights of graphene flakes using a calibration system.

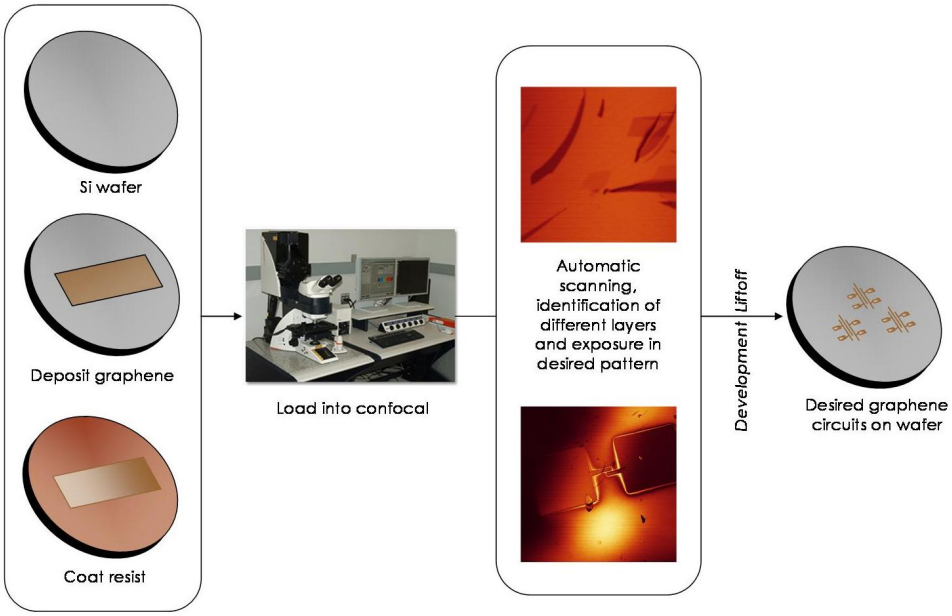


Figure 4.8: A strategy for the fabrication of graphene devices on a wafer-scale.

| Operation | e-beam lithography | Our proposed method |
|---|---|---|
| Preparation of alignment markers on substrate | Critical | Not required |
| Identification of flakes | Dependent on Raman spectroscopy | In situ while fabrication |
| Raman spectroscopy | Required (a disconnected step/instrument). | Not required |
| Resist coating | Required | Required |
| Designing the layout for fabrication of device | Comparable | Comparable (unless automated) |
| Lithography session time per sample | Limited by alignment markers per sample* | Independent of markers and hence more delocalized fabrication area enabled* |
| Lift-off | Required | Required |

Table 2: Comparison between current lithography techniques on graphene.

* For a sample with 4 flakes to be contacted, an e-beam session requires a minimum of 20 min to load/unload the sample into a vacuum chamber, and additional 20 min to align the markers. The exposure time is usually less than 10 min. This amounts to a total of approximately 50 minutes for 4 devices (on one substrate). Not to mention, the steps preceding the lithography (refer table). In comparison, the same 4 flakes on that substrate

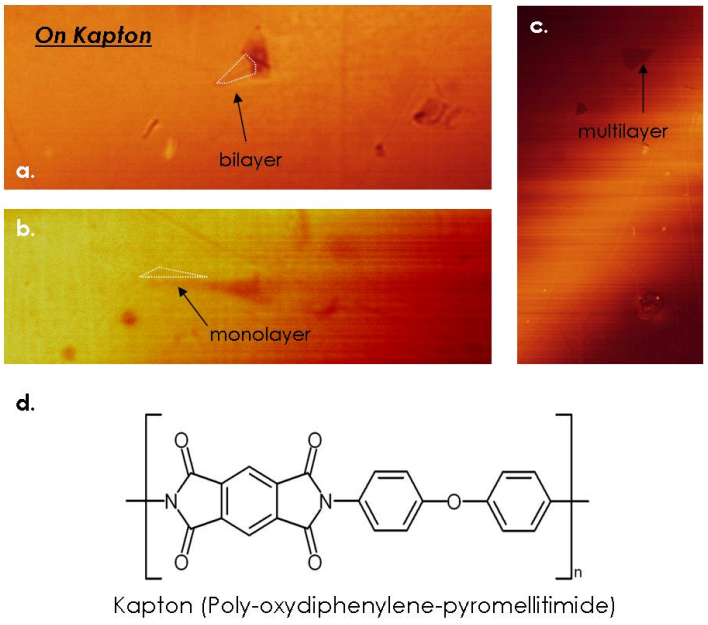


Figure 4.9: (a), (b), (c) Confocal reflection images of exfoliated graphene on Kapton, exhibiting a distribution of heights. (d)Kapton molecule.

in our lithography session which is done in ambient conditions requires only 10 minutes or less.

# Chapter 5

# Stacking Order in Bilayers

## 5.1 Electronic Structure Bilayer Graphene

As described in Chapter 2, the lattice of graphene consists of two equivalent interpenetrating triangular carbon sublattices A and B, each one containing a half of the carbon atoms. Each atom within a single plane has three nearest neighbors: the sites of one sublattice (atoms of sublattice A are marked by red) are at the centers of triangles defined by three nearest neighbors of the other one (B sublattice atoms are marked by blue). The lattice of graphene thus has two carbon atoms, designated A and B, per unit cell, and is invariant under $120^o$ rotation around any lattice site. Network of carbon atoms connected by the shortest bonds looks like a honeycomb. In bilayer graphene by contrast, carbon atoms at sites, A and B become inequivalent; two coupled hexagonal lattices on the neighboring graphene sheets are arranged according to Bernal ABAB stacking, when every A-type atom in the upper (surface) layer is located directly above an A-type atom in the adjacent lower layer, whereas B-type atoms do not lie directly below or above an atom in the other layer, but sit over a void i.e. a center of a hexagon. Figure 5.1 illustrates the assumed non-equivalent types of carbon atoms. Thus in each layer the atoms form a grid of hexagons with distances between atoms equal 0.14 nm. The distance between layers is equal 0.34 nm.

It follows that bilayer graphene (BLG) has the same hexagonal lattice as the monolayer, but has four atoms per unit cell - A, B from the top layer and A', B' from the bottom layer. As a result, the dispersion curve contains four bands. The overlap integral between these two sites (i.e. A' and B) is denoted by $\gamma_1$ and equals 0.3 eV [19]. Around the K points, the pairs A'- B repel each other and form the two higher energy bands.

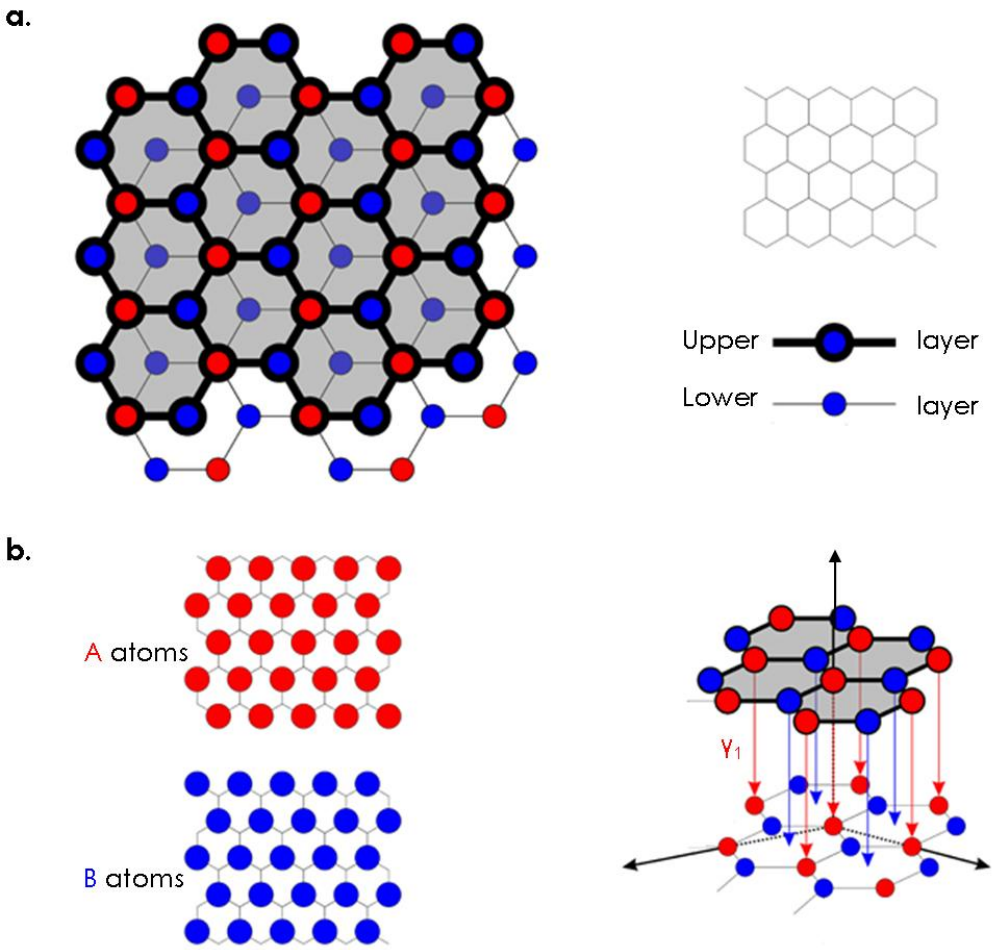


Figure 5.1: (a) Schematic representing the hexagonal graphene lattice, which is formed by two sublattices of inequivalent carbon atoms A and B. (b) The two layers in a bilayer graphene (BLG).

These higher energy bands are of the order of 300 meV ($\gamma_1$ as shown in in Figure 5.1(b)) away from Dirac point and can be neglected for low energy transport. Electrons hop between the two sites A-B' via the A-B' dimer and form the two lower energy bands (the direct overlap integral between A-B' sites $\gamma_3$ is much smaller and can be neglected). The two-component spinor for BLG is thus formed by the wavefunctions of the A and B' sublattices. The two sublattices for BLG are on two separate layers.

The dispersion relation for BLG is decribed by Equation 5.1 [63]:

$$E^2_{+-}(p) = \nu_F^2 p^2 + \gamma_1^2 + V^2/4 +_- \sqrt{\gamma_1^4/4 + (\gamma_1^2 + V^2)\nu_F^2 p^2} \tag{5.1}$$

where the + sign gives the higher energy bands and the - sign gives the lower energy bands. V is the on-site potential difference between the two sublattices A and B'.

The band structure of BLG around one K point is based on Equation 5.1. When the bias V is zero (the top and bottom layers are symmetric), the spectrum is parabolic and the conduction and valence bands are dgenerate at the K points. The effective mass of symmetric BLG is $m* = \gamma_1/2v_F^2 = 0.03m_0$ [63].

The Bernal stacking is well studied and understood since it is the building block for more ordered pyrolitic graphite (HOPG), which is a collection of such Bernal stacks. Recently, theory predicted semiconducting properties [64] of such stacks in case one of the two layers gets misaligned or twisted [82]. The introduction of rotational stacking faults in such Bernal stacks reverts the dispersion relation back from parabolic to linear, corrsponding to a more monolayer-like behaviour. Very recently, the same has been confirmed [83] using high magnetic field scanning tunneling microscopy and Landau level spectroscopy.

## 5.2 Effect of Stacking Order on Gating

A rotational stacking disorder on a bilayer cannot be detected by an optical microscope. However, using an AFM to gauge the height of the bilayer and the respective Raman spectra [84, 85], such rotational stacking disorder can be identified.

The influence of the stacking order in bilayer graphene enables one to understand some of the critical aspects of graphene transport - specifically the substrate influence and electrostatic decoupling within layers. In this study, we consider two kinds of bilayers which differ in stacking orders. As mentioned above, Bernal stacking (ABAB) is the natural form of occurrence in graphitic allotropes. A simple Bernal stack is shown in Figure 5.1. Rotation of one of the two layers about the c-axis results in a so-called misoriented bilayer. When similar rotational faults occur in three or more layers of graphene, they are termed twisted graphene. [82,83] It is, however, very difficult to fabricate such misoriented bilayers with known degree of rotation.

In the present thesis, such bilayers were identified among a host of other bilayers using the characterization techniques mentioned above. Bernal-stacked and misoriented bilay-

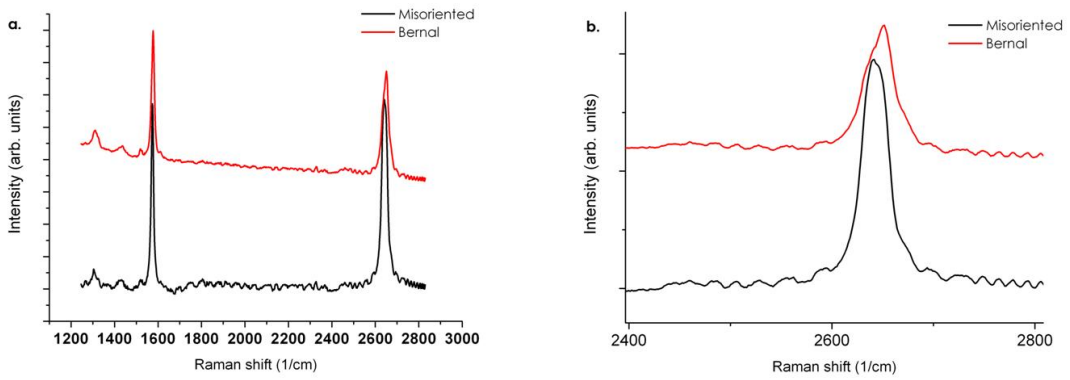


Figure 5.2: (a) Raman spectrum of the two kinds of bilayers under the 633 nm laser incidence (inset) (b) Closer view of the 2D peaks.

ers were prepared by mechanical exfoliation of highly oriented pyrolytic graphite (HOPG) on Si substrates covered by 300 nm of thermally grown $SiO_2$. The two types of sheets were located by optical microscopy and atomic force microscopy, and then distinguished by Raman spectroscopy (Figure 5.2). Electrical contacts were then defined by standard e-beam lithography, followed by evaporation of Ti (0.3 nm)/Au (15 nm) for the source and drain contacts. The degenerately doped Si substrate was used as a backgate during the electrical measurements performed under ambient. The transfer (resistance vs. gate voltage) curves obtained from a Bernal-type and a misoriented bilayer sample are compared in Figure 5.3. While in both cases ambipolar behavior is observed, the Bernal-stacked samples exhibited a broad minimum conductance which can be attributed to the chemical interaction with the underlying substrate [66]. In contrast, the measured gate dependent resistance of a misoriented bilayer devices on the same substrate closely resembled the response of monolayer graphene devices, featuring a narrow transition from the p- to the n-type regimes. This finding is consistent with theoretical and experimental studies, according to which misoriented bilayers retain the linear energy dispersion of monolayer graphene and the two monolayers behave as electrically independent systems contacted in parallel [69]. As a consequence, the back-gate dependent electrical transport characteristic is dominated by the bottom layer, wherein the carrier density is roughly seven times larger than in the top layer [65].

In order to explore the potential profiles in the two types of devices as a function of the

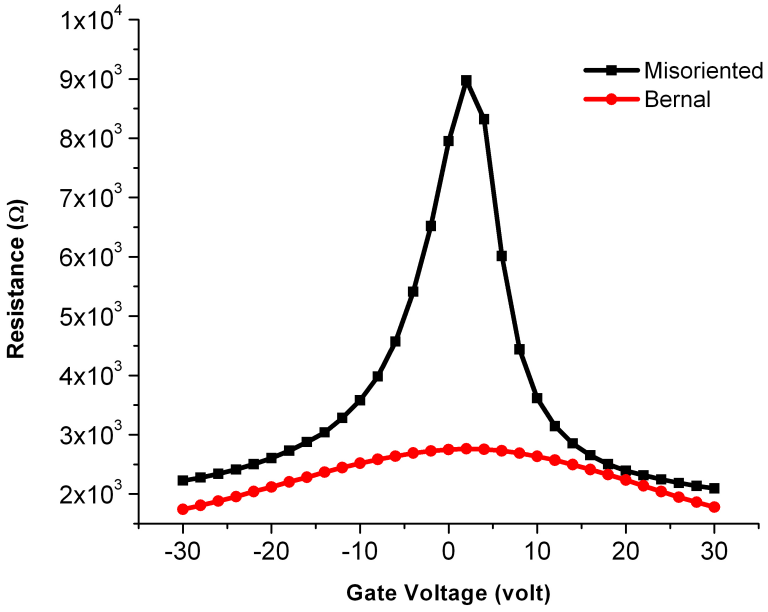


Figure 5.3: (a) Plots of electrical resistance vs backgate voltage acquired from a misoriented (black curve) and a Bernal stacked (red curve) bilayer device at room temperature.

backgate potential, we used Scanning Photocurrent Microscopy (SPCM). This technique has previously been applied to evaluate the electrostatic potential distribution in carbon nanotube [70,71] and monolayer graphene devices [72,74]. The SPCM measurements were carried out by recording the short-circuit photocurrent generated through local illumination by a diffraction-limited laser spot ( 400 nm diameter, 514 nm wavelength, power 100 $kWcm^{-2}$).

Figure 5.4 shows an AFM image and the corresponding zero-bias photocurrent maps of a Bernal stacked bilayer in the p- and n-type transport regimes. It is apparent that the photocurrent response is dominated by strong signals located around the electrode edges. These signals invert polarity when the devices are switched from the p- to the n-type regime. Such behavior is similar to that previously reported for monolayer graphene devices, and can be attributed to gate-dependent potential steps at the metal/graphene interfaces [72]. By contrast, the photocurrent signals close to the contacts in misoriented bilayer devices as seen in Figure 5.5 are only weakly affected by the backgate voltage

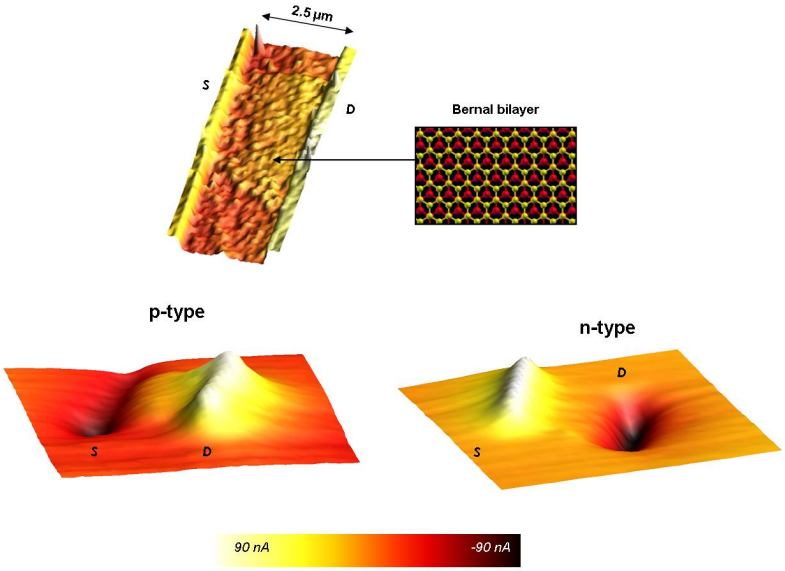


Figure 5.4: AFM image of a Bernal stacked bilayer contacted with Ti/Au electrodes, where S is the source and D is the drain (top), and three-dimensional (3D) plots of the photocurrent responses of the device in the p- and n-type regimes (bottom).

($V_{gs}$), in particular they do not invert sign even in high carrier density regimes, 30 V away from Dirac point.

To determine the origin of this difference, we compare the experimental back-gate modulated photocurrent responses at the contacts with model calculations based upon the respective dispersion relations expected for the two types of bilayers. The photocurrents measured while the laser spot was fixed directly at the metal/graphene interfaces are plotted in Figure 5.6 against the applied back-gate voltage. In close correspondence to the photocurrent maps in Figure 5.4 the contact signals in the Bernal-stacked device are seen to invert sign upon gate modulation, whereas no such change occurs in the misoriented bilayer device.

Figure 5.7(a) displays the schematic cross-section of a bilayer graphene device, wherein the graphene region underneath the electrical contacts is denoted as contact region graphene (C), and the device channel is referred to as flake (F). According to theory, the difference between the work functions of the metal ($\phi_m$) and graphene ($\phi_g$) leads to charge transfer

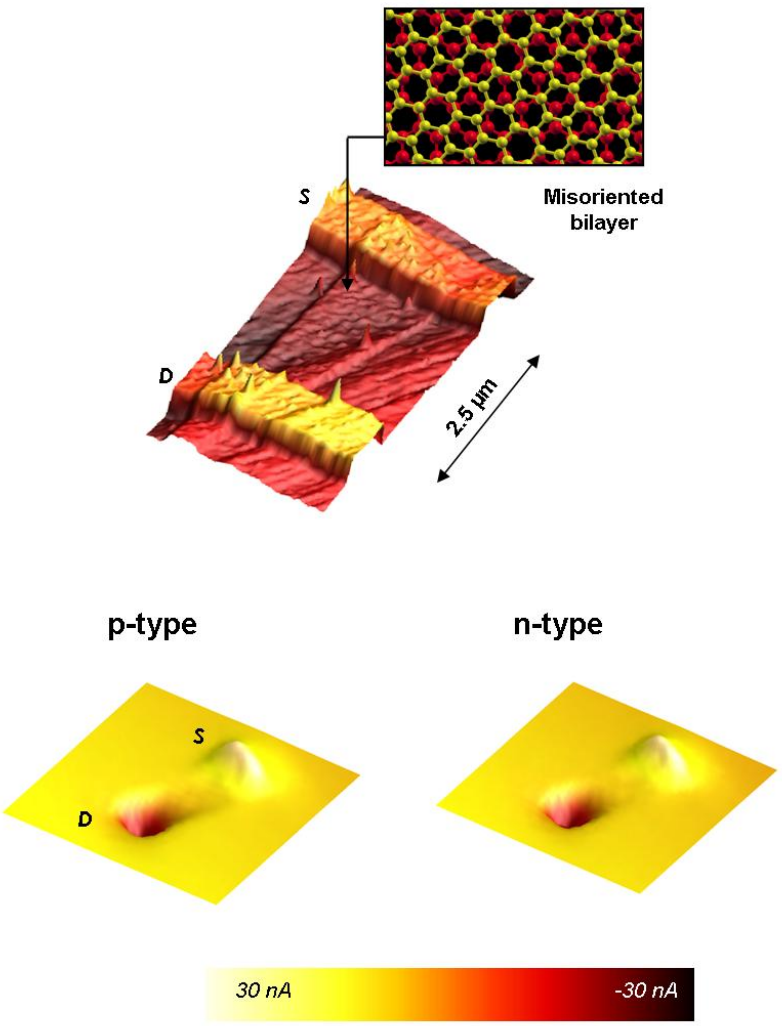


Figure 5.5: AFM image of a misoriented bilayer device (top) and corresponding 3D plots of the photocurrent responses in the p- and n-type regimes (bottom).

at the contact region, associated with a shift of the Fermi level with respect to the Dirac point ($\Delta E_F^{doping}$) [75] as depicted in figure 5.7(b). It has furthermore been demonstrated that Au contacts p-dope the underlying contact region, where the charge carrier concentration n remains largely unaffected by the gate [74]. Thus, a potential step ($\Delta V$) results at the interface between the contact region (C) and the device channel (F), whose magnitude is strongly dependent on the carrier density in the channel, which obeys the

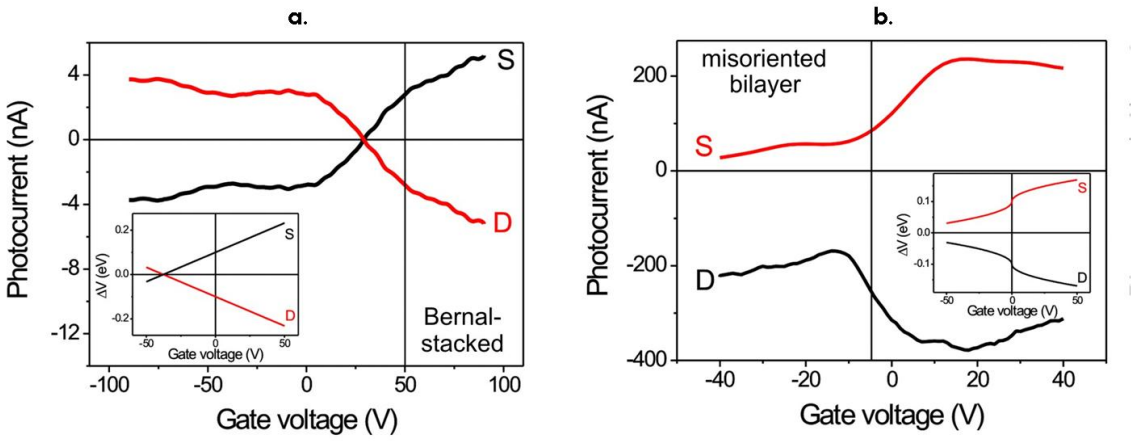


Figure 5.6: (a) Comparison between experimental and calculated data obtained for the photocurrent responses at the contacts upon sweeping the back-gate voltages, with S and D respectively denoting source and drain in the devices. (a) In the Bernal stacked bilayer device, the signals invert polarity between the p- and n-type regimes. The inset shows the gate dependence calculated using Eq. 5.3 in the text. (b) The misoriented bilayer device does not show polarity inversion at the contacts. The inset depicts the dependence calculated based upon Eq. 5.4 in the text.

relation $n = \alpha V_{gs}$ ($\alpha$ being the gate coupling parameter). Accordingly, the gate dependent potential step can be generally expressed by:

$$\Delta V = -\Delta E_F^{doping} - f(V_{gs}) = -(\phi - \phi_g - \Delta W) - f(V_{gs}) \tag{5.2}$$

where $f(V_{gs})$ represents the electrostatic doping Fermi level shift in the graphene channel as a function of the gate voltage, and $\Delta$W is the potential step at the interface between the metal contacts and the underlying graphene.

On the basis of equation 5.2 the experimentally determined back-gate modulation of the contact potential step $\Delta$V can be effectively predicted for both types of bilayers. For the Bernal-stacked graphene bilayer, insertion of the parabolic energy dispersion $E_k = +\text{-}\hbar^2k^2/(2m^*)$, with the effective mass $m^* = 0.033m_e$ and $k_F = \sqrt{\pi n}$, yields the following relation for the potential step:

$$\Delta V = -\Delta E_F^{doping} - \frac{\pi\hbar^2}{2m^*}\alpha(V_{gs} - V_{gs}^{Dirac}) \tag{5.3}$$

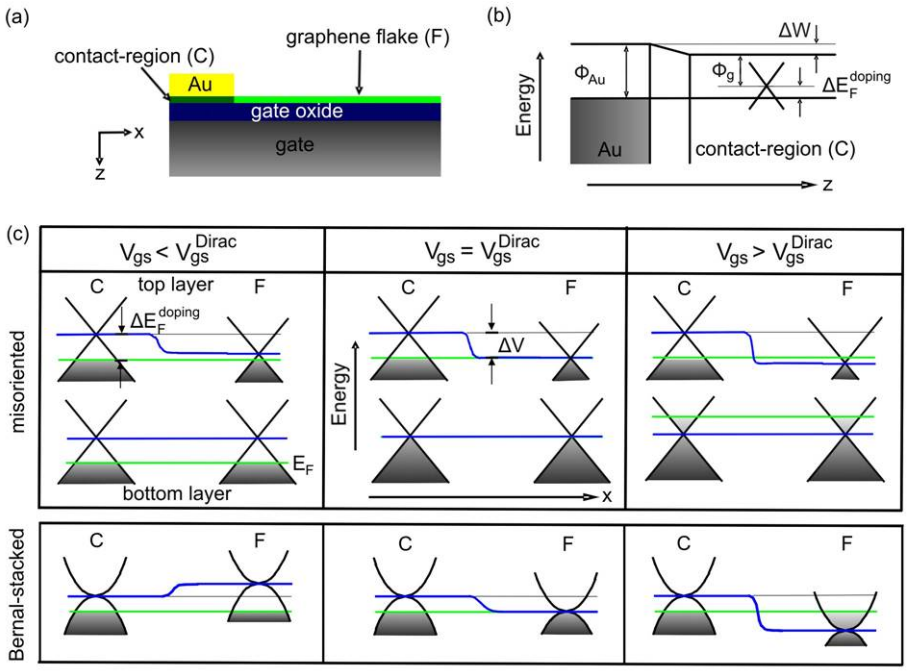


Figure 5.7: (a) Schematic cross-section of a bilayer graphene device, wherein the graphene region underneath the electrical contacts is denoted as contact region graphene C, and the device channel is referred to as flake F. (b) An energy band diagram of the device. (c) Schematic representation of the potential profile changes induced by back-gating in the two types of devices.

where $\alpha$ = 7.3 x $10^{10} cm^{-2} V^{-1}$ [76]. The corresponding linear plots obtained with $\phi_m$ = 4.7 eV, $\phi_g$ = 4.5 eV, and $\Delta E_F^{doping}$ = 0.1eV agree well with the measured data (see inset Figure 5.5(a)), except for the high carrier concentration regimes, where the experimental curves show photocurrent saturation that generally occurs for high electric fields at metal-semiconductor junctions [77] due to the exhaustion of photoexcited charge carriers. The overall gate-induced changes are schematically illustrated in Figure 5.7 (c, bottom panel), from which it is apparent that a negative gate voltage is able to balance the carrier concentration between the contact and the channel, thereby inverting the negative contact potential steps at the Dirac point. In case of the misoriented bilayers, agreement between the potential step model and the experimental data requires assuming that due to decoupling of the layers, only the top layer experiences metal contact doping (Figure 5.6(c), top panel). In this manner, the contact region graphene in the bottom layer remains unaffected by the metal contacts, and consequently its carrier density varies

together with that of the graphene channel. The contact potential step then mostly resides within the top layer, which can be similarly described as in monolayer graphene devices. In order to take into account that screening by the bottom layer should reduce the electrostatic coupling of the backgate, an effective gate coupling parameter $\alpha_{eff}$ is included in relation for the potential step within the top layer:

$$\Delta V = -\Delta E_F^{doping} - sgn(V_{gs} - V_{gs}^{Dirac})\hbar|\nu_F|\sqrt{\pi\alpha_{eff}}\sqrt{V_{gs} - V_{gs}^{Dirac}} \tag{5.4}$$

For further evaluation, we use $\alpha_{eff}$ = 1 x $10^{10} cm^{-2}V^{-1}$, a value obtained by fitting the experimental data [65] with the relation $n = V_{gs}$. Thus gained plots (inset of Figure 5.5(b)) reproduce the measured curves, including the absence of sign inversion of the potential step, and display a significantly slower modulation compared to the Bernal-stacked bilayers when all other parameters are kept constant.

The electronic decoupling in misoriented bilayer graphene provides a suitable basis for selectively controlling the charge carrier density within the layer farther from the substrate. One could employ a top gating configuration on such a device to exploit this property. We addressed this task by a polymer electrolyte gate consisting of poly-ethyl oxide (PEO) and lithium perchlorate ($LiClO_4$) on top of the conducting channel (Figure 5.8(a)), following a previously established approach for other carbon based devices [78,79]. Compared to the Si backgate, the polymer electrolyte enables more effective gating of the conducting channel, as apparent from the transfer characteristics compared in Figure 5.8b.

**How does the polymer electrolyte gate work?**

In order to compare such a top-gating with the usual back-gating measurements, it is necessary to convert the top-gate voltage into an effective doping concentration. In general, the application of a gate voltage ($V_g$) creates an electrostatic potential difference between the graphene and the gate electrode, and the induced charge carriers lead to a shift in the Fermi level ($E_f$). Therefore, $V_g$ is given by

$$V_g = \frac{E_f}{e} + \phi \tag{5.5}$$

with $\frac{E_f}{e}$ being determined by the chemical (quantum) capacitance of the graphene, and being determined by the geometrical capacitance $C_G$.

When a field is applied, free cations tend to accumulate near the negative electrode, creating a positive charge there and an uncompensated negative charge near the interface. The accumulation is limited by the concentration gradient, which opposes the Coulombic force of the electric field. When a steady state is reached, the statistical space charge

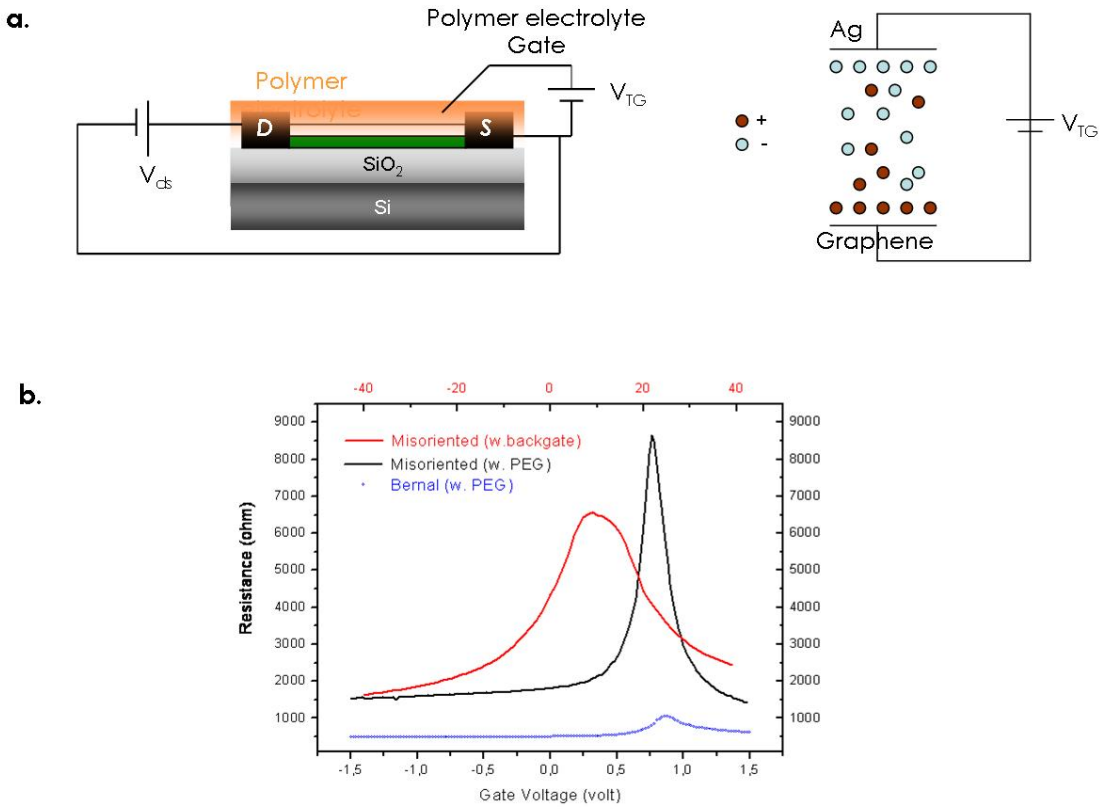


Figure 5.8: (a) A schematic cross-section of an electrochemically top-gated bilayer graphene device. (b) Comparative plots of the resistance vs gate voltage for the two types of bilayers devices in top-gated confuguration.

distribution resembles that shown in Fig. 5.8 (a). This layer of charge around an electrode is called the Debye layer. As shown in Fig. 5.8 (a), when we apply a positive potential $V_{TG}$ to the Ag top gate (with respect to the source electrode connected to graphene), the $Li^+$ ions become dominant in the Debye layer formed at the interface between the graphene and the electrolyte. The Debye layer of thickness $d_{TG}$ acts like a parallel-plate capacitor. Therefore, the geometrical capacitance in this case is $C_{TG} = \epsilon\epsilon_0/d_{TG}$, where $\epsilon$ is the dielectric constant of the PEO matrix. The Debye length is given by $d_{TG} = \frac{2ce^2}{\sqrt{(}}\epsilon kT$) for a monovalent electrolyte, where $c$ is the concentration of the electrolyte, $e$ is the electric charge and $kT$ is the thermal energy. In principle, $d_{TG}$ can be calculated if the electrolyte concentration is known. However, in the presence of a polymer, the electrolyte

ions form complexes with the polymer chains. Hence, the exact concentration of ions is not possible to measure. For polymer electrolyte gating the thickness of the Debye layer is reported to be a few nanometres (1 to 5 nm) [67]. The dielectric constant of PEO is 5 [68]. Assuming a Debye length of 2 nm, a gate capacitance $C_{TG}$ = 2.2 x $10^{-6}$ F $cm^{-2}$ is calculated.

Hence, for the back gate, $\phi >> E_F/e$, whereas for top gating the two terms in the above Equation 5.5 are comparable.

The Fermi energy in graphene changes as $E_F(n) = \hbar|\nu_F|\sqrt{\pi n}$ where $|\nu_F|$ = 1.1 x $10^6 ms^{-1}$ and is the Fermi velocity [10, 14]. For the top gate, $\phi = ne/C_{TG}$. From equation 5.5 we get

$$V_{TG} = \frac{\hbar|\nu_F|\sqrt{\pi n}}{e} + \frac{ne}{C_{TG}} \tag{5.6}$$

Using the numerical values: $C_{TG}$ = 2.2 x $10^{-6}$ F $cm^2$ and $\nu_F$ = 1.1 x $10^6$ $ms^{-1}$,

$$V_{TG} = 1.16{\times}10^{-7}\sqrt{n} + 0.723X10^{-13}n \tag{5.7}$$

where n is in units of $cm^{-2}$. Equation 5.7 allows us to estimate the doping concentration at each top-gate voltage ($V_{TG}$). Note that, as in back gating, we also obtain the minimum source−drain current at finite top-gate voltage ($V_{TG}$ = 0.7 V), as seen in Figure 5.8(b). Accordingly, a positive (or negative) $V_{TG}$-$V_{nTG}$ induces electron (or hole) doping.

So, on top-gating the device in such a configuration, a rather narrow gate voltage range of only 1.5 V is sufficient to switch the device from the n- to p-type regime. The carrier mobilities of the misoriented and Bernal-stacked bilayer devices were estimated by applying the Drude model $\mu = (ne\rho)^{-1}$. The curves plotted in Figure 5.8 correspond to the best values obtained within our sample ensemble. The misoriented bilayer device shows a higher mobility when compared to both Bernal-stacked bilayers and monolayers [78], which might be due to the screening of the charged impurities present at the substrate by the bottom graphene layer.

When SPCM measurements were carried out under electrochemical topgate operation, the sign inversion of the contact photocurrent signals characteristic of graphene monolayers and Bernal bilayers and could also be observed for the misoriented bilayers, in full accord with the model in Figures 5.9(a,b). Furthermore, the images revealed photocurrent fluctuations on the sheets, which were absent prior to the polymer deposition. These

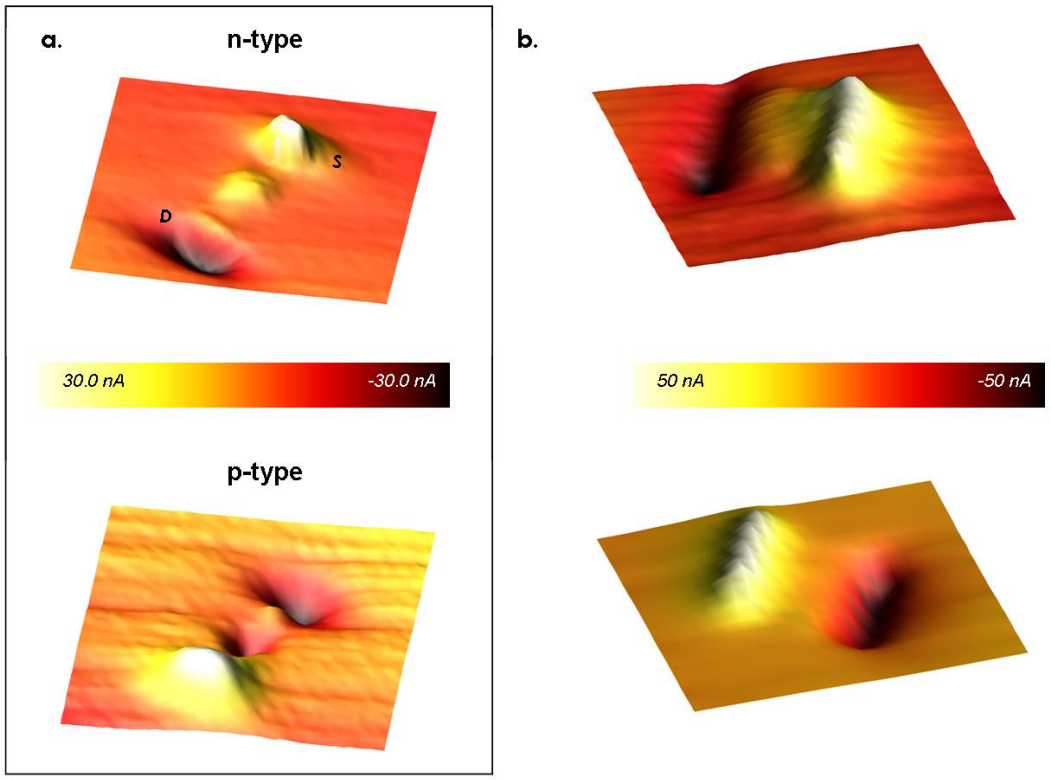


Figure 5.9: (a) Three-dimensional plots of photocurrent generated in the top-gated misoriented bilayer device in the p- and n-type regimes,(b) Similar three-dimensional plots of photocurrent generated in the top-gated Bernal bilayer device.

features most likely originate from charge impurities contained in the polymer electrolyte topgate.

The presented SPCM data directly proves that the layers in misoriented bilayer graphene are electronically decoupled from each other as a result of their rotational stacking fault, in stark contrast to Bernal-stacked bilayers, which behave as single crystals. The bottom layer in the first type of material acts like a *pseudo* substrate that electrostatically screens the top layer from the substrate, thus imparting enhanced carrier mobility within the top layer.

The above results provide direct evidence for pronounced electrostatic shielding of the top layer within misoriented bilayer graphene. With the aid of electrochemical gating it is furthermore demonstrated that the carrier mobility in such a system is superior to that of a graphene monolayer in direct contact with the substrate.

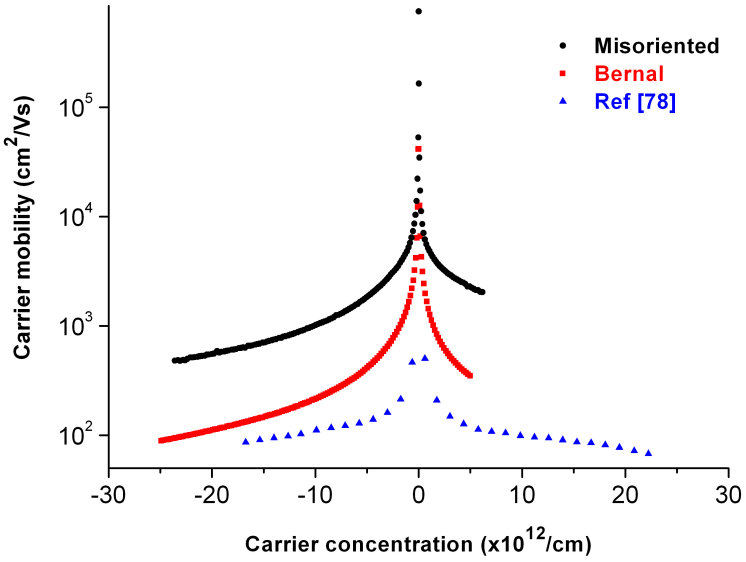


Figure 5.10: The carrier mobilities of the misoriented and Bernal-stacked bilayer devices were estimated by applying the Drude model. The misoriented bilayer device shows a higher mobility when compared to both Bernal-stacked bilayers and monolayers [78], suggestive of electrostatic screening of the charged impurities on the substrate by the bottom graphene layer.

Morever, recent experiments using a dual gate configuration have enabled to independently control the charge carrier density in misoriented graphene bilayers [65]. In other experiments, Li and colleagues [86] reported the observation of low-energy van Hove singularities in twisted graphene layers seen as two pronounced peaks in the density of states measured by scanning tunnelling spectroscopy. They demonstrated that a rotation between stacked graphene layers can generate Van Hove singularities, which can be brought arbitrarily close to the Fermi energy by varying the angle of rotation. This opens intriguing prospects for Van Hove singularity engineering in such systems.

It must be noted, however, that these systems (i.e., misoriented or twisted graphene) cannot be easily fabricated at a large scale. Nonetheless they are excellent model systems to understand some crictical points in graphene transport *viz.* to extract the best transport properties from it, the ideal substrate for graphene - would be graphene (or something very similar).

**Concluding remarks on substrate effect**

The highest mobilities have been observed in graphene sheets freely suspended between pairs of electrodes [26]. However, their poor structural stability makes suspended devices difficult to use in real applications. Large gate voltages would collapse the flake, and charge densities must be kept relatively low ($10^{12} cm^{-2}$) as a result. The need to decouple graphene (both single- and few-layer) from its environment stems from the fact that every atom is a surface atom. The thinness of graphene also allows local disorder to obscure its unique properties. Processing residues and dangling bonds on the surface of a supporting substrate lead to charge inhomogeneities that scatter conduction electrons. And because graphene adheres very well to substrates, it adopts some of the substrate's structural features, such as ripples or corrugations [57, 59], which can produce unwanted strain and thus further scattering [8].

Thermally grown $SiO_2$ is the most common supporting substrate for graphene, and $Si/SiO_2$ supported devices have improved considerably since the first demonstrations in 2004. Post-processing methods such as annealing in forming gas [57] and the passing of a high current through the graphene, also called current annealing [60], have been developed to improve the performance of $SiO_2$-supported devices. However, these techniques do not completely decouple the graphene from its substrate.

Very recently in 2010, Dean and colleagues [62] came up with a promising alternative approach to decoupling graphene from its environment in the form of hexagonal boron nitride, resting on an underlying silicon dioxide substrate. With the exception of a slightly different lattice constant, the structure of hexagonal boron nitride is almost identical to that of graphite. They showed that the surface corrugation of a sufficiently thick (around 7 nm) stack of boron nitride stamped onto a silicon dioxide substrate is indistinguishable from an atomically flat crystal of highly ordered pyrolytic graphite. Electrical measurements as a function of temperature and magnetic field revealed significant improvements in device performance. Their transport data reveal switching between the n-type and p-type regime within a modulation range of only 10V. This is a huge improvement addressing the "substrate effect".

# Chapter 6

# Towards applications

## 6.1 Top-gated Transistors

While back-gated graphene devices on a $Si/SiO_2$ substrate are useful proof-of-concept devices, they suffer from rather large parasitic capacitances and cannot be integrated with other components. Therefore, practical graphene transistors need a top-gate. The first graphene FET with a top-gate was reported in 2007 [93], representing an important milestone, and progress has been very rapid since then (Fig. 6.1). Although research into graphene is still in its infancy, graphene FETs can compete with silicon-based devices that have benefited from decades of research and investment.

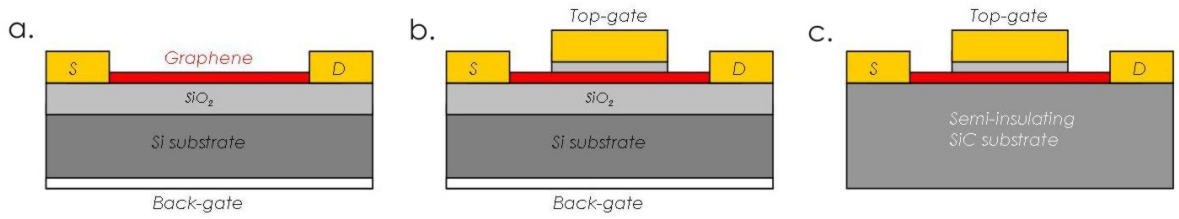


Figure 6.1: Schematics of different graphene MOSFET types: (a) back-gated MOSFET; (b) top-gated MOSFET with a channel of exfoliated graphene or of graphene grown on metal and transferred to a $SiO_2$-covered Si wafer; (c) top-gated MOSFET with an epitaxial-graphene channel (right). The channel shown in red can consist of either large-area graphene or graphene nanoribbons.

Top-gated graphene FETs have been made with exfoliated graphene [93–97], graphene

grown on nickel [98] or copper [99], and epitaxial graphene [100, 101] using $SiO_2$, $Al_2O_3$ or $HfO_2$ as the top-gate dielectric. CVD based roll-to-roll graphene on flexible substrates, which currently represents graphene's ambitious vision, is made on plastic substrates which are flexible. Hence, the top gates like $Al_2O_3$ and $HfO_2$ which are grown through Atomic Layer Deposition (ALD) techniques are not ideally suited for such applications due to the thermal limitations of plastics. A more flexible and low-processing-temperature alternative would be the polymer-based gates described in the previous chapter. The PEO/$LiClO_4$ requires a maximum processing temperature of 60°C.

In graphene transistors with top-gates, the carrier density and the type of carrier (electrons or holes) in the channel are governed by the potential differences between the channel and the gates. The position of the Dirac point depends on several factors, such as the difference between the work functions of the gate and the graphene, the type and density of the impurity charges at the interfaces at the top and bottom of the channel, and any doping of the graphene. The on/off ratios reported for FET devices with conventional graphene channels are in the range 2 to 20.

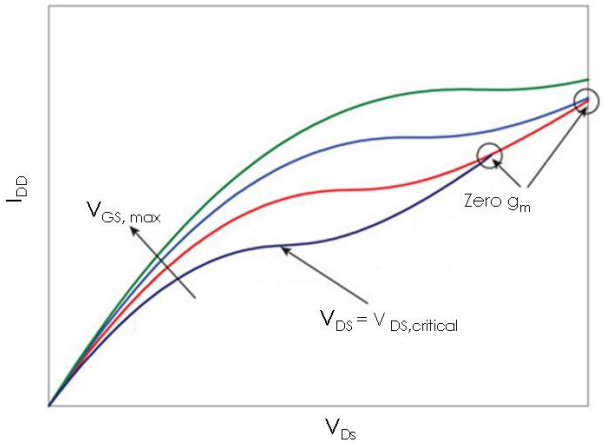


Figure 6.2: Qualitative shape of the output characteristics (drain current versus drain-source voltage) of a MOSFET with an n-type large-area-graphene channel, for different values of the top-gate voltage [103].

The output characteristics of many graphene FETs have shown either a linear shape without any saturation [94] or only weak saturation [100, 101], each of which is a disadvan-

tage with respect to device speed. However, some graphene MOSFETs have an unusual form of saturation-like behaviour that includes a second linear region [97, 98, 104](Figure 6.2). The present understanding of the origin of this behaviour is that for small values of $V_{DS}$, the transistor operates in the linear region and the entire channel is n-type. As $V_{DS}$ is increased, the drain current starts to saturate until the inflection point at a critical point where the potential conditions at the drain end of the channel correspond to the Dirac point. Once this critical point is exceeded, the conduction type at the drain end of the channel switches from n-type to p-type [103] and the transistor enters a second linear region. At sufficiently large values of $V_{DS}$, the output characteristics for different gate voltages may cross [104], leading to a zero or even negative transconductance, which is highly undesirable. This peculiar behaviour is a consequence of these devices having gapless channels and does not occur in FETs with semiconducting channels, hence the requirement to operate under low voltages (less than 2 V) when using a top gate.

Transistors made from graphene also have a very high cut-off frequency above 100 GHz [102] and show low levels of noise [61]. Graphene FETs with Gigahertz capabilities possess large-area channels of exfoliated [94–96, 102] or epitaxial graphene [100, 101]. The fastest graphene transistor reported so far is a MOSFET with a 240 nm gate that has a cut-off frequency of $f_T$ = 100 GHz [131], which is higher than those of the best silicon MOSFETs with similar gate lengths (so is the cut-off frequency of 53 GHz reported for a device with a 550 nm gate [100]). A weak point of all radiofrequency graphene MOSFETs reported so far is their unsatisfying saturation behaviour (only weak saturation or the second linear regime), which has an adverse impact on the cut-off frequency, the intrinsic gain and other figures of merit for radiofrequency devices. Nevertheless, outperforming silicon MOSFETs while operating with only weak current saturation [100] is certainly impressive.

In spite of some fundamental shortcomings, graphene FETs still have progressed very briskly towards probable applications. In May 2009, teams from Stanford University, University of Florida and Lawrence Livermore National Laboratory announced that they have created an n-type transistor, which means that both n- and p-type transistors have now been realized in graphene [92]. A month later, researchers at the Politecnico di Milano demonstrated the first graphene integrated circuit, a complementary inverter consisting of one p- and one n-type graphene transistor [87]. Late in 2010 (as this chapter was being written), the first graphene based triple-mode single-transistor was fabricated [88]. The forementioned are considered to be important steps into building very basic *circuits*

using graphene. The latter two especially have been cited as the primary steps towards building a functional circuit using graphene. Unfortunately, while inverters and amplifiers are essential components in building a circuit, their respective 'gain' must be greater than unity to be useful.

## 6.2 Gain

Depending on whether they are used to amplify or switch electronic signals, transistors can be grouped into amplifiers and switches. Transistor switches form the basis of all digital circuits in computers where they control on/off operations. Transistor amplifiers are inserted into circuits to amplify current, voltage or power. A single-transistor amplifier, which consists of one transistor and one resistor, is one of the most basic building blocks in analogue circuits. However, the graphene inverters reported todate [87, 88] suffer from a very low voltage gain. Consequently, we employed the misoriented bilayers which were described in the previous chapter to address this issue, in collaboration with the group of Roman Sordan at the Politecnico di Milano, Como, Italy.

Firstly, there are three types of single-transistor amplifiers: common-source, common-drain and common-gate. Each of these has a different characteristic that depends on the small-signal voltage gain in the device ($\Delta V_{out}/\ \Delta V_{in}$). Depending on the bias voltage, the amplifier can be configurated in either the common-source, common-drain or frequency multiplication mode of operation. As an example, let us consider the graphene device where the signal enters the gate, and exits the drain. This is therefore termed as a common-source amplifier, which provides negative gain (while the other two would provide positive gain).

Figure 6.3(a) shows an optical image of a misoriented bilayer fabricated in the complementary inverter configuration, with three contacts on top. For the convenience of explanation, let us consider the two graphene FETs between the three electrodes as D1 and D2, as labeled in the Figure. The polymer gate was added to enable gating of the decoupled top layer in the bilayer. The fabrication techniques and characterisation methods are the same as in the previous chapter. Figure 6.3(b) shows the schematic structure of the inverter configuration with one electrode acting as the source connected to an external power supply, while the other electrode is grounded. The middle electrode would act as the output. The input voltage is supplied through the polymer gate from top. Figure 6.4 (a) shows the measured transport plots of the two individual FETs (D1 and D2) on

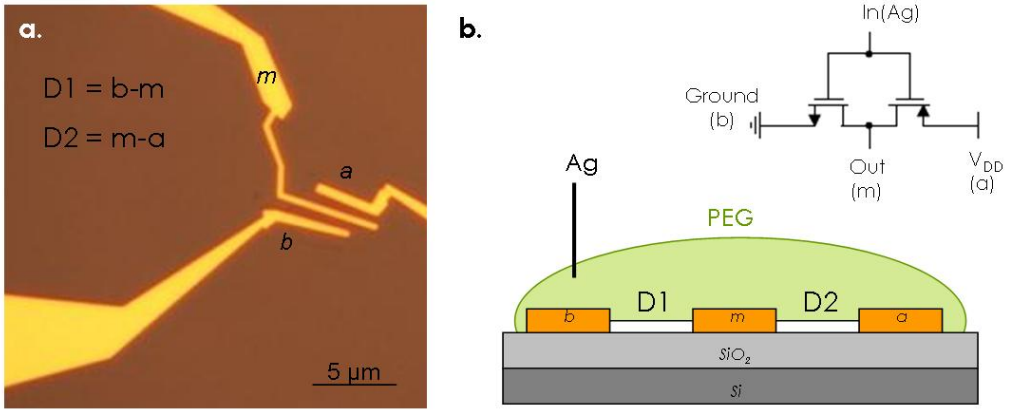


Figure 6.3: (a) Optical image of a misoriented bilayer fabricated in the complementary-inverter configuration (b) A schematic representation of the same device.

gating the PEG (R vs $V_g$). The red and blue plots represent the gate dependence of D1 and D2, respectively.

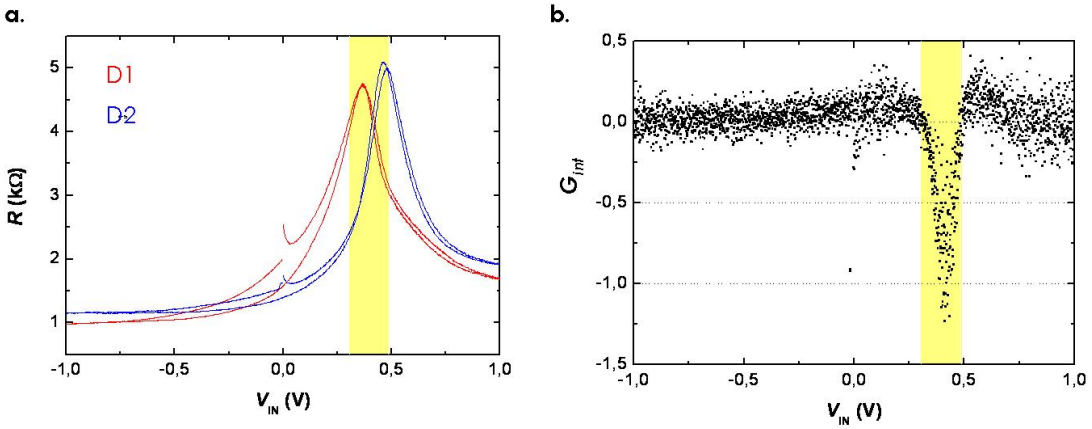


Figure 6.4: (a) Gate-dependent transport plots of polymer-top-gated the misoriented bilayer FETs (b) Plot describing the measured gain ($G_{int}$)of device D2.

Although both transistors are made on the same flake and have the same gate their

Dirac points are shifted by about 100 mV. This difference arises, since in this measurement the channel of the D2 transistor is at a higher potential than the channel of the D1 transistor, such that the D2 transistor requires higher gate potential to reach the Dirac point. Similar variance in gate potentials have been documented in other literature [81] previously. The transistors exhibit complementary behaviour between the Dirac points and hence the device inverts the input voltage. In this regime, a gain of about 1.2 is reached, as can be seen in Figure 6.4 (b). This allows tuning of the gain by choosing $V_{DD}$, which also controls the shift between the Dirac points. In total, seven misoriented graphene devices were configurated in this manner, on which a gain in the range of 0.8 to 1.2 has been recorded.

Note: Different electronic applications call for different types of amplifier, but the ideal device should be configurable into more than one type after fabrication, something that is impossible to do with conventional MOSFET technology due to the pre-determined doping in the device, but is possible with graphene due to its ambipolar nature.

## 6.3 Phase-shift detectors

Having shown a gain exceeding unity, it was possible to incorporate the graphene devices into circuits. We investigated analog and digital phase-shift detection with a polymer-electrolyte gated misoriented bilayer graphene.

A phase shift detector is a logical circuit (as seen in Figure 6.5(a)) that generates a voltage signal which represents the difference in phases between two oscillating input signals. It comprimises of two inputs and one output, where a reference signal is applied to one input and the phase or frequency modulated signal is applied to the other. The output is a signal that is proportional to the phase difference between the two inputs.

Figures 6.5 (b) shows an AFM image of the graphene FET comprised of a decoupled (misoriented) bilayer with Ti/Au electrodes on top. The bilayer was identified in the same way as described in the previous chapter, and the FET was fabricated using e-beam lithography. Polymer electrolyte gating was again employed to gate the FET, in which a solid polymer electrolyte (SPE) was used as the gate dielectric and a silver wire immersed in the polymer electrolyte layer is used to efficiently gate the decoupled upper layer in the bilayer. The SPE in this case consists of polyethyleneoxide and lithium hexafluorophosphate ($LiPF_6$) (20:7 weight ratio) in a 4:1 methanol/water mixture, and was drop-cast on top of the conducting channel. Figure 6.5 (a) shows the electronic

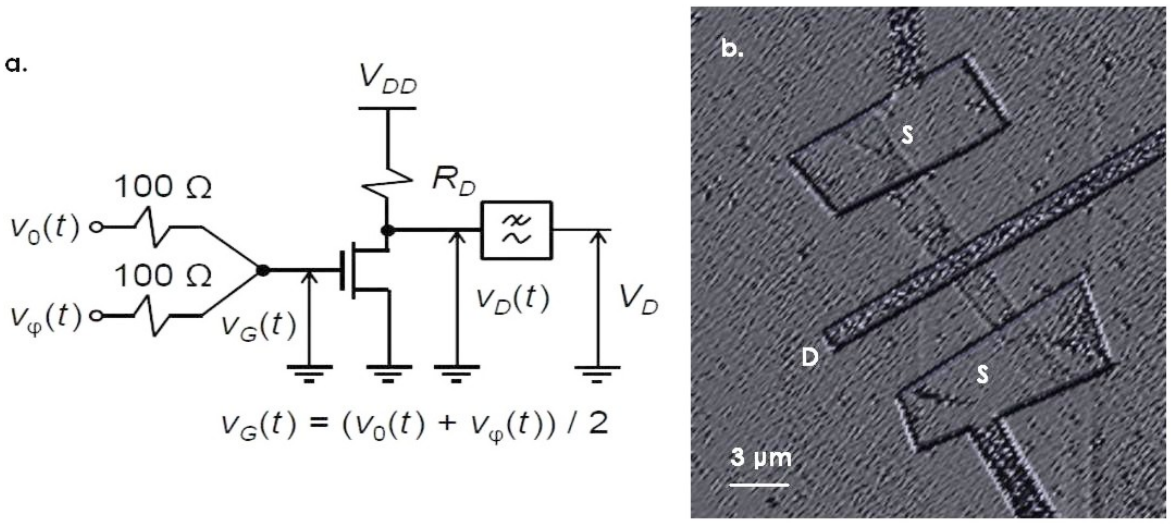


Figure 6.5: (a)A circuit diagram of a phase-shift detector comprising of one misoriented bilayer graphene transistor, three off-chip resistors, and a low-pass filter. (b) An AFM image of the misoriented graphene FETs.

equivalent circuit for phase detection. One electrode acts as the drain (D) connected to an external power supply $V_{\mathrm{DD}}$ via an off-chip pull-up resistor $R_{\mathrm{D}}$. The other electrode acts as the source which is grounded; the third electrode in Fig 6.5 (b) is not used. The input voltages are supplied through two off-chip resistors $R_{\mathrm{G}}$ to the SPE gate (G). The output dc voltage $V_{\mathrm{D}}$ is taken from the output of the low-pass filter which filters the drain voltage $v_{\mathrm{D}}$. All measurements were performed under ambient conditions.

Figure 6.6 shows a drain voltage $v_{\mathrm{D}}$ vs. gate voltage $v_{\mathrm{G}}$ transfer curve measured with the circuit shown in Fig.6.5(a). Phase detection is based on the symmetry and nonlinearity of the transfer curve in the vicinity of the charge-neutrality point (CNP). Reference $v_0$ and phase shifted $v_\varphi$ signals are connected to the two inputs of the detector resulting in the gate voltage $v_{\mathrm{G}} = (v_0 + v_\varphi)/2$. In order to detect the phase difference between the signals, the input signals must be biased at the CNP.

For analog phase detection, the input signals are then given by $v_0(t) = V_{\mathrm{GCNP}} + V_0 \sin \omega t$ and $v_\varphi(t) = V_{\mathrm{GCNP}} + V_0 \sin(\omega t + \varphi)$, where $V_{\mathrm{GCNP}}$ is the gate voltage at the CNP, $\varphi$ is the phase difference between the signals, $V_0$ their amplitude, and $f = \omega/(2\pi)$ is the signal frequency. This yields a gate voltage $v_{\mathrm{G}}(t) = V_{\mathrm{GCNP}} + V_0 \cos(\varphi/2) \sin(\omega t + \varphi/2)$, i.e., the gate voltage is also biased at the CNP with an amplitude of the ac component $\propto \cos(\varphi/2)$.

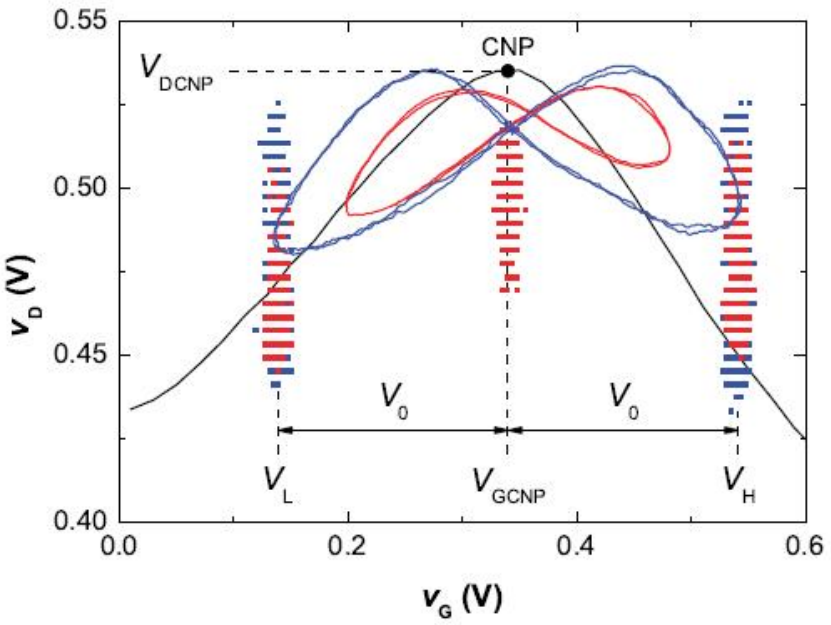


Figure 6.6: Transfer curves of the circuit shown in Fig. 6.5(a): static (dc) curve in black and dynamic ac curves in blue and red (lines/scatter). Blue plots correspond to $\varphi = 0^o$, while red plots $\varphi = 90^o$. The lines correspond to analog signals, while the scatter corresponds to the digital signals. $V_0$ = 200 mV is the amplitude of the input signals which are offset at the CNP.

A larger phase $\varphi$ results in a smaller ac amplitude of the gate voltage. Since the transfer curve decreases on both sides of the CNP, decreasing the ac amplitude of the gate voltage increases the minimum of the drain voltage $v_{\mathrm{D}}$ while the maximum remains constant, and this increases the dc offset $V_{\mathrm{D}}$ of the drain voltage.

The dependence of the output dc component $V_{\mathrm{D}}$ on the phase difference $\varphi$ can be derived by approximating the transfer curve as a second-order Taylor series $v_{\mathrm{D}} - V_{\mathrm{DCNP}} = -k(v_{\mathrm{G}} - V_{\mathrm{GCNP}})^2$. This is valid for small voltages $|v_{\mathrm{G}} - V_{\mathrm{GCNP}}|$ (i.e., small amplitudes $V_0$), where $V_{\mathrm{DCNP}}$ is the drain voltage at the CNP and $k$ is a positive constant. The drain voltage is then $v_{\mathrm{D}}(t) = V_{\mathrm{D}} + (kV_0^2/4)(1+\cos\varphi)\cos(2\omega t + \varphi)$, which has an ac component at a frequency $2f$ that was recently utilized in frequency doublers. [89] The dc component of the drain voltage is $V_{\mathrm{D}} = V_{\mathrm{DCNP}} - (kV_0^2/4)(1+\cos\varphi) \propto -\cos\varphi$, and it carries the information about the phase shift between the input signals.

Figure 6.7 shows drain voltage waveforms measured with the analog graphene phase

detector in the case of phase shifts of 0° and 90°. It is apparent that the drain voltage has a comparatively larger dc component $V_D$ for the latter case. Both drain voltage waveforms have a pronounced $2f$ component and are lagging by $\sim 25°$ behind the respective gate voltage waveforms due to gate hysteresis. The lag can be understood from Fig.6.6, where both the static (dc) and the dynamic (ac) transfer curves are shown. Parasitic capacitances between the polymer gate and source/drain contacts are so large that they cannot charge/discharge at the same rate at which the input signals are changed. Consequently, the up and the down sweeps of the gate voltage $v_G(t)$ result in different transfer curves leading to a typical hysteretic butterfly-shaped curve as the full cycle is completed. [90] The static CNP splits into two dynamic CNPs (one on either side). The time delay between the static and dynamic CNPs equally shifts both half cycles of the drain voltage without influencing phase detection.

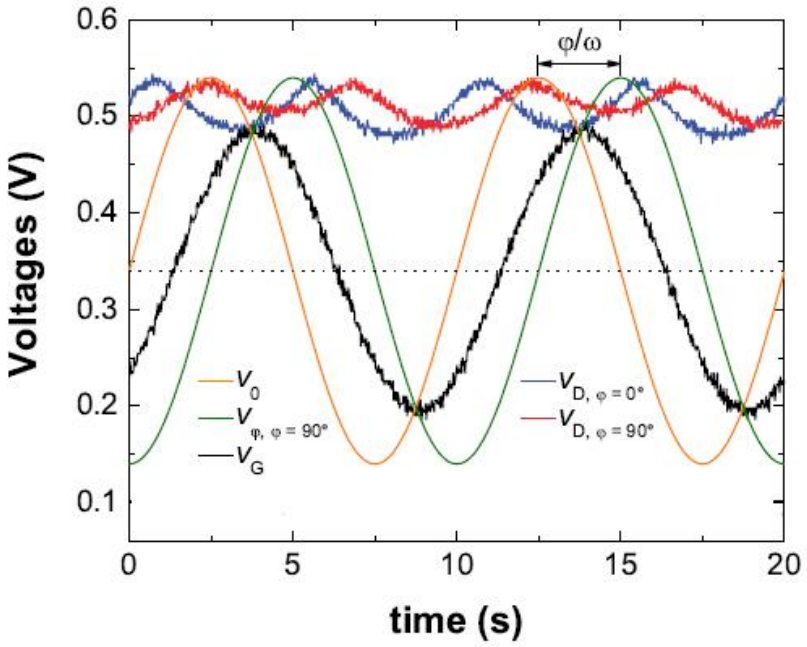


Figure 6.7: Analog phase detection: Input and output signals measured in the phase detector at a frequency $f = 100$ mHz. Reference input signal $v_0(t)$ (orange), phase-shifted input signal $v_\varphi(t)$ in the case $\varphi = 90°$ (green), measured gate voltage $v_G(t)$ in the case $\varphi = 90°$ (black), and measured drain voltages $v_D(t)$ in the case of no phase shift ($\varphi = 0°$) between the inputs, i.e., when $v_0(t) = v_\varphi(t) = v_G(t)$ (blue), and in the case $\varphi = 90°$ (red).

Figure 6.8 shows that the drain voltage $V_{\mathrm{D}}$ exhibits the predicted $(-\cos\varphi)$ dependence on the phase difference $\varphi$. Efficient phase detection requires a high sensitivity of the drain voltage $V_{\mathrm{D}}$ to $\varphi$. To achieve this, the difference between the maximum and the minimum drain voltage in the phase curve must be as large as possible. From the expression for the dc component of the drain voltage $V_{\mathrm{D}}$, this difference is $kV_0^2/2$, i.e., the constant $k$ must be as large as possible. This translates to a need for a large small-signal gain $A = dv_{\mathrm{D}}/dv_{\mathrm{G}} = 2k(V_{\mathrm{GCNP}} - V_{\mathrm{G}})$, where $V_{\mathrm{G}}$ is the gate voltage at the selected operating point. The same is true also for frequency doubling in order to increase signal-to-noise ratio. Back-gated graphene FETs could only be employed in phase detection if input signals with very large amplitude $V_0$ were used. But this would imply a significant increase in the input power dissipation $(V_0^2/R_{\mathrm{G}})\sin^2(\varphi/2)$. Moreover, the use of back-gated devices would require a large input bias $V_{\mathrm{GCNP}} > 20$ V, since such devices are strongly $p$-doped by ambient impurities.

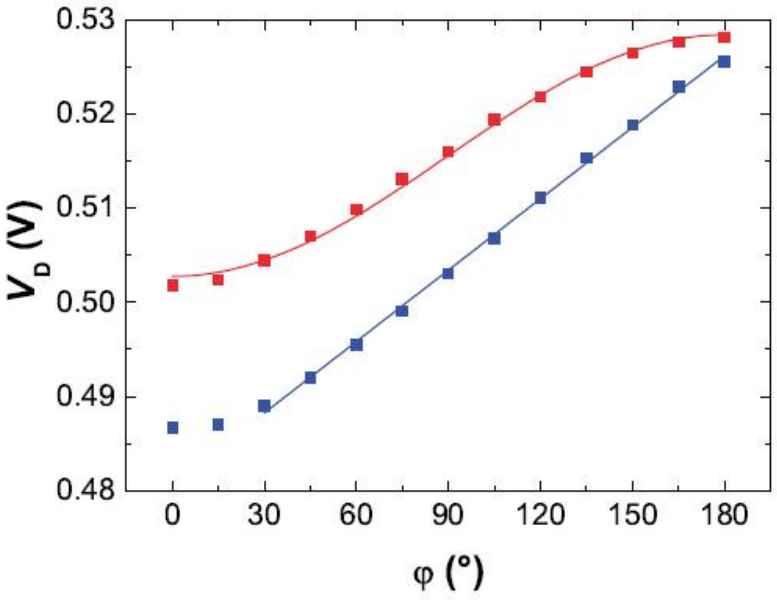


Figure 6.8: Measured dc component $V_{\mathrm{D}}$ of the drain voltage $v_{\mathrm{D}}(t)$ vs. phase shift $\varphi$ between the inputs, in the case of analog (blue) and digital (red) detection. Corresponding curve fits in the case of analog $(\propto -\cos\varphi)$ and digital $(\propto \varphi)$ detection are shown as solid lines.

Digital phase detection was realized based on the exclusive-OR functionality of the present circuit. [91] Here, $v_0(t)$ and $v_\varphi(t)$ are digital input signals, which can take either a high $V_\mathrm{H} = V_\mathrm{GCNP} + V_0$ or a low $V_\mathrm{L} = V_\mathrm{GCNP} - V_0$ value. The output drain voltage $v_\mathrm{D}(t)$ shows a high value $V_\mathrm{DH}$ when the two digital inputs $v_0(t)$ and $v_\varphi(t)$ are different and shows a low value $V_\mathrm{DL}$ when the two inputs are identical. In other words, the duty cycle of the drain voltage is $\varphi/180°$. The dc component of the drain voltage is then $V_\mathrm{D} = V_\mathrm{DL} + 2(V_\mathrm{DH} - V_\mathrm{DL})(\varphi/180°) \propto \varphi$. Figure 6.9 shows drain voltage waveforms measured with the digital phase detector for phase shifts of 0° and 90°. As in the case of analog detection, the drain voltage for $\varphi = 90°$ has a larger dc component in comparison to the case for $\varphi = 0°$. The phase curve for the case of digital detection is shown in Fig. 6.8, which follows the predicted $\propto \varphi$ dependence.

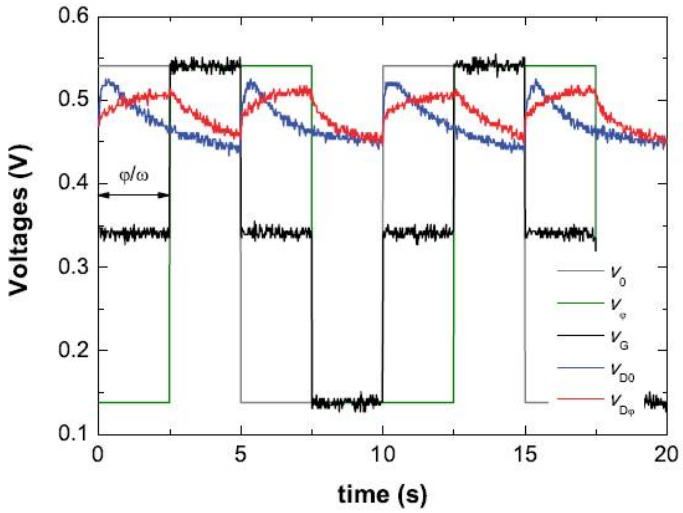


Figure 6.9: Digital phase detection: Input and output signals measured in the phase detector at a frequency $f = 100$ mHz. Reference input signal $v_0(t)$ (gray), phase-shifted input signal $v_\varphi(t)$ in the case $\varphi = 90°$ (green), measured gate voltage $v_\mathrm{G}(t)$ in the case $\varphi = 90°$ (black), and measured drain voltages $v_\mathrm{D}(t)$ in the case of no phase shift ($\varphi = 0°$) between the inputs, i.e., when $v_0(t) = v_\varphi(t) = v_\mathrm{G}(t)$ (blue), and in the case $\varphi = 90°$ (red).

Ideally, the output drain voltage must instantly switch when the gate voltage input changes its level. From Figure 6.9, it is apparent that this is however not the case. This is due to the fact that parasitic capacitances increase the transition time of the drain

voltage $v_{\mathrm{D}}(t)$ which therefore does not instantly reach levels $V_{\mathrm{DH}}$ and $V_{\mathrm{DL}}$ when the gate voltage is changed; instead, the drain voltage exponentially tends to these levels. For $\varphi = 0°$ the gate voltage takes only two possible values ($V_{\mathrm{L}}$ or $V_{\mathrm{H}}$) and the output drain voltage should be constant ($v_{\mathrm{D}}(t) = V_{\mathrm{DL}}$). However, as can be observed in Fig.6.9 (blue curve), the output drain voltage shows a spike when $v_0(t)$ changes its state. This is due to the transition time being finite when passing the operating point over the CNP. For non-zero phase shifts, the gate voltage has three states $V_{\mathrm{L}}$, $V_{\mathrm{H}}$ and the mid-state voltage corresponding to $V_{\mathrm{GCNP}}$ (see black curve in Fig.6.9). For very small phase shifts ($\varphi \leq 15°$), the detected voltage is insensitive to phase change (Fig.6.9, red curve) because the mid-state $V_{\mathrm{GCNP}}$, which corresponds to a duty state of the drain voltage $v_{\mathrm{D}}(t)$, is too short to influence the drain voltage. The transition time can also be observed in the transfer curve shown in Fig.6.6 for each of the three possible values of the gate voltage, the drain voltage takes a range of values instead of a single value. As for analog detection, large gain is necessary to discriminate between the output voltage levels $V_{\mathrm{DH}}$ and $V_{\mathrm{DL}}$. The parasitic capacitances and the ensuing hysteresis in the dynamic transfer curve could be eliminated by passivating the source/drain electrodes, which should also allow for higher clock rates and improved performance.

In summary, analog and digital phase detectors based on a misoriented bilayer graphene transistor have been demonstrated. Phase detection was enabled by a drop-cast solid polymer electrolyte gate dielectric, which increased the small-signal gain by one order of magnitude over conventional back-gated devices. In this way, simple phase detectors could be realized representing an important step towards functional graphene electronic ac circuits.

# Chapter 7

# Graphite-based Field Effect Transistors

The advent of graphene and the intense study of its electrical properties by numerous groups around the world, has also drawn attention back to more graphitic materials. In fact, the initial reports on the electric-field dependent transport measurements on graphenes included work on thin films or what is now commonly known as few-layer graphene [105, 106]. Such work derives from studies on graphite long before the discovery of free-standing graphene. Few-layer graphene can be defined as a small stack of graphene. The exact distinction between few-layer graphene and multi-layer graphene has not yet been established, but a gray range of 10 to 40 nm separates the two graphenes. However, any layered graphene stack above 40 nm univocally has been dubbed "graphite" [107,108]. In this chapter, investigations of graphite in a FET based model are presented.

## 7.1 Highly Ordered Pyrolitic Graphite

Graphite is a highly anisotropic crystal having an elongated hexagonal cell with $a_0 = 2.456$ $A^o$ and $c_0 = 6.696$ $A^o$. The four atoms of the cell occupy the positions 0,0,u; 0,0,u+1/2; 1/3, 2/3,v; and 2/3, 1/3,v+1/2. u can be taken as zero and v is almost zero and cannot exceed 0.05. The structure is shown in the Figure 7.1. It consists of widely spaced planes of carbon atoms which are hexagonally linked within the planes with the C-C distance equal to 1.42 $A^o$.

The separation of the carbon atoms between the planes is considerably greater (3.4 $A^o$). Stacking of the layers is ABABA.. and the bonding between the planes is about a hundred times less than that between those in-plane, hence the pronounced cleavage shown by graphite. (The scanning electron microscopy image in Figure 7.2, shows how

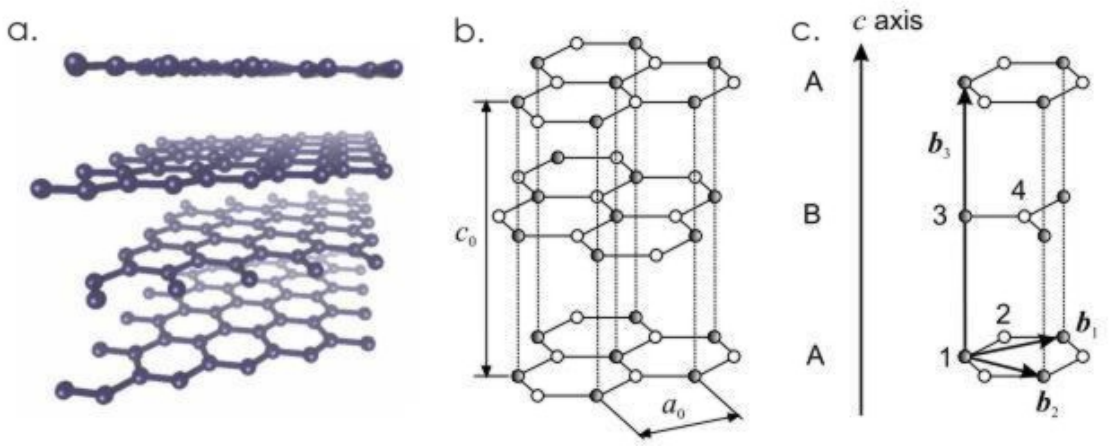


Figure 7.1: (a) Schematic of the graphite lattice - stacked layers of graphene sheets. (b) The graphite lattice stacked in an ABA sequence. (c) The hexagonal unit cell containing four atoms (numbered 1,2,3 and 4). Lattice basis vectors $b_1$, $b_2$, and $b_3$ are shown where $b_3$ is parallel to the c axis.

the graphitic planes slide over each other.)

There are two different sources of graphite - natural and synthetic graphite. The former is formed by nature in the earth's crust, where carbonaceous materials have been heated to a few thousand degrees. The first synthetic graphite was produced as a byproduct of steel-making process where graphite precipitates on top of the saturated carbon, cooling iron-melt, which is called Kish. Hence the name Kish graphite. Later, graphite was industrially synthesized from carbonaceous precursor gas by heating it to 3300$^o$C. Since it is a pyrolysis process, such graphite was named Pyrolytic graphite. Later, pressures of the order MPa were applied to orient the randomly distributed graphitic phases. To characterize the angle of deviation of the grain boundaries from the perpendicular axis of the columnar structure, a measure of the parallelism of the grains and hence the perfectness of HOPG samples, a "mosaic spread (angle)" term is used. The angular spread of the c-axes of the crystallites is of the order of 1 degree (mosaicity). By IUPAC definition, highly oriented pyrolytic graphite has not more than 1 agree mosaic spread. The lower the mosaic spread, the more highly ordered the graphite is. The term originates from X-ray crystallography. The disordering results in broadening of the (002) diffraction peak: the more disordering, the wider the peak. Therefore, the structural quality of HOPG can be related to the Full Width at Half Maximum (FWHM) of the Cu-K$\alpha$ rocking curve (radiation peak) measured

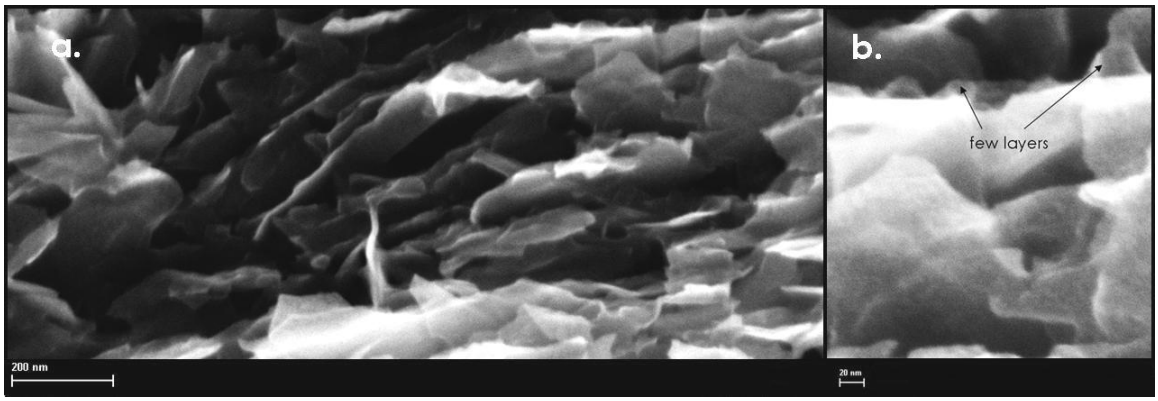


Figure 7.2: Scanning electron microscopy images of graphitic stacks. (a) Cleaved cross-section of a graphite crystallite exhibiting stacks of graphene sheets. Scale bar is 200 nm. (b) Few layers of graphene sliding over in a stack of graphene sheets. Scale bar is 20 nm.

in degrees of "mosaic spread (angle)". Thus, the smaller this angle, the higher the quality of HOPG.

Synthetic graphite remains stable at the temperatures up to 500$^o$C in air and up to 3000$^o$C in vacuum or inert atmosphere. Among the two types of synthetic graphite, Kish graphite is less pure than pyrolytic graphite. Due to the anisotropic nature of HOPG, properties such as thermal conductivity and electrical resistivity are different in different directions, i.e., along the basal plane and along the principal axis c (perpendicular to the basal plane).

### Band structure of graphite

Most theoretical calculations of the electronic structure have used as a first approximation a single two-dimensional model which neglects any interaction between adjacent layers. The electron states can be separated into $\sigma$ and $\pi$ bands. The $\sigma$ bands are contributed by the in-plane s-orbitals, while the $\pi$ bands arise from the overlap of the $p_z$ orbitals. These orbitals are normal to the layer planes and are very sensitive to the interlayer interaction which splits them into two closely spaced bands. It is this splitting which produces the $\pi$ valence and conductance band overlap at the Brilloin zone edge that gives rise to the semimetallic nature of graphite and the complex form of the Fermi surface.

Hence, the band structure of graphite can be characterized by three energy scales [115].

Please refer to Figure 7.1 for schematic understanding. The largest energy scale is set by the hopping matrix element between the in-plane atoms in the same graphene sheet (shown in white and gray), $\gamma_0 = 3.2$ eV. The next two largest ones comprise the matrix elements between adjacent Bernal-stacked graphene sheets $\gamma_1 = 0.35$ eV (between the nearest neighbour vertically) and $\gamma_3 = 0.3$ eV (for the diagonal neighbour atom). Next comes a large number of matrix elements between next-to-nearest neighbors, which are known to less accuracy but are generally believed not to exceed several tens of meV, as will be discussed in the following paragraphs. The major difference between graphite and graphene, can be explained by an overlap of the conduction and valence band in the former, which gives rise to a small (3 x $10^{18} cm^{-3}$ at T=0) but finite carrier concentration which is due to hopping between next-to-nearest planes [116]. The band overlap is on the order of the corresponding matrix element.

The question remains as to what is the magnitude of the band overlap. From an experimental point of view, the answer has been ambiguous so far due to the absence of defect-free graphite samples. The following paragraphs explain why.

## 7.2 Previous Experiments on Graphite

Various theoretical models address the issue of interlayer electronic coupling in graphite, with heterogeneous results. The popular Slonczewski-Weiss-McClure (SWMS) model [108] estimates an overlap integral of $\gamma_1$ of nearly 390 meV between the nearest layers. This value is about two orders higher than that reported by Hearing and Wallace [110], which is 5 meV. The ambiguity of measurements is primarily due to lattice defects in the measured samples, which serve as short-circuits between the graphene planes, thereby contributing to the 3D character of graphite's Fermi surface with a new DOS at the Fermi level. Another explanation is that defects act as effective doping centers which modify these density of states. In 2003, indirect evidence for such a modification was obtained by the measurement of different values of out-of-plane/basal plane resistivity ratios ($\rho_c/\rho_b$). This ratio reaches values close to 10000 at room temperature [111] for oriented graphite samples with mosaicity less than $0.3^o$, thereby suggesting a weak overlap of the p-electron wave functions in the out-of-plane direction. By contrast, a lower ratio of below 100 has been found for Kish graphite (mosaicity greater than $1^o$). This is a proof of how the quality of the crystal affects the electrical transport.

High resolution angle-dependent measurements, which enable for a greater control

of the angle between the sample and the magnetic fields [112], suggest the interlayer transport in c-axis is coherent in less ordered samples and high magnetic fields, whereas the transport is incoherent in less disordered samples. It was furthermore shown that sample defects cause better coupling between the layers thus imparting the 3D nature. This would also point towards the existence of a 2D Fermi surface in "ideal" graphite without defects.

Other experiments [114] found that the lateral size of the sample influences the Hall voltage, as a consequence of the large mean free path of the order of micrometers. The latter explains the absence of ordinary magnetoresistance (OMR) in few layer graphenes when compared to bulk HOPG [113].

Graphite is considered (semi)metallic. Metals effectively screen an applied electric field, but graphite is not a good metal, since an electric field applied normal to the graphite can penetrate tens of nanometers [122] unlike typical metals where the screening is within the first atomic layer, as has been shown theoretically [126,127] and experimentally [105].

In the following experiments, we aimed to obtain high quality graphite crystals by (1) choosing a high grade (low mosaicity) crystal, or (2) choosing a stack of appropriate height (above 40 nm). The objective was to fabricate a "graphite-based" transistor in a (polymer-based) top-gated configuration to invoke an ambipolar field effect behaviour in graphite.

The rationale behind our strategy lies in the utilization of the quasi-2D electronic structure of highly-oriented pyrolytic graphite (HOPG) providing for a large anisotropy of charge transport [117], with marked differences between basal plane and c-axis conductivity [118]. This gives indications for a strong electronic decoupling between adjacent layers of highly crystalline graphite. Here we utilize this decoupling to obtain a field-effect by careful control of charge transport through the topmost layer(s) of a graphitic crystallite. While the presence of field-effect has already been demonstrated in monolayer and few layer graphene, [119,120] it would be ideal if such a field-effect were to exist in graphite. This would enable the direct structuring of graphite avoiding a multitude of procedures that are currently necessary for the controlled preparation of graphene devices, such as exfoliation or transfer techniques.

## 7.3 Field Effect in Graphite crystallites

A HOPG crystal, with thickness of 2 mm along the c-axis and a 12x12 $mm^2$ frontal surface area was used as the parent material. The crystal (pictured in Figure 7.3b) was cleaved perpendicular to the c-axis by mechanical exfoliation using a tape and transferred onto a $Si/SiO_2$ substrate. The substrate was then inspected for stacks of graphene sheets. Graphite stacks gave more optical contrast against the background when compared to the single or bilayers in the previous chapter. Also, the higher the stack height, the greater would be the metallic lustre (Figure 7.3). AFM was then employed to determine the height of the stacks. Stacks higher than 40 nm were selected to ensure the intrinsic graphite-like behaviour prior to the fabrication. The corresponding Raman spectrum shown in Fig.7.3(c) is in accordance with literature reports for highly ordered pyrolitic graphite [121].

In order to make use of the high anisotropy and the resulting electronic decoupling between the layers efficiently, we first investigate different contact configurations on graphite crystallites. Intuitively one would expect to see the decoupling if we were to contact only the uppermost layer of the crystallite in order to maximize the contribution of basal plane electronic transport. We provide contacts exclusively to the uppermost layer by depositing a $SiO_x$ insulating layer at the edges of the crystallite in a first step followed by fabrication of the electrodes numbered 1 and 2 using standard electron beam lithography. As a control, we also fabricate a second set of electrodes (numbered 3 and 4) on the same crystallite without using the insulating layer. The contacts 3-4 touch the ends of the stack and serve as source and drain to the entire graphite channel, such that charge carriers are injected into all the sheets of the stack in parallel (denoted bulk transport). 1-2 on the other hand serve as contacts to the crystallite in such a way that the injection of carriers would take place only through the topmost layer (denoted surface transport) (figure 7.4). The resistances for 1-2 and 3-4 made in a similar geometry were measured to be 686 ohms and 529 ohms respectively for the sample in figure 7.3. This can be explained by considering that the transport across 3-4 takes place through almost all the layers in the stack giving a lower resistance in comparison to the contacts 1-2 where the transport is mainly through the upper layer(s). This gives a first indication that the contacts to the uppermost layer are indeed able to make use of the anisotropy and the electronic decoupling within the crystallite. Secondly, the electrodes 3 and 4 have a comparatively larger contact area with the HOPG surface, which may also lead to a lower contact resistance.

Further support for the anisotropy in charge transport was obtained by scanning pho-

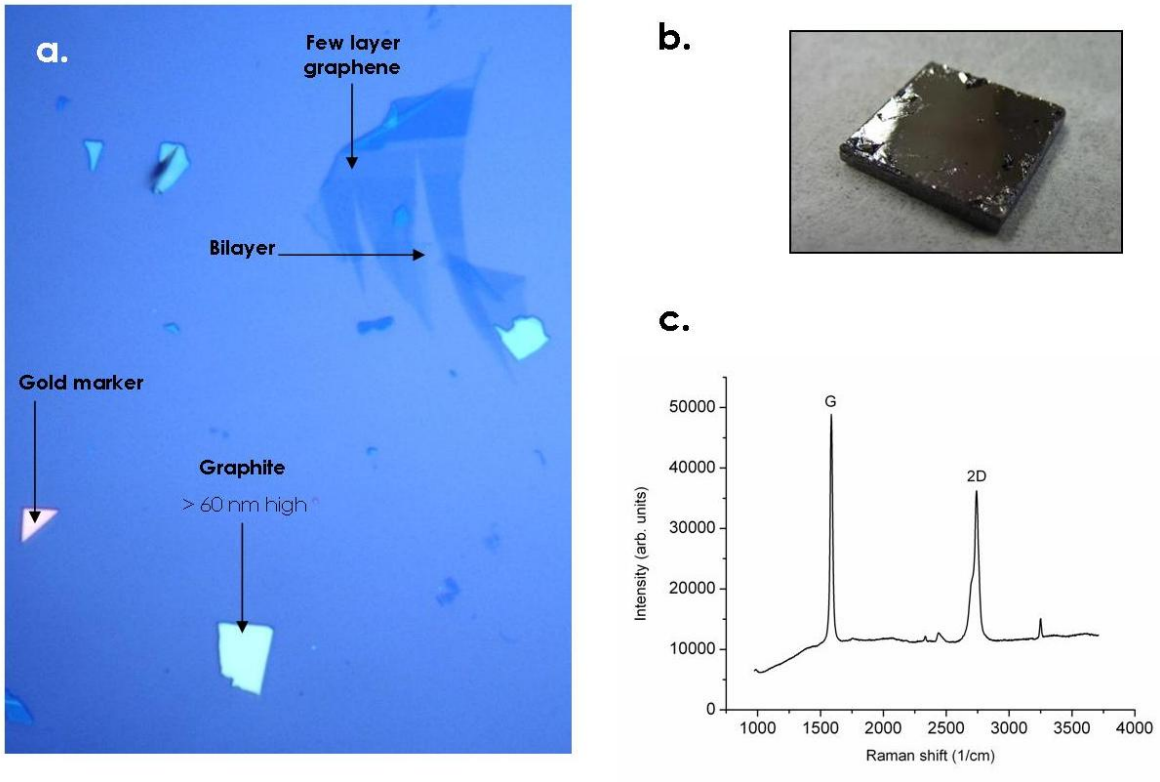


Figure 7.3: (a) Optical image of the surface of $Si/SiO_2$ which compares the contrast exhibited by the few-layer graphene and graphite. (b) Photograph of a commercially available HOPG crystal. (c) Raman spectrum of graphite flake recorded with 488 nm laser excitation.

tocurrent microscopy (SPCM). Figure 7.5 presents SPCM images of the contacted sample, where the photocurrent at zero bias is mapped upon illumination with a diffraction-limited laser spot. For the contacts 1-2, the photocurrent lobes are quite focused and located close to the contact edges. Conversely, in the case of contacts 3-4, the photocurrent signal is laterally dispersed over an extended area, pointing toward a lower spreading resistance of the two contacts in comparison to the 1-2 contact pair. Accounting for the resistance in the two configurations, the photovoltages were calculated to be 1.5 $\mu$V and 4.5 $\mu$V for the bulk (contacts 3-4) and surface (contacts 1-2) contributions respectively. The higher photovoltage suggests a larger barrier for injection of charge carriers perpendicular to the crystal and signifies an increased c-axis resistivity characteristic of pyrolytic graphites. The difference in photovoltages resulting from the design of contacts shows that when the graphite sheets are contacted from top (instead of the side), only the surface layer(s)

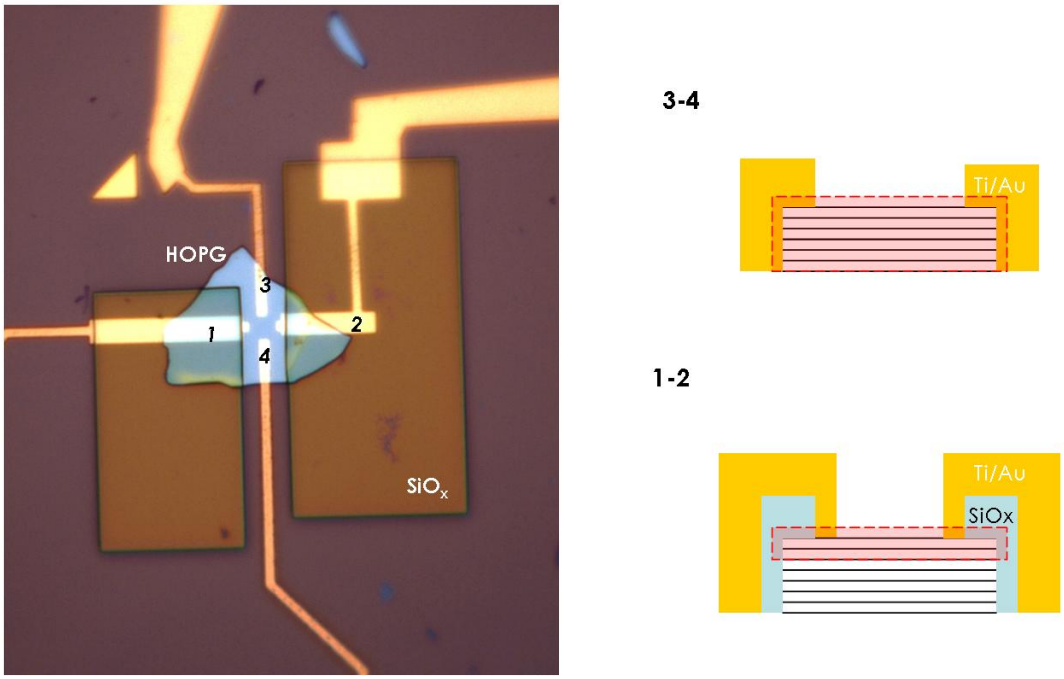


Figure 7.4: Optical image of a HOPG flake contacted in two ways - through the sides, and from the top. (right) Schematic of the cross section of the FET, where the red regions describe the participating layers in the HOPG.

would participate as the charge carrier pathway.

The field-effect in contacted graphite crystallites was subsequently investigated. Under application of a back-gate voltage no field-effect could be observed for any of the contact configurations, as shown in figure 7.6(a). However, using a polymer electrolyte gate (Ag wire in a PEO/$LiClO_4$) a modulation of device resistance as a function of the electrochemical gate voltage is clearly observable for both contact configurations (see figure 7.6(b)). It is apparent that the resistance can be tuned over 1.5 percent in a small gate voltage range of +/- 1.5 V. This observation suggests that topmost layers in the crystallite are indeed decoupled to an extent sufficient enough to obtain a small field-effect using the polymer electrolyte gate [123]. However, it is somewhat unexpected that the extent of gate action for bulk contacting (3-4) is similar to that of surface contacting (1-2). One plausible explanation for this similarity is the comparatively large channel dimensions for the 3-4 contact pair, which results in a sizeable gate modulation, akin to observations made on back-gated "few" layer graphene devices. [124] Another aspect that distinguishes

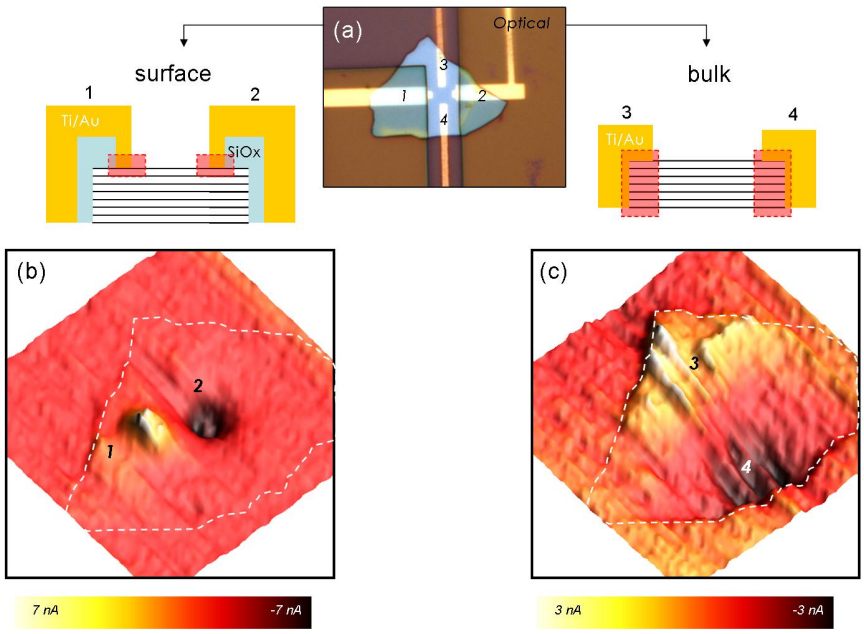


Figure 7.5: (a) Optical image of the HOPG crystallite contacted in two different configurations: injection of charge carriers through the surface (1-2) or through the bulk (3-4). (b) Photocurrent response in 3D when the surface layers of the HOPG crystallite are contacted (1-2), (c) the corresponding photocurrent image when contacted through the bulk (3-4). The dashed line marks the boundary of the crystallite.

the two configurations is that for bulk contacting (contacts 3-4) only the n-type branch is observed, while the surface-contact configuration (contacts 1-2) exhibits ambipolar behaviour. The shift in the charge neutrality point for the 3-4 contact case toward negative gate voltages could be a result of screening produced by the charged upper layers [123]. As has been documented before, defects between adjacent layers and the occurrence of local disorder may also influence the position of the resistance maximum. [125] For subsequent experiments, devices of the 1-2 contact configuration were utilized.

In order to improve the field-effect characteristics, we optimized the device configuration in a manner analogous to semiconductor device fabrication. After fabrication of a desired layout with surface contacts, a 750 nm wide strip is prepared by reactive ion etching with the help of a PMMA mask. The part of HOPG protected by the PMMA remains while the other parts of the crystallite are etched away. During the etching process, the argon:oxygen flow ratio was maintained at 100:11 (sccm) under 0.05 mbar

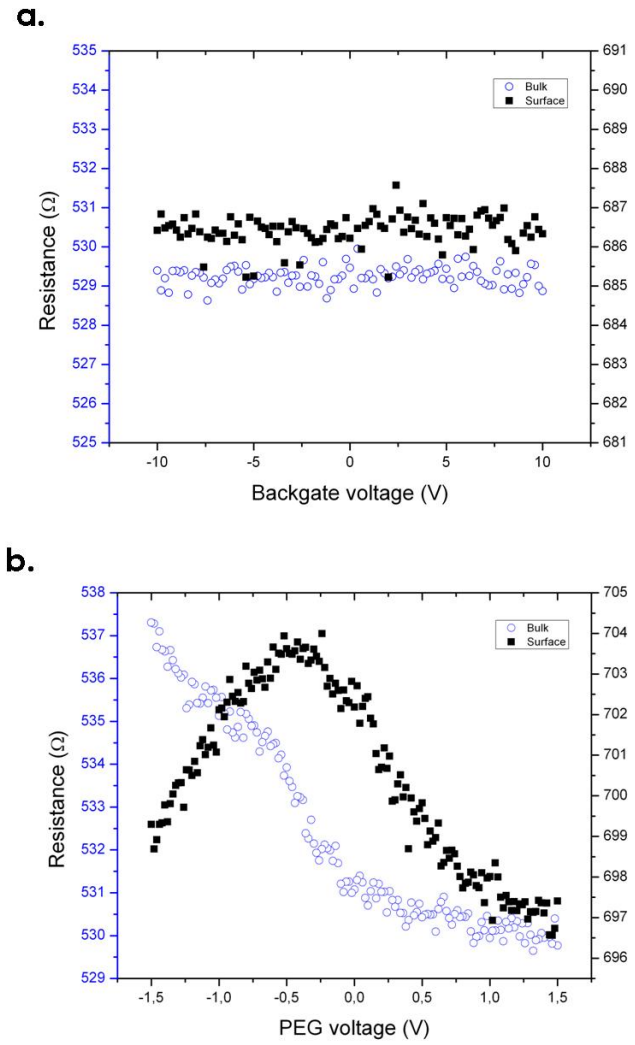


Figure 7.6: Gate dependence of resistance for the two configurations surface (1-2) on the right axis and bulk (3-4) on the left axis. (a) Backgate measurements show no field-effect.(b) Using a polymer-electrolyte gate (PEG) a field-effect can be observed in the same device.

pressure. The etching was carried out for 40 seconds at 60 W power. The AFM image of the etched HOPG strip in Figure 7.7(a). In order to ensure that the gating effects only the thin strip, the etched portions of the crystallite were passivated with a layer ( 40 nm) of $SiO_x$. The final device layout is shown in Fig 7.8(a). The transport characteristics of

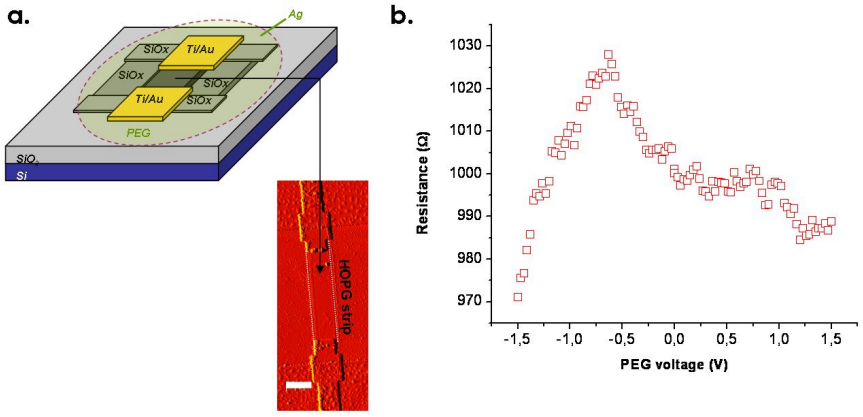


Figure 7.7: (a) Device layout showing a schematic of the transistor channel comprising a HOPG strip (AFM image in red) etched out of a graphitic crystallite. The etched regions are passivated by $SiO_x$. Scale bar is 740 nm. (b) Field-effect of the etched HOPG strip using a polymer electrolyte gate (PEG) showing a gate tunability of 10 percent.

this device configuration is shown in Fig. 7.7(b). A gate tunability of around 10 percent is apparent in this device with a field-effect mobility of 245 $cm^2/Vs$. This corresponds to an improvement in field-effect by an order of magnitude and an increase in field-effect mobility by almost 2 orders of magnitude. Higher gate tunabilities of up to 400 percent (i.e. ON/OFF ratio of 4) and field-effect mobilities in the order of a $10^2$ $cm^2/Vs$ were observed in other devices (figure 7.8), but this is a minority in our sample set.

In conclusion, an ambipolar field-effect in graphite crystallites has been demonstrated by engineering the injection of charge carriers into the uppermost layers and by utilising the polymer electrolyte gate. Towards this end we have shown the electronic decoupling between adjacent layers of graphite through careful control of contact engineering leading to controlled charge carrier injection either in the bulk or on the surface of the crystallite. As fabricated devices show a low ON/OFF ratio and a mobility of less than 10 $cm^2/Vs$. By optimizing the layout we have demonstrated that the gate tunability and the mobility can be improved. The configuration explained here has the important advantage that substrate-related effects can be efficiently screened by the bottom layers, [123] while the gating action takes place in the decoupled upper layers. The possibility of field-effect in graphite crystallites is expected to open avenues for a new field of graphite electronics. Further improvements of the device characteristics may be achieved through increased

electronic decoupling between the graphene layers, either by the use of intercalating agents or by the direct use of graphite intercalation compounds (GICs).

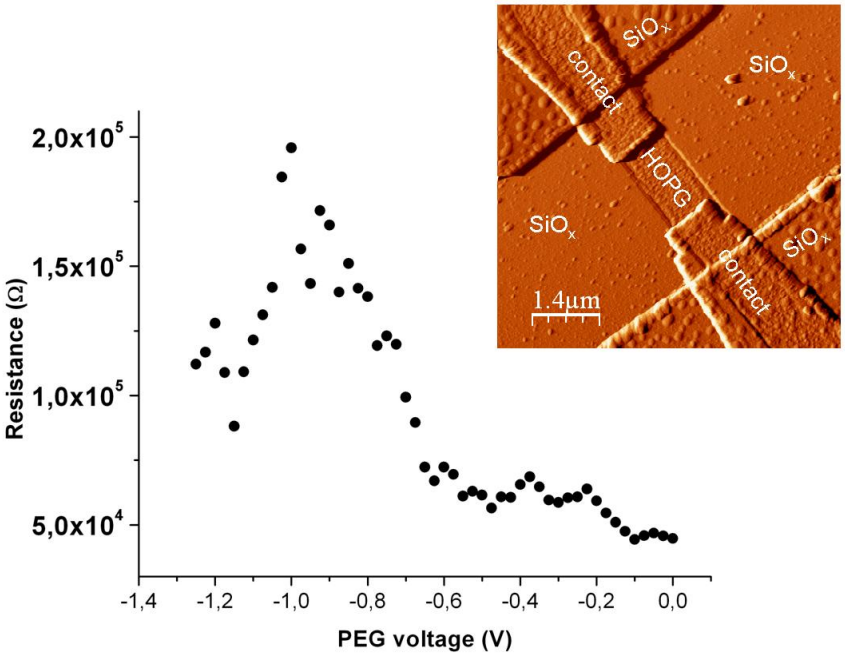


Figure 7.8: The top-gate dependence transport plot of the HOPG strip showing a gate tunability of 400 percent. Inset shows the AFM image of the device layout.

# Chapter 8

# Summary and Outlook

This thesis investigated graphene-based field effect transistors. Graphene was obtained via mechanical exfoliation and characterized phyiscially and electronically using state-of-the-art tools.

A novel lithographic method for fabricating graphene-based transistors on a lab scale was developed, which employed just one instrument. Additionally, the instruments also enabled the identification of graphene stacks of different heights, based on a caliberation system based on fluorescence quenching principle. It was shown that this technique can be adopted to all sources of graphene sheets, fabricated in any manner and on any substrate. On this basis, it was demonstrated that photolithography could be an alternate technology that can be pursued to attain graphene-based FETs.

The study of monolayer graphene-based FETs was extended to bilayers, where the difference in the stacking order of the two layers was investigated. When the graphene sheets are stacked on top of each other, the electronic structure of the system varies with the position of the subsequent sublattice atoms. It was found that deviation from the regular Bernal stacking electronically decouples the sheets from each other, which imparts effective electrostatic screening of the farther layer from the underlying backgate. Electrochemical top-gating was demonstrated as a means to selectively tune the charge carrier density in the decoupled upper layer. It was also shown that the mobility of the charge carriers was superior to similarly top-gated monolayer FETs.

While addressing the requirements of graphene-FETs to have an impact on real world electronics, an intrinsic gain of over one was shown in decoupled bilayer graphene devices, and also their incorporation into logical circuits like phase-shift detectors. This was identified as a critical step forwards towards graphene based circuits in the future. Fi-

nally, graphite-based FETs were investigated with special emphasis on design and charge injection sites to probe the possibility of field effect in such devices. Hitherto, only sample thickness and crystal defects were considered as critical factors in HOPG's electronic transport. The presented result showed an ambipolar field-effect behaviour in graphite, which was invoked by considering a suitable FET design.

**Outlook**

While fabricating graphene-based FETs using photolithography, high resolution structures down to a few hundreds of nanometers can be obtained by using UV laser sources, sub-diffraction limit exposure and high resolution photoresists. Additionally, using computerized scanning programs and simple image processing algorithms, the process can be almost completely automated, paving way for the realization of wafer scale graphene-based circuits and devices in a comparatively short time scale. This technique would be very practical to the research community in wake of the continual investigations that single and few layer graphene are currently being subjected to, in the laboratories around the world. From an application perspective, such possibility to promptly realize wafer-scale circuits could accelerate the entry of graphene-based devices into real-life applications.

Regarding graphite-based FETs, strategies to chemically decouple graphitic stacks are envisioned. Based upon the knowledge gained from few-layer behaviour in graphitic stacks, it should be possible to further enhance the on-off ratio if the graphitic layers are decoupled and fabricated with the top-gated configuration described.

Additionally, the contact resistance between the metallic source and drain contacts and the graphene channel is identified as an area where more detailed studies are needed. Until now, the lowest reported metal/graphene contact resistances are in the range 500 to 1000 $\Omega - cm$ [132, 133] which is about ten times the contact resistance of silicon MOSFETs [134] and also higher than that on carbon nanotubes [135]. Ohmic contacts are essential, particularly for short-channel devices, to preserve the carrier mobility. However, only a few studies dealing with metal/graphene contacts have been published [72,133,136] and more work is needed to understand the contact properties.

The biggest concern in the community, however, still remains that of the on/off ratio. The most popular method of introducing a bandgap into graphene for logic applications now is to create graphene nanoribbons. Nanoribbon MOSFETs with back-gate control and widths down to 5 nm have been operated as p-channel devices with on/off ratios of

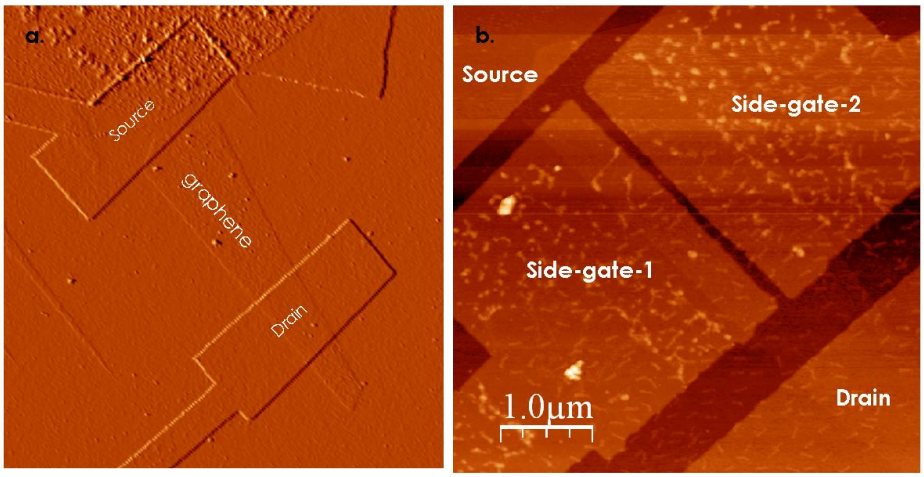


Figure 8.1: AFM images showing the fabrication steps on a graphene bilayer on $Si/SiO_2$ substrate, useful for confining the charge carriers into a pinched channel. (a) The graphene sheet on $Si/SiO_2$ substrate. (b) Close-up image of the graphene channel after fabrication of the side-gates.

up to $10^6$ [129, 130]. Such high ratios have been obtained despite simulations showing that edge disorder leads to an undesirable decrease in the on-current and a simultaneous increase in the off-current of nanoribbon MOSFETs [137, 138]. Though the on/off ratio would endorse the suitability of nanoribbon FETs in logic applications, these devices had relatively thick back-gate oxides, such that voltage sweeps of several volts were needed for switching, which is significantly more than the sweeps of 1 V needed to switch Si CMOS devices [2]. Furthermore, CMOS logic requires both n-channel and p-channel FETs with well-controlled threshold voltages, and graphene FETs with such properties have not yet been achieved. A top-gated nanoribbon FET would be a recommendation. Recently, the first graphene nanoribbon MOSFETs with top-gate have been reported [18]. These transistors comprise a thin high-dielectric-constant (high-$\kappa$) top-gate dielectric (2 nm of $HfO_2$), a room-temperature on/off ratio of 70, as well as an outstanding transconductance of 3.2 mS/m (exceeding the transconductances reported for both state-of-the-art silicon MOSFETs and $III-V$ HEMTs).

An alternative approach would be to electrostatically confine the charge carriers in bilayer graphene by using side gates. Such a device is exemplified in Figure 8.1. Here, a large graphene sheet on a $Si/SiO_2$ substrate was provided with a thin layer of 5 nm

$SiO_x$ dielectric on top and 20 nm Au side gates. Such a configuration may enable "pinching" the charge carrier channel into an area comparable to that found in nanoribbons. However, an additional perpendicular electric field might be required enable sufficient bandgap opening. As fabrication of mass-scale nanoribbons is yet to be accomplished, suitable gating design on the large-area graphene could do be a smart alternative.

### Other Applications

Owing to its unique optoelectronic properties, graphene is an interesting material for photovoltaics. Other than being a transparent electrode as a direct replacement for Indium Tin Oxide (ITO), its electronic properties can also be utilised.

Previous works [72, 74, 75, 80] show that the metal contacts dope graphene. The doping of graphene is dependent on the metal used – as depending on the work function of the metal, graphene can either be p-doped or n-doped. Usually on global illumination of a graphene FET made of same metal contacts, the built-in electric field profile in the channel between the electrodes is symmetric and the total photocurrent is zero. However, if two different metals are used on the same graphene sheet, the different doping allows for a p-n junction to generate a short-circuit current. Figure 8.2(a) shows the photocurrent

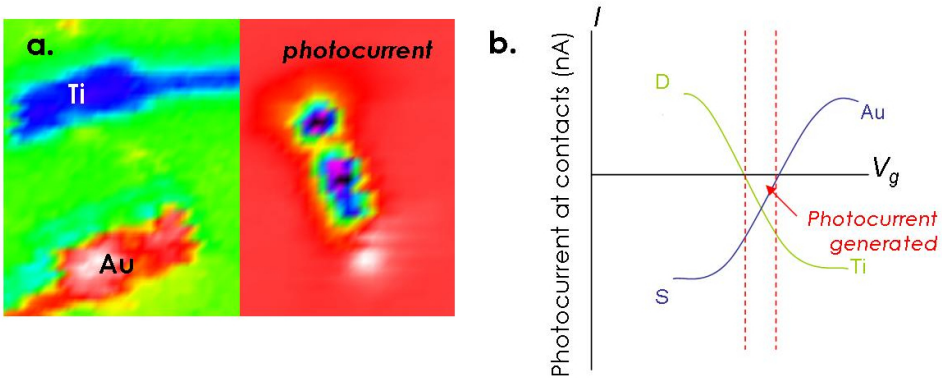


Figure 8.2: (a) Reflection image of the graphene FET under SPCM and the corresponding photocurrent response at a suitable voltage where the photocurrents from the individual contacts sum up to give a photocurrent (in nanoamperes range). Operation was done under zero bias. (b) Schematic explaining the photocurrent generated at the contacts on varying the gate voltage.

response recorded by SPCM on such a graphene FET with two different metals as contacts. The contacts were chosen as Ti and Au, as the former n-dopes graphene and the latter p-dopes graphene [75]. On choosing an appropriate gate voltage, the photocurrents can flow in the same direction, leading to an enhanced overall photocurrent (see Figure 8.2(b)). The photovoltage generated in this manner could be enhanced by careful modification of the metal contact area under the graphene, paving novel photovoltaic cells based on graphene. Work in this direction is underway [139], and the optoelectronic properties of graphene could harbinger a new breed of photovoltaics.

**Final remarks**

As graphene-based nanoelectronics is still in its infancy to make any valid conclusions as there is very long way to go before it can challenge the 50-odd year old CMOS technology.

That said, concepts that have been investigated for many years now, like spin transistors or molecular devices, seem to be farther from real application when you compare them to advancements in graphene, and it is not clear if they will ever reach the production stage. It has become clear that graphene devices based on the conventional MOSFET principle suffer from some fundamental problems and still certain principle questions like on/off ratios and mass-scale production need to be tackled. However, it is worth remembering that the research on graphene is addressed as a *replacement* technology. This or even the more novel and alternate FET designs like tunnel FETs and bilayer pseudospin FETs would have to outperform CMOS technology by many orders to replace an *existent* technology, which has a whole industry invested in it.

At the moment though, it would not be possible to say which (if any) of the alternative device concepts being considered will replace conventional transistors. Nonetheless, the latest ITRS roadmap [2] strongly recommends intensified research into graphene, and even envisions a research and development schedule for carbon-based nanoelectronics.

The work in this field is only beginning. And the expectations are high.

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# Publications

**"Graphite field-effect transistor"**
A. Sagar, K. Balasubramanian, M. Burghard and K. Kern
*Manuscript submitted* (2011).

**"Polymer-electrolyte gated graphene transistors for analog and digital phase detection"**
A. Sagar, K. Balasubramanian, M. Burghard, K. Kern and R. Sordan
*Appl. Phys. Lett.* **99**, 043307 (2011).

**"Marker-free on-the-fly fabrication of graphene devices based on fluorescence quenching"**
A. Sagar, K. Kern and K. Balasubramanian
*Nanotechnology* **21**, 015303 (2010).

**"Effect of stacking order on the electric-field induced carrier modulation in graphene bilayers"**
A. Sagar, E.J.H. Lee, K. Balasubramanian, M. Burghard and K. Kern
*Nano Letters* **9**, 3124 (2009).

**"Catalyst patterning for carbon nanotube growth on elevating posts by self-aligned double-layer electron beam lithography"**
M. Häffner, A. Heeren, A. Haug, E. Schuster, A. Sagar, M. Fleischer, H. Peisert, M. Burghard, T. Chassé and D.P. Kern
*J. Vac. Sci. Technol. B* **26**, 2447 (2008).

**"Strong p-type doping of individual carbon nanotubes by Prussian blue functionalization"**

A. Forment-Aliaga, R.T. Weitz, A. Sagar, E.J.H. Lee, M. Konuma, M. Burghard and K. Kern

*Small* **4**, 1671 (2008).

# Curriculum Vitae

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| Name | Adarsh Singh Sagar |
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| 2005-2007 | Masters from the Materials Science and Engineering Department of Drexel University, Philadelphia, USA. **Thesis Title**: "Mechanochemical Synthesis of Fenofibrate Nanoparticles" (Thesis Director: Prof. Yury Gogotsi) |
| 2001-2005 | Bachelors from the Metallurgy and Materials Technology Department of Jawaharlal Nehru Technological University, Hyderabad, India. **Thesis Title**: "Synthesis and Characterization of Carbon Nanotubes by Open-arc method" (Thesis Director: Dr. Anil Kumar, DRDO) |

**Professional Experience**

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| 2005-2007 | Research Assistant at Drexel Nanotechnology Institute, Philadelphia, USA. **Field of Research**: Mechanochemical synthesis, Characterization of carbon nanomaterials using Raman and Electron Microscopy |
| 2006 | Fellow in the Department of Chemical and Biomolecular Engineering of the University of Melbourne. **Field of Research**: Drug nanodispersions and nano-particle synthesis |
| 2006-2007 | Teaching Assistant in the Materials Science and Engineering Department of Drexel University, Philadelphia, USA. Lectured and demonstrated to 300 undergraduate engineering students about electrical and corrosion properties of materials |

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