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Numerical analysis of capacitance compact models for organic thin-film transistors

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ABSTRACT

Analytical expressions for the gate-voltage dependence of the channel capacitance and the gate-to-contacts overlap capacitances in top-contact organic thin-film transistors (OTFTs) are derived and implemented in an organic compact capacitance model. The resulting modified model is verified by experimental data of transistors with constant mobility. The same model is analyzed by numerical simulations for OTFTs with a voltage-dependent mobility. The simulation results indicate that the quasistatic model describes well the simulated capacitances. In accumulation, the modeled values are slightly overestimated because of the generally accepted assumption of the charge-sheet model. It is also demonstrated that the quasistatic regime occurs at lower frequencies because of the reduced mobility at lower charge carrier concentrations.

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1. Introduction

In recent years substantial efforts have been made in the fabrication and performance of discrete OTFTs. For commercial applications of these transistors in organic integrated circuits reliable compact models that allow the description of the electrical transistor behavior are required. The static properties are described by current–voltage (I–V) characteristics. Therefore, several DC models were developed and verified by experimental data [1–7]. In these models the increase of the mobility with the gate-source voltage was considered. Whereas in [2,4,7] this mobility model was explained by the charge trapping in deep tails of distributed states described by Shur and Hack [8], in [1,3,5,6] the model of the variable range hopping (VRH) in an exponential distributed density of states (DOS) [9] was assumed.

The dynamic behavior is determined by the intrinsic and parasitic capacitances so that capacitance models are necessary for the description. Contrary to the DC models, the developed capacitance compact models of organic transistors were not verified by experimental data since measurements of OTFTs in the quasistatic regime were not available [1,3,5,10,11]. The common point of these models is again the consideration of the special mobility dependence on the gate-source voltage. As a consequence, similar expressions have been derived with minor diverging model parameters. This is confirmed in [11] where the therein derived expressions are compared to the results given in [1]. Differences of the models are related to the consideration of the overlap regions. For instance, no expressions for the overlap capacitance are given in [1,3,5]. In contrast, in [11,10] this capacitance is discussed

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more in detail but gate- and drain-voltage-independent equations are finally assumed. Such expressions are only valid in a source/drain (S/D) bottom-contact configuration. However, OTFTs are often prepared in a bottom-gate and S/D top-contact (TOC) design as it offers a reduced contact resistance [12,13]. In this configuration the S/D contacts are on top of the organic layer with the result that the overlap capacitances are voltage-dependent.

In [17] the measured gate-source (C_{gs}) and gate-drain (C_{gd}) capacitances of the prepared OTFT with constant mobility were modeled assuming the simple Meyer's capacitance model [18] and constant overlap capacitances despite of the TOC design.

In this paper, we derive an expression to consider the gate- and drain-voltage dependence of the gate-to-contacts overlap capacitances in S/D TOC transistors. This equation and a gate-voltage dependent channel capacitance (an expression similar to the one in [18]) are implemented in the organic capacitance model of [11] originated from the DC model in [6] in which the mobility enhancement factor is explained either by charge trapping or by VRH in an exponential DOS. The influence of contact resistance effects, such as described in [14–16], are not considered in this paper.

For organic transistors with a constant mobility, the modified model is verified against experimental data adopted from [17]. For transistors with a voltage-dependent mobility, the model of Marinov and Deen [11] is verified by two-dimensional device simulations in the quasistatic regime. For this purpose, the voltage-dependent mobility model for VRH in an exponentially distributed DOS [19] was implemented in the Sentaurus Device simulator [20]. Furthermore, the frequency dependence of the transistor capacitances was investigated by the simulation. From these results, the frequency was estimated up to which the quasistatic assumption is valid for the OTFT.

2. Transistor fabrication

OTFTs in a bottom-gate/top-contact design are prepared on an alkali-free glass substrate covered with a thin (4 nm) adhesion layer of aluminum oxide [17]. The hybrid dielectric on top of the aluminum gate consist of an oxygen-plasma-grown AlO_x layer (3.6 nm-thick) and a solution-processed self-assembled monolayer (SAM) of n-tetradecylphosphonic acid (1.7 nm-thick). The active layer of the OTFT, namely the 11-nm-thick organic semiconductor (OSC) dinaphto[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) [21] and finally 25-nm-thick gold S/D contacts were evaporated through silicon stencil masks [22]. The transistors have a channel length and width of $L = 200\ \mu m$ and $W = 400\ \mu m$, respectively. The gate-to-source (L_{gs}) and gate-to-drain (L_{gd}) overlaps are symmetrical with $L_{gs} = L_{gd} = 10\ \mu m$.

3. Simulation method

Numerical simulations have been carried out with the Sentaurus Device simulator solving the Poisson and continuity equations [20]. To investigate the OTFT capacitances a small-signal analysis was performed. In this case, the response of the device to small sinusoidal signals superimposed upon an established DC bias is computed as a function of frequency and DC operating point. The result is a complex admittance matrix. The simplified simulated structure is shown in the inset of Fig. 1. The used parameters are summarized in Table 1. The values for the relative permittivity of the insulator, the DNTT thickness and the doping concentration were extracted from the measured capacitance–voltage curve for a drain-source voltage $V_{DS} = 0$ V (shown in [17]). The concentration of fixed interface states was assumed to fit the flat-band voltage (V_{FB}). With the given parameters and $V_{TH} = V_{FB} + eN_A d/C''_{is}$ a threshold voltage of $V_{TH} = -1.2$ V results. C''_{is} is the insulator capacitance per area. The intrinsic mobility was estimated from measured current–voltage characteristics of the OTFT [17]. For these transistors no dependence of the mobility on the gate-source voltage was observed.

For the investigation of the capacitance model derived in [11], the voltage-dependent mobility model described in [19] was implemented. This model is based on the hopping model of [9] only modified by the lateral field dependence.

4. Experimental and simulated results

As described above, in [17] the measured capacitances of the OTFTs were modeled with the Meyer's capacitance model [18]. Here, the quasistatic capacitance model

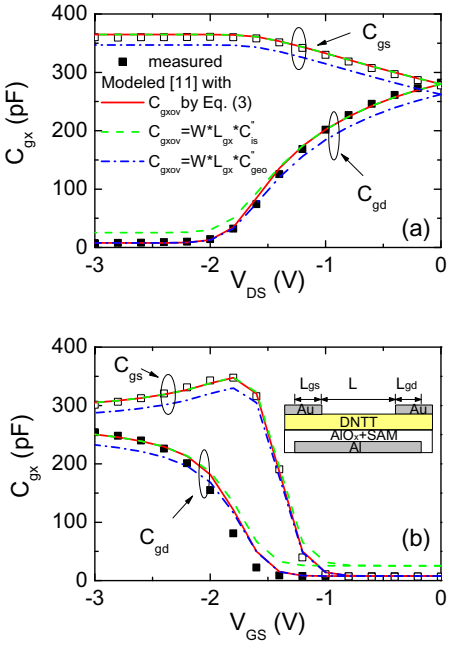

Fig. 1. Data adopted from [17] at a frequency of $f = 500$ Hz and modeled quasi-static gate-source (C_{gs}) and gate-drain (C_{gd}) capacitances as a function of V_{DS} with $V_{GS} = -3$ V (a) and V_{GS} with $V_{DS} = -0.5$ V (b), respectively. Lines represent the model by [11] including the voltage dependence of the channel capacitance, a constant fringe part of 13% and the indicated equations of the overlap capacitances. The inset shows the OTFT schematic representation used for the simulation.

Table 1
Simulation parameters.

Parameter	Symbol	Value
Al-gate work function	ϕ_{Al}	4.1 eV
Au-contacts work function	ϕ_{Au}	5.0 eV
Hybrid dielectric thickness	d_{is}	5.3 nm
Dielectric rel. permittivity	ε_{is}	3.37
DNTT affinity	χ	1.81 eV
DNTT band gap	E_G	3.38 eV
DNTT relative permittivity	ε	3
DNTT thickness	d	11 nm
DNTT intrinsic mobility	μ	2.1 $cm^2/V\,s$
DNTT doping concentration	N_A	10^{16} cm^{-3}
Fixed interface charges	N_{if}	1.1×10^{12} cm^{-2}

described in [11] will be applied. This model is based on the voltage-dependent mobility given in [6]

$$\mu = \mu_0 (V_{GS} - V_{TH})^{\left(\frac{2T_0}{T}-2\right)} = \mu_0 (V_{GS} - V_{TH})^{\gamma} \tag{1}$$

with the gate-source voltage V_{GS}, the threshold voltage V_{TH} and the mobility at a low carrier concentration μ_0. The parameter T_0 (and accordingly γ) describes the steepness of the exponentially distributed DOS

$$\mathrm{DOS}(E) = \frac{N_s}{E_0} \exp\left(\frac{E - E_{ref}}{E_0}\right) \tag{2}$$

where N_s is the concentration of states, E_{ref} is the conduction (or valence) band edge and E_0 is the effective energy width $E_0 = kT_0$. The resulting quasistatic gate charge is given by (Eq. (18) in [11])

$$Q_G = \pm C_{G0} \left(\frac{2+\gamma}{3+\gamma}\right) \frac{V_{GTS}^{3+\gamma} - V_{GTD}^{3+\gamma}}{V_{GTS}^{2+\gamma} - V_{GTD}^{2+\gamma}} \tag{3}$$

with the overdrive voltages $V_{GTS} = V_G - V_T - V_S$ and $V_{GTD} = V_G - V_T - V_D$ and the capacitance $C_{G0} = WLC''_{is}$. The intrinsic capacitances C_{GG} and C_{GD} are the derivatives of this charge with respect to the terminal voltages resulting in Eq. (23) and (24) in [11]:

$$\frac{C_{GG}}{C_{G0}} = \left(\frac{2+\gamma}{3+\gamma}\right)\left(\frac{1-\zeta^{3+\gamma}}{1-\zeta^{2+\gamma}}\right)\left[1 + (1-\zeta) \times \frac{(2+\gamma)\zeta^{1+\gamma}}{1-\zeta^{2+\gamma}}\right] - (1-\zeta)\frac{(2+\gamma)\zeta^{1+\gamma}}{1-\zeta^{2+\gamma}} \tag{4}$$

$$\frac{C_{GD}}{C_{G0}} = \left(\frac{2+\gamma}{3+\gamma}\right)\left(\frac{1-\zeta^{3+\gamma}}{1-\zeta^{2+\gamma}}\right) \times \left[\frac{(2+\gamma)\zeta^{1+\gamma}}{1-\zeta^{2+\gamma}}\right] - \frac{(2+\gamma)\zeta^{1+\gamma}}{1-\zeta^{2+\gamma}} \tag{5}$$

with $\zeta = V_{GTD}/V_{GTS}$. The capacitance C_{GS} is obtained from $C_{GG} = C_{GD} + C_{GS}$.

In the case of a constant mobility ($\gamma = 0$), the derived expressions for the capacitances reduce to the ones of the Meyer model and the experimental curves can be well described as shown in [17]. Nevertheless, the curves will be shown once more to demonstrate the quality of the voltage-dependent expressions of the channel and overlap capacitances.

4.1. Channel and overlap capacitances

In the model of [11] the channel capacitance C_{G0} is related to the insulator capacitance but this is only valid for accumulation at the insulator interface. In depletion, the channel capacitance C_{ch} is reduced. Therefore, we introduce a gate-voltage dependent expression equal to the first summand of Eq. 6 with $V_X = 0$ (similar to the one in [18,3]) for C_{ch} instead of C_{G0} to describe correctly the decrease of the gate-source capacitance near and below the threshold voltage.

Furthermore, the extrinsic capacitances due to the overlap regions of the gate with source (C_{gsov}) and drain (C_{gdov}) will be considered. These capacitances have to be added to the respective intrinsic capacitances. In [10] these capacitances are calculated with $C_{ov} = WL_{ov}C''_{is}$, only valid for a S/D bottom contact structure. Contrary, in [17] the series connection of the insulator capacitance with the one of the fully depleted semiconductor (C_{geo}) of the contact region is used for the S/D TOC OTFT. However, in this configuration a transition from the maximum capacitance C''_{is} down to the minimum value C''_{geo} depending on the operation regime of the OTFT occurs. Consequently, here we introduce an expression similar to the voltage dependence of the channel capacitance for the overlap capacitances

$$C''_{ov} = \frac{C''_{is}}{1 + \exp\frac{V_{GT} - V_X - V_\delta}{V_{SS}}} + \frac{C''_{geo}}{1 + \exp -\frac{V_{GT} - V_X - V_\delta}{V_{SS}}} \tag{6}$$

where $V_{GT} = V_{GS} - V_{TH}$ and V_δ is a voltage fit parameter. The voltage $V_X = 0$ or $V_X = V_{DS}$ for the overlap capacitances gate to source ($C_{gsov} = WL_{gs}C''_{gsov}$) and gate to drain ($C_{gdov} = WL_{gd}C''_{gdov}$), respectively. V_{SS} is a voltage parameter introduced in [6] describing the inverse subthreshold slope. The parameter V_δ is introduced since depletion at the insulator interface and associated with it the decrease of the channel and overlap capacitances occurs above the threshold voltage.

Fig. 1 shows the measured capacitances at $f = 500$ Hz along with the quasistatic curves calculated with the modified model in [11] for constant mobility ($\gamma = 0$). The prepared OTFT works in the quasistatic regime at this frequency (see below). The modeled curves include the sum of the intrinsic and parasitic components. A contribution of about 13% was assumed for the fringe part. The transition into the subthreshold region is well described by the included gate-voltage dependent channel capacitance. The curves differ in the assumed model for the overlap capacitances. Applying the constant insulator capacitance (dashed green lines), the influence of the overlap regions is overestimated whenever depletion of the semiconductor occurs in the contact regions. This is the case at low gate-source voltages (subthreshold) or at high negative drain voltages (saturation). Using the geometric capacitance (blue dash-dotted lines) smaller values are calculated for the linear operation regime of the OTFT. In the latter case a fit to the measured curves is possible by increasing the fringe factor. However, as a consequence, the parasitic components are not exactly described. On the contrary, the modeled curves including Eq. (6) with $V_{TH} = -1.2$ V, $V_{SS} = 0.1$ V and $V_\delta = 0.2$ V fit very well the

measured capacitances. This is also visible in Fig. 2 where the curves at different bias conditions are shown. Consequently, the Marinov/Deen model, modified by the new expression of the channel capacitance, describes well OTFTs with constant mobility. But for the S/D TOC design one has to include additionally the voltage-dependent expressions for the overlap regions (Eq. 6) to model correctly all the operation regimes of the transistors. The analysis of the model for OTFTs with a voltage-dependent mobility is presented in the following section.

4.2. Influence of voltage-dependent mobility

The influence of a voltage-dependent mobility on the intrinsic capacitances of an OTFT is described in detail in [11]. In conclusion, with increasing mobility enhancement factor γ the gate-source capacitance increases and the gate-drain capacitance decreases. Since measurements in the quasistatic regime for OTFTs with voltage-dependent mobility are not available yet, the applicability of the model will be investigated by numerical simulation.

As given with Eq. (1), the parameter γ increases for a broader DOS distribution. As justified below, the quasistatic assumption for OTFTs with voltage-dependent mobility is only valid at lower frequencies. Therefore, numerical simulations at a frequency of $f = 1$ Hz applying the mobility model described in [19] with $T_0 = 600$ K ($\gamma = 2$) have been carried out. Further used mobility parameters are $B_c = 2.8$ corresponding to the formation of an infinite cluster and the inverse decay length of the wave function $\alpha = 0.58 \times 10^8$ cm^{-1}. The prefactor $\sigma_0 = 1.5 \times 10^8$ S/cm was used to get a mobility of about 2 cm^2/V s at an applied gate-source voltage of -3 V. In Fig. 3 the simulated capacitances are compared to the results obtained for the model [11] including the voltage dependence of the channel and overlap capacitances. To model the capacitance in the accumulation region, the generally accepted approximation of a conductive sheet near the interface to the dielectric is assumed. Consequently, the low-frequency MIS (metal–insulator–semiconductor) capacitance is close to the dielectric capacitance C_{is}. However, in the real device there is a distribution of mobile carriers with depth also in accumulation. This distribution is accurately simulated and therefore the capacitances are a little bit smaller than the dielectric capacitance because of the series connection with the semiconductor capacitance. For this reason, the values of the modeled gate-source capacitances were divided by a factor of 1.06 ... 1.08 to better fit the simulated curves. With exception of this peculiarity, the modeled curves describe well the simulated capacitances. Therefore at low frequencies, the model of Marinov/Deen [11] extended by analytical expressions for the channel and overlap capacitances can also be applied for organic transistors with bias-dependent mobility. However, one has to investigate up to which frequency quasistatic behavior occurs.

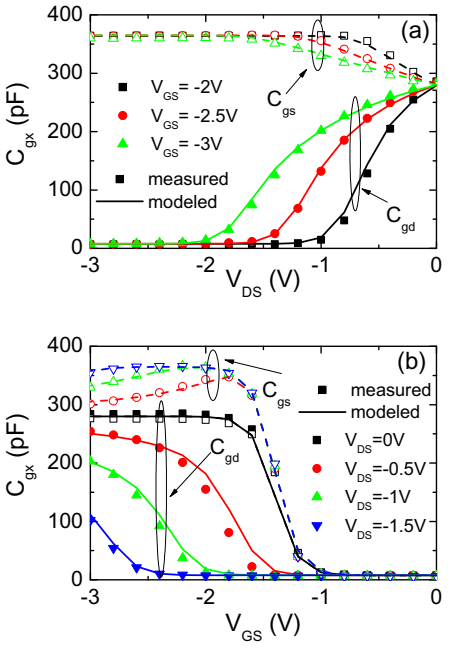

Fig. 2. Data adopted from [17] at a frequency of $f = 500$ Hz and modeled quasi-static gate-source (C_{gs}) and gate-drain (C_{gd}) capacitances as a function of V_{DS} (a) and V_{GS} (b), respectively. Lines represent the model by [11] including the voltage dependence of the channel capacitance, a constant fringe part of 13% and the overlap capacitances calculated by Eq. (6).

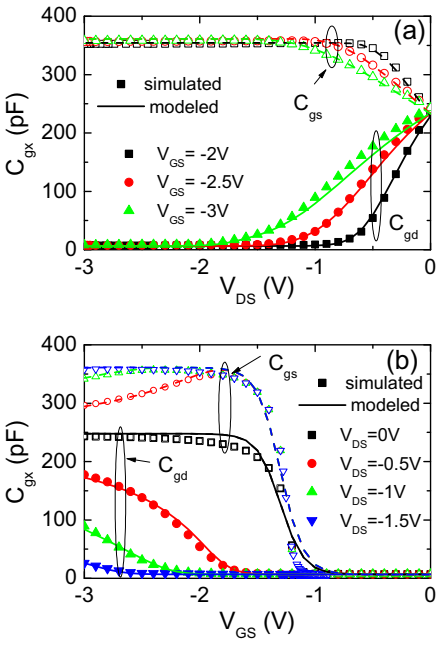

Fig. 3. Simulated ($f = 1$ Hz) and modeled quasi-static gate-source (C_{gs}) and gate-drain (C_{gd}) capacitances as a function of V_{DS} (a) and V_{GS} (b), respectively. Lines represent the model by [11] including the voltage dependence of the channel capacitance and the overlap capacitances calculated by Eq. (6). The modeled gate-source capacitance is divided by a factor of about 1.06 ... 1.08 to better fit the simulated curves. This is because the simulation takes into consideration an additional series capacitance owing to the distribution of mobile carriers with depth in the DNTT also in accumulation.

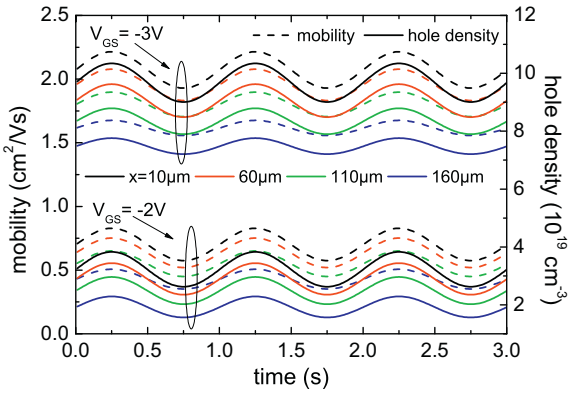

Fig. 4. Simulated low-frequency ($f = 1$ Hz) values of the mobility (dashed lines) and hole density (solid lines) near the interface to the dielectric and different positions along the channel for $V_{DS} = -0.5$ V and different V_{GS}. The position $x = 10$ µm is directly at source and the middle of the channel is at $x = 110$ µm.

4.3. Frequency dependence of the capacitances

In Fig. 4 simulated low-frequency values of the mobility and hole density near the interface to the dielectric are shown to demonstrate what the peculiarity in the case of a voltage-dependent mobility is. To get these results, a sinusoidal signal was applied at source superimposed upon the established DC bias. At $V_{GS} = -3$ V, the average value of the mobility near source ($x = 10$ µm) is about 2 cm^2/V s. At the lower negative gate-source voltage, but even in accumulation, the mobility at this position is reduced by a factor of about 3. Furthermore, since the hole density (solid lines) depends on the position along the channel also the mobility (dashed lines) is position dependent at both gate bias. Therefore, a modified frequency behavior of the capacitances compared to the case of constant mobility is expected.

To verify this prediction a small-signal analysis with the device simulator was performed. Fig. 5 shows the simulated capacitances at different frequencies for OTFTs with both a constant mobility and a voltage-dependent mobility. Comparing figure (a) and (b), the above-described tendencies regarding the influence of the mobility enhancement factor are visible. At the highest gate-source voltage C_{gs} is higher in figure (b) whereas C_{gd} is smaller. As expected for an applied drain-source voltage, in both cases for γ the gate-drain capacitance is smaller than the gate-source one and noticeable influence on C_{gd} occurs for frequencies $f > 1$ kHz. Contrary, the simulated gate-source capacitances depend strongly on the used mobility model. For OTFTs with a constant mobility, a negligible difference is simulated between the curves at 1 Hz and 500 Hz so that quasistatic behavior can be assumed also for the higher frequency. But in transistors with a voltage-dependent mobility, the gate-source capacitance at 500 Hz is strongly reduced for negative gate-source voltages smaller than 2 V. The reason is the above-described lower mobility at these gate biases resulting in a higher time constant. Since $C_{gs} = -\partial Q_G/\partial V_S$ the variation of the gate charge caused by a sinusoidal signal at source should be frequency

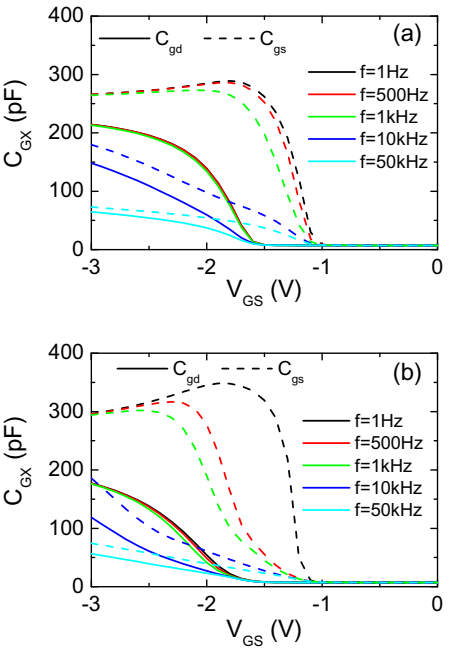

Fig. 5. Simulated gate-source (C_{gs}) and gate-drain (C_{gd}) capacitances at different frequencies for $V_{DS} = -0.5$ V as a function of V_{GS} for constant ($\gamma = 0$) (a) and voltage-dependent mobility ($\gamma = 2$) (b).

dependent. This effect is shown in Fig. 6. For the depicted frequencies, no difference in the charge variation is simulated in transistors with a constant mobility. However, in OTFTs with a voltage-dependent mobility, the accumulated charges cannot follow the signal. Therefore, as the frequency increases, the gate charge variation reduces and a phase shift occurs resulting in reduced gate-source capacitances.

In conclusion, in the case of the assumed mobility parameters, the transistor works in the quasistatic regime up to a frequency of only 1 Hz. Since some of the material and device parameters (doping concentration, flat-band voltage) can only be estimated from quasistatic CV curves,

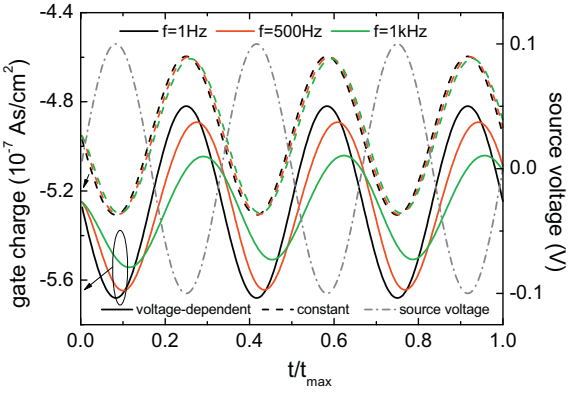

Fig. 6. Simulated gate charge for $V_{GS} = -2$ V and $V_{DS} = -0.5$ V as a function of time (time divided by maximum time for three periods) with sinusoidal signal applied at source.

measurements at these frequencies would be necessary. In addition, hopping transport occurs in materials with lower mobility than the one assumed in this simulation resulting in lower frequencies for the quasistatic regime. Therefore it should be difficult to measure the quasistatic CV curves for such materials.

5. Conclusion

We have modified the capacitance model in [11] by implementation of analytical expressions for the channel and overlap capacitances of the TOC OTFT. In the case of OTFTs with constant mobility, the resulting model was verified by a comparison with measured capacitance curves in all operation regions. A better fit compared to that of other models was achieved. At present, measured capacitances in OTFTs with voltage-dependent mobility are not available. Therefore, we verify the complete model (including the overlap regions) by numerical simulation of an organic transistor in TOC design including the mobility model described in [19]. It was shown that the modeled curves describe well the simulated capacitances at low frequencies. Small differences have been noted in accumulation owing to the usual approximation of a conductive sheet near the interface to the dielectric, which results in a negligible error of the modeled curves ($< 8\%$). Furthermore, an investigation of the frequency dependence of the capacitances has been performed. The comparison of simulated capacitances shows a reduced frequency limit assuming a voltage-dependent mobility compared to the case of a constant value. The reason is the reduced mobility because of the lower hole concentration for smaller negative gate voltages. Future measurements of solution-based OTFT with the hopping process as transport mechanism have to show, whether the used mobility model is valid or not. In particular, the continuous decrease of the mobility for strongly reduced carrier concentrations is disputable.

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References

[1] E. Calvetti, L. Colalongo, Zs. M. Kovács-Vajna, Organic thin film transistors: a DC/dynamic analytical model, Solid-State Electron. 49 (2005) 567–577.
[2] M. Estrada, A. Cerdeira, J. Puigdollers, L. Reséndiz, J. Pallares, L.F. Marsal, C. Voz, B. Iñiguez, Accurate modeling and parameter extraction method for organic TFTs, Solid-State Electron. 49 (2005) 1009–1016.
[3] M. Fadlallah, G. Billiot, W. Eccleston, D. Barclay, DC/AC unified OTFT compact modeling and circuit design for RFID applications, Solid-State Electron. 51 (2007) 1047–1051.
[4] B. Iñiguez, R. Picos, D. Veksler, A. Koudymov, M.S. Shur, T. Ytterdal, W. Jackson, Universal compact model for long- and short-channel thin-film transistors, Solid-State Electron. 52 (2008) 400–405.
[5] F. Torricelli, Zs. M. Kovács-Vajna, A charge-based OTFT model for circuit simulation, IEEE Trans. Electron. Dev. 56 (2009) 20–30.
[6] O. Marinov, M.J. Deen, U. Zschieschang, H. Klauk, Organic thin-film transistors: Part I: Compact DC modeling, IEEE Trans. Electron. Dev. 56 (2009) 2952–2961.
[7] C.H. Kim, A. Castro-Carranza, M. Estrada, A. Cerdeira, Y. Bonnassieux, G. Horrowitz, B. Iñiguez, A compact model for organic field-effect transistors with improved output asymptotic behaviors, IEEE Trans. Electron. Dev. 60 (2013) 1136–1140.
[8] M.S. Shur, M. Hack, Physics of amorphous silicon based alloy field-effect transistors, J. Appl. Phys. 55 (1984) 3831–3842.
[9] M. Vissenberg, M. Matters, Theory of the field-effect mobility in amorphous organic transistors, Phys. Rev. B, Condens. Matter 57 (1998) 12964–12967.
[10] A. Castro-Carranza, M. Estrada, J.C. Nolasco, A. Cerdeira, L.F. Marsal, B. Iñiguez, J. Pallarès, Organic thin-film transistor bias-dependent capacitance compact model in accumulation regime, IET Circ. Dev. Syst. 6 (2012) 130–135.
[11] O. Marinov, M.J. Deen, Quasistatic compact modelling of organic thin-film transistors, Org. Electron. 14 (2013) 295–311.
[12] D.J. Gundlach, L. Zhou, J.A. Nichols, T.N. Jackson, P.V. Necliudov, M.S. Shur, An experimental study of contact effects in organic thin film transistors, J. Appl. Phys. 100 (2006) 024509-1–024509-13.
[13] S. Scheinert, G. Paasch, Interdependence of contact properties and field- and density-dependent mobility in organic field-effect transistors, J. Appl. Phys. 105 (2009) 014509-1–014509-9.
[14] Ch. Liu, Y. Xu, G. Ghibaudo, X. Lu, T. Minari, Y.-Y. Noh, Evaluating injection and transport properties of organic field-effect transistors by the convergence point in transfer-length method, Appl. Phys. Lett. 104 (2014) 013301.
[15] J.A.J. Tejada, J.A.L. Vilanueva, P.L. Varo, K.M. Awawdeh, M.J. Deen, Compact modeling and contact effects in thin film transistors, IEEE Trans. Electron. Dev. 61 (2014) 266–277.
[16] O. Marinov, M.J. Deen, C. Feng, Y. Wu, Precise parameter extraction technique fr organic thin-film transistors operating in the linear regime, J. Appl. Phys. 115 (2014) 034506.
[17] T. Zaki, S. Scheinert, I. Hörselmann, R. Rödel, F. Letzkus, H. Richter, U. Zschieschang, H. Klauk, J. Burghartz, Accurate capacitance modeling an characterization of organic thin-film transistors, IEEE Trans. Electron. Dev. 61 (2014) 98–104.
[18] T. Ytterdal, Y. Cheng, T. Fjeldly, Device Modeling for Analog and RF CMOS Circuit Design, John Wiley & Sons Ltd., Chichester, West Sussex, 2003.
[19] B.N. Limketkai, P. Jadhav, M.A. Baldo, Electric-field-dependent percolation model of charge-carrier mobility in amorphous organic semiconductors, Phys. Rev. B 75 (2007) 113203.
[20] Sentaurus Device User Guide, Version G-2012.06 (Synopsys2012).
[21] U. Zschieschang, F. Ante, D. Kälblein, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Someya, J. Blochwitz-Nimoth, H. Klauk, Dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) thin-film transistors with improved performance and stability, Org. Electron. 12 (2011) 1370–1375.
[22] F. Ante, D. Kälblein, T. Zaki, U. Zschieschang, K. Takimiya, M. Ikeda, T. Sekitani, T. Someya, J.N. Burghartz, K. Kern, H. Klauk, Contact resistance and megahertz operation of aggressively scaled organic transistors, Small 8 (2012) 73–79.