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Spatial control of the threshold voltage of low-voltage organic transistors by microcontact printing of alkyl- and fluoroalkyl-phosphonic acids

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Abstract

Low-voltage-driven organic thin-film transistors (organic TFTs) with spatially controlled threshold voltages (−1.2 and −0.36 V) were fabricated for the first time. Using the microcontact printing method, tetradecylphosphonic acid (HC14-PA) and pentadecylfluoro-octadecylphosphonic acid (FC18-PA) were transferred to form ultrathin layers in different regions on a substrate. Together with plasma-grown aluminum oxide (AlO_x) layer, the stamped layers were shown to have equal insulating ability as the dipped method monolayer. The feasibility of the area-selective stamping method was displayed using locally controlled inverter circuits. The shift of turn-on voltage for those transistors was consistent with the threshold voltage shift of the transistors.

Recently, organic thin-film transistors (organic TFTs) have attracted attention because they are a key element in realizing a new class of devices such as flexible displays,[1,2] radio frequency identification tags,[3] and large-area sensor arrays.[4] As a result of organic transistor technology advancement, large-scale integration such as processors[5] and shift registers[6,7] has become possible. An important prerequisite for the reliable operation of such highly complex circuits are large noise margins that are indispensable for the successful suppression of inadvertent switching events in the unavoidable presence of electronic noise.[8] Large noise margins in turn require precise and deterministic control of the threshold voltage of the transistors. Doping is widely used in inorganic transistors to control threshold voltage; however, many dopants are unstable and diffuse into organic materials, which makes it difficult to control the threshold voltage in organic transistors.

Alternatively, surface modification is a very effective method to control the threshold voltage in organic transistors. The threshold voltage can be controlled using cross-linked organic insulating polymers,[9] thin layers of hexamethyldisilazane,[10] and self-assembled monolayers (SAMs).[11,12] In particular, SAMs in combination with ultrathin metal oxide dielectrics are particularly attractive, since they provide very low operation voltages of only a few volts, along with deterministic control of the threshold voltage, through the alkyl-chain length[13] and/or the electron-donating or -withdrawing properties of materials such as fluoroalkylphosphonic acid.[14,15] Typically, SAMs are formed by dipping the entire substrate into a solution of the molecules, so that all TFTs on the substrate end up having the same threshold voltage.[11–13,16] However, for certain applications it is highly desirable to have TFTs with two different threshold voltages in specific locations on the same substrate. For example, to control the switching voltage of a p-type metal-oxide-semiconductor (pMOS) inverter, the threshold voltages of two transistors that consist of the inverter should be spatially controlled. In principle, this can be accomplished by a printing process such as area-selective microcontact printing, which also provides a wide patterning range of surface modification materials. However, to our knowledge this possibility has not been exploited so far.

Reported herein is the fabrication of organic transistors with different threshold voltages on the substrate that are defined by area-selective microcontact printing ("stamping") using polydimethylsiloxane (PDMS). Solutions of tetradecylphosphonic acid (HC14-PA) or pentadecylfluoro-octadecylphosphonic acid (FC18-PA) were printed ("stamped") on the surface of Al gate electrodes coated with a few nanometers-thick aluminum oxide (AlO_x). The average thickness of the stamped ultrathin layer was one or two monolayers. Their insulating

properties were equivalent to those of single SAMs prepared by conventional dipping and the leakage current density was two or three orders of magnitude smaller than the transistors without SAMs. The difference in threshold voltage between TFTs with the HC14-PA gate dielectric and TFTs with the FC18-PA gate dielectric was 0.83 V, which is about 42% of the supply voltage (2 V). By stamping HC14-PA and FC18-PA SAMs onto different regions on the same substrate, TFTs having different threshold voltages were realized in specific locations of the substrate, allowing the availability of TFTs with different threshold voltages to be exploited for the realization of robust integrated circuits.

The development of the device structure is schematically shown in Fig. 1(a). The Al gate electrodes with a thickness of 30 nm were evaporated through a shadow mask onto a Si substrate with a 500 nm thick oxidized surface. The surface of the electrode was oxidized by plasma (200 W, 30 s) to form a thin, dense AlO_x layer. The SAMs were then transferred onto the Al/AlO_x stack from a PDMS (Sylgard® 184 Silicone Elastomer Kit; Midland, MI).[17,18] The stamp was first dipped into 2-propanol solution of 1 mmol/l either HC14-PA or FC18-PA solutions for 5 min and then placed onto the Si/Al/AlO_x surface for 10 min to allow a molecular monolayer to self-assemble on the AlO_x surface. For comparison, SAMs formed by dipping were also prepared in which the substrate was immersed in a 2-propanol solution of 1 mmol/l of HC14-PA or FC18-PA and then rinsed with pure 2-propanol.[13] The last step in both the stamping and dipping process was to bake the substrate on a hotplate at 100 °C for 10 min. A 30 nm thick layer of organic semiconductor dinaphtho[2,3-*b*:2′,3′-f]thieno[3,2-*b*]thiophene (DNTT)[19] was evaporated at room temperature. Finally, the source and drain electrodes with a channel length of 40 μm were evaporated. An optical microscopic image of the fabricated transistor is shown in Fig. 1(b).

Figure 1(c) shows the leakage current density measured on Al/AlO_x/SAM/Au capacitors (without semiconductor) based on SAMs of either HC14-PA or FC18-PA prepared by either stamping or dipping, plus a control device without SAM. The top surface size for the Au electrodes was 700 × 100 μm^2. In Fig. 1(c) it can be seen that all the capacitors with SAMs, either dipped or stamped, exhibited a current density that was two or three orders of magnitude smaller than that without SAM, confirming the important role of SAM in suppressing gate leakage. The difference in current density demonstrates that a pinhole-free thin layer was formed using the stamping process. Also note that stamped SAMs exhibited leakage currents that were smaller than dipped SAM samples, which have previously shown the ability to integrate at the circuit level (see also Supplementary information).[18] Further integration studies using stamped SAMs will be examined at a later time.

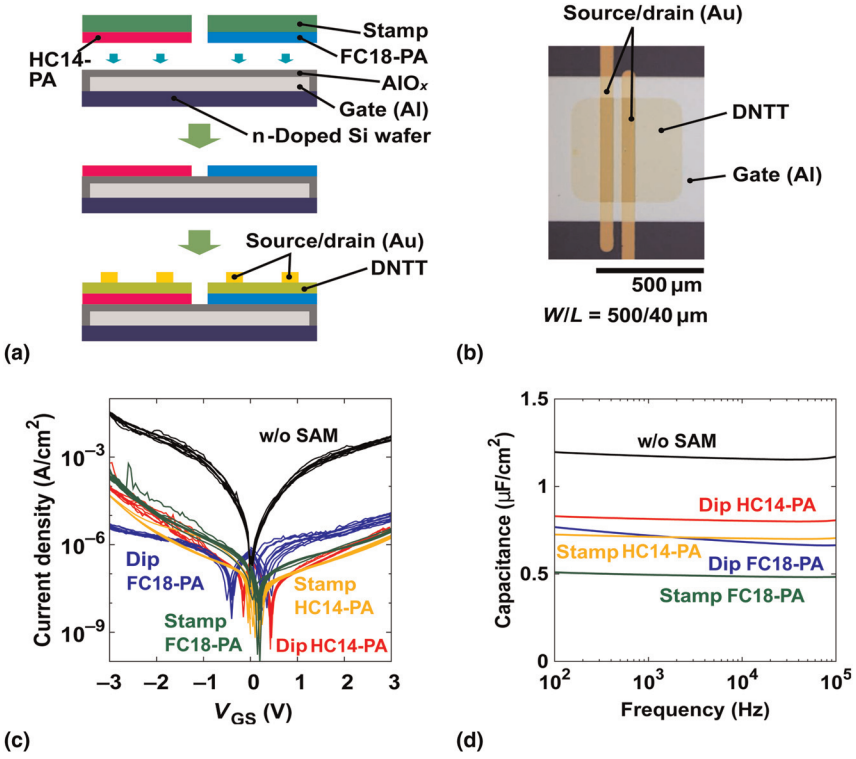

Figure 1. (a) Schematic of the stamping process, including the process to prepare SAMs of two different phosphonic acids in different regions on the same substrate by microcontact printing (stamping). (b) Photograph of a completed organic transistor. (c) Leakage current density as a function of applied voltage measured on five different SAM capacitors (red: dipped HC14-PA; blue: dipped FC18-PA; yellow: stamped HC14-PA; green: stamped FC18-PA; black: control device without SAM). The measurement was replicated ten times to assure uniformity. (d) Capacitance as a function of frequency under a bias voltage of 1 V.

Figure 1(d) shows the capacitance frequency response. It can be seen that the capacitances of all the devices with SAMs were in the range expected from previous reports: close to 800 nF/cm^2 for HC14-PA[20] and (600 ± 100) nF/cm^2 for FC18-PA.[16] Note that dipped samples always exhibit larger capacitance than stamped samples. Assuming that the dielectric constant of SAMs is 2.5,[21] the thickness of the SAM layers was evaluated from the capacitance as 0.9 and 1.2 nm for dipped and stamped HC14-PA layers, respectively, as compared to 1.4 and 2.7 nm for dipped and stamped FC18-PA layers, respectively, which were very close to the SAM molecule length of 2.3 nm. In AFM observation, the surface morphology of DNTT grains on dipped SAM is different from that on stamped SAM, which can be ascribed to the difference of the surface smoothness of SAM layers even though the average thickness was one or two monolayers for both HC14-PA and FC18-PA samples, since the grain size of the DNTT is affected by the smoothness of the SAM layer underneath[13] (see also Supplementary Fig. 1 online). The multilayer of stamped samples is considered to be due to the excess SAM molecules, which were not rinsed. It is important to remember that the leakage current of stamped samples was smaller than that of dipped samples, as shown in Fig. 1(c). Although this is an indirect measure, it still provides evidence that the possible existence of sub-monolayer coverage can be excluded. Future structural characterization is necessary.

Transistor characteristic properties were measured in ambient air at room temperature using a semiconductor parameter analyzer (Agilent 4156C) Agilent Technologies (Santa Clara, CA). The representative transfer curves for transistors without SAMs and those dipped or stamped with SAMS are shown in Fig. 2 (a). The mobilities and the threshold voltages were extracted from the transfer curves. Histograms of the threshold voltages of 38 transistors are shown in Fig. 2(b) (for a summary, see also Supplementary Table 1 online), along with the field-effect mobilities that were also extracted from the transfer curves. Regardless of the process and/or species of SAM, all samples with SAMs exhibited larger mobility than those without SAM, as expected.[13] The HC14-PA samples had a higher mobility than the FC18-PA samples, which is also in line with previous reports.[12,14,16] Furthermore, all the samples with SAMs exhibited larger on/off ratios than those samples without SAMs, as a result of smaller gate leakage currents. Most importantly, the choice of SAM molecule has a pronounced effect on the threshold voltage of the TFTs, regardless of whether the SAMs were prepared by stamping or dipping, as can be clearly seen in Fig. 2(a). The difference in threshold voltage between TFTs with HC14-PA and TFTs with FC18-PA was 0.83 V, which is about 42% of the supply voltage (2 V). Systematic changes of the threshold voltages were clearly observed, although the distribution of stamped samples was slightly larger than that of dipped samples.

To show the feasibility of the stamping approach for spatially controlling threshold voltage transistors, inverters were fabricated and characterized. As shown in Fig. 2(c), the drive TFTs were comprised of FC18-PA, while the load

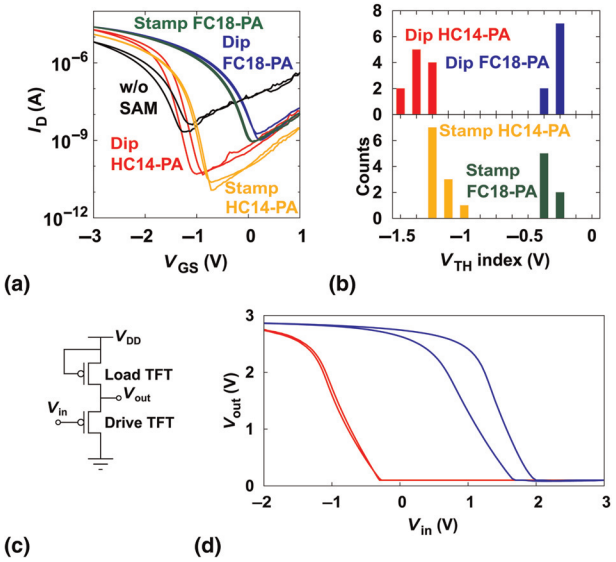

Figure 2. (a) Transfer characteristics of DNTT transistors without SAMs and with SAMs of HC14-PA or FC18-PA prepared by stamping or dipping. The measurements were performed with a drain–source voltage $V_{DS} = -2$ V. (b) Histogram of the threshold voltages of 38 TFTs, showing the distinct dependence of threshold voltage on the choice of SAM molecule (HC14-PA or FC18-PA), regardless of the process (stamping or dipping). (c) Circuit schematic of the inverters. (d) Static transfer characteristics of inverters in which the drive and load TFTs have the same threshold voltage (blue curve) or different threshold voltages (red curve). In both inverters, the drive TFT uses an FC18-PA, while the load TFT is based either on an FC18-PA (blue curve) or on an HC14-PA (red curve). The effect on the switching voltage of the inverter is clearly seen.

TFTs used stamped FC18-PA or HC14-PA (for the fabricated device image, see also Supplementary Fig. 2 online). Figure 2 (d) shows the input and output characteristics of the inverters, and it can be seen that the inverters had distinctly different switching voltages. When the load and drive TFTs had the same threshold voltage (−0.36 V), the inverter switched at positive input voltages (blue curve), but when the threshold voltage of the load TFT (−1.19 V) was more negative than the threshold voltage of the drive TFT (−0.36 V), the switching voltage was negative. The consistent behavior of turn-on voltage in the integrated circuits clearly shows the feasibility of the spatial control of threshold voltage by stamping. Both samples showed hysteresis, which might be caused by carrier trappings at the insulator–semiconductor interface[9,22] and other reasons. A more detailed investigation is needed in order to identify the exact reason for the hysteresis. Further optimization of the process conditions is important to improve the uniformity of threshold voltage by stamping for sophisticated design of integrated circuits and is an important direction for the future.

Acknowledgments

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Supplementary materials

For supplementary material for this article, please visit http://dx.doi.org/10.1557/mrc.2011.11

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Spatial Control of the Threshold Voltage of Low-Voltage Organic Transistors by Microcontact-Printing of Alkyl- and Fluoroalkyl-phosphonic Acids

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Details of Figure 1(c)

Ideally, FC18-PA is expected to have smaller leak current density, however, actual devices were affected by many factors such as drift currents by small pinholes, sweep direction and the number of sweeps. The two minima observed in the dipped samples were shifted due to the independent sweep in the positive direction and in the negative direction.

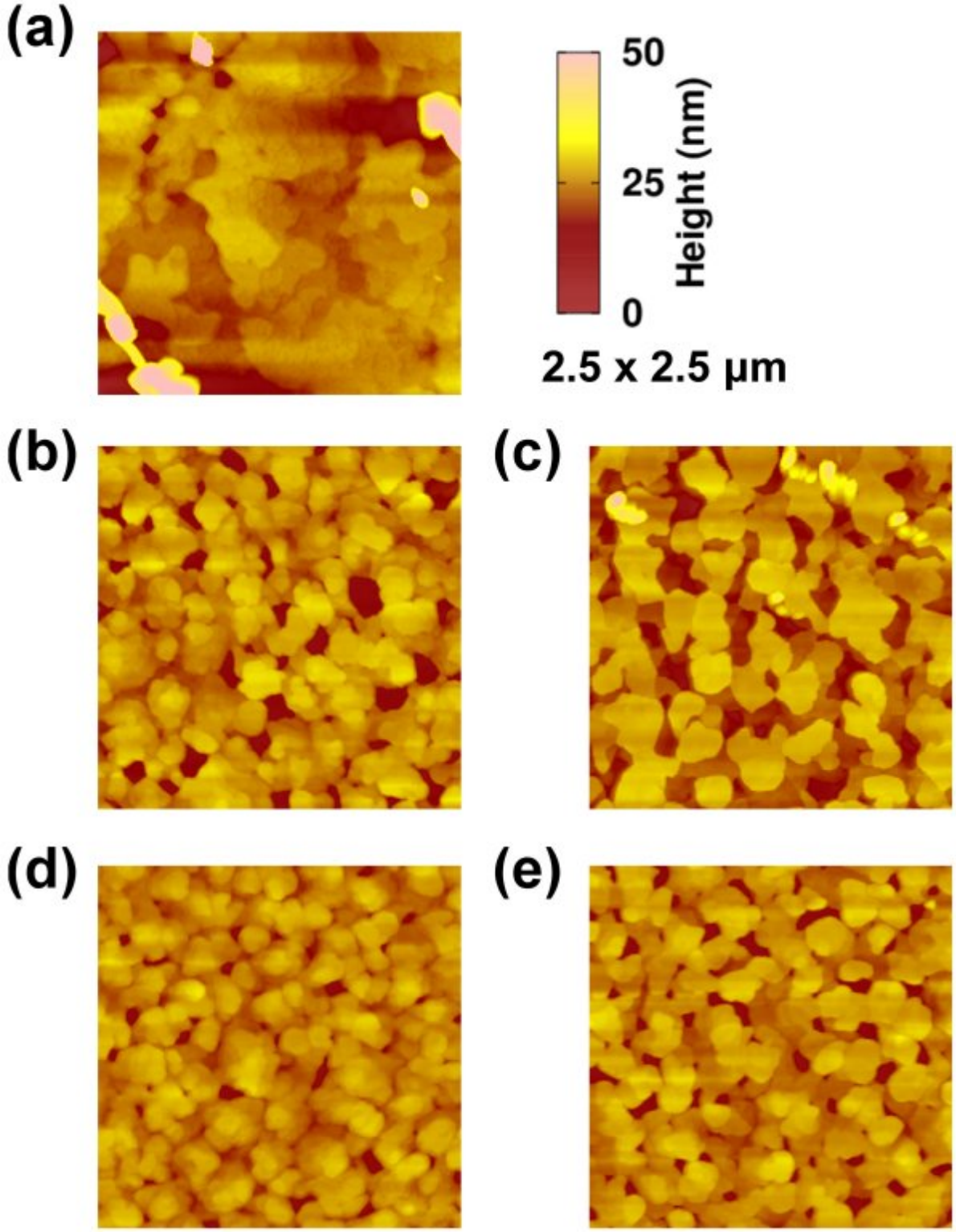
Table SI. Summary of the threshold voltages and field-effect mobilities of DNTT transistors with SAMs of C41 or FC prepared by stamping or dipping, or without SAM.

Figure S1. AFM images of DNTT layers deposited on AlO_x and on dipped or stamped SAM layers. The scan area is $2.5 \times 2.5 \mu m^2$. The grain sizes of each sample were (a) on AlO_x 2.4×10^4 nm^2, (b) on dipped HC14-PA 3.2×10^4 nm^2, (c) on dipped FC18-PA 8.3×10^4 nm^2, (d) on stamped HC14-PA 3.4×10^4 nm^2, and (e) on stamped FC18-PA 3.1×10^4 nm^2.

Figure S2. Optical image of a load inverter with stamped SAMs. The load transistor has channel width of 2 mm and channel length of 50 μm. The drive transistor has channel width of 35 mm and channel length of 50 μm.

Table SI

	V_{TH} (V)		mobility ($cm^2/V \cdot s$)	
	average	standard deviation	average	standard deviation
HC14-PA (dipping)	-1.34	0.068	1.90	0.122
FC18-PA (dipping)	-0.27	0.052	0.81	0.026
HC14-PA (stamping)	-1.19	0.071	1.05	0.314
FC18-PA (stamping)	-0.36	0.048	0.79	0.373
without SAM	-1.26	0.151	0.31	0.091


(a)
50
25
0
Height (nm)
2.5 x 2.5 μm
(b)
(c)
(d)
(e)