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Bias-stress stability of low-voltage p-channel and n-channel organic thin-film transistors on flexible plastic substrates

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ABSTRACT

The bias-stress stability of low-voltage organic p-channel and n-channel thin-film transistors (TFTs) based on five promising organic semiconductors and fabricated on flexible polyethylene naphthalate (PEN) substrates has been investigated. In particular, it has been studied to which extent the bias-stress-induced decay of the on-state drain current of the TFTs is affected by the choice of the semiconductor and by the gate-source and drain-source voltages applied during bias stress. It has been found that for at least some of the organic p-channel TFTs investigated in this study, the bias-stress stability is comparable to that of a-Si:H and metal-oxide TFTs, despite the fact that the organic TFTs were fabricated at significantly lower process temperatures, which is important in view of the fabrication of these devices on plastic substrates.

1. Introduction

Organic thin-film transistors (TFTs) are potentially useful for flexible, large-area electronics applications, such as bendable, rollable or foldable active-matrix organic light-emitting diode (AMOLED) displays [1–6]. In an AMOLED display, each pixel contains several TFTs, one of which has the task of supplying the electric current that is required to drive the organic LED of that pixel to the specified brightness. Since the brightness (luminance) of organic LEDs is typically a steep function of the electric current flowing through the LED [7], the long-term stability of the drain current of the drive TFTs in AMOLED displays during continuous on-state biasing is very important. In TFTs based on disordered materials, such as hydrogenated amorphous silicon (a-Si:H), amorphous or polycrystalline metal oxides, and conjugated organic semiconductors, the stability of the on-state drain current during continuous operation is typically limited by the bias-stress effect, *i.e.*, by the time-dependent trapping of charges from the gate-induced carrier channel into localized defect states in the semiconductor, in the gate dielectric, and/or at the semiconductor/dielectric interface. While the trapped charges no longer contribute to the drain current, they continue to contribute to the charge balance of the transistor, so that the time-dependent decay in drain current during bias stress is accompanied by a time-dependent shift of the threshold voltage of the transistor in the direction of the applied gate-source voltage.

The physical mechanisms and the analytical description of the bias-stress effect in organic TFTs have been the subject of a large number of previous publications and reviews

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[8–11]. In addition, many reports have discussed how the bias-stress stability of organic TFTs is affected by various parameters, such as the TFT architecture [12], the properties of the gate dielectric [13–16], the presence of grain boundaries in the organic semiconductor [17], the material chosen for the source and drain contacts [18], the application of a post-process anneal [19], the presence of trace amounts of water in the transistor [20], and the magnitude of the applied gate-source and drain-source voltages [9,21–23]. With few exceptions [5,19,24,25], the organic transistors examined in these reports were all fabricated on rigid silicon or glass substrates. Since conclusions drawn from bias-stress experiments conducted on TFTs fabricated on silicon or glass substrates are not necessarily applicable to TFTs fabricated on plastic substrates (due, for example, to the impact of surface roughness [26] and thermal budget [27]), it is useful to investigate and benchmark the bias-stress stability of organic TFTs specifically fabricated on plastic substrates. Here we compare the bias-stress stability of low-voltage organic TFTs fabricated on flexible polymeric substrates using five different vacuum-deposited small-molecule semiconductors, three of which provide field-effect mobilities ranging from about 2 to 4 cm^2/Vs in p-channel TFTs, while the other two have shown great potential for the realization of organic n-channel TFTs with good air stability.

The schematic cross-section of the TFTs is shown in Fig. 1, along with the five semiconductors employed in this study: dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT; [29]), 2,9-didecyl-DNTT (C_{10}-DNTT; [30]) and 2,9-diphenyl-DNTT (DPh-DNTT; [31]) for the p-channel TFTs, as well as hexadecafluorocopperphthalocyanine (F_{16}CuPc; [32]) and N,N′-bis-(heptafluorobutyl)-2,6-dichloro-1,4,5,8-naphthalene tetracarboxylic diimide (NTCDI–Cl_2–($CH_2C_3F_7$)$_2$; [33]) for the n-channel TFTs. The three thienoacenes DNTT, C_{10}-DNTT and DPh-DNTT were chosen for this study because of their exceptional combination of large field-effect mobilities, excellent air stability and high thermal stability [34,35] in flexible p-channel TFTs. F_{16}CuPc was one of the first semiconductors developed for organic n-channel TFTs and shows good air stability owing to its large electron affinity [36]. NTCDI–Cl_2–($CH_2C_3F_7$)$_2$ is currently the semiconductor with the largest reported field-effect mobility for organic n-channel TFTs operated in air (4.2 cm^2/Vs) [37].

2. Transistor fabrication

DNTT, C_{10}-DNTT and DPh-DNTT were synthesized as reported earlier [29–31]. Tetradecylphosphonic acid, which was used to form self-assembled monolayers as part of the ultrathin gate dielectric, was purchased from PCI Synthesis, Newburyport, MA, USA. F_{16}CuPc was purchased from Sigma Aldrich. NTCDI–Cl_2–($CH_2C_3F_7$)$_2$ was provided by BASF SE, Ludwigshafen, Germany. 125-μm-thick flexible polyethylene naphthalate film (Teonex® Q65 PEN) was kindly provided by William A. MacDonald,

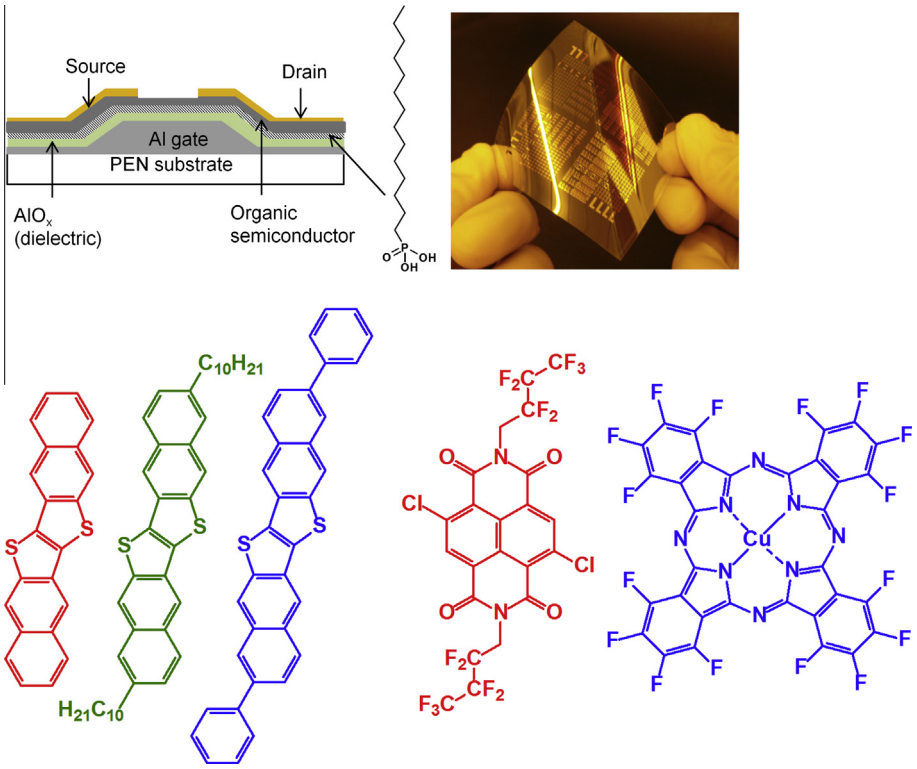

Fig. 1. Schematic cross-section of the organic transistors, photograph of one of the flexible PEN substrates, and chemical structures of the five organic semiconductors investigated in this study: (from left to right) DNTT, C_{10}-DNTT and DPh-DNTT for the p-channel TFTs, and NTCDI–Cl_2–($CH_2C_3F_7$)$_2$ and F_{16}CuPc for the n-channel TFTs.

DuPont Teijin Films, Wilton, UK. All TFTs were fabricated in the bottom-gate, top-contact (inverted staggered) device structure on flexible PEN substrates. To define the gate electrodes, 30-nm-thick aluminum was deposited by thermal evaporation in vacuum through a polyimide shadow mask (CADiLAC Laser, Hilpoltstein, Germany). A gate dielectric composed of a 3.6-nm-thick layer of aluminum oxide (obtained by briefly exposing the aluminum surface to an oxygen plasma) and a 1.7-nm-thick self-assembled monolayer (SAM) of *n*-tetradecylphosphonic acid (obtained by immersing the substrate into a 2-propanol solution of the phosphonic acid) was then formed on the gate electrodes [25]. In the next step, the organic semiconductor layer with a thickness of 20–30 nm was deposited onto the AlO_x/SAM gate dielectric by sublimation in vacuum through a shadow mask. Finally, 30-nm-thick gold was deposited by thermal evaporation in vacuum through a shadow mask to define the source and drain contacts of the TFTs. The small thickness (5.3 nm) and large capacitance per unit area (600 nF/cm^2; [28]) of the AlO_x/SAM gate dielectric allow the transistors and circuits to operate with voltages of about 3 V. The maximum substrate temperature during the TFT fabrication process was between 60 and 90 °C, which is the substrate temperature during the vacuum deposition of the organic semiconductor. All TFTs have a channel length of 30 µm and a channel width of 100 µm. All measurements were performed in ambient air at room temperature.

3. Results and discussion

Fig. 2 shows the measured transfer and output characteristics of a p-channel TFT based on DPh-DNTT and of an n-channel TFT based on NTCDI–Cl_2–$(CH_2C_3F_7)_2$, both fabricated on flexible PEN substrates. Both TFTs have an on/off current ratio of 10^7. The field-effect mobilities extracted from the transfer characteristics are 1.9 cm^2/Vs for the DPh-DNTT p-channel TFT and 0.16 cm^2/Vs for the NTCDI–Cl_2–$(CH_2C_3F_7)_2$ n-channel TFT. For the other three semiconductors, the following carrier mobilities were obtained: DNTT: 1.8 cm^2/Vs; C_{10}-DNTT: 4.1 cm^2/Vs; F_{16}CuPc: 0.03 cm^2/Vs (see also Table 1). All of these mobilities are similar to the largest mobilities reported previously for these semiconductors in flexible, low-voltage TFTs [25,35,38–41].

Before discussing bias stress, the shelf-life stability of the TFTs will be briefly examined. For this experiment, the substrates were stored in ambient air with a humidity of about 50% for a period of a few weeks, and the electrical TFT characteristics were measured occasionally without applying bias stress. Fig. 3 shows how the transfer and output characteristics of a DPh-DNTT p-channel TFT and those of an NTCDI–Cl_2–$(CH_2C_3F_7)_2$ n-channel TFT develop over time during this shelf-life experiment. As can be seen, there is essentially no change in the threshold voltage and very little change in the field-effect mobility of either of the TFTs during shelf-life storage (40 days in air for the DPh-DNTT TFT; 10 days in air for the NTCDI–Cl_2–$(CH_2C_3$

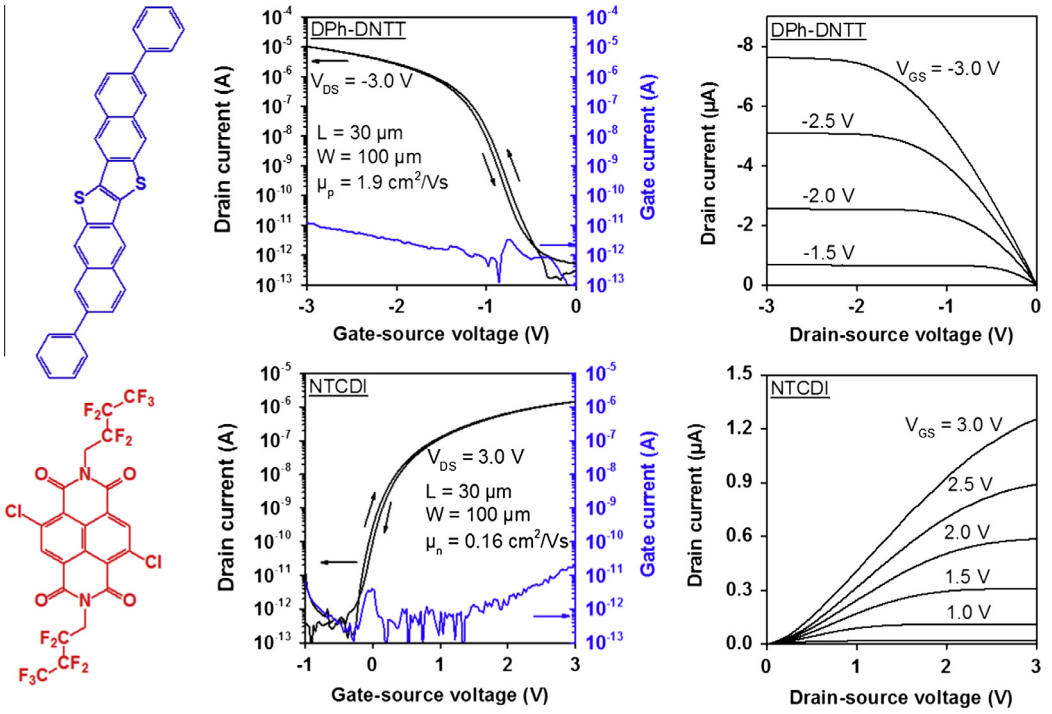

Fig. 2. Transfer and output characteristics of a fresh DPh-DNTT p-channel TFT and a fresh NTCDI–Cl_2–$(CH_2C_3F_7)_2$ n-channel TFT, measured shortly after device fabrication.

Table 1
Measured field-effect mobilities, on/off current ratios, subthreshold swings and threshold voltages of flexible TFTs based on the five organic semiconductors investigated in this study.

Semiconductor Carrier type	DNTT p-Channel TFT	C_{10}-DNTT p-Channel TFT	DPh-DNTT p-Channel TFT	F_{16}CuPc n-Channel TFT	NTCDI–Cl_2–$(CH_2C_3F_7)_2$ n-Channel TFT
Process temperature	60 °C	80 °C	80 °C	90 °C	65 °C
Field-effect mobility	1.8 cm^2/Vs	4.1 cm^2/Vs	1.9 cm^2/Vs	0.03 cm^2/Vs	0.16 cm^2/Vs
On/off current ratio	10^6	10^8	10^7	10^6	10^7
Subthreshold swing	100 mV/dec	200 mV/dec	180 mV/dec	360 mV/dec	110 mV/dec
Threshold voltage	−1.2 V	0.4 V	−0.8 V	0.1 V	0.2 V

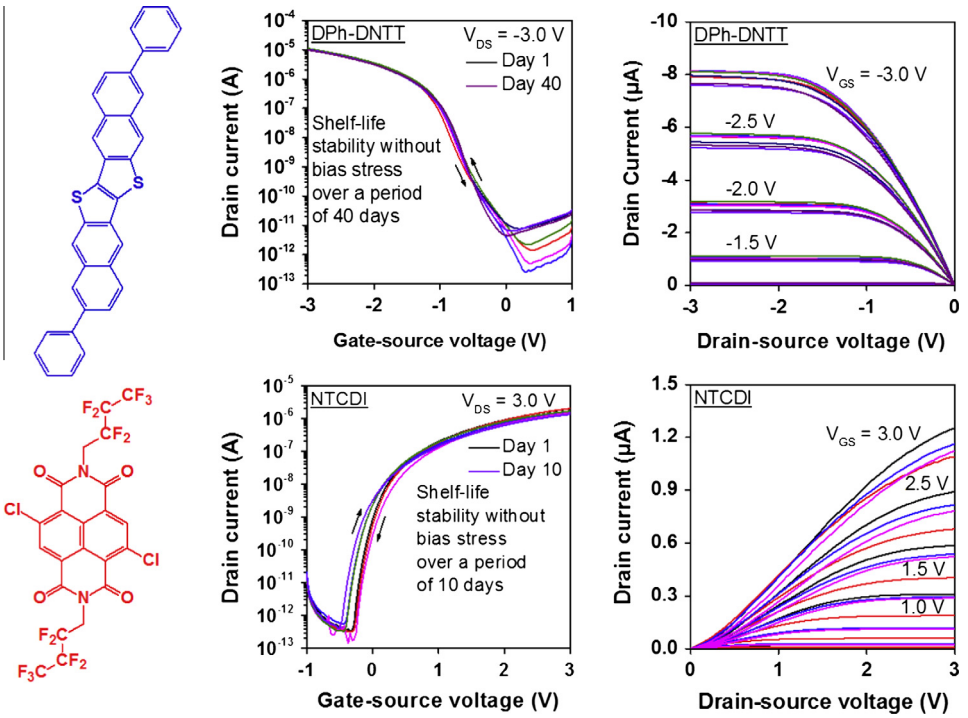

Fig. 3. Shelf-life stability (without applying any bias stress) of DPh-DNTT p-channel and NTCDI–Cl_2–$(CH_2C_3F_7)_2$ n-channel TFTs.

$F_7)_2$ TFT). Shelf-life tests over longer periods have been the subject of several previous reports [25,34,36,38,39].

During continuous application of constant gate-source and drain-source voltages (negative voltages in the case of p-channel TFTs, positive voltages in the case of n-channel TFTs), the on-state drain current can be expected to decay over time, due to the trapping of charges from the gate-induced carrier channel into localized states. A useful basis for meaningful comparisons of the stability against this bias-stress-induced current decay among TFTs based on different materials and/or different technologies is the 10%-current-decay lifetime, which according to Hekmatshoar et al. [42] is defined as the time until the drain current has dropped to 90% of its initial value. Hekmatshoar et al. also demonstrated the large extent to which the 10%-lifetime depends on the applied gate-source voltage, making it necessary to measure it for a range of applied voltages in order to facilitate useful benchmarking [42]. For hydrogenated amorphous silicon (a-Si:H) n-channel TFTs fabricated at substrate temperatures ranging from 200 °C to 350 °C and stressed with gate-source voltages ranging from 7.5 V to 120 V, Hekmatshoar et al. determined 10%-lifetimes ranging from less than a minute (lowest process temperature, largest gate bias) to more than a decade (highest process temperature, smallest gate bias) [27,42].

Fig. 4 shows how the drain current of flexible organic p-channel and n-channel TFTs based on DPh-DNTT and NTCDI–Cl_2–$(CH_2C_3F_7)_2$ develops over time during bias stress with applied gate-source and drain-source voltages ranging from ±2 V to ±3 V (corresponding to gate fields ranging from 3.8 to 5.5 MV/cm). This is a useful range of gate-source voltages for the TFTs employed in this study, since gate-source voltages below ±2 V will be too close to the threshold voltage for some of the semiconductors, while gate-source voltages above ±3 V might damage the gate dielectric when applied over extended periods of time. The drain-source voltage was either set to be equal to the applied gate-source voltage ($V_{GS} = V_{DS}$) or was set to ±3 V; this corresponds to a range of biasing conditions that is representative for those under which the drive TFTs in

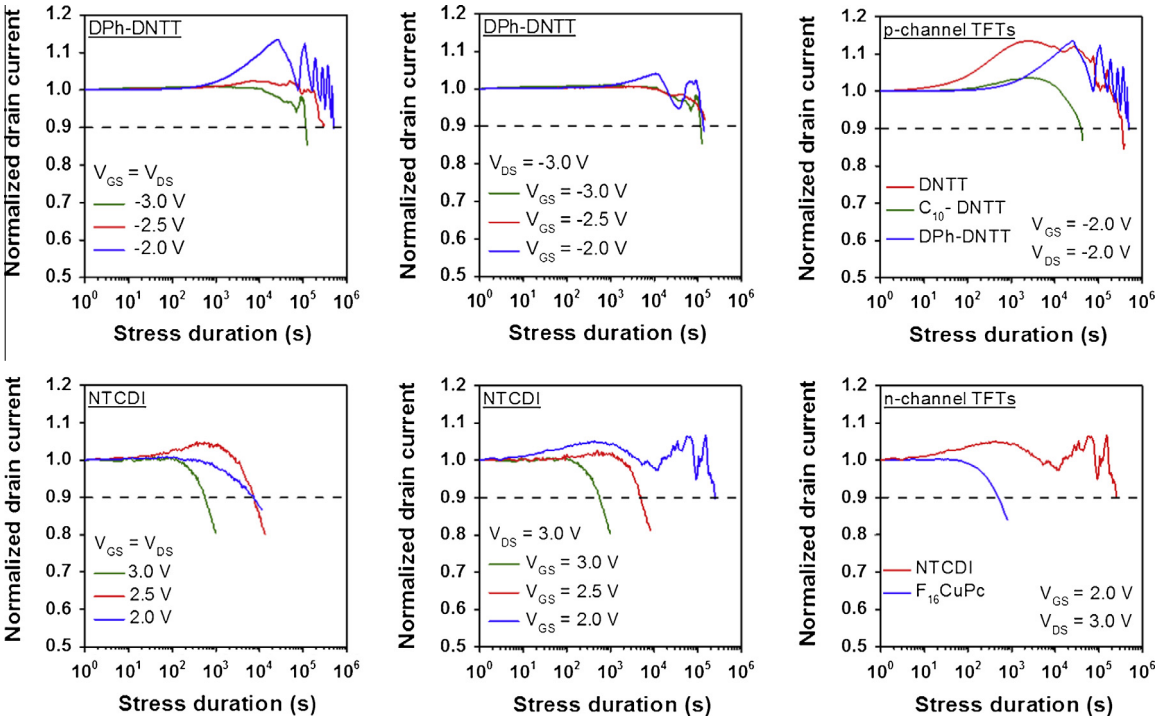

Fig. 4. Development of the drain current of p-channel TFTs based on DPh-DNTT, DNTT and C_{10}-DNTT and of n-channel TFTs based on NTCDI–Cl_2–$(CH_2C_3F_7)_2$ and F_{16}CuPc during continuous bias stress with gate-source and drain-source voltages ranging from ±2 to ±3 V over periods of up to six days.

AMOLED display pixels operate most of the time. Identical measurements were carried out on TFTs based on all five semiconductors, and the results for one set of applied voltages are shown in Fig. 4. Note that each bias-stress measurement was conducted on a fresh (*i.e.*, not previously stressed) transistor.

From these measurements, the 10%-current-decay lifetimes were extracted. The results are summarized in Table 2. Depending on the choice of the semiconductor and on the voltages applied during bias stress, the 10%-lifetimes of the flexible DNTT, C_{10}-DNTT, DPh-DNTT, F_{16}CuPc and NTCDI–Cl_2–$(CH_2C_3F_7)_2$ TFTs range from 15 s to about 1 week. In Fig. 5a, the 10%-lifetimes of all TFTs are plotted as a function of the applied gate-source voltage, once for the measurements in which the applied drain-source voltage was identical to the applied gate-source voltage ($V_{GS} = V_{DS}$) and once for the measurements in which the applied drain-source voltage was set to ±3.0 V. The results confirm that a larger applied gate-source voltage generally leads to a shorter 10%-lifetime and *vice versa*, as was previously reported by Hekmatshoar et al. [42] and others [9,21,22]. In principle, the results also allow conclusions regarding the bias-stress stability of organic TFTs depending on the choice of the semiconductor. However, it should be kept in mind that since the TFTs have different threshold voltages depending on the choice of the semiconductor (see Table 1), the same applied gate-source voltage will induce a different density of charge carriers in each TFT, which in turn may result in a different trap rate during bias stress. To account for this, the 10%-lifetimes are plotted in Fig. 5b as a function of the difference between the applied gate-source voltage and the threshold voltage (gate overdrive voltage V_{GS}–V_{th}). As can be seen, for the p-channel

Table 2
10%-Current-decay lifetimes measured during bias stress under five different bias conditions on flexible TFTs based on the five organic semiconductors investigated in this study.

Abs (V_{GS}) during bias stress (V)	Abs (V_{DS}) during bias stress (V)	DNTT p-channel TFT (s)	C_{10}-DNTT p-channel TFT (s)	DPh-DNTT p-channel TFT (s)	F_{16}CuPc n-channel TFT (s)	NTCDI–Cl_2–$(CH_2C_3F_7)_2$ n-channel TFT (s)
2.0	2.0	364,000	40,000	502,000	290	7300
2.5	2.5	209,000	13,000	302,000	55	7300
3.0	3.0	27,000	20,000	115,000	15	550
2.0	3.0	417,000	32,000	145,000	480	251,000
2.5	3.0	58,000	20,000	132,000	185	4800

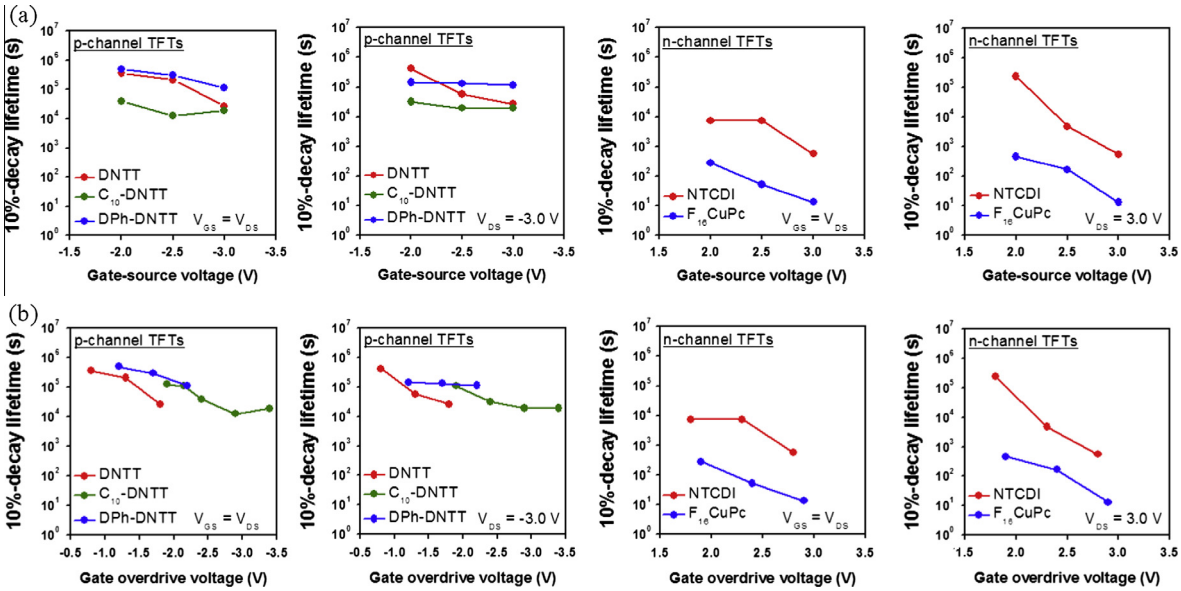

Fig. 5. Dependence of the measured 10%-current-decay lifetimes of DNTT, C_{10}-DNTT and DPh-DNTT p-channel and NTCDI–Cl_2–$(CH_2C_3F_7)_2$ and F_{16}CuPc n-channel TFTs on the gate-source and drain-source voltages applied during bias stress. (a) The 10%-decay lifetimes are plotted as a function of the applied gate-source voltage. (b) The 10%-decay lifetimes are plotted as a function of the gate overdrive voltage, which is the difference between the applied gate-source voltage and the threshold voltage of the TFT.

TFTs, DPh-DNTT and C_{10}-DNTT provide somewhat better stability than DNTT. For the n-channel TFTs, the results show that in addition to a substantially larger electron mobility, NTCDI–Cl_2–$(CH_2C_3F_7)_2$ also provides significantly better bias-stress stability over the entire range of gate-source and drain-source voltages compared with F_{16}CuPc. In general, the p-channel TFTs examined in this study all provide larger carrier mobilities and better bias-stress stability compared with the n-channel TFTs.

Closer examination of Fig. 4 shows that the drain current does not decay monotonically over time during bias stress. Especially for small applied gate-source voltages, *i.e.*, when the bias-stress effect is relatively small, the drain current actually *increases* during the first few hours of bias stress. This is believed to be due to an initial time-dependent decrease of the contact resistance that has been previously reported to occur in pentacene TFTs [43,44] and that has been confirmed to also occur in TFTs based on at

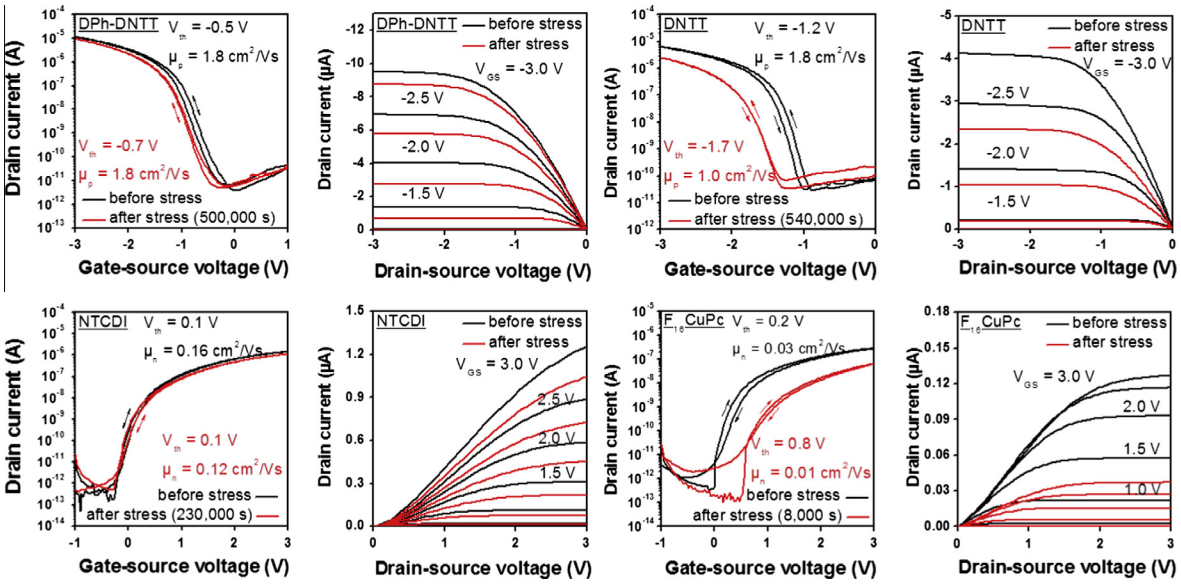

Fig. 6. Measured transfer and output characteristics of DPh-DNTT and DNTT p-channel and NTCDI–Cl_2–$(CH_2C_3F_7)_2$ and F_{16}CuPc n-channel TFTs before and after bias stress.

least some of the organic semiconductors employed in the present study [45], although the exact physical or chemical mechanism(s) responsible for this time-dependent decrease of the contact resistance are not yet clear.

Concurrent with the observed bias-stress-induced decay of the on-state drain current, the threshold voltage of the TFTs will shift in the direction of the gate-source voltage applied during bias stress, *i.e.*, towards more negative threshold voltages in the case of p-channel TFTs and towards more positive threshold voltages in the case of n-channel TFTs. Fig. 6 shows the extent of this bias-stress-induced threshold voltage shift produced by one particular bias-stress condition ($V_{GS} = V_{DS} = \pm 2$ V). For these experiments, the transfer characteristics were measured once before bias stress and again immediately after (within a few seconds of) completion of the bias-stress experiment. The smallest threshold-voltage shifts are seen for the DPh-DNTT p-channel TFTs ($\Delta V_{th} = -0.2$ V after 138 h of bias stress) and for the NTCDI–Cl_2–$(CH_2C_3F_7)_2$ n-channel TFTs ($\Delta V_{th} \sim 0$ V after 64 h of bias stress), which is in line with the trends seen in the 10%-current-decay lifetimes summarized in Table 2 and Fig. 5.

A comparison of the transfer characteristics recorded before and after long-term bias stress further reveals that for some of the semiconductors investigated in this study, the carrier mobility decreases during bias stress. For example, the carrier mobility of the DNTT TFTs drops from 1.8 cm^2/Vs before bias stress to 1.0 cm^2/Vs after 110 h of bias stress. Note that this is not the intrinsic mobility of the semiconductor channel, but an effective (apparent) mobility that is extracted from the transfer characteristics and is smaller than the intrinsic channel mobility due to the influence of extrinsic factors, most importantly due to the contact resistance [46]. For pentacene TFTs, Wang et al. have reported an increase of the contact resistance during bias stress [47,48], which would cause the effective mobility to decrease, even if the intrinsic mobility was not affected by the bias stress. Thus, it is reasonable to hypothesize that the bias-stress-induced decrease of the effective mobility seen in Fig. 6 is due to an increase in the contact resistance, rather than to a decrease of the intrinsic channel mobility. To test this hypothesis it is useful to monitor the relaxation of the transistors after bias stress. The reason is that in organic TFTs, the bias-stress-induced changes are usually not permanent, *i.e.*, after the applied voltages are reduced or removed, at least some of the trapped charge carriers are released, the threshold voltage shifts back towards its initial value, and the original current–voltage characteristics are at least partially recovered. In Fig. 7 this is shown for the DPh-DNTT p-channel TFTs and the NTCDI–Cl_2–$(CH_2C_3F_7)_2$ n-channel TFTs. For both TFTs, an almost complete recovery of the original current–voltage characteristics is observed after a period 1 or 2 days of relaxation with the transistor terminals floating. In those TFTs in which the bias stress had produced a notable drop in the effective mobility (especially in the DNTT TFTs), a partial recovery of the effective mobility was observed (see Table 3).

To benchmark the 10%-current-decay lifetimes of TFTs fabricated using different materials or different

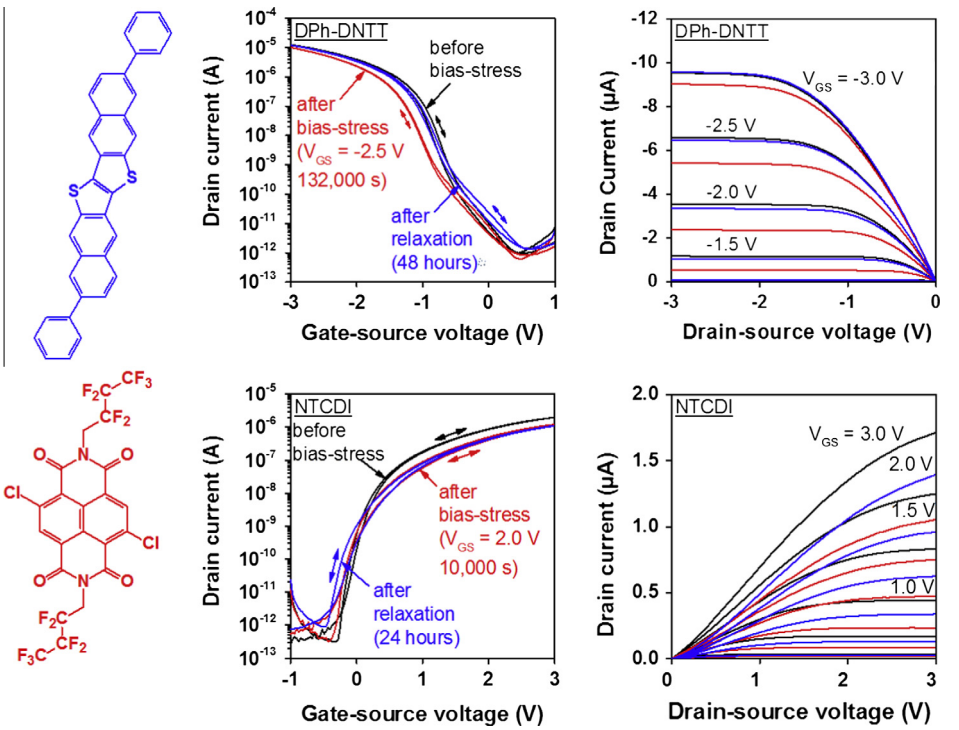

Fig. 7. Transfer and output characteristics of DPh-DNTT p-channel and NTCDI–Cl_2–$(CH_2C_3F_7)_2$ n-channel TFTs before bias stress, after bias stress and after relaxation of the transistors, showing the complete recovery of the original current–voltage characteristics after relaxation.

Table 3
Changes in the effective field-effect mobility and the threshold voltage of the TFTs during and after bias stress.

Semiconductor Carrier type	DNTT p-Channel TFT	C_{10}-DNTT p-Channel TFT	DPh-DNTT p-Channel TFT	F_{16}CuPc n-Channel TFT	NTCDI–Cl_2–$(CH_2C_3F_7)_2$ n-Channel TFT
V_{GS} during bias stress	−2.0 V	−2.0 V	−2.0 V	2.0 V	2.0 V
V_{DS} during bias stress	−2.0 V	−2.0 V	−2.0 V	3.0 V	3.0 V
Duration of bias stress	398,000 s	44,000 s	661,000 s	16,000 s	252,000 s
Effective mobility before bias stress	1.8 cm^2/Vs	4.1 cm^2/Vs	1.8 cm^2/Vs	0.03 cm^2/Vs	0.16 cm^2/Vs
Effective mobility after bias stress	1.0 cm^2/Vs	2.4 cm^2/Vs	1.8 cm^2/Vs	0.01 cm^2/Vs	0.13 cm^2/Vs
Effective mobility after recovery	1.6 cm^2/Vs	n/a	1.8 cm^2/Vs	0.02 cm^2/Vs	0.12 cm^2/Vs
Threshold voltage before bias stress	−1.2 V	0.4 V	−0.8 V	0.1 V	0.2 V
Threshold voltage after bias stress	−1.7 V	0.1 V	−1.1 V	0.9 V	0.3 V
Threshold voltage after recovery	−1.2 V	n/a	−0.8 V	0.8 V	0.2 V

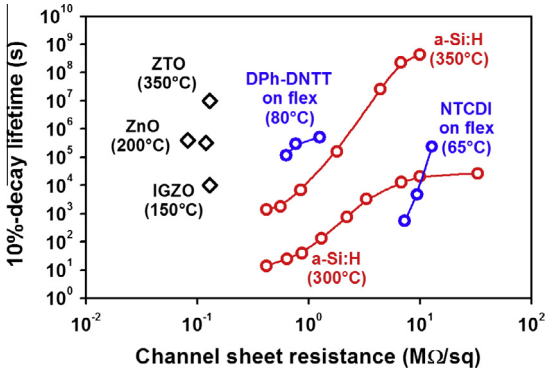

Fig. 8. Comparison of the bias-stress stability of TFTs fabricated in various technologies (a-Si:H, metal oxides, organic TFTs) on the basis of the 10%-current-decay lifetime plotted *versus* the channel sheet resistance. The a-Si:H data were taken from Ref. [42], the metal-oxide TFT data were taken from Refs. [49–51] and the organic-TFT data were taken from Table 2.

technologies, Hekmatshoar et al. [42] suggested to plot the 10%-lifetimes against the transistor's channel sheet resistance, which is inversely proportional to the field-effect mobility, the gate-dielectric capacitance per unit area and the applied gate-source voltage. Fig. 8 summarizes some of the data reported by Hekmatshoar et al. [42] and others [49–51] for a-Si:H and metal-oxide TFTs fabricated at various process temperatures ranging from 150 to 350 °C and, for comparison, the data obtained in this study for DPh-DNTT p-channel and NTCDI–Cl_2–$(CH_2C_3F_7)_2$ n-channel TFTs fabricated at process temperatures below 100 °C. For each data point, the channel sheet resistance was extracted from the output characteristics (drain current *vs.* drain-source voltage) measured before bias stress at the same gate-source voltage applied during the bias-stress experiment. From the data reported for a-Si:H and metal-oxide TFTs, two trends emerge. One is that for the same TFT, the 10%-lifetime is shorter when the channel sheet resistance is smaller, *i.e.*, when the gate-source voltage applied during bias stress is larger. This trend has been well documented [9,21–23,27,42] and is likely related to the fact that the gate-induced carrier density and hence the trapping rate increase with increasing gate-source voltage. The second trend is that inorganic TFTs fabricated at higher process temperatures have longer 10%-lifetimes than inorganic TFTs fabricated at lower process temperatures [42], which is likely related to the fact that in the fabrication of inorganic TFTs, higher process temperatures generally produce films and interfaces with smaller defect densities. However, process temperatures above about 200 °C make it difficult to fabricate the TFTs on flexible plastic substrates, which often have glass transition temperatures below about 200 °C. (Plastics with higher glass transition temperatures exist, but they tend to be more expensive than polyethylene naphthalate and polyethylene terephthalate, which have glass transition temperatures below 150 °C.) Fig. 8 shows that the bias-stress stability of at least some of the organic p-channel TFTs investigated in this study is actually better than that of many inorganic TFTs, despite the fact that the organic TFTs were fabricated at much lower process temperatures on polyethylene naphthalate substrates. But Fig. 8 also shows that more work is needed to further improve the bias-stress stability of flexible organic n-channel TFTs.

4. Conclusions

In conclusion, the bias-stress stability of flexible p-channel and n-channel transistors based on five promising organic semiconductors was investigated and compared with that of several inorganic TFTs reported in literature. Particular emphasis was put on quantifying the extent to which the bias-stress-induced decay of the on-state drain current of the TFTs is affected by the choice of the semiconductor and by the applied gate-source and drain-source voltages. For TFTs based on at least some of the semiconductors investigated in this study, especially 2,9-diphenyl-dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DPh-DNTT), the bias-stress stability is already comparable to that of a-Si:H and metal-oxide TFTs, despite the fact that the organic TFTs were fabricated at significantly lower process temperatures, which is important in view of the fabrication of these devices on plastic substrates.

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$C_3F_7)_2$ employed in this study. Sibani Bisoyi would like to thank Klaus von Klitzing for providing the opportunity to work at the Max Planck Institute for Solid State Research.

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