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Use of scanning capacitance microscopy for controlling wafer processing

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Abstract

Scanning capacitance microscopy and electrostatic force microscopy have been used to characterize commercial semiconductor devices at various stages of the fabrication process. These methods, combined with conventional atomic force microscopy, allow to visualize qualitatively the oxide thickness, the nature of dopants and the exact position of implanted areas.

1. Introduction

IC manufacturing involves hundreds of complex process steps. Over the years semiconductor industry has developed or adopted many tools to check process integrity at each critical step in order to insure yield and reliability of the final circuit. However, as the critical size becomes smaller, classical tools such as scanning electron microscopy (SEM) or electrical measurements become more expensive, more difficult to use and to interpret; sometimes they even reach their practical limits. Moreover, size reduction creates qualitatively new problems that cannot be solved with classical control methods. In this context, atomic force microscopy (AFM) is emerging as a versatile and non-destructive new tool for failure analysis and process characterization at the nanometer scale. We will demonstrate this for the related techniques scanning capacitance microscopy (SCM) and electrostatic force microscopy (EFM) which will be applied to industrial samples at various stages of the fabrication process.

SCM is based on the properties of a metal–insulator–semiconductor diode. A metallic or metallized AFM tip is used for imaging the wafer topography in conventional contact mode. The tip also serves as an electrode for simultaneously measuring the metal-silicon-oxide-semiconductor (MOS) capacitance. The counter electrode is the backside of the wafer. SCM has been used to determine the 2D dopant profile of wafer cross-sections [1–8]. It is sensitive to carrier density concentrations from 10^{15} to 10^{20} atoms/cm^3, with a lateral resolution of 20–150 nm, depending on tip geometry and dopant level [9]. SCM is an alternative to conventional dopant profiling techniques like secondary ion-mass spectroscopy, spreading resistance profiling or selective etching revealed by optical or electron microscopy [10–12]. SCM has the advantage to be non-destructive, however, extraction of absolute dopant concentrations requires reverse simulation incorporating tip geometry and sample oxide thickness [13,14]. Apart from imaging the dopant nature and concentration SCM is also suitable for visualizing the thickness of a silicon oxide layer [15]. Up to now SCM has mainly been used on model samples especially designed for calibration purposes or for demonstration measurements.

We present SCM measurements performed on commercial wafers at various stages of the fabrication process in order to show the utility of this technique in

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semiconductor industry. In addition to SCM, we apply EFM to specific parts of the wafer where SCM is hampered by buried pn interfaces. To our knowledge, there is only one former study where SCM was applied to commercial wafers to solve manufacturing problems [16]. Whereas in the former study the wafers were examined after the full manufacturing flow, our analysis is performed at various stages during the production process.

2. Experimental

Our measurements have been performed using a commercial AFM (AutoProbe M5 from Thermomicroscopes) equipped with an LC circuit serving as capacitance sensor and operating in a frequency range from 830 to 1030 MHz. The sensitivity of this detector is $\approx 10^{-19}$ F. The tip–sample capacitance is determined by measuring the shift of the resonance frequency of the LC resonator. Since the stray capacitance of the setup is about two orders of magnitude larger than the tip–sample capacitance ($\approx 10^{-15}$ F), it is difficult to measure the absolute value of the latter. Thus, we measure the dC/dV signal using a lock-in amplifier by applying an AC bias modulation voltage to the sample. Moreover, a variable DC bias voltage can also be applied to the sample. A schematic of our setup is presented in Fig. 1a. SCM images presented below have been taken by applying a DC bias voltage of 0 V and an AC modulation with 2.5 V rms at ≈ 100 kHz. The time required for the simultaneous acquisition of a topographic and capacitance image is typically 2–5 min. In order to illustrate the principle underlying our measurement we briefly discuss the characteristics of a MOS diode, in our case formed by the tip–oxide–wafer junction. A typical C–V curve at high frequency of an n-doped MOS diode is sketched in Fig. 1b. Note that the bias is applied to the semiconductor electrode. In the accumulation region we have

$$C_0 = \epsilon_{ox} \frac{A}{d},$$

where ϵ_{ox} is the dielectric constant of silicon oxide, A is the effective area and d is the silicon oxide thickness. In the strong inversion regime the capacity reaches its minimum

$$C_{min} = \frac{A\epsilon_{ox}}{d + (\epsilon_{ox}/\epsilon_s) W_m},$$

where ϵ_s is the dielectric constant of silicon and W_m is the depletion width [17]. As W_m is a known function of the doping, C–V measurements allow to extract the dopant concentration locally. Our lock-in amplifier reports the signed version of the differential capacitance signal, hence we can also identify the dopant nature (n or p) as shown in Fig. 1c. With the settings used for our experiments we obtain with the lock-in amplifier a signal which is roughly proportional to the difference between C_0 and C_{min} because the AC modulation sweeps the junction from the accumulation regime all the way to the depletion regime. Despite the well known fact that the SCM signal is very difficult to calibrate in terms of absolute values, we will demonstrate below that one can readily obtain valuable information about the oxide thickness variation if the dopant concentration is constant, or also visualize the nature of the dopants, and variations of their concentration, if the oxide thickness is constant. However, the SCM signal becomes very difficult to interpret if both quantities vary simultaneously.

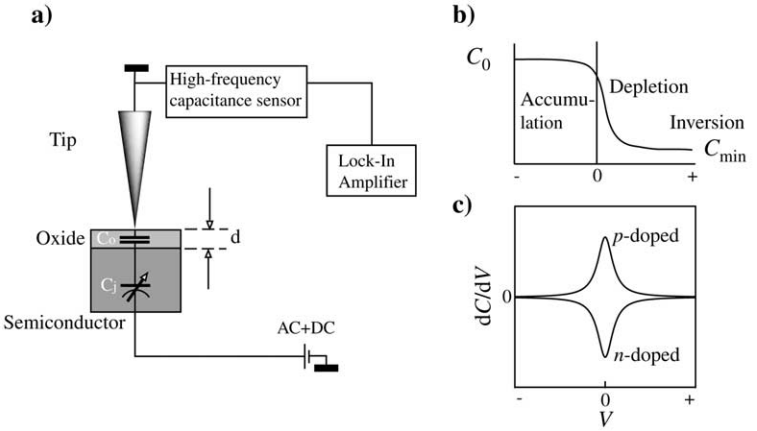

Fig. 1. (a) Schematic of the AFM/SCM design. (b) Typical C–V curve of n-doped MOS diode with bias applied to the semiconductor electrode. (c) Sketch of a $dC/dV(V)$ curve of a MOS diode. The sign identifies the nature of the dopants, n or p.

3. Scanning capacitance microscopy results

The SCM method has been applied to transistors built in 0.5 μm technology at an early stage of processing. At this stage, a 6000 Å thick field oxide has already been grown and a thin sacrificial oxide (200 Å) is present above the active area. The quality of this sacrificial oxide crucially determines the quality of the gate oxide which is grown in a later step. The doping is uniform below the silicon oxide around the transistor. Typical topographic and SCM images taken over one such transistor are displayed in Fig. 2. At this stage of processing the position of the bird's beak can be very precisely visualized in the SCM image showing the actual electrically active area. A larger SCM signal (coloured dark in the figure) can be seen near the edges of the active area. It corresponds to a thinning of the oxide linked probably to the well-known white ribbon effect or local stress. Up to now only TEM or high resolution SEM were able to reveal this phenomenon. These techniques require the complex and wafer destructive preparation of cross-sections. Due to the restriction to cross-sectional samples also no information about variations of the thinning along the perimeter was available preventing

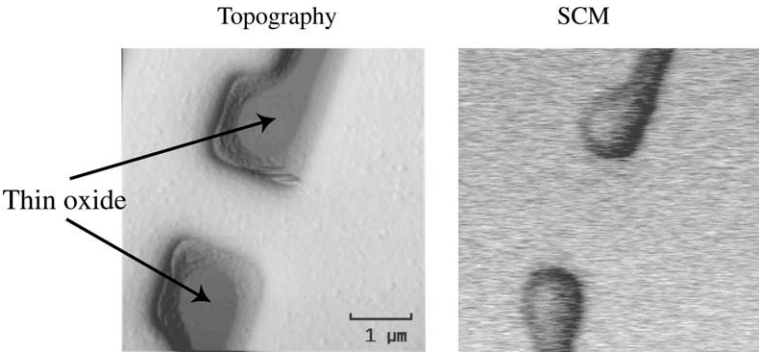

Fig. 2. Left: topography of a partially processed 0.5 μm transistor recorded with AFM. Right: SCM image of the same area. The SCM signal is large on the thin oxide and clearly reveals the non-uniformity of the oxide thickness (see text).

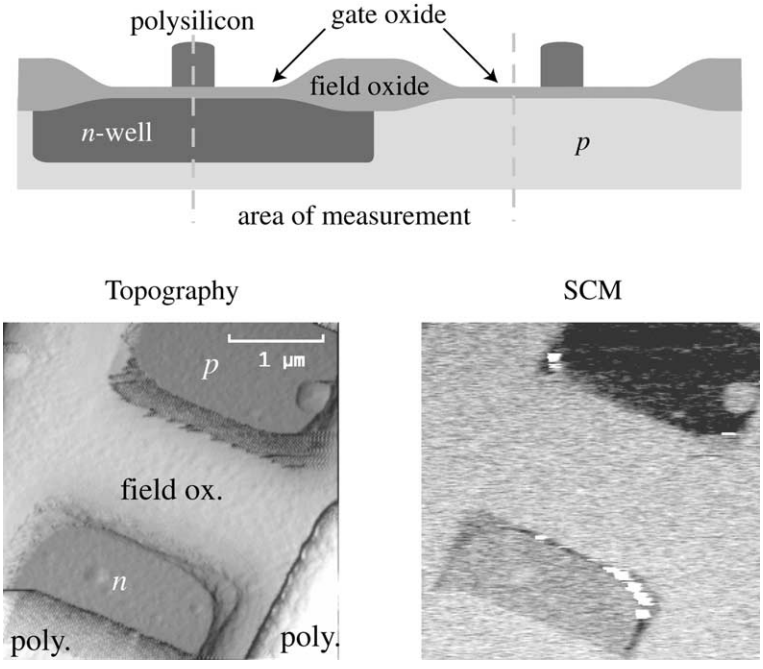

Fig. 3. Top: schematic cross-section of the active region of two adjacent PMOS and NMOS transistors. Left: AFM image of the transistor. Right: corresponding SCM image. The nature of the dopants can be identified (see text).

for instance to explore the influence of corners or to check the presence of local thinning or pitting. From the SCM image we can conclude that the thickness of the gate oxide is not uniform, exceeding our tolerance of ±5% at this stage of the fabrication process. In Fig. 3 we present SCM results on a similar wafer after being further processed. At this stage of fabrication the dopant implantation was performed and polysilicon lines have been added (see areas labelled polysilicon in Fig. 3). The SCM image shows three different signal levels. On the field oxide and on the electrically isolated polysilicon lines the signal is approximately zero. The large positive signal (in black in Fig. 3) on the gate oxide is ascribed to the p doping of the substrate of the NMOS transistor. Tentatively, one would expect the SCM signal over the n well to be negative and hence brighter than the gray level representing zero signal and characterizing the oxide. However, the signal over the n well is reduced because there the MOS diode is in series with a pn junction in the underlying Si substrate. Thus, the current is blocked at the buried pn interface and does not participate in the measurement of the capacitance. Despite the unconventional signal order caused by the pn interface buried under the n well, the three areas p doped, field oxide and n well are clearly discerned in the SCM image. Note that the uniformity of the gate oxide is good on this sample and that the oxide thinning at the edge no longer appears.

A further application of SCM is to reveal the positioning of operations that leave no topographic marks. For example SCM is well suited for determining the relative position of implanted areas on wafers. In Fig. 4 we demonstrate that visualization of the dopant areas can be easily achieved with SCM. The wafers have been fully delayered with HF etch as last operation before measurements and the naturally regrown oxide layer is sufficiently thick to enable SCM measurements. A wrong mask alignment during the dopant implantation can straightforwardly be detected (compare Fig. 4b and c). Note that this information is not available by electron microscopy in a non-destructive way.

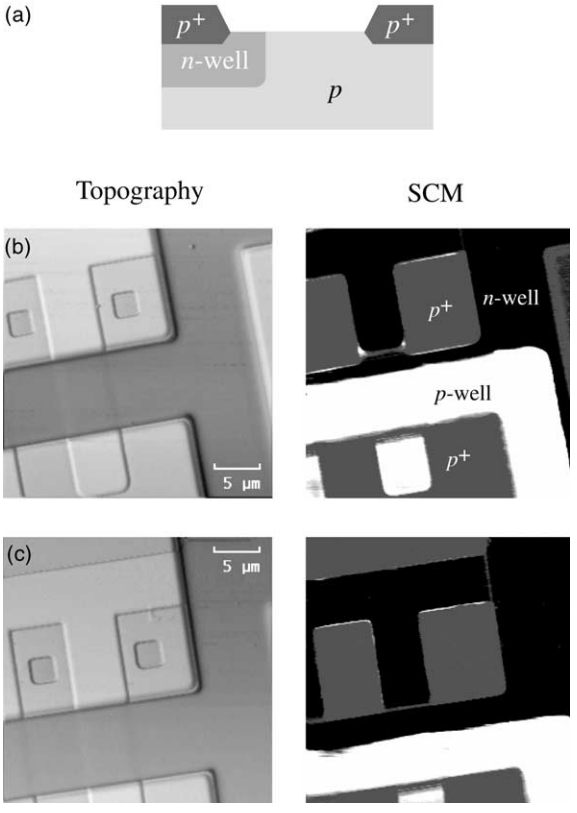

Fig. 4. (a) Schematic cross-section of the wafer. (b) AFM and SCM images of a wafer with mask misalignment; the n well adjacent to the p^+ areas is too narrow and current leakage occurs. (c) AFM and SCM images of a wafer with correct mask alignment.

4. Electrostatic force microscopy results

The SCM detection of an electrically insulated n well inside a p zone is hampered by the pn junction. Thus, we have explored the possibility of applying EFM [18–21]. In this method the AFM cantilever is mechanically excited at its resonance frequency (typically 200–500 kHz) and oscillates at the average distance z a few nanometers above the sample surface, as in conventional non-contact AFM mode. A voltage $U = U_{DC} + U_{AC}\sin(\omega t)$ is applied to the tip while the sample is grounded (we typically use a frequency $\omega \approx 2$–20 kHz). The resulting electrostatic force is then

$$F_{el} = -\frac{1}{2}\frac{dC}{dz}\left[\left(U_{DC}^2 + \frac{U_{AC}^2}{2}\right) + 2U_{DC}U_{AC}\sin(\omega t) - \frac{U_{AC}^2}{2}\cos(2\omega t)\right],$$

where C is the effective capacitance. Thus, the cantilever vibrates at the frequency ω and 2ω. The amplitude of

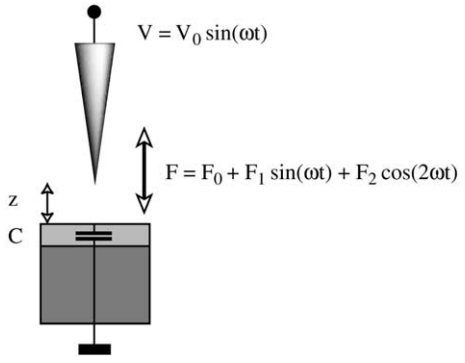

Fig. 5. Schematic of EFM measurements.

the cantilever oscillation at the second harmonic frequency is proportional to dC/dz and can be measured with lock-in technique [18]. Fig. 5 shows a sketch of the principles.

We have performed EFM measurements on EEPROM cells during the manufacturing process. FIB cross-sections of the tunnel oxide (injection window) had shown a local thinning near the bird's beak (see Fig. 6d). If this thinning had been extended over larger areas it could have been a major concern for reliability. In this case SCM could not be applied as a probe of oxide thickness variation because the underlying doping resulted in a buried pn junction. The EEPROM topography measured with AFM and a schematic cross-section are shown in Fig. 6a and b, respectively.

AFM and EFM zoom-in images of the tunnel window are presented in Fig. 7. The region covered by the thin oxide is very well revealed by means of EFM. As in the previous application (0.5 μm transistors) the size and shape of the electrically active area are easily visualized. This information is very useful since the true surface of the injection window is an important parameter to determine the real coupling for reading and programming the cell. Also when looking at the edge of the window it is easy to see that oxide thinning is relatively small and uniform. Note that since the measurement performed is electric the measured oxide thickness is also an effective electrical thickness. A minor drawback of EFM measurements is the possible transfer of electrostatic charges to the oxide surface. This leads to a sudden change in the cantilever height due to the varying electrostatic force and due to charging and discharging. These changes in tip height become visible upon close inspection of the

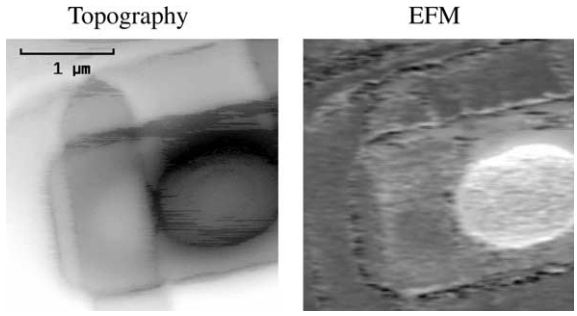

Fig. 7. Left: AFM topographic image of the tunnel window of an EEPROM cell. Right: corresponding EFM image.

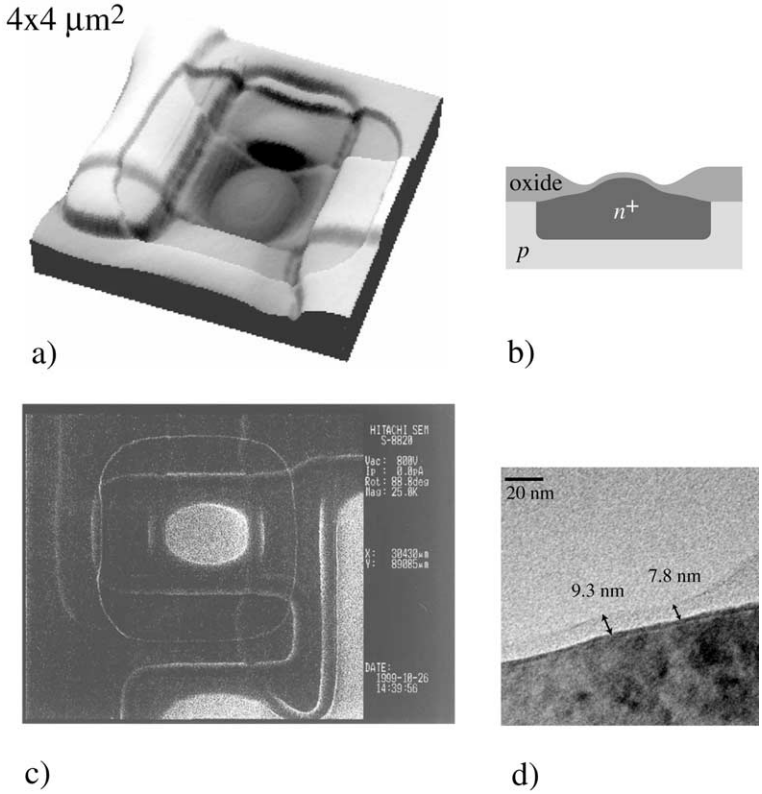

Fig. 6. (a) 3D representation of the EEPROM topography as measured by AFM. (b) Sketch of a cross-section. (c) SEM image of a similar EEPROM structure. (d) FIB cross-section showing the thinning of the tunnel oxide.

topographic image shown in Fig. 7. Although the lateral resolution of EFM is not as good as SCM because the tip–sample distance is larger, it is a valuable technique for characterizing devices where pn junctions defeat SCM characterization.

The topographic AFM measurements taken during this case study have demonstrated to be very useful by themselves. The pseudo 3D representation of the AFM topography in Fig. 6a shows very clearly the structure of the injection window. Compare the ease of reading the picture with respect to a similar SEM image shown in Fig. 6c. In the AFM measurement, it can be seen that the window is curved (note that the curvature is slightly exaggerated by the 3D presentation). This effect is due to succession of many cleaning and wet etching processes and would not have been revealed by SEM. From the AFM topograph we conclude that the injection window is neither defined by lithography nor by implantation but instead by field oxide growth and subsequent cleaning and wet etching steps.

5. Conclusions

The characterization of commercial semiconductor wafers at various stages of processing has been achieved using SCM and EFM. Even though our results are still qualitative, the identification of the exact position of doped areas or the variations of the oxide thickness can easily be visualized and this information has served as valuable input for process optimization in the fabrication process. SCM and EFM are tools which complement conventional microscopic techniques such as SEM and TEM. They often prove to be easier to use, they are non-destructive, and less expensive, considering both the investment for equipment and the cost per measurement.

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