Graphene

A Graphene Nanoribbon Memory Cell

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Over the past few years there has been a surge of interest in graphene, a recently isolated[1] one-atom-thick layer of carbon atoms arranged in a honeycomb lattice. From the application point of view this interest has mainly been driven by the high carrier mobility of graphene[2–4] which enables fabrication of field-effect transistors (FETs) with much smaller channel resistance compared to their Si counterparts.[5] In this manner, the ultimate limits of Si technology expected at the sub-10 nm scale may be overcome.[6] However, due to the absence of a bandgap in graphene and the formation of electron-hole puddles,[7] graphene FETs cannot be turned off, thus limiting their application in conventional electronic circuits. Alternative approaches, which do not require the presence of a bandgap, have been followed toward the implementation of graphene-based frequency doublers,[8] logic gates,[9] integrated circuits,[10] binary phase-shift keying modulators,[11] and ferroelectric gated memories.[12] Moreover, memory devices have been realized on the basis of nanoelectromechanical breaking and switching of graphene under high vacuum conditions, which results in a very low off current.[13–15] Another strategy to increase the on/off ratio relies upon patterning of graphene nanoribbons (GNRs), wherein quantum confinement and edge effects open a bandgap inversely proportional to the ribbon width.[16–18] Here we demonstrate a high performance GNR memory cell based on a nondestructive storage mechanism, i.e., gate voltage pulses of opposite polarity are used to switch between the distinct on and off states of the device.

The memory devices were fabricated by Ar ion-beam etching (IBE) of graphene monolayers using V_2O_5 nanofibers as etching masks.[19–21] To this end, graphene was mechanically exfoliated from highly oriented pyrolitic graphite onto a highly doped Si substrate covered with 300 nm of SiO_2 as gate dielectric.[1] V_2O_5 nanofibers were then deposited from aqueous solution, comprising 0.2 g ammonium metavanadate and 2 g acidic ion exchange resin (DOWEX 50WX8–100) in 40 ml deionized water.[22] Nanofibers with an average length of several μm and a rectangular cross section of approximately 4–8 nm × 10–20 nm were obtained after ageing of the solution for several weeks under ambient conditions (see Supporting information S1). Prior to nanofiber deposition, the SiO_2 surface was modified by (3–aminopropyl)-triethoxysilane. Graphene monolayers covered by a few V_2O_5 nanofibers were located by optical and atomic force microscopy (AFM). Subsequently, monolayers identified with the aid of confocal Raman spectroscopy[23] were contacted by Ti(1 nm)/AuPd(25 nm) electrodes defined by e-beam lithography. In addition to the source and drain contacts at the nanofiber ends, control electrodes were attached to the bare graphene and a nanofiber on SiO_2. The resulting contact configuration is exemplified in the inset of **Figure 1**. Finally, the samples were briefly (3 s) exposed to an Ar ion beam (with an accelerating voltage of 200 V, a beam current of 20 mA, and a pressure of 10^{-4} mbar) in order to etch the exposed graphene, followed by removal of remaining parts of the V_2O_5 nanofibers by dilute HCl solution. The last step was

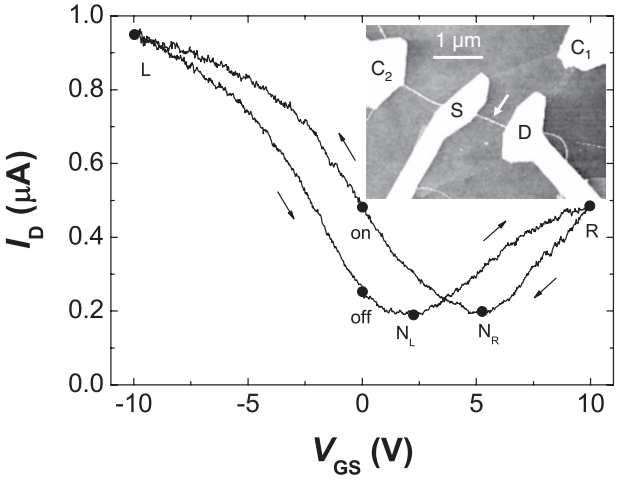

Figure 1. Transfer curve of an exemplary memory device recorded under ambient conditions at a drain-source voltage $V_{DS} = 1$ V. The gate sweep direction is indicated by the arrows. The left and right turning points of the sweep are denoted by L and R, respectively, and the current minima along the corresponding sweeps by N_L and N_R. The total sweep time is 9 min. Inset: AFM topography image of a GNR memory device after Ar IBE. The GNR (marked by the white arrow) is contacted by source (S) and drain (D) electrodes. Control electrodes C_1 and C_2 serve to test the resistance of the monolayer graphene and the V_2O_5 nanofiber after etching, respectively.

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optional, as the device operation proved to be independent of the presence of residual V_2O_5. A negligible electrical conductivity of the unprotected graphene (>100 GΩ) could be confirmed with the help of control electrode C_1 (see Supporting information S2). The control electrode C_2 was used to trace the resistance change of the V_2O_5 nanofiber upon etching, whereupon an increase from 100 MΩ to insulating was found. Accordingly, after etching finite resistance was detectable only between the S and D electrodes.

The obtained GNRs were electrically characterized in conventional FET configuration using the doped silicon substrate as a back gate. The transfer curve (drain current I_D vs. gate-source voltage V_{GS}) of a representative memory device, acquired under ambient conditions, is depicted in Figure 1. It exhibits a pronounced hysteresis, with an on/off ratio in the full voltage range of 5 (points L and N_L), and 2 at V_{GS} = 0 V (points on and off). The hysteresis could originate from charge trapping by water molecules around the GNR (see Supporting information S3), possibly combined with hydroxyl groups on the substrate, in analogy to carbon nanotube (CNT) devices.[24–28] The hysteresis allows selection of a gate voltage at which the GNR assumes two different conductance states depending on the sweep direction.[24,29,30] In order to eliminate static power dissipation in the input stage, these two states (marked by on and off in Figure 1) are chosen at V_{GS} = 0 V. For the present samples, the very thin nanofiber masks do not entirely protect the underlying graphene, such that the etching time has to be limited in order to keep the on resistance sufficiently low (~MΩ) to clock the devices in the lower radio-frequency range (~kHz). The best results have been attained with an etching time of 3 s, yielding an on/off ratio of 2. While a higher on/off ratio is obtained by longer etching, this also increases the on resistance and slows the device operation (see Supporting information S4).

A static pulse response measurement of the same device is presented in **Figure 2**. Triggering was done using a bipolar pulse-wave signal with a period of 3.5 min and a duty cycle of 10% which ensures stable and well-distinguished on and off states are reached. At such a low clock rate, the on/off ratio observed in Figure 1 is preserved. When the device is in the off state, a positive pulse moves the operating point as off→N_L→R→N_R→on (Figure 1), i.e., the device flips its state and remains in the new (on) state even after the gate voltage is reset. Since the currents in the on and off states are between the currents at the point R and the charge neutrality points N_L and N_R, both a current overshoot and undershoot occur during the pulse. Similarly, a negative gate pulse moves the operating point as on→L→off which restores the off state of the memory. In this case, only a current overshoot (at point L) is detected during the negative pulse.

Corresponding dynamic pulse response measurements at two different clock rates of the input signal are shown in **Figure 3**. The device was triggered with a bipolar pulse-wave signal with frequencies of up to 1 kHz. At the latter frequency, the difference between the currents in the on and off state is reduced due to the shorter pulse duration.[31] This effect is more evident for extremely small duty cycles, such as 0.1% in Figure 3(c). In this case, the pulse

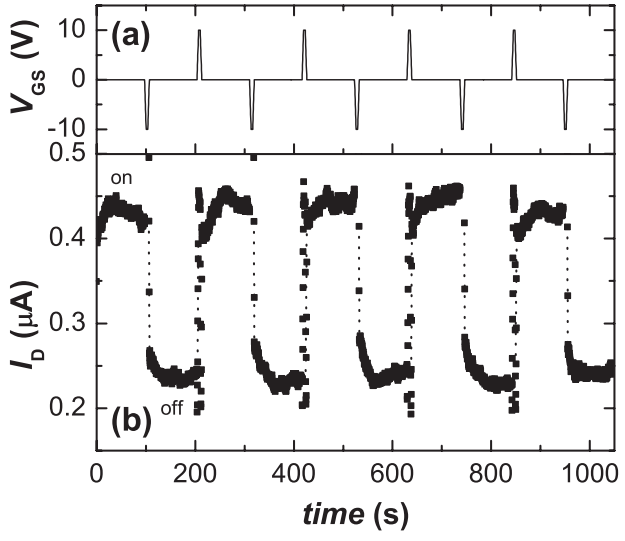

Figure 2. Memory effect in the fabricated GNR device. a) Switching of the device in Figure 1 by a trigger signal with an amplitude 10 V and a duty cycle of 10%. b) Drain current under ambient conditions at V_{DS} = 1 V.

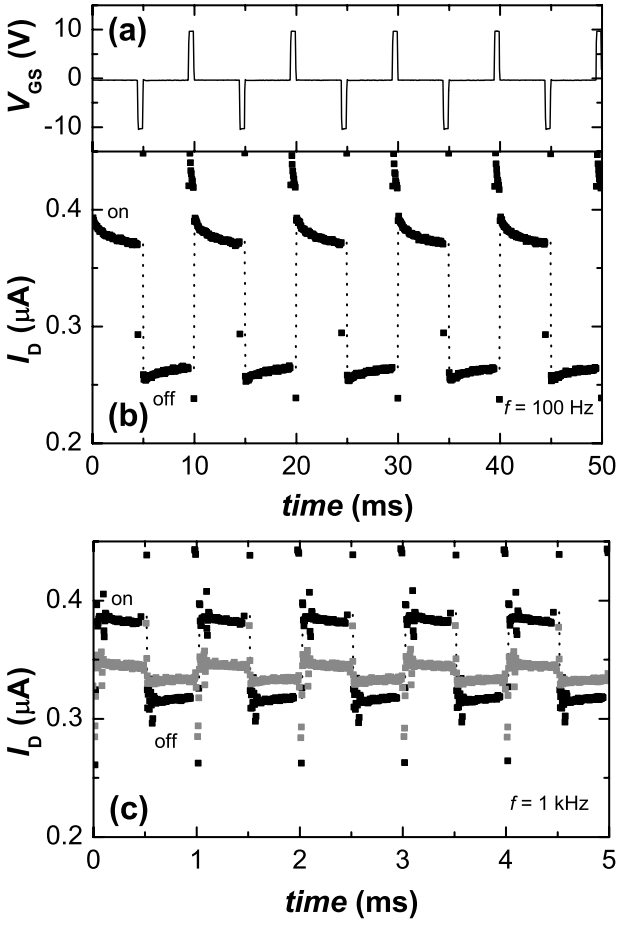

Figure 3. Digital waveforms gained from the device of Figure 1 under ambient conditions. a) Trigger signal at a frequency f = 100 Hz and a duty cycle of 10%. b,c) I_D at V_{DS} = 1 V recorded with an input signal frequency of f = 100 Hz (panel b) and f = 1 kHz (panel c). At 1 kHz, two different duty cycles were used: 10% (black; pulse duration of 50 μs) and 0.1% (gray; pulse duration of 500 ns).

duration is only 500 ns at 1 kHz, resulting in a difference between the on and off currents of only 5%. Compared to the pulse durations in the range of 1 to 10 ms reported for CNT-FET memories with a SiO_2 gate dielectric[29,32,33] the present devices can be switched approximately three orders of magnitude faster. The highest operating clock frequency was found to be ~5 kHz (at a duty cycle of 10%), which is not limited by the device itself but rather by the bandwidth of the current sense amplifier used to measure the drain current. The obtained high clock rate, which exceeds that reported for other CNT and graphene memory devices by several orders of magnitude,[13,33] demonstrates that it is not only possible to trigger the device with very short pulses but also that the device has a very short transition time (<1 ms). Such clock rates are not evident in other CNT or graphene memory devices, for which transition times are not explicitly given. Even faster and more stable charging/discharging may be achievable with different gate dielectrics,[33] or by an improved etching process which reduces the on resistance of the GNRs.

In contrast to nonvolatile CNT memory devices,[24,29,30] the GNR memory cell was found to be volatile under ambient conditions. The on and off state were found to slowly drift to an intermediate conductance over ~6 hours, as apparent from **Figure 4**. This change was observed both in powered (V_{DS} = 1 V constantly applied) and unpowered (V_{DS} = 1 V only applied for data acquisition) devices. This drift was significantly reduced by placing the samples in vacuum. The traps discharge over approximately 1 day at a pressure of ~10^{-2} mbar and >3 days at ~10^{-5} mbar. One further gate sweep is sufficient to charge the traps and restore the states. The appreciable volatility under ambient hints toward interaction between water molecules and functional groups on the SiO_2 (e.g., silanol groups)[26,28,34] or hydroxyl groups located at the GNR edges. The importance of surface water gains further support from the device behavior at low temperatures (100 K), under which condition no discharging was observed over long periods of time (>2 days; see Figure S6 in the Supporting information). It is noteworthy that the stored data was also retained during the same period of time if the device was powered by V_{DS} = 1 V, demonstrating its good durability and stability. The device was also operated for many hours at various clock rates (<10 kHz) and temperatures without any degradation or failure, yielding an endurance of >10^7 cycles. These characteristics render the GNR devices suitable for application as both static random access memory and nonvolatile flash memory cells.

In summary, we have demonstrated GNR-based memory devices that can be operated under ambient conditions with digital signal switching in the kHz range. The retention time could be further improved via appropriate device encapsulation or chemical functionalization of the GNR edges, with the latter offering the prospective of simultaneously reduced carrier scattering. Very fast memories with clock frequencies that outperform conventional dynamic random access memories may be achievable by GNRs with well-defined crystallographic orientation.

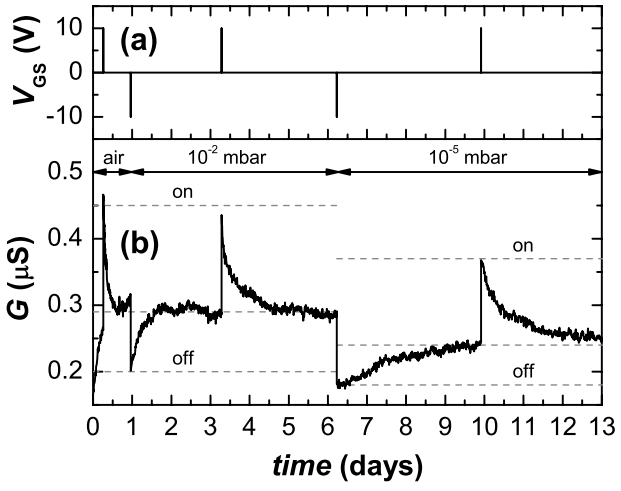

Figure 4. Data retention in the unpowered memory device of Figure 1. a) Trigger signal. b) Conductance acquired under ambient conditions and at room temperature at a pressure of 10^{-2} mbar and 10^{-5} mbar.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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[1] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, A. A. Firsov, *Science* **2004**, *306*, 666–669.
[2] K. I. Bolotin, K. J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, H. L. Stormer, *Solid State Commun.* **2008**, *146*, 351–355.
[3] X. Du, I. Skachko, A. Barker, E. Y. Andrei, *Nature Nanotech.* **2008**, *3*, 491–495.
[4] X. Hong, A. Posadas, K. Zou, C. H. Ahn, J. Zhu, *Phys. Rev. Lett.* **2009**, *102*, 136808.
[5] Y.-M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H.-Y. Chiu, A. Grill, P. Avouris, *Science* **2010**, *327*, 662.
[6] J. D. Meindl, Q. Chen, J. A. Davis, *Science* **2001**, *293*, 2044–2049.
[7] J. Martin, N. Akerman, G. Ulbricht, T. Lohmann, J. H. Smet, K. v. Klitzing, A. Yacoby, *Nature Phys.* **2008**, *4*, 144–148.
[8] H. Wang, D. Nezich, J. Kong, T. Palacios, *IEEE Electron Device Lett.* **2009**, *30*, 547–549.
[9] R. Sordan, F. Traversi, V. Russo, *Appl. Phys. Lett.* **2009**, *94*, 073305.
[10] F. Traversi, V. Russo, R. Sordan, *Appl. Phys. Lett.* **2009**, *94*, 223312.
[11] N. Harada, K. Yagi, S. Sato, N. Yokoyama, *Appl. Phys. Lett.* **2010**, *96*, 012102.

[12] Y. Zheng, G.-X. Ni, C.-T. Toh, M.-G. Zeng, S.-T. Chen, K. Yao, B. Özyilmaz, *Appl. Phys. Lett.* **2009**, *94*, 163505.
[13] B. Standley, W. Bao, H. Zhang, J. Bruck, C. N. Lau, M. Bockrath, *Nano Lett.* **2008**, *8*, 3345–3349.
[14] Y. Li, A. Sinitskii, J. M. Tour, *Nature Mater.* **2008**, *7*, 966–971.
[15] A. Sinitskii, J. M. Tour, *ACS Nano* **2009**, *3*, 2760–2766.
[16] V. Barone, O. Hod, G. E. Scuseria, *Nano Lett.* **2006**, *6*, 2748–2754.
[17] Y.-W. Son, M. L. Cohen, S. G. Louie, *Phys. Rev. Lett.* **2006**, *97*, 216803.
[18] M. Y. Han, B. Özyilmaz, Y. Zhang, P. Kim, *Phys. Rev. Lett.* **2007**, *98*, 206805.
[19] R. Sordan, M. Burghard, K. Kern, *Appl. Phys. Lett.* **2001**, *79*, 2073–2075.
[20] J. Bai, X. Duan, Y. Huang, *Nano Lett.* **2009**, *9*, 2083–2087.
[21] A. Fasoli, A. Colli, A. Lombardo, A. C. Ferrari, *Phys. Status Solidi B* **2009**, *246*, 2514–2517.
[22] J. Muster, G. T. Kim, V. Krstić, J. G. Park, Y. W. Park, S. Roth, M. Burghard, *Adv. Mater.* **2000**, *12*, 420–424.
[23] A. C. Ferrari, J. C. Meyer, V. Scardaci, C. Casiraghi, M. Lazzeri, F. Mauri, S. Piscanec, D. Jiang, K. S. Novoselov, S. Roth, A. K. Geim, *Phys. Rev. Lett.* **2006**, *97*, 187401.
[24] J. B. Cui, R. Sordan, M. Burghard, K. Kern, *Appl. Phys. Lett.* **2002**, *81*, 3260–3262.
[25] W. Kim, A. Javey, O. Vermesh, Q. Wang, Y. Li, H. Dai, *Nano Lett.* **2003**, *3*, 193–198.
[26] J. S. Lee, S. Ryu, K. Yoo, I. S. Choi, W. S. Yun, J. Kim, *J. Phys. Chem. C* **2007**, *111*, 12504–12507.
[27] T. O. Wehling, A. I. Lichtenstein, M. I. Katsnelson, *Appl. Phys. Lett.* **2008**, *93*, 202110.
[28] A. D. Bartolomeo, M. Rinzan, A. K. Boyd, Y. Yang, L. Guadagno, F. Giubileo, P. Barbara, *Nanotechnology* **2010**, *21*, 115204.
[29] M. Radosavljevi , M. Freitag, K. V. Thadani, A. T. Johnson, *Nano Lett.* **2002**, *2*, 761–764.
[30] M. S. Fuhrer, B. M. Kim, T. Dürkop, T. Brintlinger, *Nano Lett.* **2002**, *2*, 755–759.
[31] D. Estrada, S. Dutta, A. Liao, E. Pop, *Nanotechnology* **2010**, *21*, 085702.
[32] L. Marty, A. Iaia, M. Faucher, V. Bouchiat, C. Naud, M. Chaumont, T. Fournier, A. Bonnot, *Thin Solid Films* **2006**, *501*, 299–302.
[33] M. Rinkiö, A. Johansson, G. S. *Paraoanu*, P. Törmä, *Nano Lett.* **2009**, *9*, 643–647.
[34] D. B. Asay, A. L. Barnette, S. H. Kim, *J. Phys. Chem. C* **2009**, *113*, 2128–2133.

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