Contact resistance effects in organic n-channel thin-film transistors

THIS IS A TEMPORARY TITLE PAGE
It will be replaced for the final print by a version
provided by the service academique.

Thèse no. 6805 (2015)
présentée le 24 septembre 2015
à la Faculté des Sciences de Base
Laboratoire de Science à l'Échelle Nanométrique
Programme Doctoral en Physique
École Polytechnique Fédérale de Lausanne

pour l'obtention du grade de Docteur ès Sciences
par

Reinhold Rödel

acceptée sur proposition du jury:

Prof. Cécile Hébert, président du jury
Prof. Klaus Kern, directeur de thèse
Dr. Hagen Klauk, co-directeur de thèse
Prof. Holger Frauenrath, rapporteur
Prof. Jana Zaumseil, rapporteuse
Prof. Jens Pflaum, rapporteur

Lausanne, EPFL, 2015

Abstract

Organic thin-film transistors (TFTs) have undergone tremendous progress in the past few years. Their great potential in terms of mechanical flexibility, light weight, low-cost and large-area fabrication makes them promising candidates for novel electronic products, such as sensor arrays, radio-frequency identification tags and flexible displays. For the realization of these applications and to improve their performance it is necessary to miniaturize organic TFTs to dimensions of a few micrometers or even less. However, with such aggressive scaling, the device physics becomes more and more important. Especially the contact resistance at and close to the interface between the organic semiconductor and the source/drain metal limits the performance of the organic TFTs at miniaturized dimensions.

In this thesis, the contact properties of bottom-gate, top-contact n-channel organic transistors are investigated using the gated four-probe (GFP) technique. The TFTs employ the small-molecule semiconductor N,N'-bis-(1H,1H-heptafluorobutyl)-1,7-dicyano-perylene-3,4:9,10-tetracarboxylic diimide (PDI-FCN_2) and are fabricated on flexible plastic substrates. The transistors are air-stable and can be operated at low voltages of about 3 V, owing to a thin hybrid gate dielectric composed of aluminum oxide and a self-assembled molecular monolayer.

The GFP method enabled a detailed investigation of the influence of a multitude of factors, including the gate-source and drain-source voltages, the contact length, the temperature and the contact metal, on the contact resistance. The contact properties are found to be very sensitive to the thickness of the organic semiconductor layer. In transistors in which this layer is relatively thin, ohmic contact resistances as small as about 0.6 $k\Omega\,cm$ were measured. In transistors with a relatively thick organic semiconductor layer, device physics becomes more complex and the current-voltage characteristics of the contact become nonlinear. Space-charge limited currents are identified as the probable origin of this nonlinear behavior.

The good performance of the PDI-FCN_2 transistors allows the realization of simple integrated circuits. Flexible organic complementary ring oscillators are fabricated and signal propagation delays per stage as short as 6 μs are demonstrated at a supply voltage of 3.6 V.

Keywords: Organic thin-film transistor, organic semiconductor, contact resistance, gated four-probe technique, flexible electronics, ring oscillator

Zusammenfassung

Organische Dünnschichttransistoren (englisch: thin-film transistors, TFTs) haben in den letzten Jahren gewaltige Fortschritte vollzogen. Ihr großes Potentialin Hinsicht auf mechanische Flexibilität, geringes Gewicht und günstige sowie großflächige Produktion macht sie zu interessanten Kandidaten für neuartige elektronische Produkte wie Sensorfelder, Funkfreqenz-Identifizierung (englisch: radio frequency identification, RFID) und flexible Bildschirme. Für die Realisierung dieser Anwendungen und zur Verbesserung der Leistungsfähigkeit ist es notwendig, die organischen Dünnschichttransistoren auf Dimensionen von wenigen Mikrometern oder darunter zu miniaturisieren. Durch eine derartige Skalierung werden jedoch verschiedene Aspekte der Bauelementphysik zunehmend kritisch. Insbesondere der Kontaktwiderstand an und in der Umgebung der Grenzfläche zwischen organischem Halbleiter und den Source/Drain-Kontakten limitiert die Leistungsfähigkeit der Transistoren bei miniaturisierten Abmessungen.

In dieser Arbeit werden die Kontakteigenschaften organischer n-Kanal Transistoren mittels Vierpunktmessung untersucht. Dabei wird eine Geometrie verwendet, bei der sich die Gate-Elektrode sowie das Dielektrikum unter dem organischen Halbleiter befinden, während die Source/Drain-Kontakte auf den Halbleiter aufgedampft werden. In den Dünnschichttransistoren wird das Molekül N,N'-bis-(1H,1H-heptafluorobutyl)-1,7-dicyano-perylene-3,4:9,10-tetracarboxylic diimide (PDI-FCN_2) als organischer Halbleiter eingesetzt, und die Herstellung erfolgt auf einem flexiblem Plastiksubstrat. Die Transistoren sind luftstabil und können dank eines dünnen hybriden Dielektrikums, bestehend aus Aluminiumoxid und einer selbstorganisierten molekularen Monolage, bei Spannungen von ca. 3 V betrieben werden.

Die Vierpunktmethode erlaubt eine detaillierte Untersuchung des Einflusses von einer Vielzahl von Faktoren, einschließlich der Gate-Source- und Drain-Source Spannungen, der Kontaktlänge, der Temperatur und des Kontaktmaterials, auf den Kontaktwiderstand. Die Kontakteigenschaften hängen sehr sensibel von der Schichtdicke des organischen Halbleiters ab. In Transistoren, bei denen diese Schicht relativ dünn ist, wurden kleine und ohmsche Kontaktwiderstände in der Höhe von etwa 0.6 $k\Omega\,cm$ gemessen. In Transistoren mit einer relativ dicken Halbleiterschicht wird die Bauteilphysik zunehmend komplex, und nichtlineare Strom-Spannungs-Kennlinien des Kontaktes können beobachtet werden. Raumladungsbegrenzte Ströme wurden als wahrscheinliche Ursache für dieses Phänomen

identifiziert.
Die vorteilhaften Eigenschaften der PDI-FCN_2-Transistoren erlauben die Realisierung einfacher integrierter Schaltungen. Flexible organische komplementäre Ringoszillatoren wurden hergestellt und kleine Signalverzögerungen pro Inverterstufe bis zu 6 μs bei einer Versorgungsspannung von 3.6 V werden gezeigt.

Schlagwörter: Organischer Dünnschichttransistor, organischer Halbleiter, Kontaktwiderstand, Vierpunktmessung, flexible Elektronik, Ringoszillator

Contents

List of Figures

List of Tables

List of acronyms

a-Si:H	hydrogenated amorphous silicon	2
AFM	atomic force microscopy	30
CMOS	complementary metal-oxide semiconductor	20
CNL	charge neutrality level	18
DNTT	dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene	34
DOS	density of states	9
FET	field-effect transistor	1
GFP	gated four-probe	30
HOMO	highest occupied molecular orbital	5
KPFM	Kelvin probe force microscopy	30
LUMO	lowest unoccupied molecular orbital	5
MIS	metal-insulator-semiconductor	13
MOSFET	metal-oxide-semiconductor field-effect transistor	1
MTR	multiple trapping and release	8
OLED	organic light-emitting diode	2
OPVC	organic photovoltaic cell	2
OTFT	organic thin-film transistor	2
PDI-FCN_2	N,N'-bis-(1H,1H-heptafluorobutyl)-1,7-dicyano-perylene-3,4:9,10-tetracarboxylic diimide	21
PEN	polyethylene naphthalate	33
RFID	radio frequency identification	3

S/D	source and drain	12
SAM	self-assembled monolayer	25
SCLC	space-charge-limited current	11
SEM	scanning electron microscopy	34
TFT	thin-film transistor	1
TLM	transmission line method	28
UHV	ultra-high vacuum	19
VRH	variable range hopping	9
XRD	x-ray diffraction	22

List of symbols

χ	electron affinity of the semiconductor	17
Δ	potential across interfacial layer	18
ΔV_{ch}	potential drop across the channel	30
ΔV_D	potential drop across the drain contact region	30
ΔV_S	potential drop across the source contact region	30
ε_S	permittivity of the semiconductor	11
μ	charge-carrier mobility	7
μ_0	intrinsic mobility	23
μ_{eff}	effective mobility	23
Φ_b	barrier height	17
Φ_m	work function of the metal	17
Φ_s	work function of the semiconductor	17
ρ_{bulk}	bulk contact resistivity	25
ρ_C	contact resistivity	25
ρ_D	drain contact resistivity	25
ρ_{int}	interface contact resistivity	25
ρ_S	source contact resistivity	25
τ	signal delay per stage	107
Θ	derivative of the contact resistivity with respect to the gate overdrive voltage	52
C_{ch}	channel capacitance	32
C_G	gate capacitance	32
C_i	gate dielectric capacitance per unit area	13
C_n	fringe capacitances of the n-channel transistor	109
C_{ov}	overlap capacitance	32
C_p	fringe capacitances of the p-channel transistor	109
C_{semi}	depletion layer capacitance of the semiconductor	16
C_{traps}	capacitance associated with traps at the dielectric-semiconductor interface	16
d	nominal semiconductor thickness	34

$\vec{E}$	electric field	6
e	elementary charge	7
E_A	activation energy	76
E_F	Fermi energy	17
E_{vac}	vacuum level	17
f_{osc}	oscillation frequency	107
f_T	cutoff frequency	32
g_m	transconductance	15
G_{sheet}	sheet conductance	37
I_D	drain current	12
i_G	displacement current	31
I_G	gate leakage current	12
I_{TE}	thermionic emission current across a metal-semiconductor interface	19
J	current density	11
k_B	Boltzmann constant	9
L	channel length	12
L_1	position of the first potential probe	30
L_2	position of the second potential probe	30
L_3	position of the third potential probe	62
L_C	contact length (gate to source/drain overlap)	25
$L_{C,D}$	drain contact length	32
$L_{C,S}$	source contact length	32
L_T	transfer length	26
$L_{T,D}$	transfer length on the drain side	26
$L_{T,S}$	transfer length on the source side	26
m	exponent in the current-voltage characteristics of the contact	66
n	charge-carrier density	7
n_{st}	number of inverter stages	105

R_C	total contact resistance	23
R_{ch}	channel resistance	23
$R_C W$	width-normalized total contact resistance	23
R_D	drain contact resistance	23
R_S	source contact resistance	23
R_{sheet}	sheet resistance	23
R_{tot}	total transistor resistance	23
S	subthreshold swing (or slope)	16
T_C	characteristic temperature in the trap limited SCLC theory	12
T	temperature	7
V_1	channel potential at position L_1	30
V_2	channel potential at position L_2	30
V_C	potential drop across the contact region	29
V_{ch}	potential drop across the channel region	29
V_{CO}	crossover voltage	69
$\vec{v_D}$	drift velocity	6
V_{DD}	supply voltage	106
$V_{GD,eff}$	effective gate-drain voltage above threshold	64
V_{DS}	drain-source voltage	12
V_{Gch}	average gate-channel voltage	38
V_{GD}	gate-drain voltage	64
V_{GS}	gate-source voltage	12
$V_{GS} - V_{th}$	gate overdrive voltage	38
V_{IN}	input voltage	106
V_{OUT}	output voltage	106
$V_{GS,eff}$	effective gate-source voltage above threshold	66
V_{th}	intrinsic threshold voltage	13
$V_{th,eff}$	effective threshold voltage	54
$V_{th,SD}$	threshold voltage from second derivative method	56
$V[x]$	potential in the channel at position x	13
W	channel width	13
W_{SC}	width of the space-charge region	17

x	lateral position in the channel	13
y	perpendicular distance from the semiconductor/dielectric interface	14

1 Introduction

The history of semiconductors started in the 19th century when experiments revealed the surprising properties of these materials, namely the unexpected temperature dependence of the electrical resistance, the photovoltaic effect and rectification. Today, semiconductors are a key element of most electrical devices and the materials that allow the realization of transistors, the basic building block of modern electronics. Transistors are microelectronic devices that amplify and switch electrical signals. Embedded in integrated circuits, they enabled the development of the computers, phones, household aids and many more applications that we use today.

The idea of the transistor dates back to 1925 when Julius E. Lilienfeld described its principles in a patent [1]. In 1934, Oscar Heil patented a similar device and noted that the active material should be a semiconductor [2], but neither Lilienfeld nor Heil were able to fabricate a working device - most likely because high-quality semiconductors were not available at that time. The transistors described by Lilienfeld and Heil are very similar to what is nowadays called a field-effect transistor (FET) - a transistor in which the conductivity of one type of charge carrier is controlled by an electric field.

It took more than twenty years until the first successful and reproducible demonstration of the transistor by John Bardeen and Walter Brattain (1947) and William Shockley (1948) at Bell Labs. In 1956, they were jointly awarded the Nobel Prize in Physics "for their researches on semiconductors and their discovery of the transistor effect". Although their transistors were not FETs, but bipolar junction transistors (BJTs, a type of transistor that is barely used nowadays), their invention was stimulating for further research.

In 1960, Dawon Kahng and Martin M. Atalla built the first FET, a metal-oxide-semiconductor field-effect transistor (MOSFET), also at Bell Labs [3]. In this FET implementation, crystalline silicon was used both as supporting substrate and active material. Thanks to more than half a century of intensive materials and device research and development as well as excellent materials properties (such as bulk charge-carrier mobilities around 10^3 cm^2/Vs), today's silicon MOSFETs have exceptional static and dynamic performance, high integration densities and very low manufacturing costs per transistor, making them the by far the most common type of transistor.

Another transistor configuration, the thin-film transistor (TFT), was invented in 1962 by Paul Weimer [4]. In TFTs, thin films of a semiconductor layer are deposited onto a sup-

porting substrate. TFTs lack the high crystallinity of the active material and therefore have a lower performance than MOSFETs, but can be implemented on a variety of substrates, allowing large-area applications such as displays. Common TFT active materials are hydrogenated amorphous silicon (a-Si:H) or polycrystalline silicon.

Compared to its inorganic counterpart, organic electronics is a much younger scientific field, although first observations of conductive organic materials date back to 1862 when Henry Letheby obtained a partly conductive polymer, probably polyaniline. Organic charge transfer complexes, which have a somewhat higher conductivity, were reported only in the 1950s. Although conductivity in organic materials was in principal an exciting phenomenon, interest in these materials remained limited due to poor reproducibility, difficulties in controlling the material purity and low conductivity. A breakthrough was achieved with the discovery of high electrical conductivity and the ability to tune it over seven orders of magnitude in oxidized iodine-doped polyacetylene by Alan J. Heeger, Alan MacDiarmid and Hideki Shirakawa in 1977. They were awarded the 2000 Nobel Prize in Chemistry "for the discovery and development of conductive polymers". The 1977 breakthrough was followed by great progress in organic electronic devices, which can be classified into three main categories: organic light-emitting diodes (OLEDs) [5, 6], organic photovoltaic cells (OPVCs) [7–9] and organic thin-film transistors (OTFTs). OLEDs are already used in commercial applications, mostly for displays in devices like smartphones, cameras or TVs. OPVCs are supposedly at the threshold to commercialization, with a limited industrial production already ongoing. OTFTs are currently in the state of academic and industrial research, although a number of impressive demonstrators already exist.

The first preliminary field-effect measurements in organic films date back to the 1960s and 1970s [10, 11]. Significant work on OTFTs was conducted in the late 1980s, but the charge-carrier mobilities were still quite low, in the range of 10^{-5} to 10^{-3} $\mathrm{cm}^2/\mathrm{Vs}$ [12–14]. Only in the 1990s the charge-carrier mobilities reached values comparable to those of a-Si:H TFTs ($\sim 0.1 - 1$ $\mathrm{cm}^2/\mathrm{Vs}$), leading to a growing interest in organic transistors [15]. Modern OTFTs reach mobilities in the range of 1 $\mathrm{cm}^2/\mathrm{Vs}$ to 10 $\mathrm{cm}^2/\mathrm{Vs}$ or even higher [16–18], demonstrating great advance and potential. However, organic transistor technology is still in its infancies and has to deal with several problems such as stability, reliability, reproducibility and uniformity. These problems are partly caused by the fact that in the field of organic electronics not only one material is investigated. Instead, the class of organic semiconductors includes a wide variety of materials with specific properties, and the physical processes in devices made of different materials can be quite diverse. Consequently, it is no surprise that several fundamental aspects of organic electronic devices are still poorly understood.

On the other hand, the wide variety of available materials and modifications provides a

significant advantage, because it allows the optimization of the organic material properties depending on the target application. As an example, chemical modifications can be used to make an organic semiconductor molecule more stable [16], make it sensitive to specific substances in view of sensor applications [19], or introduce solubility [20], allowing processing via printing techniques.

Organic transistors are not expected to compete with silicon devices in high-end applications, both due to limitations in OTFT performance and because silicon technology is superior and more economic in many aspects. Instead, the interest in OTFTs mainly stems from the fact that they can be processed at very low temperatures, making them compatible with unconventional substrates like glass, plastic or even paper. Hence, potential applications aim in the direction of novel products that are bendable and rollable, such as backplanes for flexible active-matrix displays [21, 22], e-paper [23] or sensors including e-skin [24–26]. In addition, research and development is driven by the possibility of large-area processing and the hope for low-cost and high-throughput fabrication [27], which would be appealing for low-end or disposable applications like radio frequency identification (RFID) [28–30].

More demanding applications, such as flexible, high-resolution diplays, require higher integration densities and higher switching speeds of the transistors [23]. A common way to improve these properties is the reduction of the lateral dimensions, most importantly the channel length. However, as the channel length is reduced, parasitic contact resistances can become dominant. This problem is more serious compared to inorganic transistor technologies, because contact doping is more complicated and less efficient in OTFTs.

This thesis aims at a better understanding and a more detailed picture of the contact effects in organic transistors. Therefore, special emphasis was placed on performing the investigations in a realistic environment, i.e., under conditions that are close to application requirements. Electron-transporting OTFTs usually have a lower performance than their p-channel counterparts, thus restricting the capabilities of low-power complementary circuits [31, 32]. Therefore, the analysis was performed on n-channel organic transistors with the aim of alleviating this limiting factor.

This thesis is organized as follows. Chapter 2 provides a brief introduction to organic semiconductors and organic transistors, including details about the charge transport, the related interfaces, the particular organic semiconductor employed in this work, and the properties of the contacts and how they are determined. In chapter 3, the fabrication and characterization of the organic thin-film transistors is explained, with a focus on the method for contact resistance analysis employed in this work. Chapter 4 deals with a detailed analysis of the contact properties of n-channel organic transistors. The impact of numerous parameters on the source and drain contact resistance is investigated, and conclusions are drawn regarding the origin of the contact resistance. The stability of

organic transistors is a major issue for possible applications. Therefore, the shelf-life stability and the sensitivity to bias stress of the transistors employed in this work is studied in chapter 5. Finally, chapter 6 presents the fabrication and characterization of integrated organic complementary circuits.

2 Theory

2.1 Organic semiconductors

The element carbon is unique in several aspects and leads to the largest variety of chemical compounds. One reason for that is the ability to hybridize in three different configurations, formed by the superposition of the s and p orbitals. In one of these configurations, the sp^2 hybridization, the $2s$ and the $2p_x$ and $2p_y$ orbitals mix, forming three σ bonds. The remaining $2p_z$ orbital is oriented perpendicular to the sp^2 orbitals, and materials in which some or all neighboring carbon atoms are sp^2 hybridized are called conjugated materials. A simple example of a conjugated molecule is benzene, illustrated in figure 2.1. It consists of six sp^2-hybridized carbon atoms arranged in a ring. The three sp^2 orbitals of each carbon atom are oriented in one plane and form σ bonds with two other carbon atoms and one hydrogen atom, these bonds are rather strong and localized. In contrast, the $2p_z$ orbitals of the carbon atoms form π bonds, whose combination is termed π molecular orbitals. These orbitals are delocalized over the entire molecule, which is often illustrated by an alternation of single bonds (only σ bonds) and double bonds (σ and π bonds) between the carbon atoms in one of the two equivalent resonance forms (figure 2.1a) [33]. An alternative illustration that more accurately describes the delocalization would be a ring representing the delocalized electron cloud (figure 2.1b).

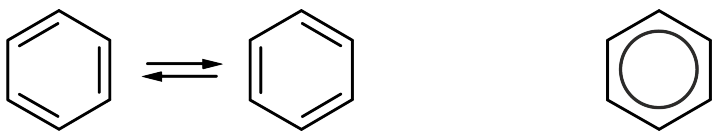


Figure 2.1: **Common representations of benzene.** (a) Resonance structures of benzene. (b) Benzene ring structure illustrating the even distribution of the π electron density.

Due to their delocalized character, the molecular π orbitals are crucial for charge transport in these molecules. Thereby, the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) are most relevant, because they correspond approximately to the valence and conduction band of conventional inorganic semicon-

ductors. Accordingly, the energy difference between the HOMO and the LUMO plays a similar role as the band gap.
Generally speaking, organic semiconductors are conjugated organic molecules with semiconducting properties. Benzene has a HOMO-LUMO gap of around 6.0 eV [34], making it an insulator. However, it is for example possible to linearly fuse benzene rings to form various acenes, an important class of organic semiconductors. By adding benzene rings, the π electrons are delocalized over more and more carbon atoms. In analogy to the particle in a box problem, the confinement effects are weakened as the molecule gets larger, reducing the difference between the energy levels. Thus, the HOMO-LUMO gap decreases with the number of fused benzene rings. Pentacene, for example, which consists of five linearly fused benzene rings (figure 2.2), has a HOMO-LUMO gap of around 2.1 eV [34] and is one of the most prominent organic semiconductors.

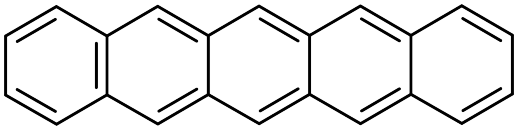


Figure 2.2: **Chemical structure of pentacene.**

Acenes belong to one class of organic semiconductors, the small molecules. Small molecules have a low molar mass and can therefore usually be purified and deposited by thermal sublimation. Due to the great number of possible structures, the variety of small-molecule organic semiconductors is very large. They can also be functionalized to add or change certain properties. Pentacene, for example, can be made soluble by attaching bulky side groups [20, 35].
Polymers are the second class of organic semiconductors. Due to their high molecular weight, they can usually only be processed from solution. Further information about polymer semiconductors can be found in [36–38].

2.2 Charge transport in organic semiconductors

As discussed above, the ability for intramolecular charge transport is determined by the π molecular orbitals. Charge transport within the organic semiconductor material, however, requires transport from one molecule to the other, i.e., intermolecular charge transport.
The Drude model is a quite simple model describing charge transport of delocalized carriers, but it is useful to define several material parameters. In the Drude model, charge carriers are accelerated by an external electric field $\vec{E}$ to a drift velocity, whose mean value $\vec{v_D}$ is given by:

$$\vec{v_D} = \mu \cdot \vec{E}, \tag{2.1}$$

where μ is the charge-carrier mobility. μ is an important material parameter because it determines the electrical conductivity σ by:

$$\sigma = \mu \cdot n \cdot e \tag{2.2}$$

with the charge-carrier density n and the elementary charge e.
In conventional inorganic semiconductors, strong covalent bonds between the atoms lead to significant overlaps of the electronic orbitals, resulting in broad energy bands. For high crystallinity, charge transport in these materials is usually described by band transport, characterized by a dependence of the mobility on the temperature T of $\mu \propto T^{-b}$ with a real number $b > 0$. The decrease of μ with increasing temperature is due to phonon scattering. In organic semiconductors, such a behavior has been observed only for highly pure crystals, for example of naphthalene [39]. It is, however, questionable if this is a proof for band transport [40, 41].
An important characteristic of organic semiconductors are the weak van der Waals bonds between the molecules that result in a small intermolecular overlap of the electronic orbitals. Therefore, the electronic "bands" in an organic semiconductor are narrow (with a bandwidth of typically 0.1 eV), around two orders of magnitude smaller than in crystalline silicon [42]. The electronic properties (e.g. HOMO and LUMO position) are therefore quite similar to those of the individual organic molecules due to the small overlap of the orbitals. Since the efficiency of charge transport through an organic semiconductor depends also on the overlap of the π orbitals of neighboring molecules (the transfer integral), the weak van der Waals bonds are limiting the charge transport. Hence, even highly pure organic semiconductor crystals have lower carrier mobilities than their inorganic counterparts.
In most organic devices, the organic semiconductor materials are not in the form of single crystals, but are polycrystalline or even amorphous. Charge transport in organic semiconductor devices is therefore usually determined by localized states in the forbidden energy gap. These states can be created by energetic and positional disorder, which includes impurities, defects, grain boundaries and interface states. In addition, the small band width in organic semiconductors results in large residence times of the charge carriers on a molecule [43]. These long residence times allow the formation of polarons, i.e., a polarization of the π electron cloud of neighboring molecules caused by an additional charge carrier on a molecular site. The polarization changes the local potential and consequently also leads to localization [44].

2.2.1 Charge transport models

Currently, there is no model that comprehensively describes the charge transport in all organic semiconductors. The reason for this is not only the wide range of existing organic semiconductor molecules with different properties, but also the influence of numerous factors on the charge transport [45]. Some of these factors are properties of the semiconductor layer, such as molecular packing, impurities and disorder, and these properties are affected by the particular process conditions during fabrication. In addition, charge transport can be influenced by extrinsic factors like the temperature, the electric field strength, the charge-carrier density and the pressure. Hence, a multitude of models have been proposed, based on different physical mechanisms, assumptions and approximations. However, the charge transport mechanisms in organic semiconductors are still only poorly understood, which is even true for the relatively simple case of molecular crystals [46].
In the following, a small selection of charge-transport models based on disorder in organic semiconductors is briefly discussed.

Multiple trapping and release

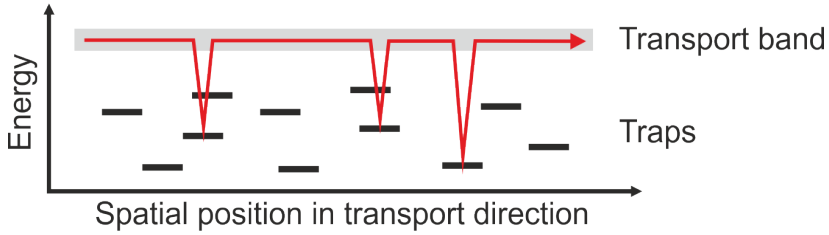


Figure 2.3: **Illustration of the transport mechanism in the multiple trapping and release model.** Charge carriers in a transport band enable the charge transport. Frequently, they are trapped in localized states, but they can be thermally released.

The multiple trapping and release (MTR) model combines the picture of delocalized band transport and the presence of localized states. It was originally developed to describe the charge transport in amorphous and polycrystalline silicon TFTs [47] and later expanded to organic semiconductors [48]. The model assumes extended, delocalized states in a narrow transport band and localized states with energies in the HOMO-LUMO gap. As illustrated in figure 2.3, charge transport is enabled by a fraction of charge carriers in the transport band. Upon trapping into localized states, the charge carriers do not contribute to charge transport anymore, but they can be released by a thermal activation process. The charge-carrier mobility in the MTR model can be described by [43, 49]:

$$\mu \propto \exp\left(\frac{-(E_C - E_t)}{k_B T}\right) n^{T_0/T-1}, \tag{2.3}$$

where E_C is the energy of the transport band edge, E_t is the energy of the trap level, k_B is the Boltzmann constant and T_0 is a characteristic temperature.

Variable range hopping

If the disorder is greater, more (or all) states are localized, and charge transport in a transport band is only possible under special conditions, or not at all. Instead, charges have to hop from one localized state to the next, as depicted in figure 2.4. For hopping due to static disorder, a phonon-assisted tunneling mechanism is usually assumed [50], leading to a dependence of the hopping rate W_{ij} on the hopping distance R_{ij} and, in case of a hop from a state with energy E_i to a state with higher energy E_j, the energy difference between the to states. This is described by the Miller-Abrahams expression [51, 52]:

$$W_{ij} = \nu_0 \exp\left(-\gamma |R_{ij}|\right) \begin{cases} \exp\left(-\frac{E_j - E_i}{k_B T}\right) & \forall E_j > E_i \\ 1 & \text{else} \end{cases}, \tag{2.4}$$

where ν_0 is the phonon vibration frequency and γ is the inverse localization radius [50]. In the concept of variable range hopping (VRH), hops are not only allowed to the nearest neighbor. Instead, hopping over a larger distance to states with similar or lower energy can be more favorable than hopping over a short distance with large energy difference, as evidenced by equation 2.4.

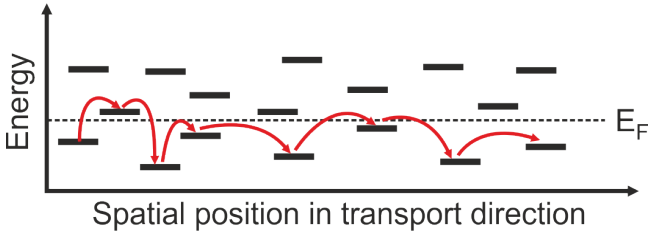


Figure 2.4: **Illustration of the transport mechanism in the variable range hopping model.** Charge carriers hop between localized states by a phonon-assisted tunneling mechanism.

VRH is a subclass of the hopping models and covers several specific models. One of the most intuitive approaches was proposed by Mott [53], where the hopping conductivity is calculated using a constant density of states (DOS). Maximized transition rates are obtained through a balance of tunneling and thermal activation. The resulting charge-carrier mobility is also known as Mott's law and has the temperature dependence [54]:

$$\mu \propto \exp\left(-\left(\frac{T_1}{T}\right)^{1/(1+D)}\right), \tag{2.5}$$

where T_1 is a characteristic temperature and D is the hopping space dimensionality. This result was later confirmed using percolation theory [55].
Following Mott's derivation, several other VRH models were developed, assuming for example different distributions of the density of states. A popular model developed for amorphous organic TFTs was proposed by Vissenberg and Matters [56] and is based on percolation theory in an exponential DOS. They obtained the following expression for the field-effect mobility:

$$\mu \propto \left(\frac{(T_2/T)^3}{C_1\,\Gamma(1-T/T_2)\,\Gamma(1+T/T_2)}\right)^{T_2/T} \cdot \left(C_2\,n^2\right)^{T_2/T-1}, \tag{2.6}$$

where C_1 and C_2 are constants and T_2 is another characteristic temperature. The mobility has an Arrhenius-like temperature dependence with a weakly (logarithmically) temperature-dependent activation energy.

Grain boundaries

Vapor-deposited thin films of small molecules are usually polycrystalline and several models specifically address the transport across the grain boundaries in such films. According to these models, the channel of an OTFT consists of grains having an average length of L_G and a mobility of μ_G in series with grain boundaries having an average length of L_{GB} and a mobility of μ_{GB}. The channel mobility μ is then given by [57]:

$$\frac{L_G + L_{GB}}{\mu} = \frac{L_G}{\mu_G} + \frac{L_{GB}}{\mu_{GB}}. \tag{2.7}$$

The charge transport within the grains is usually assumed to be band-like and accordingly the mobility is limited mainly by the grain boundaries. Different mechanisms for the charge transport across the grain boundaries were assumed, e.g. thermionic emission, tunneling or MTR [49, 57]. The temperature dependence of the mobility is determined by the responsible mechanism, but usually has the form $\mu \propto \exp\left(\frac{-E_A}{k_B T}\right)$, with an activation energy E_A.

Parameters influencing the charge-carrier mobility

As mentioned above, the charge-carrier mobility μ in organic semiconductors can be influenced by many factors, two of which will be briefly discussed below.

Charge-carrier density: Several important charge-transport models for organic semiconductors, including the MTR model and the VRH model by Vissenberg and Matters, predict an increase of the charge-carrier mobility as the charge-carrier density is increased (equations 2.3 and 2.6). This can be easily understood as follows: Concerning MTR, an increase of the charge-carrier density shifts the Fermi level towards the transport band. Accordingly, traps that are energetically closer to the transport band are involved where thermal release is more probable, leading to an increased mobility. Concerning VRH, an increase in the charge-carrier concentration leads to an increased mobility if the density of states increases with energy around the Fermi level, because the shift of the Fermi level towards higher energy then leads to a higher density of states available for hopping. In grain boundary models, the barrier height and width of the grain boundaries and therefore also the charge-carrier mobility and its activation energy depend on the charge-carrier density, with barrier heights and widths that decrease with increasing charge-carrier density [57].

Electric field: In large electric fields E in the direction of charge transport, μ can depend on E due to the Poole-Frenkel effect. Detrapping is enhanced by the electric field, and thus the charge-carrier mobility increases with E as [58]:

$$\mu \propto \exp\left(\beta\sqrt{E}\right) \tag{2.8}$$

with a temperature-dependent parameter β given by [59]:

$$\beta = \frac{1}{k_B T}\left(\frac{e^3}{\pi\varepsilon_S}\right)^{0.5}, \tag{2.9}$$

where ε_S is the permittivity of the semiconductor.

Space-charge-limited current

In insulators and semiconductors with a low density of free charge carriers and a low-resistance injecting electrode, the conduction is usually determined by a space-charge-limited current (SCLC). In the case of no traps, large electric fields, a field-independent charge-carrier mobility and considering only the drift current, the current density J is given by the Mott-Gurney law [59–61]:

$$J = \frac{9}{8}\varepsilon_S \mu \frac{V^2}{d^3}, \tag{2.10}$$

where d is the thickness of the material and V is the applied voltage. The current increases nonlinearly with V, because the conduction is mainly determined by charge carriers injected due to the application of V, meaning that both the drift velocity and the charge-

carrier concentration depend on the applied voltage. Below a certain crossover voltage that is determined by the concentration of free charge-carriers already present prior to applying a voltage, the current is ohmic [61].
Trap states in the material affect the current-voltage characteristics depending on the energetic trap distribution. In the case of shallow traps, i.e., traps within an energy of about k_BT below the transport level, the square-law dependence of the current on the voltage is preserved, and equation 2.10 is just multiplied with the fraction of free and trapped charge. Deeper trap states modify the shape of the I-V characteristics. In the case of an exponential distribution of trap states, the dependence of current on voltage changes to [60]:

$$J \propto V^{T_C/T+1}, \tag{2.11}$$

where T_C is a characteristic temperature determining the steepness of the trap distribution.

2.3 Organic thin-film transistors

Organic transistors are usually realized in the TFT configuration. A TFT is a FET that is made of several layers - the active part (a thin organic semiconducting film), two electrodes for the injection and extraction of charge carriers (source and drain (S/D) terminals) and the gate electrode, which is electrically isolated from the semiconductor by a gate dielectric.
A typical device with a channel length L is shown in figure 2.5, illustrating n-channel operation. Upon application of a gate-source voltage (V_{GS}), charge carriers are accumulated in the semiconductor and a conducting channel is formed at the gate dielectric/organic semiconductor interface. This is different from MOSFETs, where the conducting channel is formed by an inversion channel and not by an accumulation layer. If the channel is formed, an applied drain-source voltage (V_{DS}) will drive a drain current (I_D). In contrast, the application of V_{DS} will result in (ideally) no current flowing through the device if the conductive channel is not created by the gate field. Thus, the transistor operates as a switch which is controlled by the voltage V_{GS}. The gate leakage current (I_G) is an undesirable leakage current through the dielectric that needs to be minimized by proper materials selection and processing.

2.3.1 Current-voltage characteristics

The following discussion considers n-channel operation; for p-channel transistors, the polarities have to be reversed. Following the Drude model, the drain current I_D of the

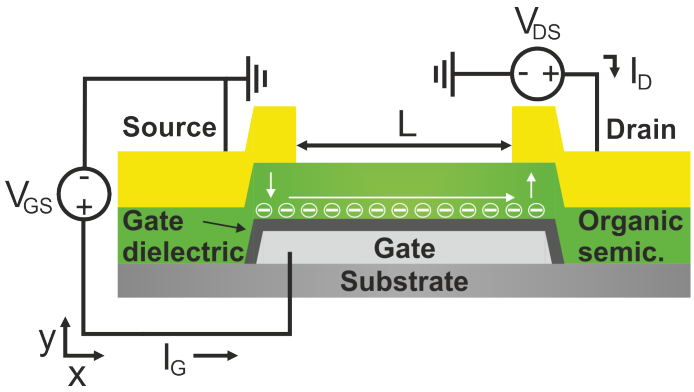


Figure 2.5: **Working principle of an n-channel organic thin-film transistor.** The transistor consists of three terminals (source, drain and gate), an active layer (the organic semiconductor) and a gate dielectric that isolates gate and semiconductor. Upon application of a gate-source voltage of sufficient magnitude, charge carriers (in this case electrons) are accumulated in the semiconductor region close to the dielectric interface, the channel. A drain-source voltage can then drive the flow of charge-carriers from source to drain.

transistor can be calculated using equation 2.2. It is, however, quite complex to exactly derive the charge-carrier density for the metal-insulator-semiconductor (MIS) structure that is formed by the gate, the gate dielectric and the organic semiconductor.
The conducting channel is only a few monolayers thick [62, 63]. It is therefore reasonable to simplify the problem and assume a thickness of zero, so that the MIS structure is similar to a parallel-plate capacitor. This simplification is named charge-sheet model [64], and it allows a simpler derivation of the transistor's current-voltage characteristics [65]. A more detailed and complex consideration can be found in [66, 67].
We start by considering the resistance $\mathrm{d}R$ over a short distance $\mathrm{d}x$ in the channel:

$$\mathrm{d}R = \frac{\mathrm{d}x}{W\mu\, Q[x]}, \tag{2.12}$$

where W is the channel width and $Q[x]$ is the surface charge density at the lateral position in the channel x. In a plate capacitor, the charge is given by the product of capacitance and voltage. In a TFT, the voltage between gate and channel depends on x (being V_{GS} at the source side and $V_{GS} - V_{DS}$ at the drain side) and can be expressed as $V_{GS} - V[x]$, where $V[x]$ is the potential in the channel at position x. In addition, a work function difference, donor or acceptor states and charge trapping have to be accounted for, which is done by introducing the threshold voltage V_{th} [65]. Hence, $Q[x]$ can be expressed by:

$$Q[x] = C_i(V_{GS} - V_{th} - V[x]) \tag{2.13}$$

with the gate dielectric capacitance per unit area C_i. Combining equations 2.12 and 2.13

and substituting $\mathrm{d}V = I_D\,\mathrm{d}R$ results in

$$I_D \int_0^L \mathrm{d}x = \mu C_i W \int_0^{V_{DS}} \mathrm{d}V (V_{GS} - V_{th} - V[x]). \tag{2.14}$$

Integration leads to:

$$I_{D,lin} = \mu C_i \frac{W}{L} \left(V_{GS} - V_{th} - \frac{V_{DS}}{2} \right) V_{DS}. \tag{2.15}$$

Two additional assumptions were necessary for the derivation of the drain current. The first is the gradual channel approximation, in which the variation of the electrical field along the channel (x-direction) is assumed to be much smaller than the variation in the y-direction (perpendicular to the channel), which is necessary in order to decouple the two-dimensional problem into two one-dimensional problems. The second assumption is that μ is independent of V_{DS}.

Linear and saturation regions

Equation 2.15 predicts the following cases: For $V_{GS} - V_{th} << V_{DS}$, the conducting channel is nearly uniform and can be modeled as a resistor; the drain current increases almost linearly with V_{DS} for constant V_{GS}. This is the so-called linear region (or linear regime). For higher V_{DS}, the slope $\frac{\partial I_D}{\partial V_{DS}}$ gradually decreases due to a smaller number of accumulated charges on the drain side, until I_D reaches a maximum at $V_{GS} - V_{th} = V_{DS}$. At this bias condition, (almost) no charges are accumulated at the drain, which is called pinch-off. For a further increase of V_{DS}, this pinch-off point will move towards the source side. Equation 2.15 is not valid in this region anymore, because there is no accumulation layer at the drain side. To account for this situation, $V_{DS} = V_{GS} - V_{th}$ is inserted in equation 2.15:

$$I_{D,sat} = \mu C_i \frac{W}{2L} \left(V_{GS} - V_{th} \right)^2. \tag{2.16}$$

In this case, the drain current does not depend on V_{DS}, which is called the saturation region. Figure 2.6 illustrates the electrical characteristics of a transistor. The transfer curve (figure 2.6a) plots the drain current as a function of the gate-source voltage for a constant drain-source voltage. In addition to the linear and saturation regions, there are two more operation regimes, namely the off-state region and the subthreshold region. Note the logarithmic scale that is employed for better visibility of all regions. The output curves (figure 2.6) plot the drain current as a function of the drain-source voltage for a set of gate-source voltages.
Using equations 2.15 and 2.16, the charge-carrier mobility and the threshold voltage of a transistor can be obtained from both the linear and the saturation regimes by fitting the

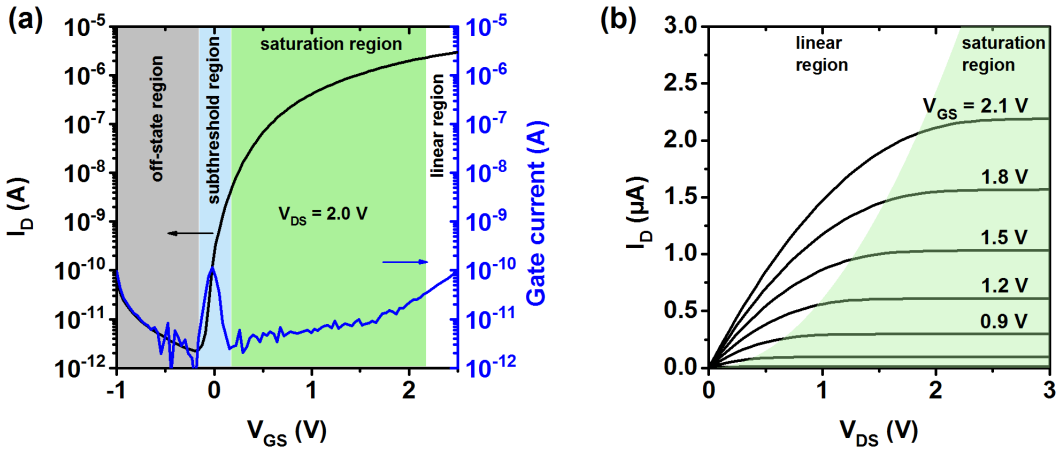


Figure 2.6: **Current-voltage characteristics of an n-channel organic transistor showing the different operation regions.** (a) Transfer curve (I_D as a function of V_{GS} for a constant V_{DS}) on a logarithmic scale. Four operation regions are marked. The gate current is also shown (blue). (b) Output curves (I_D as a function of V_{DS} for a set of constant V_{GS} values). For $V_{DS} > V_{GS} - V_{th}$ the drain current saturates.

experimental curves. Examples are shown in figure 2.7.
Ideally, $I_D[V_{GS}]$ curves and $\sqrt{I_D[V_{GS}]}$ curves are straight lines in the linear and saturation regime, respectively. However, in reality the slope of these curves is often not constant. In this case, it can be more useful to obtain the charge-carrier mobility pointwise. Derivation of equation 2.15 results in the differential mobility:

$$\mu_{lin}[V_{GS}] = \frac{L}{WC_iV_{DS}} \frac{\partial I_D}{\partial V_{GS}}, \tag{2.17}$$

which is valid in the linear regime. Similarly, the expression for the differential mobility in the saturation regime can be obtained from equation 2.16:

$$\mu_{sat}[V_{GS}] = \frac{2L}{WC_i} \left(\frac{\partial \sqrt{I_D}}{\partial V_{GS}} \right)^2. \tag{2.18}$$

Another important parameter is the transconductance g_m, defined as $g_m = \frac{\partial I_D}{\partial V_{GS}}$. In the linear regime, the transconductance is the slope of the transfer curve.
An alternate way to determine the threshold voltage in the linear region is the so-called second derivative method [68, 69]. In this method, the threshold voltage is estimated as the gate-source voltage at which the second derivative of the (linear) transfer curve has its maximum, an example is shown in the inset of figure 2.7a.

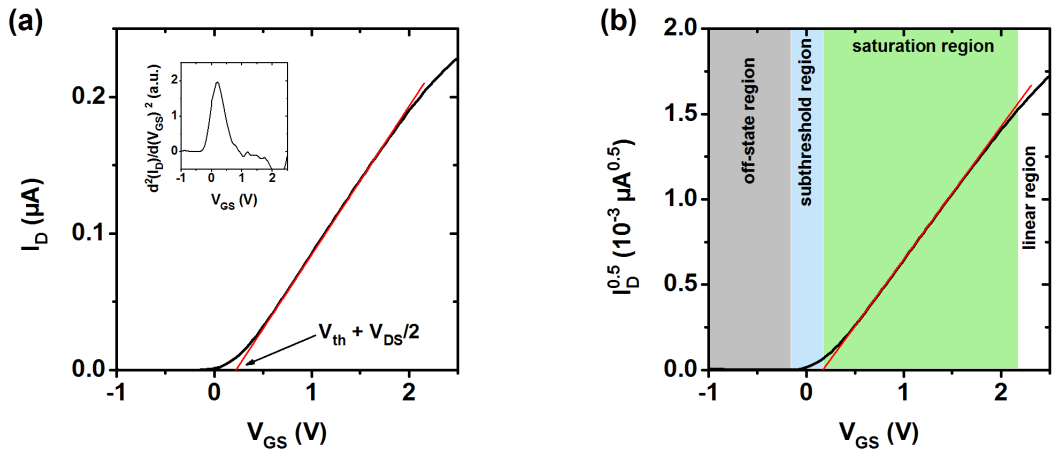


Figure 2.7: **Extraction of transistor parameters from transfer curves.** (a) In the linear regime, the experimental transfer curve is linearly fitted with equation 2.15 to obtain the mobility from the slope and the threshold voltage from the x-axis intercept. Inset: Second derivative of the drain current with respect to V_{GS} for the threshold voltage extraction with the second derivative method. (b) In the saturation regime, mobility and threshold voltage can be extracted using a quadratic fit (equation 2.16).

Off-state region

Equations 2.15 and 2.16 are only valid if a charge sheet layer is formed, i.e., if $V_{GS} > V_{th}$. For $V_{GS} << V_{th}$, the transistor is in the off state. The current in this region is determined by the band gap and doping and should be as small as possible to reduce power consumption.

Subthreshold region

At gate-source voltages slightly below threshold, the free charge-carrier concentration is small and the current is dominated by diffusion. In this region, the current increases exponentially with V_{GS}, and the subthreshold swing S is a measure for how swift the drain current changes with V_{GS}. S can be extracted from the inverse slope of a logarithmic transfer curve and is determined by [67]:

$$S \equiv \ln(10)\frac{\mathrm{d}V_{GS}}{\mathrm{d}(\ln(I_D))} = \ln(10)\left(\frac{kT}{e}\right)\left(\frac{C_i + C_{semi} + C_{traps}}{C_i}\right), \tag{2.19}$$

where C_{semi} is the depletion layer capacitance of the semiconductor (can usually be ignored in TFTs) and C_{traps} is the capacitance associated with traps at the dielectric-semiconductor interface. At room temperature, the (trap-free) minimum of S is 60 mV/decade.

2.3.2 Metal-organic semiconductor interfaces

The interface between the metallic source/drain contacts and the organic semiconductor is of particular importance in an OTFT because this is where the charge transfer into and out of the active material takes place. The energy level diagram before and after contact of an ideal metal-semiconductor interface is shown in figure 2.8. In general, if two materials are brought into contact, thermal equilibrium is obtained by the alignment of their Fermi energies E_F. This means that a difference of the work functions of the metal (Φ_m) and the semiconductor (Φ_s) will result in a charge flow between the two materials, creating a space-charge region of width W_{SC} and level bending. The work function is defined as the difference between the vacuum level E_{vac} and the respective Fermi energy, as can be seen in figure 2.8a. In this picture, an energy barrier for the electron transfer of height Φ_b is formed as [67]:

$$\Phi_b = \Phi_m - \chi, \tag{2.20}$$

where χ is the electron affinity of the semiconductor. A similar barrier for holes can be calculated using the ionization potential.

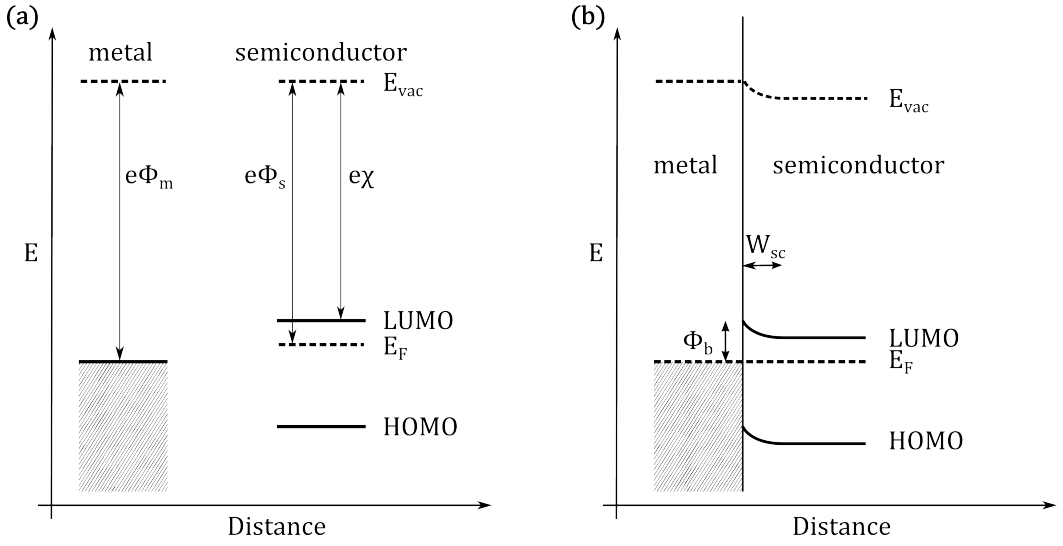


Figure 2.8: **Energy level diagrams of an ideal metal/semiconductor (n-type) contact.** (a) Energy levels of the isolated elements. (b) Band diagram of the connected system.

In practice, this simple picture usually fails. Even for relatively ideal systems using inorganic semiconductors, the presence of interface states and interface layers as well as image-force lowering lead to significant deviations of the experimental barrier height when compared with the result of equation 2.20. For metal/organic semiconductor junctions, no

unified model exists so far and the literature is somewhat controversial. In addition, the interface properties can depend strongly on the specific materials and processes involved. Overviews of several supposedly important effects can be found in [70–73], some of which will be briefly discussed below.

The first problem occurring when considering a metal/organic semiconductor interface is determining the type of interaction between the two materials, which can range from physisorption to chemisorption. While in the case of physisorption the electronic structure is mostly unperturbed by the adsorption process, a chemical reaction takes place during chemisorption.

Regarding physisorption, several effects have to be accounted for. First, the metal work functions taken from the literature are often not suitable for the calculation of the energy barrier. One reason is the push-back (or pillow) effect that modifies the metal surface dipole by pushing the electron cloud closer to the metal surface, resulting in a decrease of the effective metal work function by up to several tenth of eV. Secondly, it has to be considered that the energy of the transport gap within the first nanometers of the interface is reduced by screening due to image charges on the metal surface and that the LUMO level has a certain width. Finally, integer charge transfer is expected for physisorption, which can result in Fermi level pinning where the work function of the interface is independent of the metal work function. All these phenomena affect the height of the real energy barrier.

In the case of weak chemisorption, the molecular orbitals are hybridized due to the presence of the metal, leading to a shift and broadening of the energy levels. As a result, a continuum of states is induced in the energy gap, which is filled up to the so-called charge neutrality level (CNL). The CNL is assumed to depend mostly on the specific semiconductor and not much on the metal.

In summary, the information about the isolated work functions and HOMO/LUMO energies is only of little use for determining the energy level alignment at the metal/organic semiconductor contact. The work function of the metal can be altered by charge transfer, the push-back effect and metal-induced gap states. In the literature, this is often summarized in a so-called interface dipole Δ that shifts the vacuum level of the interface, as shown in figure 2.9. As an example, the work function of gold is often cited as 5.1 eV [74], but measurements on gold surfaces which were exposed to air yield work functions around 4.5 eV, thus significantly decreasing the energy barrier for electrons [71].

As for the HOMO and LUMO levels, a transport gap narrowing due to the image charge has to be considered at the interface. Additionally, HOMO and LUMO levels are often measured using cyclic voltammetry in solution, and values of the thin film may differ.

A further influence on the interface can be the order of deposition, i.e., organic-on-metal versus metal-on-organic. Although there are substantially fewer investigations of the latter case due to the technical difficulties of accessing that interface, there are some

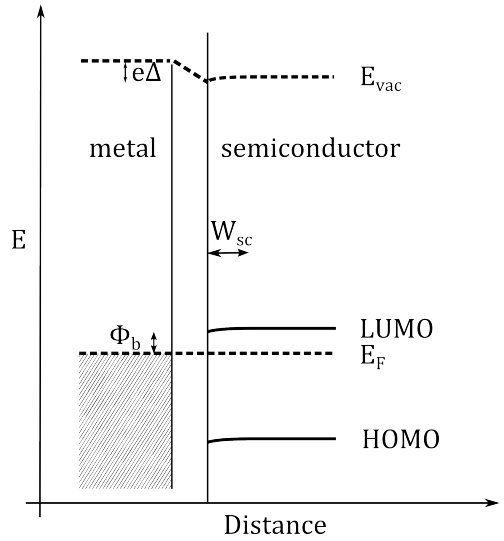


Figure 2.9: **Energy level diagram of a metal/semiconductor (n-type) contact with an interface dipole.** The interface dipole shifts the work function of the metal and changes the energy barrier.

indications that the hot metal atoms can diffuse into the semiconductor [73]. Interestingly, the effective work function of the metal-on-organic interface seems to be similar to the "contaminated" case (4.5 eV in the case of gold, see above), even though the metal was deposited in ultra-high vacuum (UHV) [71].
Finally, it has been neglected so far that the source/drain contact - organic semiconductor interface is not an isolated system in a TFT. Instead, the bias conditions (V_{GS} and V_{DS}) can have a profound influence on the height and shape of the energy barrier [66, 75–79].

Current transport mechanisms across the interface

Three main mechanisms are usually considered in the context of charge-carrier injection across a metal-organic interface: thermionic emission, tunneling and defect-assisted injection [80]. A simplified comparison is shown in figure 2.10. Combinations of these mechanisms, for example thermionic field emission, are also possible.
In the thermionic emission theory, carriers can be transported by thermal excitation across the barrier. Hence, the current across the interface I_{TE} depends on the barrier height and the temperature:

$$I_{TE} \propto T^2 \exp(-e\Phi_b/k_B T). \tag{2.21}$$

In the forward direction (and due to the Schottky effect in the reverse direction as well [72]), the current will depend on the voltage applied across the interface.
If the barrier width is small, tunneling trough the potential barrier can become possible. The tunneling current depends exponentially on the barrier height and width, but not on

the temperature. Carriers can also overcome the barrier by thermally activated hopping transport using interface or trap states in the energy gap.

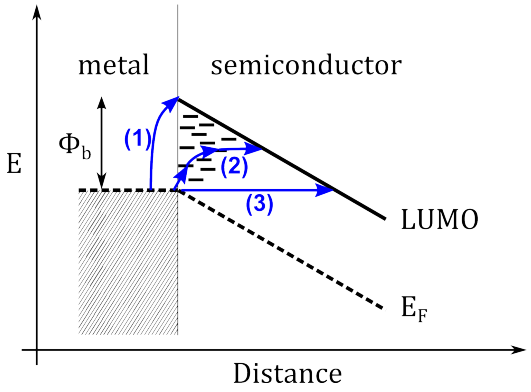


Figure 2.10: **Transport mechanisms across a biased metal-semiconductor contact.** The simplified schematic illustrates (1) thermionic emission, (2) trap-assisted injection and (3) tunneling. Level bending is neglected.

2.3.3 n-channel OTFTs

The majority of modern integrated circuits are based on the complementary metal-oxide semiconductor (CMOS) technology, i.e., pairs of n-channel and p-channel transistors are used for logic operations. Except during switching, one of the transistors in the pair is always off, thus significantly reducing power consumption [81]. Another advantage is the higher noise immunity of the complementary technology.

In MOSFETs, n-channel and p-channel operation are realized by selective doping of the same active material. For organic semiconductors, some recent reports demonstrate that doping is in principle also possible in these materials [82–85]. However, the doping mechanisms in organic semiconductors are somewhat different from those in inorganic materials [85, 86], and their understanding is still in its infancy. One of the main problems is that the doping efficiency depends strongly on the specific pair of organic semiconductor and dopant. The doping concentrations necessary in organic materials are also significantly higher, above 1 %, compared to less than 0.01 % in silicon [87].

Consequently, most OTFTs use semiconductors with no intentional doping. In this case, organic transistors usually show p-channel operation, while n-channel operation is less common in OTFTs and mostly with lower performance or only very limited ambient stability [31]. This phenomenon has several reasons. In addition to the observation that the LUMO bandwidth is typically smaller than the HOMO bandwidth [88], an important factor that influences the type of operation is the energy level alignment at the metal-organic semiconductor interface. This alignment can provide quite asymmetric charge

transfer properties for electrons and holes, thereby strongly favoring one type of operation. In a simple picture, this would mean that a semiconductor with a high electron affinity in contact with a low-work-function metal favors electron injection, while a semiconductor with a small ionization potential in contact with a high-work-function metal benefits hole injection. Using low-work-function metals as contact materials to obtain n-channel OTFT operation is problematic, because such metals suffer from oxidation and can chemically react with the organic semiconductors [89]. On the other hand, lower LUMO energies have been achieved by functionalization of the organic molecules' conjugated core with strong electron-withdrawing groups such as -F, -Cl, -Br, and -CN [32, 90, 91]. However, as discussed in section 2.3.2, it should be kept in mind that the energy level alignment is difficult to predict and that the nominal energy levels usually do not give the expected results.

Another important aspect for organic n-channel transistor operation is electron trapping, which seems to be of greater importance than hole trapping in most organic materials. Major sources for electron traps in OTFTs are the dielectric/organic semiconductor interface [31, 66] as well as components of the ambient atmosphere such as H_2O, O_2 [32, 91, 92] and hydrated oxygen complexes [93]. Concerning the first, the dielectric surface has to be of good quality, which can be achieved by appropriate surface treatments [66, 89]. Concerning the electron traps created by ambient gases, two methods are usually employed to improve the performance of the transistors in air. The first is to prevent the gases from reaching the transistor channel, either by encapsulation of the entire device [94–96] or by using organic molecules that create densely packed films which provide a kinetic barrier for the ambient gases [91]. The second and most important approach to improve the ambient stability and performance of OTFTs is to use molecules with a low LUMO energy to stabilize the charge carriers with respect to the oxidation reactions [89, 92]. Usually, a LUMO energy of -4.0 eV or lower is believed to provide a certain level of ambient stability.

2.3.4 The organic semiconductor PDI-FCN_2

The organic semiconductor employed in this work is N,N'-bis-(1H,1H-heptafluorobutyl)-1,7-dicyano-perylene-3,4:9,10-tetracarboxylic diimide (PDI-FCN_2), commercialized by Polyera as ActivInk^{TM} N1100, which was introduced by Jones et al. in 2004 [90, 91]. As shown in figure 2.11a, the molecule is based on an aromatic perylene core. Several modifications using strong electron-withdrawing groups lead to an increase in the electron affinity to promote stable and efficient n-channel OTFT operation (see section 2.3.3). The major contribution to the lowering of the LUMO level comes from the addition of the two imide moieties [97] and the functionalization of the core with two cyano groups. The fluoroalkyl substitutions at the imide positions further lower the LUMO energy slightly

to a final value of around -4.5 eV [91], but their main advantages are the introduction of solubility, allowing solution processing, and the promotion of close packing through fluorocarbon self-segregation [90]. In addition, they create a kinetic barrier for molecules from the ambient atmosphere, thereby increasing air stability [91]. The optical HOMO-LUMO gap of PDI-FCN_2 is 2.3 eV [91], thus allowing low off-state currents in transistors made of this material.

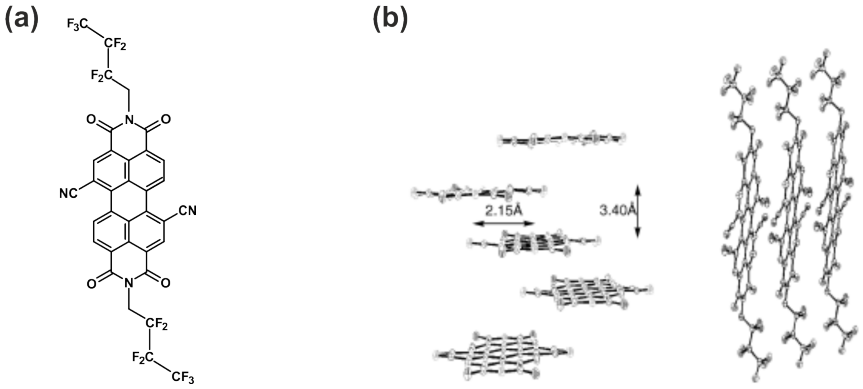


Figure 2.11: **Structure of PDI-FCN_2.** (a) Molecular structure of the 1,7 isomer. (b) Crystal structure, viewed along the unit cell diagonal (left) and viewed along the *ab* face diagonal (right). Image adapted from [90].

Two isomers (cyanated at the 1,7 or 1,6 positions) of PDI-FCN_2 exist, although this supposedly has no influence on the electronic structure and the charge-transport properties [90]. The crystal structure of PDI-FCN_2, obtained from single crystals using x-ray diffraction (XRD), shows a slightly twisted polycyclic core having a torsion angle of about 5° with slip-stacked face-to-face molecular packing and a minimum interplanar spacing of 3.4 Å (figure 2.11b) [90]. This tight packing allows a large overlap of the π orbitals of neighboring molecules, promoting efficient charge transport. The molecular long-axis length is 22.8 Å [90]. Cell parameters of the triclinic Bravais lattice can be found in [90, 98]. Various material properties of PDI-FCN_2 are summarized in table 2.1.
PDI-FCN_2 OTFTs have been fabricated using vacuum deposition [90, 91, 99–102] and solution processing [103, 104], yielding high electron mobilities measured in air of up to 2.7 cm^2/Vs and 1.3 cm^2/Vs, respectively. In addition, several reports on single crystal FETs based on PDI-FCN_2 [105–109] showed electron mobilities of up to 6 cm^2/Vs in vacuum and 3 cm^2/Vs in air [106] at room temperature and up to 11 cm^2/Vs at cryogenic temperatures [105].

HOMO	LUMO	Max. optical absorption	Crystallization motif
-6.8 eV [91]	-4.5 eV [91]	523 nm [91]	Slipped-stacked face-to-face [90]

Table 2.1: **Material data for PDI-FCN$_2$.**

2.4 Contact resistance

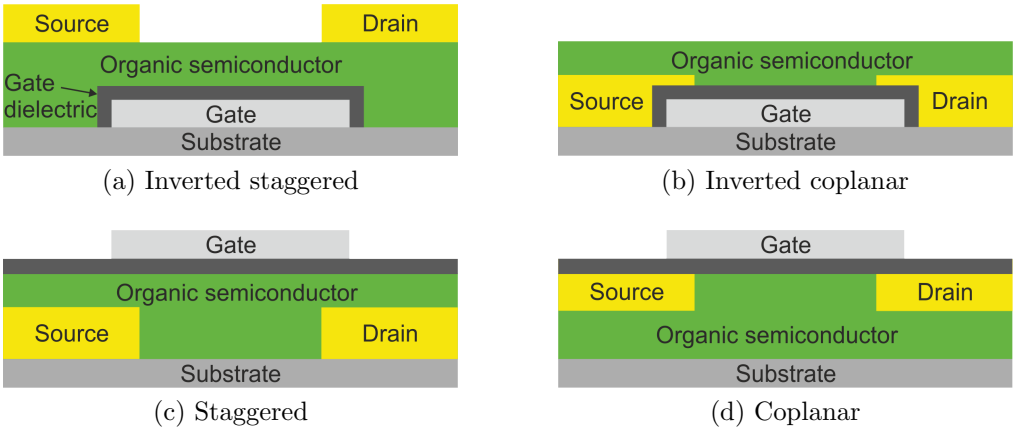
In an ideal transistor, the current through the device is determined solely by the channel, having no conductivity in the off state and maximum conductivity in the on state. However, in a real device, parasitic contact resistances exist at and/or close to the S/D contacts, limiting the current-driving capabilities of the transistor. In addition, these resistances can introduce nonidealities in the current-voltage characteristics.
The contact resistance R_C is composed of the contributions at the source (R_S) and drain (R_D) side. The total resistance of the transistor $R_{tot} = V_{DS}/I_D$ is given by the sum of the channel resistance (R_{ch}) and the contact resistance:

$$R_{tot} = R_{ch} + R_C = R_{sheet}\frac{L}{W} + R_S + R_D, \tag{2.22}$$

where $R_{sheet} = R_{ch}\frac{W}{L}$ is the sheet resistance. Contact resistance values are often given in the width-normalized form $R_C\,W$ in order to simplify comparisons of contact resistances obtained from transistors with different geometries. Equation 2.22 shows that the contribution of the contact resistance to the total transistor resistance is expected to be more and more pronounced as the channel length is reduced. However, small channel lengths are necessary to increase the operation frequency of transistors [31], and these parasitic resistances can then become dominant and significantly limit the device performance.
The presence of contact resistances invalidates the equations 2.15 and 2.16 for the ideal transistor. A workaround is to adapt these equations and to include the contact effects by replacing μ with the effective mobility μ_{eff} (also called apparent mobility). The true, ideal channel mobility is then referred to as intrinsic mobility μ_0. In the literature, the parameter "field-effect mobility" often refers to the effective mobility, because a contact analysis is rarely performed. However, the effective mobility can deviate quite substantially from the intrinsic field-effect mobility of the material. Although the physical meaning of the effective mobility is questionable, it can be useful for modeling, since it describes the slope of a measured transfer curve.
The origins of the contact resistance can be manifold. An intuitive explanation is a contribution from an energy barrier at the S/D contact interfaces. However, this is not always the only or even the most important factor. Since the underlying mechanisms also depend on the configuration of the TFT, the common device architectures are discussed in the following section.

2.4.1 Device architecture

The device architectures available for organic thin-film transistors are in principle the same as those for other TFT technologies and are illustrated in figure 2.12 [66]. While the top-gate top-contact (coplanar) structure is uncommon, the other three geometries are all employed and have their specific advantages and disadvantages.



(a) Inverted staggered (b) Inverted coplanar

(c) Staggered (d) Coplanar

Figure 2.12: **Schematics of the thin-film transistor configurations.** (a) Bottom-gate top-contact (inverted staggered). (b) Bottom-gate bottom-contact (inverted coplanar). (c) Top-gate bottom-contact (staggered). (d) Top-gate top-contact (coplanar).

Organic materials are usually quite sensitive and potentially damaged by the chemicals of conventional lithography. Therefore, with few complex exceptions [110], this technique is usually only employed in bottom-contact structures where the advantage of being able to define small feature sizes is used prior to depositing the organic layer. However, deposition of an organic semiconductor on a metal often results in disordered and low-mobility regions close to the contacts [111]. Surface treatments of the metallic contacts proved to be potentially helpful in this context [112]. Deposition of the S/D contacts after the semiconductor is possible using vacuum sublimation or printing methods.

The relative position of the gate is important for the quality of the dielectric/semiconductor interface, which is of particular importance because it is the interface located next to the conducting channel. Organic semiconductors often grow as islands, and the resulting rough interface to the dielectric in top-gate structures can be disadvantageous for the charge transport properties. In addition, the choices for the dielectric are limited in the case of a top gate, and some high-quality dielectrics cannot be employed in this configuration.

Concerning the contact resistance, the main difference is whether the gate and the S/D contacts are on opposite sides of the semiconductor (staggered) or on the same side (copla-

nar). While the staggered structure has an additional contribution to the contact resistance arising from the need to transport the charges from the S/D contacts through the bulk semiconductor to the channel, coplanar structures suffer from the fact that the area available for charge injection and extraction is much smaller (defined by the height of the S/D contacts; usually several tens of nanometers) [72]. Several studies indicate that the staggered configuration yields superior contacts compared to the coplanar case [80, 111]. In this work, the bottom-gate top-contact (inverted staggered) structure is employed, combining the advantages of the lower contact resistance of the staggered configuration and the smooth dielectric interface. It also allows the use of self-assembled monolayers (SAMs) to create a high-quality dielectric. Since top contacts allow no traditional lithography, patterning is done using shadow masks (see section 3.1).

2.4.2 Current crowding model

In staggered OTFTs, the charge carriers are injected at the source contact, travel through the bulk of the organic semiconductor and are then transported in the accumulation layer at the dielectric interface before they leave through the drain contact. These aspects can be combined into a complex resistor network, described in the framework of the current crowding model [113–115] that was originally invented to describe a-Si:H TFTs [116]. As shown in figure 2.13a, the contribution from the S/D metal/organic semiconductor interface (ρ_{int}) and from the transport through the bulk semiconductor (ρ_{bulk}) can be summarized in the vertical part of the contact resistance, i.e., the contact resistivity $\rho_C = \rho_{int} + \rho_{bulk}$. If ρ_C is different at the source and the drain side, it is distinguished as ρ_S and ρ_D, respectively. The contact resistivities have the dimension resistance $\times$ area and are usually given in the unit $[\Omega\, cm^2]$.
Since the charge-carrier density is much higher at the dielectric interface, charge flow in the horizontal plane is only considered in the accumulation layer. This layer is characterized by the sheet resistance R_{sheet} and extends also under the source and drain contacts where they overlap with the gate electrode. The geometrical extension of this overlap is characterized by the contact length L_C, which may again be different at source and drain (see figure 2.13a).
A direct consequence of this resistor network is that the current injection and extraction is not restricted to the edge of the source or drain contact. Instead, in principle the whole contact area can take part in the charge transfer, but this will not be uniform: the current density has its maximum close to the contact edge and drops further away from it (figure 2.13b). This behavior is controlled by the balance of the vertical components (ρ_C) and horizontal components (R_{sheet}): the larger ρ_C is compared to R_{sheet}, the larger the part of the contact will be that is involved in charge injection and extraction. This

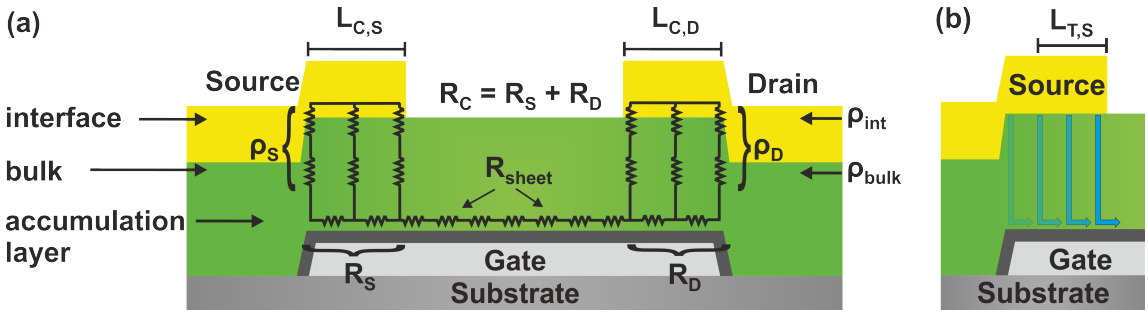


Figure 2.13: **Schematic of an OTFT illustrating the current crowding model.** (a) Components of the contact resistances and resistor network. (b) Nonuniform current flow, illustrated on the source side.

self-regulating effect can partly compensate for poor contacts, so that large energy barriers are less severe in the staggered configuration than in the coplanar case [72, 117].
By dividing the resistor network into infinitesimal pieces, analytical expressions for the source and drain resistances can be derived [113, 118]:

$$R_S = \frac{1}{W} R_{sheet} L_{T,S} \coth\left(\frac{L_{C,S}}{L_{T,S}}\right), \tag{2.23}$$

$$R_D = \frac{1}{W} R_{sheet} L_{T,D} \coth\left(\frac{L_{C,D}}{L_{T,D}}\right), \tag{2.24}$$

where L_T is the transfer length and the additional indices denote its value on the source ($L_{T,S}$) or drain ($L_{T,D}$) side. The transfer length is a characteristic length that describes the extension of the effective area of the contact that participates in charge transfer (figure 2.13b). For physically long contacts ($L_C >> L_T$), around 63 % of the current flow is within a distance L_T from the contact edge. As discussed above, the contact area involved in charge transfer is controlled by the balance of the vertical and horizontal components of the contact resistance. This is also obvious in the expressions for the transfer lengths [116]:

$$L_{T,S} = \sqrt{\frac{\rho_S}{R_{sheet}}} \qquad \text{and} \qquad L_{T,D} = \sqrt{\frac{\rho_D}{R_{sheet}}}. \tag{2.25}$$

In the equations 2.23 and 2.24, two limiting cases are possible: If the contact length is much larger than the transfer length ($L_C >> L_T$), the exact value of L_C is not important anymore. This is the case already discussed above: the effective area of the contact used for charge transfer is determined by the transfer length, multiplied by the width of the contacts. In this case, equation 2.23 simplifies to:

$$R_S \approx \frac{1}{W} R_{sheet} L_{T,S} = \frac{1}{W} \sqrt{R_{sheet}\, \rho_S}. \tag{2.26}$$

A similar expression is of course true for the drain resistance. On the other hand, if the contact length is much smaller than the transfer length ($L_C << L_T$), the extension of the effective contact area is limited by its physical size. Accordingly, the contact resistance will increase if L_C is decreased. In this scenario, equation 2.23 can be approximated by:

$$R_S \approx \frac{1}{W} R_{sheet} \frac{L_{T,S}^2}{L_{C,S}} = \frac{\rho_S}{W L_{C,S}}. \tag{2.27}$$

2.4.3 Definitions of the terms "resistance" and "ohmic"

Since there is some inconsistency in the literature, it is important to discuss the definitions of some terms here. Most importantly, the term "resistance" is not exclusively used for contact resistances following Ohm's law in this work, although the symbol of a classical resistor will be frequently used for illustrations. Instead, in this work a "resistance" is always defined by the quotient of voltage drop and current *at a specific bias condition*. Contact resistances following Ohm's law, i.e., contact resistances that do not depend on the voltage drop across the contact, will be referred to as "ohmic". Contrariwise, the terms "ohmic" resistance or "ohmic" contact will *not* be used here to imply that the contact resistance is small compared to the channel resistance [80].

2.4.4 Methods for the contact-resistance extraction

Due to the significance of the contact resistances for the transistor operation, several methods have been developed to assess them from electrical measurements. Most of these methods can be divided into four categories, namely modeling of the electrical characteristics, transmission line methods, Kelvin probe force microscopy and gated four-probe measurements. All these techniques have advantages and drawbacks, some of which will be discussed in the following sections. More comprehensive overviews can be found in [72, 80].

Modeling of the electrical characteristics

Modeling relies on the extraction of parameters from a single transfer or output curve or a combination of both. The obvious advantage of these methods is the simplicity of the measurement; conventional current-voltage data from just one device are necessary.
The first step is to find an appropriate mathematical description for the electrical characteristics. Concerning contact resistances, the simplest idea would be to take equation 2.15 for the linear transfer curve and to add a term for a constant parasitic resistance in series with the channel resistance [119]. A straightforward approach would then be to directly fit the experimental data with the model equation to obtain the model parameters, but a

meaningful and well-defined fit is usually not achievable due to the number of unknowns. Therefore, the extraction of parameters is often done stepwise with the help of auxiliary functions that use specific functional dependencies of parameters on V_{GS} or V_{DS}. Prominent examples of these auxiliary functions are the Y-function [120, 121], the differential method [122] and the H-function [123], which employ derivatives and integrals of transfer curves with respect to V_{GS}.
After the model parameters are obtained, they can be used to reproduce the experimental curve, which is potentially useful for circuit simulation [124, 125].
Despite the tempting possibility of obtaining additional information with just the normal electrical characteristics of the transistor, parameter extraction with these methods has several drawbacks. On the one hand, complex formulations and mechanisms are often necessary in order to accurately describe an experimental curve. Given the still limited understanding of the mechanisms in organic transistors, it can be questionable if the chosen physical model really applies. Sometimes, unphysical models are intentionally used to account for specific features in the experimental curve. As an example, a nonlinearity in output curves is sometimes modeled using pairs of anti-parallel diodes at the contacts [63, 126], which is not in accordance with the physics of Schottky barriers at source and drain.
On the other hand, parameter extraction using complex equations is difficult given the limited amount of data. Assumptions and simplifications are necessary to treat this problem. Concerning the modeling of contact resistances, common assumptions and simplifications include:

- The contact resistances are constant (and do not depend on the gate-source voltage).
- The drain resistance is negligible.
- In the saturation regime, the contact resistance is insignificant.
- The contact resistance is ohmic.

All these points are problematic and unlikely true in all transistors. Especially the first point, which is a necessary assumption for the use of the auxiliary functions described above, is usually not fulfilled, particularly in the staggered structure [63, 115]. However, without additional independent measurements, it can be difficult to predict if the model assumptions are met.

Transmission line method

The transmission line method (TLM), also frequently named transfer line method, is one of the most popular methods for the contact-resistance extraction, due to the fact that it

is relatively easy to use and does not require special transistor configurations. The TLM is based on the implications of equation 2.22: Since only the channel resistance but not the contact resistance depends on the channel length, measurements of transistors with different L allow to distinguish between these two components. As shown in figure 2.14, plotting the total resistance of transistors that differ only in the channel length and that are measured at the same bias conditions should give a straight line. An extrapolation of this line to $L = 0$ yields the contact resistance, which is usually done for several gate-source voltages.

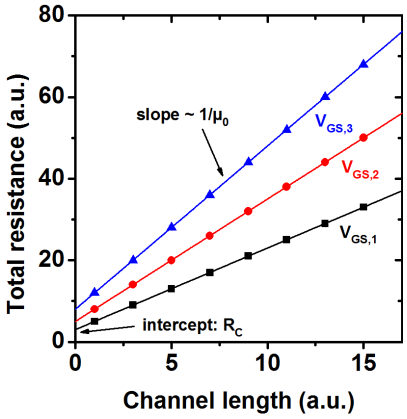


Figure 2.14: **Example of a TLM plot.** The total resistance of several transistors that differ only in the channel length is plotted as a function of the channel length, yielding the contact resistance from the intercept at $L = 0$ and the intrinsic mobility from the slope of the linear fit. The measurement is usually performed at several gate bias conditions.

Biasing transistors with different channel lengths at the same V_{DS} results in different potential drops across the contact regions V_C, because the voltage across the channel V_{ch} depends on the channel length and $V_{DS} = V_{ch} + V_C$. In case of non-ohmic contact resistances, this leads to a functional dependence of R_C on L, invalidating the use of the TLM. This is problematic, since nonlinearities in the output curve, which are a sign of such non-ohmic behavior, are frequently observed in OTFTs. A workaround would be to operate all transistors at the same I_D (and same V_{GS}) [72], but this makes the technique much more extensive and is rarely employed.
The transmission line method is usually applied at small V_{DS} (in the linear regime). In this case, equation 2.22 can be approximated as:

$$R_{tot} = R_{sheet}\frac{L}{W} + R_C \approx \frac{1}{\mu_0 C_i \left(V_{GS} - V_{th}\right)}\frac{L}{W} + R_C, \tag{2.28}$$

where μ_0 is the intrinsic mobility, which is the charge-carrier mobility of the ideal transistor (excluding contact effects). μ_0 can be obtained from the inverse slope of the linear fit to

the TLM plot (see figure 2.14).
A major problem of the TLM is the need to measure several transistors and the resulting scattering of the parameters R_C, μ_0 and V_{th}. Another issue with the TLM is that it only yields the total contact resistance, whereas the individual source and drain resistances are not accessible.

Kelvin probe force microscopy

Kelvin probe force microscopy (KPFM) is a powerful tool to measure the surface potential with high spatial resolution. KPFM is a scanning probe technique related to atomic force microscopy (AFM), but with an electrically conductive tip. By measuring the potential offset between the surface and the scanning tip, a map of the surface potential can be obtained. For OTFTs, KPFM can be used to obtain the complete potential profiles of the transistor channel, including the potential drops at source and drain caused by the contact resistances [127–131].
The main advantages of KPFM are that it is performed on a single device and no assumptions have to be made for the functional dependencies of parameters. The contact resistance is also obtained directly without extrapolations. Therefore, very detailed and model-independent results can be obtained. In addition, KPFM is not restricted to specific bias conditions and can therefore also be performed in the saturation regime. The main drawback of the technique is that a quite complex measurement setup is necessary, instead of simple current-voltage characteristics.

Gated four-probe measurements

Gated four-probe (GFP) measurements require a special TFT layout in which two narrow electrodes are placed between the source and drain contacts and slightly overlap with the channel area (see figure 2.15a). During a measurement of the current-voltage characteristics of the TFT, these electrodes are charged to the local channel potentials, which are recorded with high input-impedance voltmeters.
In the linear regime, the charge-carrier density in the channel is almost uniform, giving a linear potential profile in the channel from source to drain. Since the potentials V_1 and V_2 (with respect to the grounded source) at the positions L_1 and L_2 are known from the measurement, they can be used to linearly extrapolate the channel potential to the source and drain contacts (positions 0 and L) (figure 2.15b). If the channel potential is truly linear, any deviation of the extrapolated potentials from ground (source) or V_{DS} (drain) must originate from contact resistances. The contact resistances can thus be calculated from the potential drops at the source (ΔV_S) and at the drain (ΔV_D) using $R_S = \frac{\Delta V_S}{I_D}$ and $R_D = \frac{\Delta V_D}{I_D}$, while μ_0 can be obtained from the potential drop across the channel ΔV_{ch}.

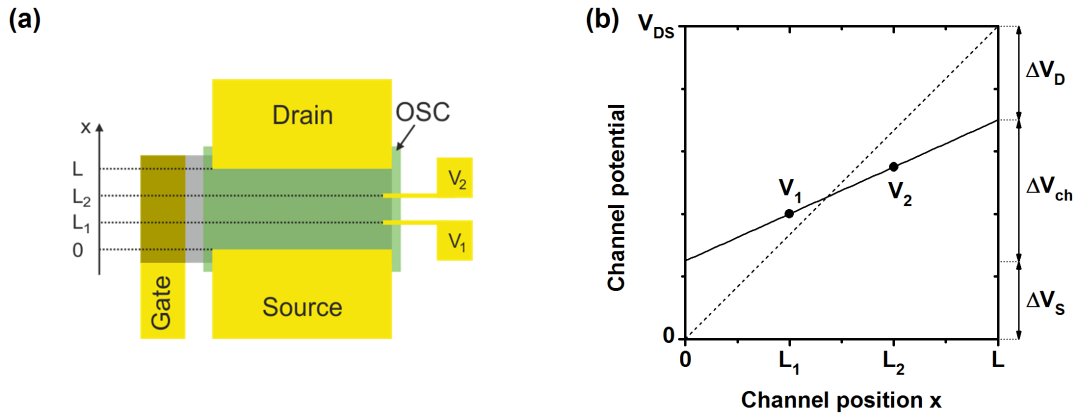


Figure 2.15: **Principles of the GFP technique.** (a) Top-view schematic of an OTFT in the GFP layout, showing the two narrow electrodes at the channel positions L_1 and L_2 that sense the voltages V_1 and V_2, together with the source and drain contacts, the gate electrode and the organic semiconductor (OSC). (b) Potential profile in the channel of an OTFT in the linear regime. In the classical GFP method, the potential is extrapolated to the source and drain contacts, revealing the individual potential drops at the contacts. The dashed line represents the potential profile for an ideal transistor without contact resistances.

Although not as detailed as KPFM, the GFP method is a sophisticated technique that reliably gives the individual source and drain resistances from the standard electrical characteristics of a single OTFT using only a few general assumptions [114, 132–134]. In addition, there are no requirements regarding the dependence of the contact resistance on V_{GS} or V_{DS} in the GFP technique. The main disadvantage is the need for a special device layout that has to be designed carefully so that the electrical characteristics of the device are not disturbed by the presence of the voltage probes [72].
The standard GFP method is only valid in the linear regime of transistor operation, but a workaround has been suggested by Richards et al. that partly extends the technique to the saturation regime [114]. A slightly adapted version of this more sophisticated GFP method is used in this work and is described in section 3.3.1.

2.5 Dynamic transistor operation

In many practical applications, the OTFT has to operate dynamically at high frequencies. For digital applications, this means that a fast switching between the on-state (logic ”1”) and off-state (logic ”0”) is necessary. For every switching event, the gate capacitor has to be charged or discharged, resulting in a displacement current i_G at the gate of the transistor. For switching between 0 V and V_{GS} and in the case of similar source and drain

contact lengths ($L_{C,S} = L_{C,D} = L_C$), i_G reads [31]:

$$i_G = 2\pi i\, f\, V_{GS}\, C_G \approx 2\pi i\, f\, V_{GS}\, C_i W (L + 2\, L_C) \tag{2.29}$$

with the imaginary unit i, the frequency f and the gate capacitance C_G, which consists of the channel capacitance C_{ch} and the two overlap capacitances C_{ov} at source and drain (see figure 2.16).

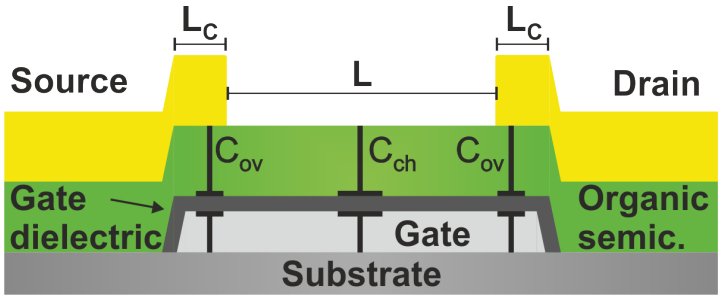


Figure 2.16: **Capacitances in an OTFT.**

The cutoff-frequency f_T is defined as the frequency at which this displacement current is as large as the drain current, i.e., the current gain is unity. Since the drain current is independent of the frequency, f_T can be approximated as:

$$f_T = \frac{\mu V_{DS}}{2\pi L(L + 2L_C)} \qquad \text{in the linear regime,} \tag{2.30}$$

$$f_T = \frac{\mu (V_{GS} - V_{th})}{2\pi L((2/3)L + 2L_C)} \qquad \text{in the saturation regime.} \tag{2.31}$$

The factor (2/3) in the second equation is due to the inhomogeneous charge distribution in the channel under saturation conditions [135, 136].
The cutoff-frequency does not directly give the operation frequency of circuits, such as ring oscillators, but equations 2.30 and 2.31 are instructive to understand the main mechanisms. The maximum operation frequency of a thin-film transistor depends on its current driving capability and the parasitic capacitances. For optimum performance, the former factor requires a high charge-carrier mobility, small contact resistances, high driving voltages and a small channel length. Parasitic capacitances are reduced for smaller channel and contact lengths. Consequently, for a given material combination and bias condition, the maximum operation frequencies can be enhanced by reduced lateral dimensions.

3 Fabrication and characterization

3.1 Fabrication

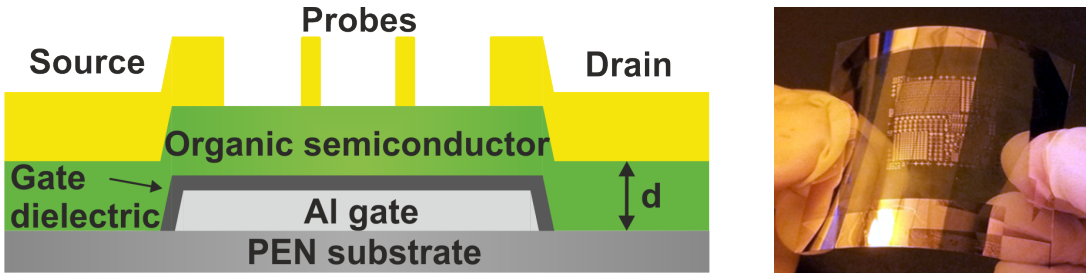


Figure 3.1: **Device fabrication.** (a) Cross section of the OTFTs used in this study (not to scale), showing the potential probes together with the other layers. (b) Photograph of devices on a flexible PEN substrate.

A schematic cross section of the devices fabricated in this work is shown in Fig. 3.1a. The organic TFTs were fabricated on 125-μm-thick flexible polyethylene naphthalate (PEN) substrates (Teonex® Q65 PEN; kindly provided by William A. MacDonald, DuPont Teijin Films, Wilton, UK) in a bottom-gate, top-contact (inverted staggered) structure. Prior to OTFT fabrication, the substrates were preheated in an oven at 120 °C to reduce shrinking or other deformations during subsequent heating steps. Afterwards, the substrates were cleaned using purified water, acetone, 2-propanol and an ultrasonic bath. No planarization layer was used to smoothen the relatively rough PEN surface (root mean square (RMS) roughness of about 3.9 nm, see section 4.1).
All metal and semiconductor layers were deposited by thermal evaporation in a Leybold UNIVEX 300 vacuum evaporation system at a base pressure of 10^{-5} mbar or below; the deposition rates were measured using a quartz microbalance. Patterning of these layers was accomplished using high-resolution silicon stencil masks [137], of which an exemplary image is shown in figure 3.2a. At first, Au contact pads (for the gate electrode) and interconnects (for integrated circuits) were deposited through a first stencil mask (deposition rate of ≈1 Å/s). 30-nm-thick Al gates were defined by a second stencil mask (deposition rate of 10-12 Å/s). The samples were then briefly exposed to an oxygen plasma

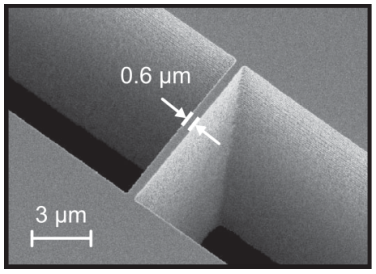


Figure 3.2: **Stencil masks.** Scanning electron microscopy (SEM) image of a high resolution silicon stencil mask used to pattern the source/drain layer of the OTFTs. The thickness of the mask is 20 μm. Image from [135].

(30 s, 10 mTorr, 30 sccm O_2, 200 W) in an OXFORD reactive ion etch system in order to increase the quality and the thickness of the native aluminum oxide layer to 3.6 nm and also to create a high density of hydroxyl groups on the Al/AlO_x surface. Afterwards, the samples were immersed in 2-propanol solutions of pentadecylfluoro-octadecylphosphonic acid molecules [138]. These molecules use the hydroxyl groups to bind to the surface, probably covalently [139, 140], forming a self-assembled monolayer (SAM). After keeping the samples in the solution for at least one day, the samples were rinsed in 2-propanol to remove excess molecules.

Since the resulting hybrid AlO_x/SAM gate dielectric is quite thin, having a thickness of about 5.7 nm, it has a high capacitance per unit area of around 550 nF/cm^2 (obtained from admittance measurements), that makes it possible to operate the transistors with voltages of 3 V or less. Due to the combination of two different components, the leakage current densities through the dielectric are very small [141]. Furthermore, the SAM provides a clean surface with a water contact angle of around 112° and a small surface energy of about 12 mN/m [138], which is usually favorable to achieve high charge-carrier mobilities [31].

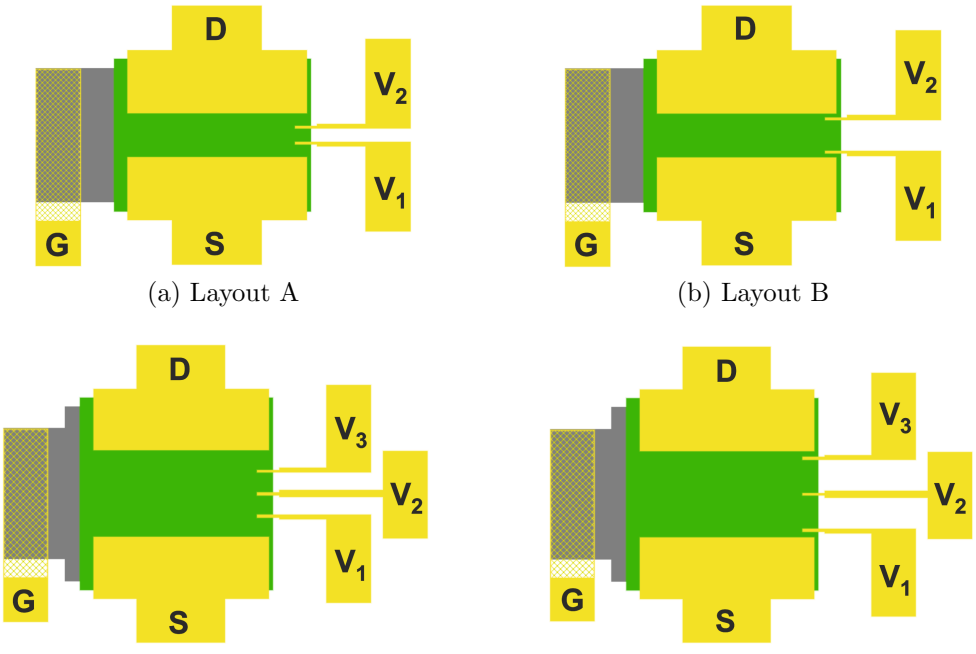
Onto the gate dielectric, the small-molecule organic semiconductor PDI-FCN_2 was deposited through a third stencil mask at a substrate temperature of 140 °C and with a deposition rate of 0.2 Å/s. The combination of the fluorinated SAM and the substrate temperature of 140 °C during deposition was found optimal for the formation of well-ordered semiconductor films with high charge-carrier mobilities [102]. The nominal thickness of the semiconductor layer d was varied between 6 nm and 35 nm, estimated using a density of 1.85 g/cm^3 that has been reported for single crystals [90].

For complementary circuits, dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) was used to realize the p-channel transistors. These transistors were fabricated next to the n-channel devices with the same layer structure (except for the different organic semiconductor). The nominal thickness of the DNTT layer was 20 nm, and it was deposited at a substrate temperature of 60 °C and with a deposition rate of 0.3 Å/s through another

stencil mask.
Finally, 30-nm-thick gold source/drain contacts and potential probes were evaporated through the last stencil mask, using a deposition rate of 0.3 Å/s. It is worth noting that many properties of the devices, such as mechanical flexibility of the substrate, low-voltage operation and good air stability of the semiconductor were chosen to meet the requirements of potential applications, i.e., the analysis was performed in a realistic environment.

3.2 Four-probe layouts

Top-view schematics of the four-probe geometries used in this work are shown in figure 3.3. The W and L are typically 400 μm and 100 μm with 5-μm-wide potential probes penetrating 25 μm into the channel. The channel area covered by the probes is less than 1 %, ensuring that the probes are not affecting the device behavior. Both semiconductor and gate are patterned to avoid probing gated areas outside the channel, which would lead to perturbations of the measurement [133]. Four different layouts for the probe positions were used, with two probes dividing the channel into equal segments (layout A), with two probes closer (10 μm distance) to the source/drain contacts (layout B) and two layouts with a longer channel length of 200 μm to leave space for a third probe in the middle of the channel (layout C and D). Exemplary photographs of two devices are shown in figure 3.4, and details of the geometries are summarized in table 3.1.



(a) Layout A (b) Layout B

(c) Layout C (d) Layout D

Figure 3.3: **Top-view schematics of the GFP layouts used in this work.**

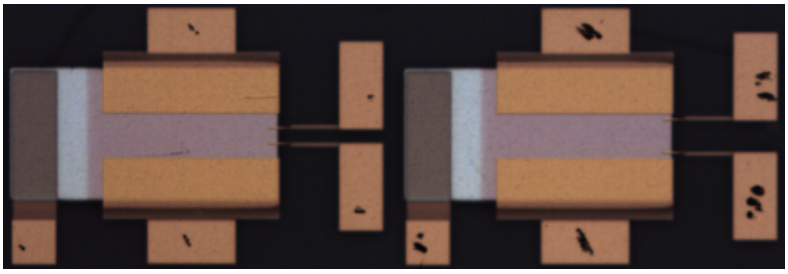


Figure 3.4: **Photograph of OTFTs in the GFP layouts A (left) and B (right).**

Layout	W (μm)	L (μm)	L_1 (μm)	L_2 (μm)	L_3 (μm)
A	400	100	32.5	67.5	-
B	400	100	12.5	87.5	-
C	400	200	48.75	100	151.25
D	400	200	17.5	100	182.5

Table 3.1: **Summary of the geometries of the GFP layouts.** L_1, L_2 and L_3 are the positions of the probes in the channel (see figure 2.15 for comparison).

3.3 Electrical measurements

Electrical measurements were performed in air at room temperature in a cleanroom using a Micromanipulator 6200 manual probe station, low-noise triaxial cables and an Agilent 4156C Precision Semiconductor Parameter Analyzer with a resolution of 1 fA and 2 μV. Temperature-dependent measurements were performed in a high vacuum chamber at a pressure of about 10^{-8} mbar. In this case, the connection to the parameter analyzer was realized by wire-bonding the pads to a chip-carrier.
Prior to electrical measurements, three quick transfer curves were measured in order to stabilize the threshold voltage of the transistors and to minimize shifts during a single measurement. Transfer curves were usually measured in the forward (off to on) and backward (on to off) direction, while the forward curve was used for parameter extraction (except for the subthreshold swing).
Dynamic characterization was performed using a Tektronix TDS1001B digital storage microscope.

3.3.1 The GFP method used in this work

The basics of the conventional GFP technique were explained in section 2.4.4. The more evolved method used in this work, which is based on the method of Richards et al. [114],

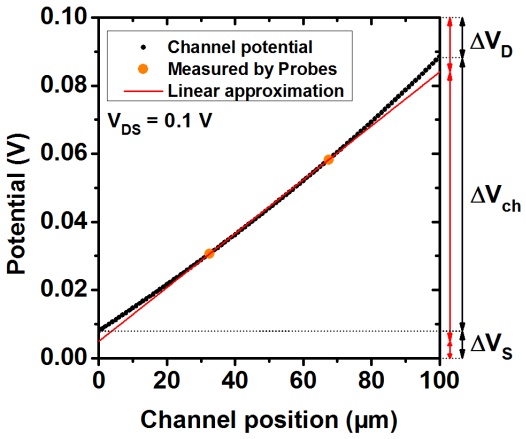


Figure 3.5: **Principles of the GFP method used in this work.** For a nonlinear potential profile, a linear approximation of the potentials measured from the probes leads to significant deviations of the estimated potential drops at source and drain compared to the real values. However, the potential drop across the channel is nearly identical for both cases.

is described in this section.

At first, the experimental data of a transfer curve measured at small V_{DS} is required. Due to the nonzero value of V_{DS}, the charge carrier concentration varies slightly in the channel, even at $V_{GS} - V_{th} >> V_{DS}$. This means that the sheet resistivity in the channel is higher at the drain side than at the source side, leading to a slight bending of the potential profile: it is flatter close to the source region and steeper close to the drain region. The assumption of a perfectly linear potential profile could now lead to an underestimation of the potential drop at the source contact and an overestimation of the potential drop at the drain contact. However, for the potential drop across the channel ΔV_{ch}, the downwards and upwards bending of the potential profile partly compensate for each other. Accordingly, if this bending is small, i.e., at $V_{GS} - V_{th} >> V_{DS}$, the real ΔV_{ch} is very similar to the case of a perfectly linear potential profile. These principles are illustrated in figure 3.5.

Hence, the procedure starts with a linear extrapolation of the channel potential using the probe potentials, analogous to the conventional GFP procedure shown in figure 2.15b, but considering at first only ΔV_{ch}. Using this, the channel resistance is obtained by dividing ΔV_{ch} by the drain current, which then gives the sheet conductance $G_{sheet} = 1/R_{sheet}$:

$$R_{ch} = \frac{\Delta V_{ch}}{I_D} = \frac{1}{G_{sheet}} \cdot \frac{L}{W}. \tag{3.1}$$

The idea is to obtain a complete dataset of G_{sheet} values as a function of the gate field, which can then be used to locally calculate the potential profile. The average potential in the channel, implying symmetric probe positions, is $(V_1 + V_2)/2$ (in case of identical potential drops at source and drain this would be equivalent to $V_{DS}/2$). Hence, the

average difference between the gate potential and the average channel potential V_{Gch} is $V_{Gch} = V_{GS} - (V_1 + V_2)/2$. The sheet conductance at a specific V_{Gch}, resulting from a specific gate-source voltage, can then be calculated as:

$$G_{sheet}[V_{Gch}] = \frac{I_D[V_{GS}]}{V_2[V_{GS}] - V_1[V_{GS}]} \cdot \frac{L_2 - L_1}{W}. \tag{3.2}$$

Repeating this calculation for all V_{GS} yields a map of the sheet conductance as a function of V_{Gch}. Since the number of data points is limited, $G_{sheet}[V_{Gch}]$ is interpolated for all V_{Gch} to improve accuracy.

The sheet conductance can then be used to locally calculate potential differences between two nearby positions in the channel x_1 and x_2:

$$V[x_2] - V[x_1] = \frac{1}{G_{sheet}[V[x_1]]} \cdot I_D[V_{GS}] \cdot \frac{x_2 - x_1}{W}, \tag{3.3}$$

thus allowing the stepwise calculation of the potential profile starting from the probe positions L_1 and L_2. The extrapolations to source and drain then allow the calculation of the contact resistances from the corresponding potential drops ($R_S = \frac{\Delta V_S}{I_D}$ and $R_D = \frac{\Delta V_D}{I_D}$). The main advantage of the potential profiling is that it allows the handling of nonlinear potential profiles. If $G_{sheet}[V_{Gch}]$ is known from a transfer curve taken at $V_{GS} - V_{th} >> V_{DS}$, this data can be used to calculate the potential profile at higher V_{DS} as well. The only requirements are that the mobility is independent of the lateral electric field and that the gradual channel approximation is still locally valid. The second premise prevents the further calculation of the channel potential as soon as $V[x] \approx V_{GS} - V_{th}$. This means that R_D cannot be measured under saturation conditions, but still for larger V_{DS} as long as the channel shows no pinch off. The determination of R_S, on the other hand, is possible even deep in saturation conditions, because the channel potential on the source side is smaller.

In the method introduced in [114], the information about $G_{sheet}[V]$ (or in that publication the equivalent information about $\mu[V]$) is obtained from a linear extrapolation only at the highest V_{GS} and the smallest V_{DS}, where linearity is ensured. The complete $\mu[V]$ is then built up using

$$\frac{\mathrm{d}I_D}{\mathrm{d}V_{GS}} = \frac{WC_i}{L_2 - L_1} \left(V[L_1]\mu[V[L_2]] - V[L_1]\mu[V[L_2]] \right), \tag{3.4}$$

which is valid for all gate and drain voltages and for any μ subject to the gradual channel approximation. Instead, $G_{sheet}[V]$ was calculated pointwise in this work using a linear approximation of the channel potential. This introduces a small error when $V_{GS} - V_{th}$ is small as discussed above, but avoids using a derivative, which can be disadvantageous if noise is present in the experimental data.

3.4 Atomic force and scanning electron microscopy

Atomic force microscopy images were obtained using a Bruker Nanoscope III MultiMode® or an Asylum Cypher™ S in ambient air. Tapping mode using cantilevers with a resonance frequency between 200 and 500 kHz or contact mode using a soft cantilever ($k \approx 0.01$ N/m) was utilized. Analysis was performed with the help of the WSxM software [142].
Scanning electron microscopy measurements were performed on a Zeiss Merlin® microscope. Imaging was done using the in-lens secondary electron detector.

4 Gated four-probe characterization

This chapter deals with the analysis of the contact resistance in PDI-FCN_2 TFTs with different semiconductor thicknesses. Preliminary to this, in section 4.1 the morphology of the thin films is discussed and their suitability for the analysis is shown, while the basic electrical characteristics are presented in section 4.2. A detailed analysis of the contact resistances using the gated four-probe method follows in sections 4.3 to 4.7. In these sections, the emphasis is on the influence and interplay of a multitude of parameters on the contact properties in order to shed light on the main mechanisms determining these parasitic resistances. A conclusion of the contact analysis and a discussion of possible physical mechanisms at the contacts are given in section 4.10.

4.1 Thin-film morphology

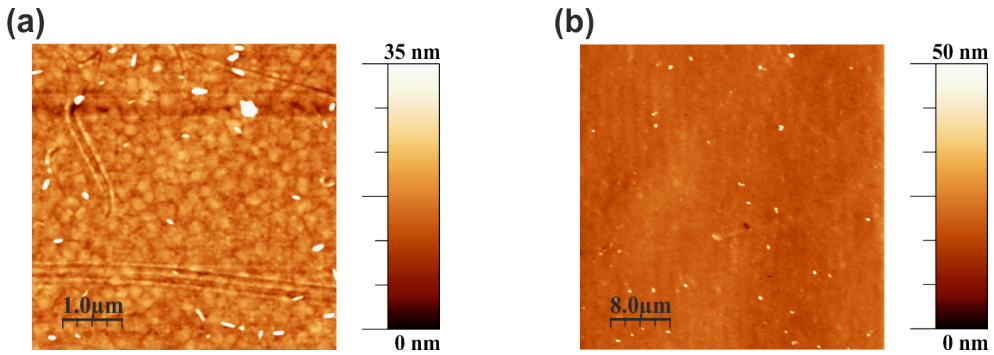


Figure 4.1: **AFM topography measurements on a PEN substrate.** (a) Topography of a PDI-FCN_2 thin film with a nominal thickness of 35 nm on PEN/Al/AlO_x/SAM obtained in tapping mode. (b) Topography of a 40×40 μm^2 area of a PEN substrate. The height scale is cropped for better visibility.

The molecular arrangement in the organic films is known to have a significant influence on the charge-transport properties in OTFTs [31, 143]. Figure 4.1a shows the AFM morphology image of a nominally 35-nm-thick PDI-FCN_2 film vacuum-deposited onto a PEN/Al/AlO_x/SAM substrate. Several trenches and surface peaks are visible. They

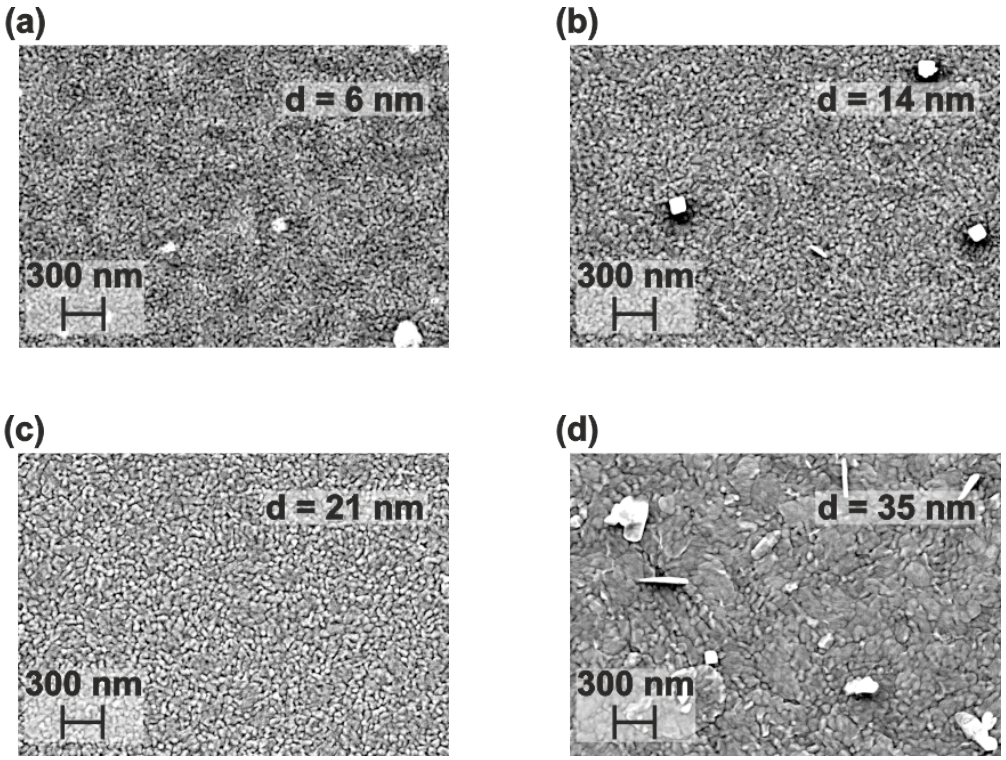


Figure 4.2: **SEM images of the surface of PDI-FCN_2 thin films.** The images were obtained at an acceleration voltage of 1 kV and depict the surface of PDI-FCN_2 films with nominal thicknesses of (a) 6nm, (b) 14nm, (c) 21nm and (d) 35nm on a PEN/Al/AlO_x/SAM substrate.

probably originate from the underlying PEN substrate, whose topography is shown in figure 4.1b. The root mean square (RMS) roughness of the bare PEN surface is around 3.9 nm, in agreement with literature values [144]. The surface peaks have a height of up to ≈100 nm, which is not reflected in the height scale of the images in order to promote the visibility of other features. The large-scale image of the bare PEN substrate also reveals a certain corrugation of the surface.

Figure 4.1a also shows some features of the PDI-FCN_2 thin-film morphology. Three-dimensional islands are visible in the image, but the pronounced features of the underlying substrate complicate a further analysis, and this was even worse for samples with thinner organic semiconductor films (not shown). Therefore, the semiconductor morphology was investigated by scanning electron microscopy. Figure 4.2 shows SEM images of PDI-FCN_2 layers with nominal semiconductor thicknesses of 6 nm to 35 nm, again on a PEN substrate. Up to a nominal thickness of 21 nm, the images mainly show a relatively flat surface with a fine granularity. At a nominal semiconductor thickness of 6 nm, darker spots indicate that the topmost layer is not completely closed. For a nominally 35-nm-thick film, pronounced island growth and steps are visible.

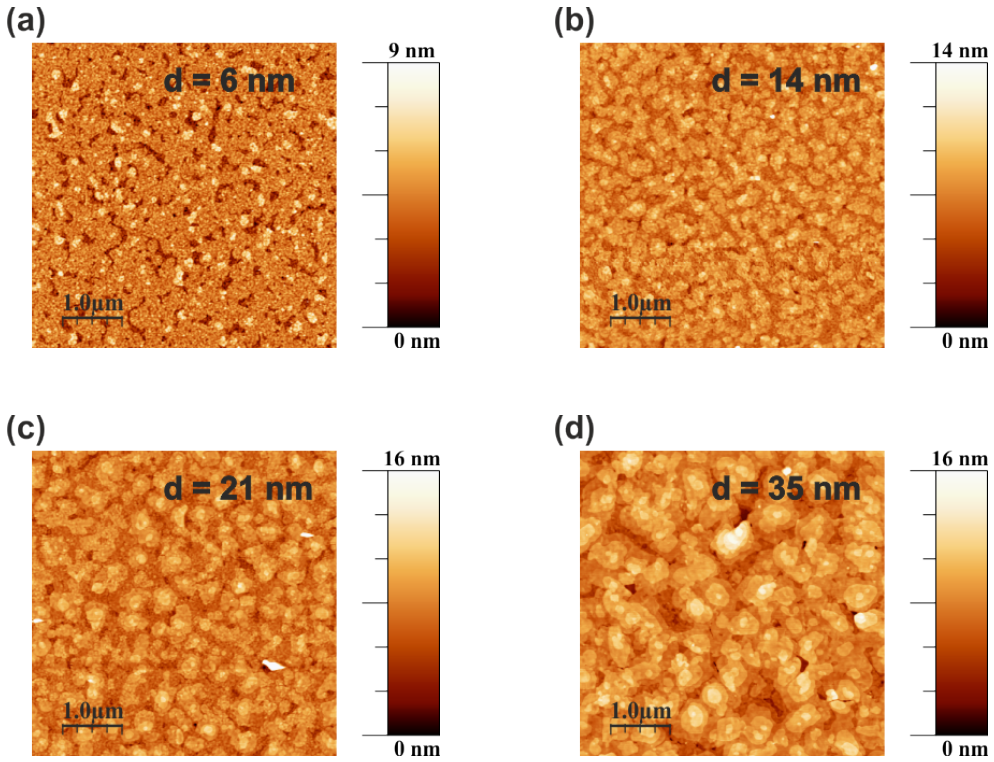


Figure 4.3: **AFM topography images of PDI-FCN$_2$ thin films on a Si substrate.** Morphology of PDI-FCN$_2$ thin films with nominal thicknesses of (a) 6 nm, (b) 14 nm, (c) 21 nm and (d) 35 nm obtained in tapping mode. For better feature visibility, these images were taken on reference samples with the same layer composition described in section 3.1, but a smoother silicon wafer instead of a PEN foil served as the substrate. The images have a size of 5 × 5 μm^2.

SEM images are useful to study the surface morphology, but they do not contain information about feature heights. Therefore, and also as a reference, AFM topography images of PDI-FCN$_2$ thin films fabricated on a silicon substrate are shown in figure 4.3. Apart from the different substrate, the layer composition of these reference samples is unchanged (Si/Al/AlO$_x$/SAM/PDI-FCN$_2$). Thanks to the smaller roughness of the Si substrate, the PDI-FCN$_2$ film morphology is clearly visible. At a nominal semiconductor thickness of 6 nm, most of the surface is formed by a closed layer of PDI-FCN$_2$ molecules, while only some small areas show a gap or the beginning of an additional layer. As the amount of deposited material is increased, pronounced three-dimensional island growth takes place. The step height of the layers can be estimated to a value of around 2 nm. Considering the long-axis length of a PDI-FCN$_2$ molecule of 2.3 nm [90], the molecules are probably standing approximately upright with only a small tilt angle. This molecular orientation, which is beneficial for the horizontal charge transport in the TFT, is commonly encountered in the growth of organic molecules on insulators and has been observed before in thin films of PDI-FCN$_2$ [90, 103]. On the other hand, the π-π-overlap in the direction normal to the

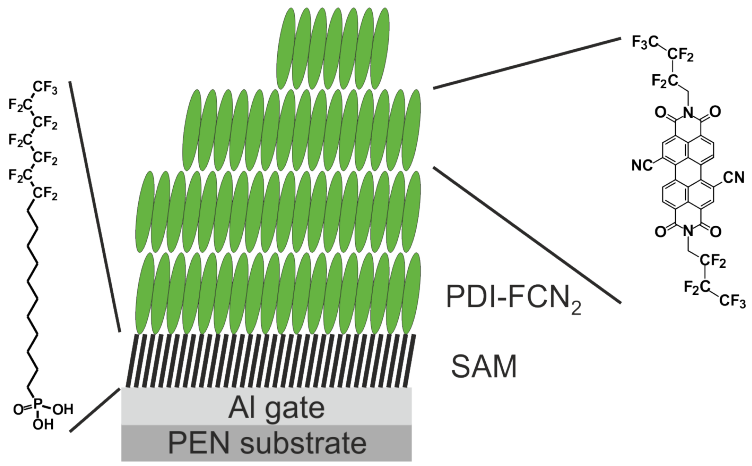


Figure 4.4: **Schematic of the molecular layer structure.** Simplified schematic cross section of a sample with a PDI-FCN_2 thin film showing the assumed molecular arrangement.

substrate is reduced in this molecular orientation, which is detrimental for vertical charge transport [98]. A schematic of the molecular arrangement is given in figure 4.4.
A comparison of the images taken on the PEN and the Si substrate indicates that the higher roughness of the PEN surface leads to delayed island growth, higher granularity and a smaller island size, which could result in a lower charge-carrier mobility [143, 145]. An important aspect of the AFM and SEM images is the small density of large features, e.g. lamellas or needle-shaped structures, that are frequently formed during the growth of organic semiconductors [17, 146]. These features can have extreme peak heights and can result in a quite inhomogeneous material distribution, preventing a meaningful analysis of TFT parameters depending on the nominal semiconductor thickness. In contrast, the comparatively smooth and continuous growth of the PDI-FCN_2 layers ensures that the layer thickness is continuously increasing with the amount of deposited material. To analyze this in more detail and to investigate if the gold source/drain layer on top of the PDI-FCN_2 film has an impact on the semiconductor film, SEM cross section images of a complete OTFT layer structure were recorded. To do so, an area at the edge of a PEN substrate including all layers (Al, hybrid dielectric, PDI-FCN_2 and Au) was covered with an about 0.5-μm-thick layer of Pt by ion beam-induced deposition. This layer served as a protective layer during the following focused ion beam sputtering process that created a trench with a depth of several tens of microns and exposed a clean cross section of the OTFT layer structure. A side view of this trench, including the area of interest, is depicted in figure 4.5a. A cross section of the OTFT layers is shown in figure 4.5b, where the measured layer thicknesses are also indicated. Since the nominal semiconductor thickness was 35 nm in this case, the measured thicknesses agree very well with the

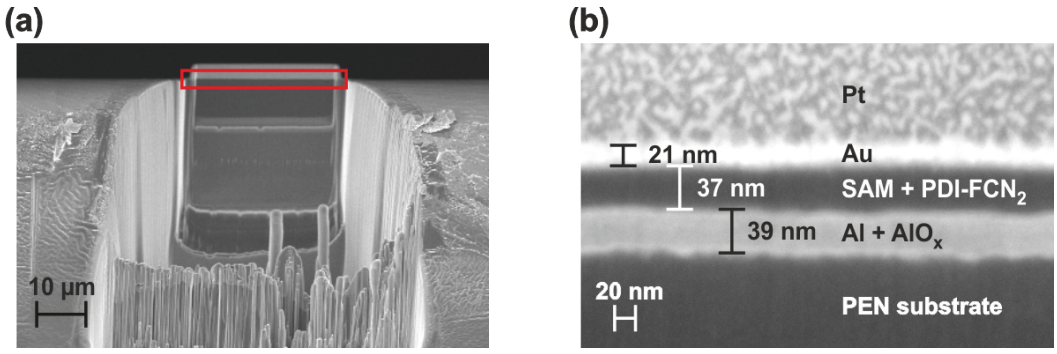


Figure 4.5: **SEM cross section image of an OTFT layer structure on PEN.** (a) Side view of the trench created by focused ion beam sputtering and the exposed OTFT layer structure in the region marked by the red rectangle. (b) Cross section of the OTFT layers. The nominal semiconductor thickness is 35 nm, which agrees well with the measured layer thickness. In addition, no sign of pronounced Au metal penetration into the PDI-FCN_2 layer is visible.

expected values. Only the gold layer appears to be too thin, as nominally 30 nm were deposited; this probably has to do with intermixing or alloying and insufficient contrast with the Pt layer. The PDI-FCN_2 layer seems to be relatively uniform and flat.
An important observation is that the images show no sign of Au metal penetration into the PDI-FCN_2 layer. When small and hot metal atoms impinge on the soft surface of an organic semiconductor, interdiffusion or chemical reactions are possible [73, 147–149], which could have a significant influence on the charge transport properties in this region. Although such effects cannot be completely ruled out, the lack of any sign in the SEM image makes significant and deep interdiffusion unlikely.

4.2 Electrical characteristics

Figure 4.6 displays the transfer characteristics of one representative transistor for each nominal semiconductor thickness in the linear regime ($V_{DS} = 0.1$ V, top) and in the saturation regime ($V_{DS} = 3.0$ V, bottom). The transistors have a channel width of $W = 400$ μm, a channel length of $L = 100$ μm and a contact length of $L_C = 100$ μm. In order to show all aspects of the curves, the graphs on the left show the drain current or its square root on a linear scale, while the graphs on the right have a logarithmic scale.
First, the curves in the linear regime of operation are discussed. The electrical characteristics exhibit small gate leakage currents (usually below 0.1 nA), on/off current ratios of about 10^5 and a hysteresis that is in general small, but somewhat larger for $d = 6$ nm. The subthreshold swing is in the range of 130-160 mV/decade in all transistors. It should be noted that measurements on reference samples (layer structure Si/Al/AlO_x/SAM/PDI-

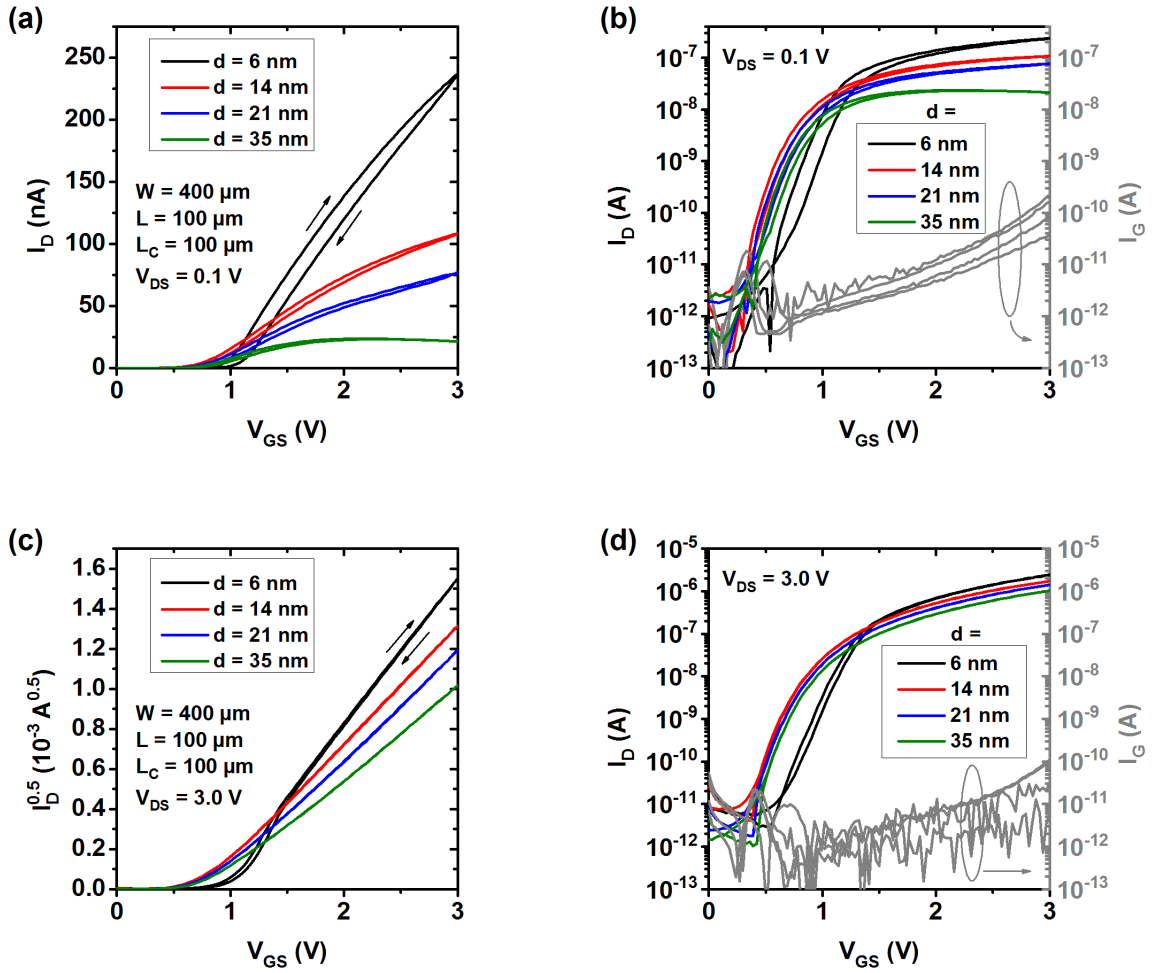


Figure 4.6: **Transfer characteristics of TFTs with different nominal semiconductor thicknesses.** All transistors have $W = 400$ μm, $L = 100$ μm and $L_C = 100$ μm. Images (a) and (b) show the curves in the linear regime ($V_{DS} = 0.1$ V), while images (c) and (d) illustrate the transfer curves in the saturation regime ($V_{DS} = 3.0$ V). Different scales were used on the left and right side to show all features of the transfer curves. The TFTs were fabricated on PEN substrates.

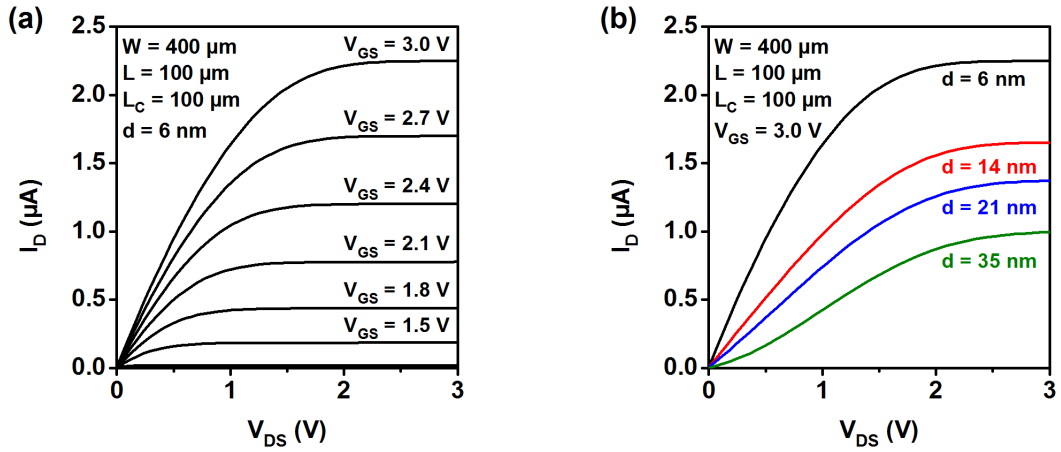


Figure 4.7: **Output characteristics.** (a) Output curves for a nominal semiconductor thickness of 6 nm shown for various V_{GS}. The curves are linear at small V_{DS} and exhibit a pronounced saturation behavior. (b) Output curves at $V_{GS} = 3.0$ V shown for all semiconductor thicknesses.

FCN_2) with an even smaller nominal semiconductor thickness than shown here ($d = 3$ nm) exhibit almost no field effect because the semiconductor layer is not closed.

With increasing semiconductor thickness, the transconductance decreases, which may be interpreted as a decrease of the field-effect mobility. However, as discussed in section 2.4, the mobility extracted directly from the experimental transfer curve, the effective mobility μ_{eff}, can differ from the intrinsic charge-carrier mobility in the channel. For the largest nominal semiconductor thickness used in this study (35 nm), the graphs also show a decrease of the drain current at large V_{GS}. This leads to a negative transconductance, an interesting phenomenon that indicates a significant deviation from the ideal transistor behavior and is usually not found in organic transistors [150].

In the saturation regime, the differences between the curves obtained for different d are smaller. The hysteresis is smaller and the effective mobility is more similar and always positive for all values of d. A bump in the transfer curve for $d = 6$ nm at small gate-source voltages, a specific feature already slightly visible in the linear regime, is now much more pronounced.

The output characteristics for $d = 6$ nm are shown in figure 4.7a. At small V_{DS}, the drain current features the ideal linear increase with the drain-source voltage, and a pronounced saturation behavior is present at large V_{DS}. For all semiconductor thicknesses, the output curves measured at $V_{GS} = 3.0$ V are plotted in figure 4.7b. As already observed in the transfer characteristics, the drain current becomes monotonically smaller as d is increased. In addition, a superlinear increase of the drain current is visible at small V_{DS} for $d = 35$ nm. The reasons and consequences of the above-mentioned features in the transfer and output characteristics will be analyzed and discussed in the following sections.

4.3 Gate-source voltage dependence

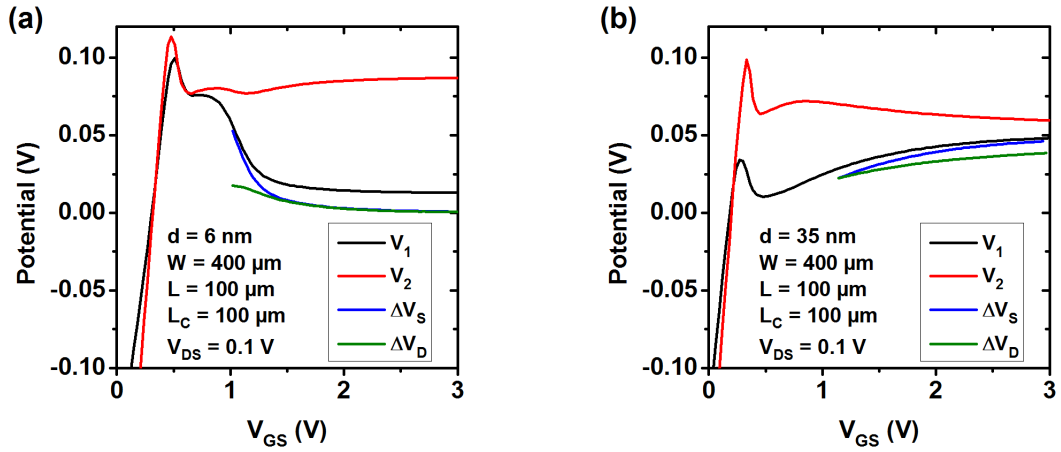


Figure 4.8: **Exemplary potential data obtained from gated four-probe measurements.** Measured channel potentials and calculated potential drops as a function of the gate-source voltage for (a) $d = 6$ nm and (b) $d = 35$ nm. The transistors have the GFP layout B.

From the I_D-V_{GS} characteristics alone it is quite difficult to obtain further insight into the transistor properties. However, using the information gathered from the potential probes, the intrinsic contributions to the transistor resistances can be easily disentangled using the GFP technique. Representative plots of the measured channel potentials V_1 and V_2 obtained at $V_{DS} = 0.1$ V and the calculated potential drops at the source (ΔV_S) and the drain (ΔV_D) as a function of V_{GS} are given in figure 4.8 for nominal semiconductor thicknesses of 6 nm and 35 nm. At small gate-source voltages, the potential probes measure potentials outside the range of the applied biases. This behavior is probably a result of static charge buildup on the semiconductor film surface and in the cables of the measurement system while the channel is not conductive [132]. At larger V_{GS}, the channel is much more conductive and the potentials sensed by the probes reflect the channel potential in the transistor, allowing a meaningful calculation of the potential drops at source and drain. It should be noted that the differences between ΔV_S and ΔV_D for $d = 6$ nm at relatively small gate-source voltages were only visible for some, but not all transistors having that nominal semiconductor thickness.

Figure 4.9 shows the individual channel, source and drain resistances on a log scale as a function of the gate-source voltages for all nominal semiconductor thicknesses. The channel resistances are quite similar for all values of d, meaning that the charge transport in the accumulation channel (and therefore the intrinsic mobility) is barely affected by the amount of deposited semiconductor material. This indicates that the accumulation layer

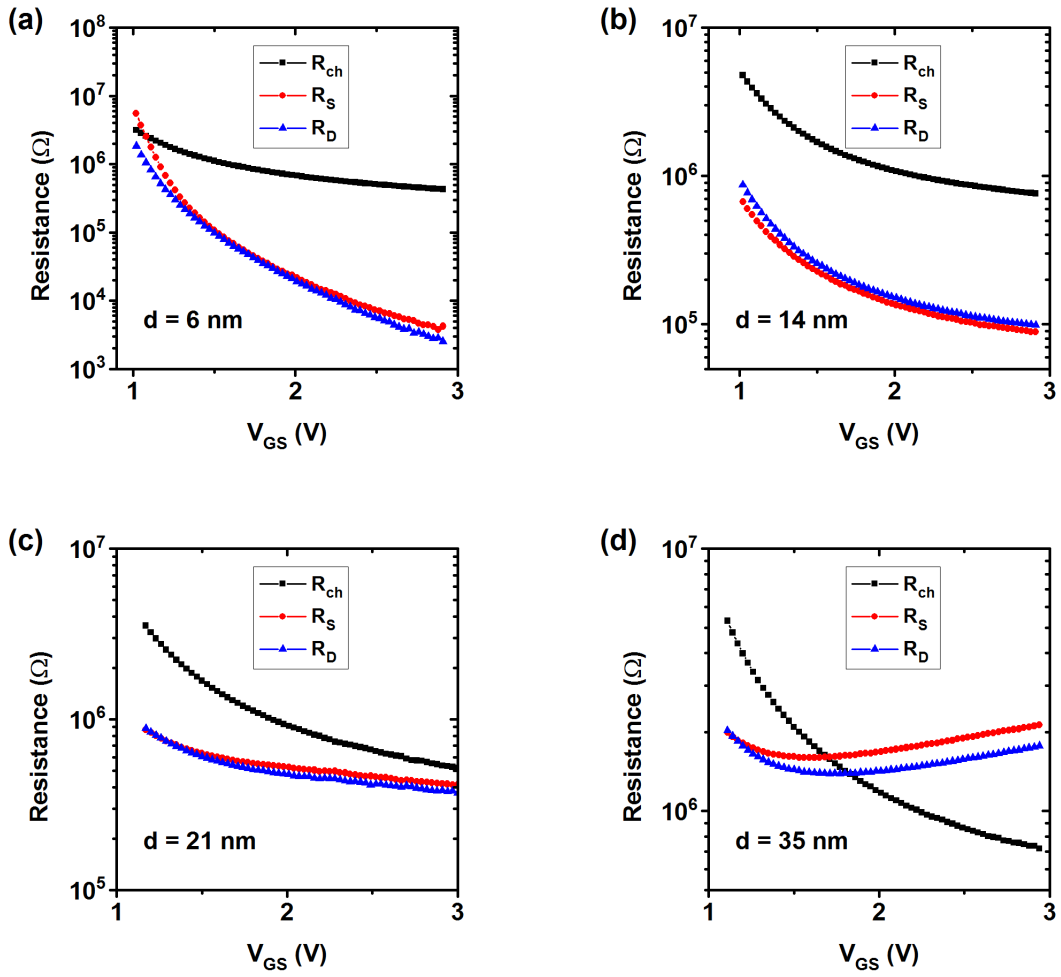


Figure 4.9: **Channel, source and drain resistances as a function of the gate-source voltage.** Intrinsic resistances of transistors with a channel width of 400 μm, a channel length of 100 μm and a contact length of 100 μm, measured at $V_{DS} = 0.1$ V. As the nominal semiconductor thickness is increased from 6 nm (a) to 35 nm (d), the magnitude and the functional dependence of the contact resistances change drastically, while the channel resistance is similar for all thicknesses. The source and drain resistances have the same functional dependence on V_{GS} and are essentially identical in magnitude.

is indeed very thin and that at least the first molecular layer is (almost) closed. On the other hand, drastic differences in the source and drain resistances are visible that must therefore be responsible for the observed differences in the transfer characteristics.
For all nominal semiconductor thicknesses, R_S and R_D are on the order of 1 MΩ at V_{GS} slightly above threshold. In the case of $d = 6$ nm, the soure and drain resistances then drop by almost three orders of magnitude as V_{GS} is increased to 3 V. In the same V_{GS} range, the channel resistance decreases much less, by only about one order of magnitude. The drop of R_S and R_D becomes less and less pronounced as the semiconductor thickness is increased and even turns into a slight increase at larger V_{GS} for $d = 35$ nm. Apparently, this slight increase of the contact resistances with increasing gate-source voltage is responsible for the drop of the drain current at high V_{GS} seen for $d = 35$ nm (figure 4.6a).
For all nominal semiconductor thicknesses, R_S and R_D have a similar magnitude and similar dependence on V_{GS}. Therefore, figure 4.10a summarizes the graphs of figure 4.9 by plotting the width-normalized total contact resistance $R_C W = (R_S + R_D)W$ as a function of the gate overdrive voltage $V_{GS} - V_{th}$, highlighting the drastically different functional dependencies of the contact resistances on the gate bias for different nominal semiconductor thicknesses. For a nominal semiconductor thickness of 6 nm and at high V_{GS}, $R_C W$ drops to values in the range of around 0.3 kΩ cm to 0.8 kΩ cm (mean value ≈0.6 kΩ cm, see section 4.3.2), which is among the smallest contact resistances reported for organic n-channel TFTs [72, 82, 151], despite the operation in ambient air and the lack of any contact treatment [152, 153]. This contact resistance is also comparable to that of high-performance organic p-channel TFTs [17, 154, 155]. A summary of the smallest contact resistances reported for organic TFTs in the literature is given in table 4.1.

Reference	Semiconductor	Type	Method	in	Interlayer	$R_C W$ (kΩ cm)
This work	PDI-FCN_2	n-channel	GFP	air	-	0.6
Ma [151]	PDI-C13	n-channel	TLM	N_2	-	0.9
Khim [82]	PCBM	n-channel	TLM	N_2	CsF	0.16
Acton [152]	C_{60}	n-channel	TLM	N_2	-	0.85
Kim [153]	P(NDI2OD-T2)	n-channel	TLM	N_2	$Ba(OH)_2$	0.53
Ante [154]	DNTT	p-channel	TLM	air	-	0.6
Hofmockel [17]	C_{10}-DNTT	p-channel	TLM	air	-	0.33
Stadlober [155]	pentacene	p-channel	TLM	N_2	AuO_x	0.08

Table 4.1: **Summary of some of the smallest contact resistances reported for OTFTs.** The width-normalized contact resistance values are given for the highest reported gate-source voltage.

At a moderate gate overdrive voltage of 1 V, the width-normalized source and drain contact resistances are plotted as a function of the nominal semiconductor thickness in

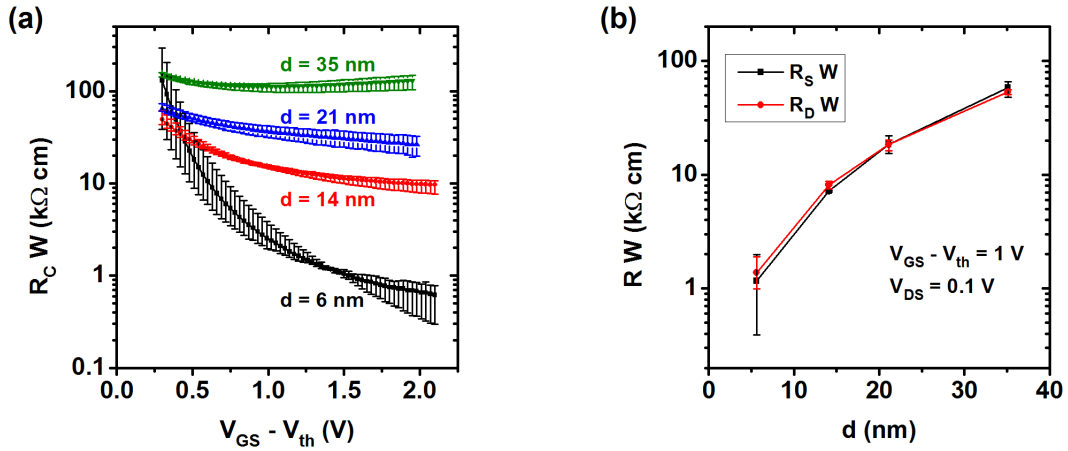


Figure 4.10: **Comparison of the contact resistances for different nominal semiconductor thicknesses.** Values were averaged using parameters from four transistors with $W = 400\ \mu$m, $L = 100\ \mu$m and $L_C = 100\ \mu$m at $V_{DS} = 0.1$ V, error bars indicate the full range of measured values. (a) Width-normalized contact resistance for all values of d as a function of the gate overdrive voltage. (b) Width-normalized source and drain resistances as a function of the nominal semiconductor thickness at $V_{GS} - V_{th} = 1$ V.

figure 4.10b, showing an increase that is stronger than linear, but not exponential. It is again evident that the values obtained for R_S and R_D are very similar.

As discussed in section 2.4.2, the current crowding model describes R_S and R_D as combinations of the horizontal accumulation layer sheet resistance and the vertical contact resistivities. Since the sheet resistances are similar for all semiconductor thicknesses, it is instructive to analyze the vertical components. Figure 4.11a plots the source contact resistivities as a function of the gate overdrive voltage at $V_{DS} = 0.1$ V; the drain contact resistivities are very similar (not shown). As will be discussed later in section 4.4, the current crowding model is probably valid under these conditions. ρ_S was calculated numerically from R_S and R_{sheet} using equation 2.23. The functional dependence of ρ_S on the gate bias is very different for different nominal semiconductor thicknesses. This characteristic was already observed for the contact resistances, but is more pronounced for the contact resistivities. In the considered V_{GS} range, ρ_S drops by roughly four orders of magnitude when $d = 6$ nm, but by only about one order of magnitude when $d = 14$ nm. ρ_S is fairly independent of V_{GS} for $d = 21$ nm and it increases with V_{GS} for $d = 35$ nm. The smallest contact resistivities measured here are in the range of $10^{-1}\ \Omega\,\mathrm{cm}^2$ to $10^{-2}\ \Omega\,\mathrm{cm}^2$. These values are excellent for organic thin-film transistors, even outperforming a-Si:H TFTs, where $\rho_C \approx 0.2\ \Omega\,\mathrm{cm}^2$ [118, 156]. Contact resistivities as small as $10^{-4}\ \Omega\,\mathrm{cm}^2$ are reached in zinc oxide transistors [157], and values as small as $10^{-9}\ \Omega\,\mathrm{cm}^2$ are obtained in silicon MOSFETs [158].

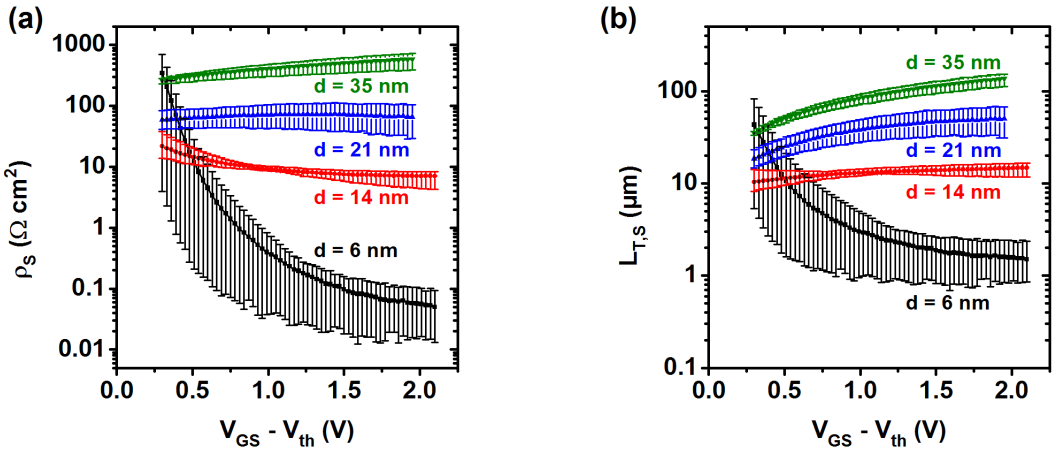


Figure 4.11: **Parameters from the current crowding model for all nominal semiconductor thicknesses.** Values were averaged using parameters from four transistors with $W = 400$ μm, $L = 100$ μm and $L_C = 100$ μm at $V_{DS} = 0.1$ V, error bars indicate the full range of measured values. (a) Source contact resistivity as a function of the gate overdrive voltage. (b) Source transfer length as a function of the gate overdrive voltage.

The source contact resistivity as a function of the nominal semiconductor thickness is plotted semilogarithmically in figure 4.12a; the behavior of the drain contact resistivity is similar. Since the contact resistivity comprises only the vertical component, the dependence on d is more pronounced than that of the contact resistance. However, there is still no apparent functional dependence of ρ_S on d, indicating that either the interface resistivity is significant for at least some of the thicknesses or that the real thickness deviates from the nominal value, for example due to surface roughness. Also, the dependence of ρ_S on d is different for different gate overdrive voltages.

An empirical model describes the contact resistivity (or the contact resistance) as being composed of a constant part ρ_0 and a part that is inversely proportional to the gate overdrive voltage [114, 115, 159]. This model can be generalized to allow an arbitrary power-law dependence on the gate overdrive voltage [126, 160], giving:

$$\rho_S = \rho_0 + A(V_{GS} - V_{th})^{\alpha}, \tag{4.1}$$

where A is a fitting parameter. In order to test this model, the derivative of the source contact resistivity with respect to the gate overdrive voltage was calculated: $\Theta = \partial\rho_S/\partial(V_{GS} - V_{th})$. In a log-log plot of Θ versus the gate overdrive voltage, a straight line should be obtained if equation 4.1 holds true. Such a graph is given in figure 4.12b for three of the nominal semiconductor thicknesses used in this study. For $d = 21$ nm, the data was too noisy and is not shown.

A good agreement with an inversely proportional dependence (α = -1), as proposed in

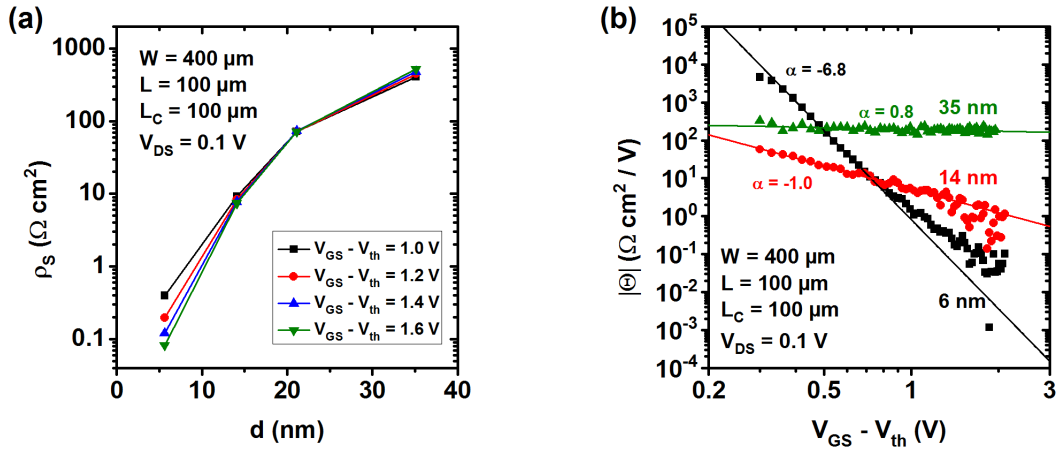


Figure 4.12: **Thickness and gate-source voltage dependence of the contact resistivity.** (a) Source contact resistivity as a function of the nominal semiconductor thickness at $V_{DS} = 0.1$ V for various gate overdrive voltages. (b) Absolute value of the derivative of ρ_S with respect to $V_{GS} - V_{th}$ as a function of $V_{GS} - V_{th}$ at $V_{DS} = 0.1$ V. Straight lines are linear fits. Values for α (equation 4.1) extracted from the slopes are given next to the corresponding data.

the original model, is obtained for a nominal semiconductor thickness of 14 nm, and a value of $\rho_0 = 3.8\ \Omega\,\mathrm{cm}^2$ is determined. For relatively thick organic semiconductor films ($d = 35$ nm), the $V_{GS} - V_{th}$-dependence changes to an almost direct proportionality with $\alpha = 0.8$ and $\rho_0 = 170\ \Omega\,\mathrm{cm}^2$. On the other hand, for $d = 6$ nm a good agreement is obtained with α = -6.8, but only for a limited range of gate overdrive voltages (0.4 V to 0.9 V).

Apart from a quantification of the V_{GS}-dependence, the physical meaning of most values of α is unclear or limited. However, α = -1 means that the conductivity of the contact scales linearly with the charge density induced in the channel, which is the normal case if the charge carrier concentration in the bulk semiconductor is approximately proportional to the gate bias [114]. The opposite is true for $\alpha = 1$, which denotes a proportionality between the contact resistivity and the charge-carrier concentration.

The source transfer length as a function of the gate overdrive voltage, calculated from equation 2.25, is plotted in figure 4.11b. Again, the drain behaves similarly and is thus not shown. For $d = 6$ nm, ρ_S drops much faster with increasing V_{GS} than R_{sheet}. Consequently, a smaller area is sufficient for charge transfer at high V_{GS}, and thus $L_{T,S}$ decreases with increasing V_{GS} down to very small values of around 1 μm to 2 μm. For $d = 14$ nm, ρ_S and R_{sheet} have a similar functional dependence on V_{GS}. Hence, as a consequence of equation 2.25, the transfer length is roughly constant. For nominal semiconductor thicknesses of 21 nm and 35 nm, the contact resistivity depends only weakly on the gate-

source voltage, or it increases with increasing V_{GS}. However, as usual the sheet resistance decreases with increasing V_{GS} and accordingly, the area for effective charger transfer and therefore the transfer length increase, reaching very high values of more than 100 μm for $d = 35$ nm.

4.3.1 Intrinsic mobility and intrinsic threshold voltage

As was demonstrated in figure 4.9, the channel resistance as a function of the gate-source voltage can be obtained from the GFP measurements. This data can be used to calculate the transfer curves as they would appear without the influence of the contact resistance, using $I_D[V_{GS}] = V_{DS}/R_{ch}[V_{GS}]$. In figure 4.13, these intrinsic transfer curves are compared with the measured ones for $d = 6$ nm and $d = 35$ nm, using data from transistors with $W = 400$ μm, $L = 100$ μm and $L_C = 100$ μm at $V_{DS} = 0.1$ V. In figure 4.9a, it can be seen that for $d = 6$ nm, the contact resistance is comparable to the channel resistance at small gate-source voltages, while it is negligible compared to the channel resistance at large V_{GS}. Consequently, the drain current in the measured curve is suppressed at small V_{GS} due to contact effects, but then approaches the intrinsic curve with increasing gate-source voltage. Thus, the pronounced drop of R_C with increasing V_{GS} results in a steeper slope of the measured transfer curve compared to the slope of the intrinsic curve. Consequently, effective values of the field-effect mobility μ_{eff} and threshold voltage $V_{th,\mathit{eff}}$ extracted directly from the measured transfer curves are larger than the intrinsic parameters.
For $d = 35$ nm, the opposite behavior is observed. The contact resistance is now dominant at large V_{GS}, but smaller than the channel resistance at small gate-source voltages. In this case, the influence of the contact resistance leads to a smaller effective mobility and smaller threshold voltage compared to the intrinsic values.
The fact that the contact resistances can alter the shape of the transfer curve in a quite arbitrary manner is an important observation. Usually, the contact resistance in organic transistors is assumed to be most important at large V_{GS} and to always reduce the effective mobility compared to the intrinsic mobility [49, 133, 134, 156, 161]. From the analysis above it can be concluded that this scenario is not necessarily true and that the effective mobility and threshold voltage can in fact both be either underestimations and overestimations with respect to the intrinsic values.
Effective and intrinsic mobilities and threshold voltages for all nominal semiconductor thicknesses are summarized in figure 4.14 and table 4.2. The intrinsic values show some substrate-to-substrate fluctuations, but no clear correlation with the semiconductor thickness. The intrinsic mobilities are comparable to other high-performance n-channel OTFTs operated in air [32] and similar to the mobilities measured in [90] for PDI-FCN_2 TFTs.

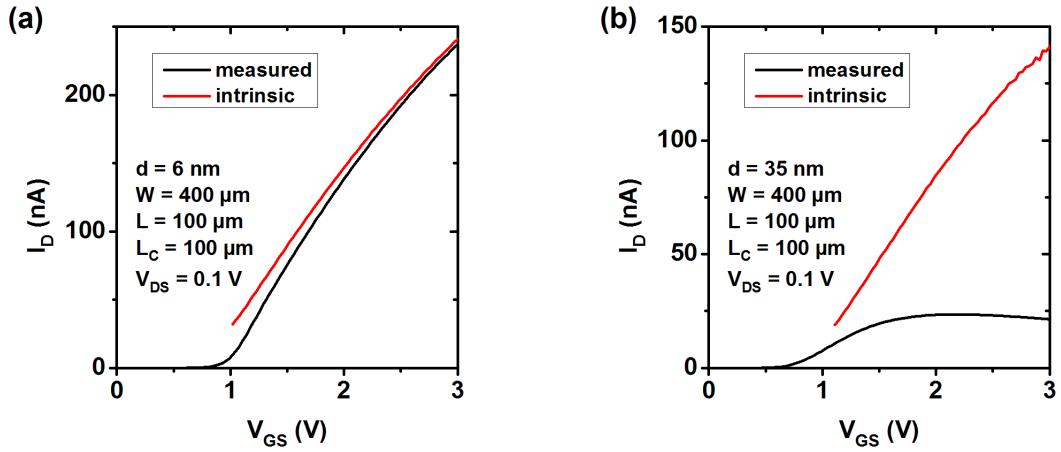


Figure 4.13: **Comparison of measured and intrinsic transfer curves.** (a) At a nominal semiconductor thickness of 6 nm, the contact resistance is large compared to the channel resistance at small V_{GS}, but decreases rapidly with increasing V_{GS}. As a consequence, the measured curve approaches the intrinsic (contact resistance-free) curve at large V_{GS} with a slope that is steeper than that of the intrinsic curve. (b) At a nominal semiconductor thickness of 35 nm, the opposite behavior is observed. The dominance of the contact resistance over the channel resistance increases with increasing V_{GS}, leading to a slope of the measured transfer curve that is smaller than that of the intrinsic curve.

d (nm)	μ_{eff} (cm^2/Vs)	μ_0 (cm^2/Vs)	$V_{th,eff}$ (V)	V_{th} (V)	S (mV/decade)	$R_S W$ (kΩ cm)	$R_D W$ (kΩ cm)
6	0.56	0.51	0.88	0.77	163	1.2	1.4
14	0.28	0.36	0.73	0.74	129	7.2	8.1
21	0.21	0.41	0.81	0.92	149	18.5	18.4
35	0.13	0.34	0.74	0.89	161	58.4	53.3

Table 4.2: **Summary of transistor parameters for different semiconductor thicknesses.** For all transistors, $W = 400$ µm, $L = 100$ µm, $L_C = 100$ µm and $V_{DS} = 0.1$ V. R_S and R_D were extracted at $V_{GS} - V_{th} = 1$ V. All parameters were averaged over four transistors.

Sejfić et al. obtained higher field-effect mobilities in PDI-FCN_2 transistors employing the same SAM as in this work, but using a smoother substrate and higher voltages [102]. For the threshold voltages, the values extracted using the second derivative method ($V_{th,SD}$) are added for comparison. Although this method is believed to be robust against contact effects [68, 69], $V_{th,SD}$ follows the same trend as $V_{th,eff}$ and is just shifted to slightly higher values.

The threshold voltage is an important parameter for the analysis in this work, because many comparisons have to be done at the same gate overdrive voltage to ensure a similar

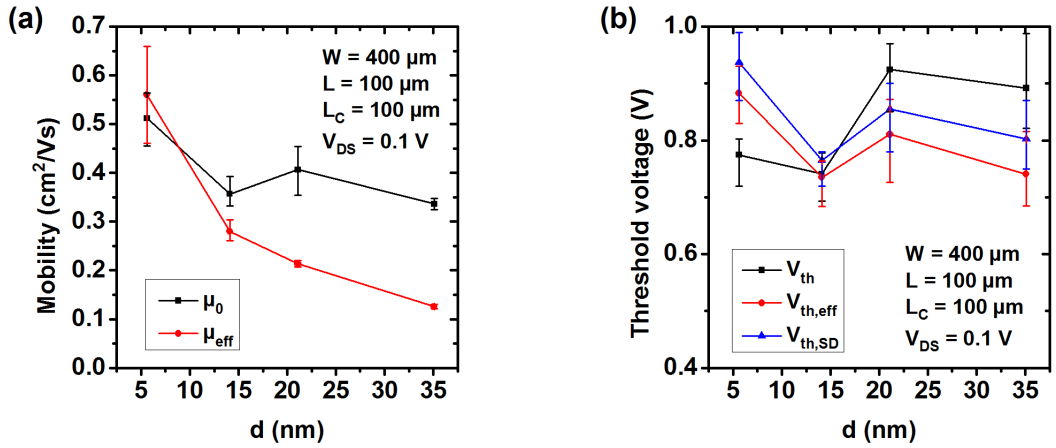


Figure 4.14: **Comparison of effective and intrinsic mobilities and threshold voltages.** Values were averaged using parameters from four transistors with $W = 400$ μm, $L = 100$ μm and $L_C = 100$ μm at $V_{DS} = 0.1$ V, error bars indicate the full range of measured values. (a) Intrinsic (μ_0) and effective (μ_{eff}) mobility as a function of the nominal semiconductor thickness. (b). Intrinsic (V_{th}) and effective ($V_{th,eff}$) threshold voltage and the threshold voltage obtained using the second derivative method ($V_{th,SD}$) as a function of the nominal semiconductor thickness.

induced charge density and therefore meaningful conditions for comparison. Therefore, the term threshold voltage always refers to the intrinsic value throughout this work (unless clearly stated otherwise) and is just abbreviated V_{th} for simplicity.

An interesting consequence of the above-mentioned observations is that the shape of the transfer curve can be quite different for TFTs having different channel lengths. To analyze this in more detail, the contact and sheet resistances obtained from GFP measurements performed on transistors with $L = 100$ μm and $d = 6$ nm was used to calculated the shape of the transfer curve for a transistor with $L = 4$ μm and is compared with experimental data in figure 4.15. The contact length (L_C) is 10 μm in both cases. Apparently, the reduction of the channel length significantly alters the shape of the transfer curve, leading to an increased effective threshold voltage. A good agreement is obtained between the measured and the calculated curve for $L = 4$ μm, confirming that the larger influence of the contact resistance at small channel lengths is responsible for this behavior and that the parameters obtained from GFP measurements are transferable to transistors with small L.

4.3.2 Impact of the four-probe layout

In general, the measured contact resistances obtained from OTFTs fabricated using the four-probe layout A and B are very similar. For a nominal semiconductor thickness of

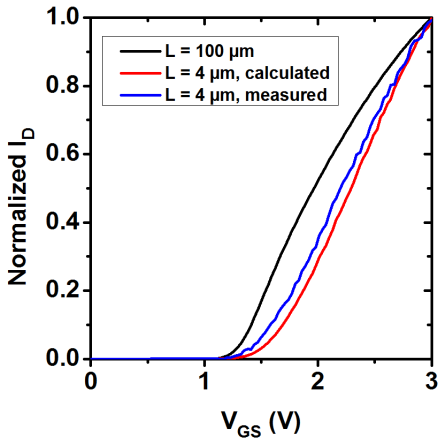


Figure 4.15: **Impact of the channel length on the shape of the transfer curve.** Normalized transfer curves of transistors with a channel length of 4 μm and 100 μm, a contact length of 10 μm and a nominal semiconductor thickness of 6 nm. Using the contact and sheet resistances obtained from GFP measurements on the $L = 100$ μm device, the curve was also calculated for $L = 4$ μm. The greater influence of the contact resistance at small channel lengths significantly alters the shape of the transfer curve, resulting in a larger effective threshold voltage.

6 nm and at large V_{GS}, however, smaller contact resistances are reproducibly obtained for layout B as shown in figure 4.16a. This effect is much weaker for $d = 14$ nm and not visible for larger semiconductor thicknesses. An explanation for this phenomenon can be found by comparing the contact resistance under these conditions with the resistance of the channel over the width of the potential probe (5 μm): if the contact resistance is much larger, the current will almost exclusively flow in the accumulation layer, so that the potential profile in the channel is unaffected by the presence of the potential probes. If, however, the contact resistance is sufficiently small, a part of the drain current flows through the (metallic) potential probe, which reduces the total resistance of that part of the channel and therefore changes the potential profile. It is important to note that the potential probes do not affect the total drain current because they penetrate only slightly into the channel and therefore occupy only a small fraction of the channel. Consequently, the electrical characteristics are practically unaffected by the presence of the potential probes.

Nevertheless, an influence on the extracted contact resistances is still possible, as shown in figure 4.16, where the potential profiles for both layouts are simulated. For the estimation of the potential profiles, $V_{DS} = 0.1$ V and voltage drops (ΔV_S, ΔV_D) for the charge transfer between the metal contact or probe and the organic semiconductor of 0 V, 1 mV and 10 mV are considered. The resistance of the potential probe is assumed to be zero, and

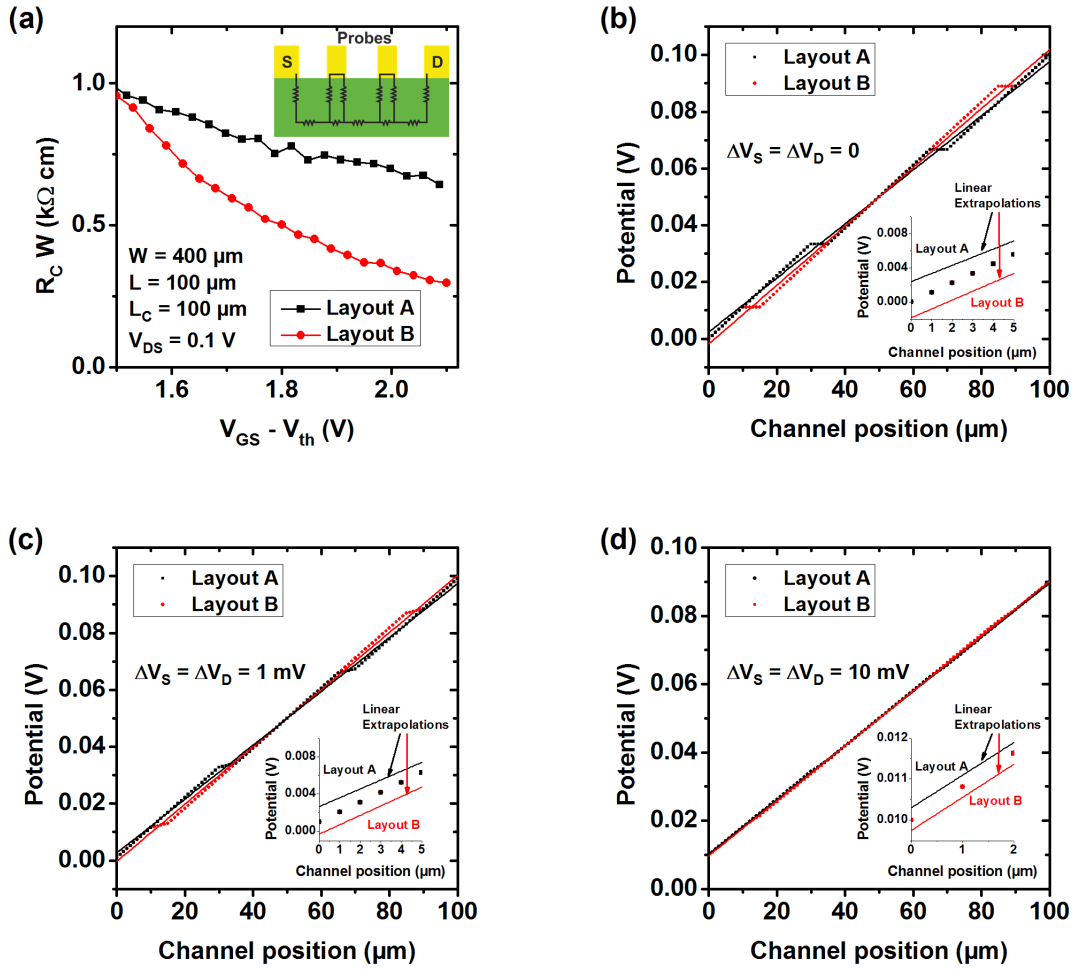


Figure 4.16: **Impact of the GFP layout on the extracted contact resistance.** (a) Comparison of the extracted contact resistance for $d = 6$ nm as a function of the gate overdrive voltage at high V_{GS} for layouts A and B. Inset: schematic of the circuit used for the simulation (not to scale). (b-d) Simulated potential profiles in the channel of OTFTs fabricated in the GFP layout A and B. A drain-source voltage of $V_{DS} = 0.1$ V and voltage drops for charge transfer between metal contact or probe and organic semiconductor of 0 V, 1 mV and 10 mV are considered. Insets: magnification of the region close to the source contact.

the resistance in the region of the probes is calculated assuming two parallel resistances: the resistance of the channel part below the probe and the resistance resulting from the charge transfer into and out of the metallic probe. A schematic of the circuit used for the simulations is shown in the inset of figure 4.16a.
Under these conditions, the potential profile is flat at the probe positions at $\Delta V_S = \Delta V_D = 0$ V, causing errors in the contact resistances extracted from a linear extrapolation of the probe potentials. While layout A overestimates the contact resistances, layout B gives smaller values, consistent with the measurement results described above. When ΔV_S and ΔV_D are increased, the deviations of the potential profile at the probe positions are smaller and the errors in the extracted contact resistances are reduced. However, the errors are still significant at $\Delta V_S = \Delta V_D = 1$ mV, which is roughly the condition for $d = 6$ nm and at large V_{GS}. Therefore, the real R_C values in figure 4.16a and figure 4.10a probably lie in between those measured from layouts A and B. The mean values might be overestimations because they were averaged using three devices having layout A and one having layout B.
Since contact resistances are often quite large in organic transistors, this issue of the GFP technique has not been of great concern in the past, but it should be considered whenever the contact resistances are small compared to the channel resistance below the potential probe contacts. It should be noted that very small contact resistances are also difficult to measure by TLM because the linear extrapolation error in this case can easily be larger than the contact resistance. In other words, both the GFP technique and TLM are somewhat problematic whenever the contact resistance is very small.

4.4 Contact length dependence

As explained in section 2.4.2, the current crowding model predicts that the contact resistance increases when the contact length is reduced to values similar to or smaller than the transfer length. On the other hand, small contact lengths are crucial in order to reduce the parasitic capacitances and to obtain high operation frequencies (section 2.5).
The current crowding model is regularly used for the contact analysis in organic TFTs, but its validity is rarely verified [154]. In addition, the assumption of a resistive transport in the vertical direction has been under debate, and several modifications, for example in the framework of space-charge limited currents (SCLC) [162, 163], have been proposed. We therefore measured the source and drain resistances for a wide range of contact lengths, as shown in figure 4.17. The contact lengths were measured separately for source and drain using an optical microscope. The red lines in both graphs simulate equations 2.23 and 2.24, and the parameters R_{sheet} and ρ_S were taken from the devices with $L_C = 100$ μm. There is a very good agreement between the measured and calculated data for all semiconductor

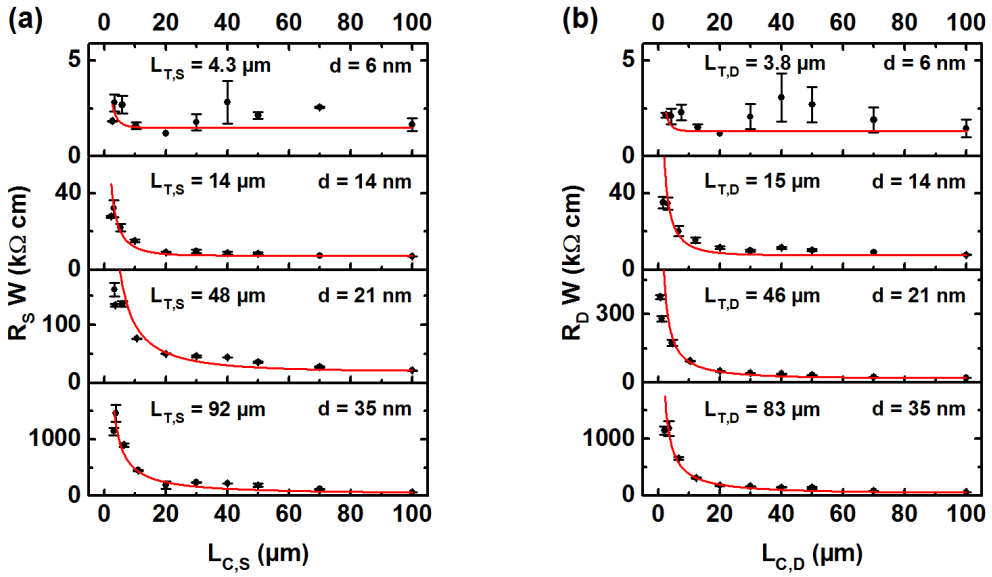


Figure 4.17: **Contact length dependence of the contact resistances.** Width-normalized (a) source and (b) drain resistances as a function of the according contact length for all semiconductor thicknesses at $V_{GS} - V_{th} = 1.0$ V and $V_{DS} = 0.1$ V, measured for transistors with $W = 400$ µm and $L = 100$ µm. The red lines are calculated using equations 2.23 and 2.24, the parameters R_{sheet} and ρ_S were taken from the devices with $L_C = 100$ µm. All contact resistances were measured and averaged from two transistors, one having the GFP layout A and one having layout B. Error bars show the full range of measured values.

thicknesses and for both source and drain resistance, confirming the applicability of the current crowding model for these transistors. Deviations for small contact lengths could conceivably be caused by inaccuracies in the determination of the contact length using the microscope or by a charge flow that is not perpendicular to the surface of the gate electrode, effectively increasing the contact length [154, 164]. Only for $d = 6$ nm, the comparison is complicated due to the parameter variations and the very small transfer length (≈3 µm), but the measurements confirm that the contact resistance does not systematically increase with decreasing contact length as long as the contact length is well above the calculated transfer length.

Equations 2.23 and 2.24 in combination with equation 2.25 predict the source and drain resistances if R_{sheet} and ρ_S are known. The sheet resistance is obtained from the channel resistance, and it is assumed that it is constant over the entire length of the accumulation layer, i.e., in the channel and below the source/drain contacts. As mentioned in section 4.1, several publications describe the possibility of the diffusion of metal atoms from the source or drain contact into the semiconductor layer below, possibly causing structural damage [73, 147–149]. However, the fact that the simulations are able to accurately predict R_S

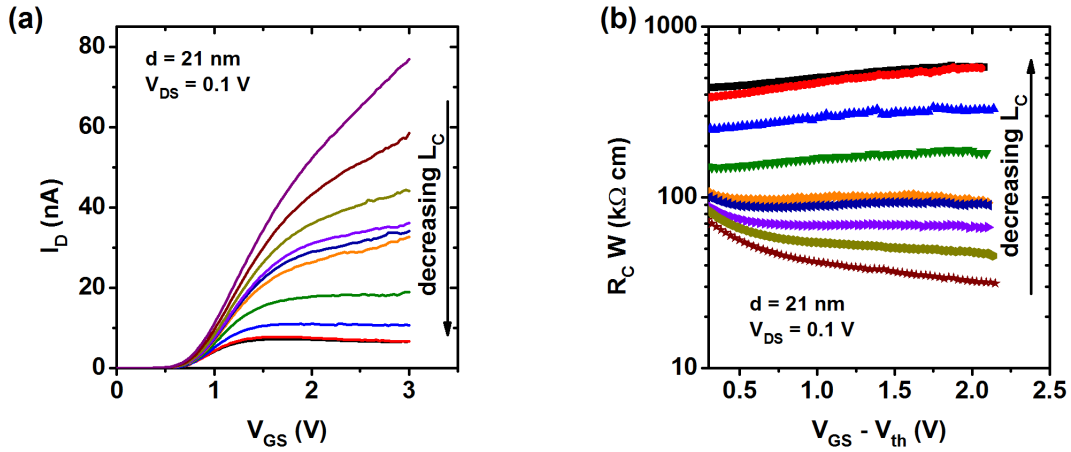


Figure 4.18: **Impact of the contact length on the transfer characteristics for $d = 21$ nm.** (a) Transfer curves at $V_{DS} = 0.1$ V of transistors with contact lengths ranging from 1 μm to 100 μm, showing the occurrence of negative transconductance at small L_C. (b) Corresponding width-normalized contact resistance as a function of the gate overdrive voltage.

and R_D using the channel sheet resistance is a strong indication that the sheet resistance below the source/drain contacts is not affected by the overlying metal layer.
The transfer curves of the transistors with $d = 21$ nm measured at $V_{DS} = 0.1$ V, used for the extraction of the contact resistances in figure 4.17, are shown in figure 4.18a. It can be seen that the drain current decreases monotonically as the contact length is reduced, which is a result of the increased contact resistance as the area available for charge transfer becomes smaller. However, as illustrated in figure 4.18b, the increase in the contact resistance is accompanied by a change of the V_{GS}-dependence of R_C: while the contact resistance decreases with increasing V_{GS} for large contact lengths, the opposite case is true for small L_C, leading to a negative transconductance, similar to what was found for $d = 35$ nm in figure 4.6. To understand this, one has to recall the structure of the contact resistance in a staggered TFT: R_C is composed of the sheet resistance in the accumulation layer and the contact resistivity in the direction perpendicular to the channel. The sheet resistance obviously always decreases with increasing gate-source voltage, and it contributes significantly to R_C at large contact lengths. However, its influence is reduced when the contact length is decreased, and for $L_C << L_T$ the contact resistance is almost entirely determined by the contact resistivity. For $d = 21$ nm, ρ_C exhibits a small increase with increasing V_{GS}, which is of course similar for all contact lengths, but in R_C this is concealed by the gate-source voltage dependence of R_{sheet} at large contact lengths.

4.5 Drain-source voltage dependence of the contact resistances

All results from GFP measurements shown and discussed so far were obtained in the linear regime at a small drain-source voltage of 0.1 V. The GFP technique is usually restricted to this regime, but as discussed in section 3.3.1, this constraint is lifted in the method used in this work.

The V_{DS}-dependence of R_S and R_D was investigated by measuring several transfer curves (including the potential information) over a range of V_{DS}. For the calculation of the potential profile at larger drain-source voltages, $G_{sheet}[V_{Gch}]$ and V_{th} must be known. These parameters are extracted from a transfer curve at $V_{DS} = 0.1$ V, which was measured immediately prior to each measurement at larger V_{DS} in order to account for any bias-stress effects such as threshold voltage shifts (see chapter 5). To verify the procedure, layouts C or D with the additional potential probe in the middle of the channel were employed. The information from this additional probe was not utilized for any calculations; instead, it was used to test the extrapolation technique. This was done by calculating the channel potential also in between the probes (from the probe at channel position L_1 to the one at L_3). This allows a comparison of calculated and measured potentials at the positions L_2 and L_3, where especially the additional data point in the middle (at L_2) enables a verification of the curvature.

Figure 4.19 plots the potential profiles in the case of a nominal semiconductor thickness of 6 nm, calculated for a gate overdrive voltage of 1.0 V at different drain-source voltages. For all V_{DS} the calculated profiles show an excellent agreement with the reference potential in the center of the channel, confirming the applicability of the method.

It is evident from figure 4.19a that the potential profile is indeed almost linear for $V_{GS} - V_{th} >> V_{DS}$, as expected. This implies that the source and drain resistances could be reasonably well determined using a linear approximation of the channel potential (conventional GFP method) under these bias conditions without the need for the accurate potential extrapolation of the more sophisticated GFP method employed in this work. As discussed in the following, this is not necessarily true.

The inset of figure 4.19a shows a magnification of the potential profile $V_{DS} = 0.1$ V and $V_{GS} - V_{th} = 1.0$ V in the channel region close to the drain. It is visible that the accurately calculated potential profile deviates slightly from the linear approximation. Usually, this slight deviation would have almost no influence on the extracted source and drain resistances. However, as the potential drops at the contacts are already quite small, even the small absolute differences lead to quite large relative differences of ΔV_S and ΔV_D, as indicated by the arrows in the inset of figure 4.19a. If the voltage drop at the contacts is larger (which is for example the case for PDI-FCN_2 TFTs with thicker

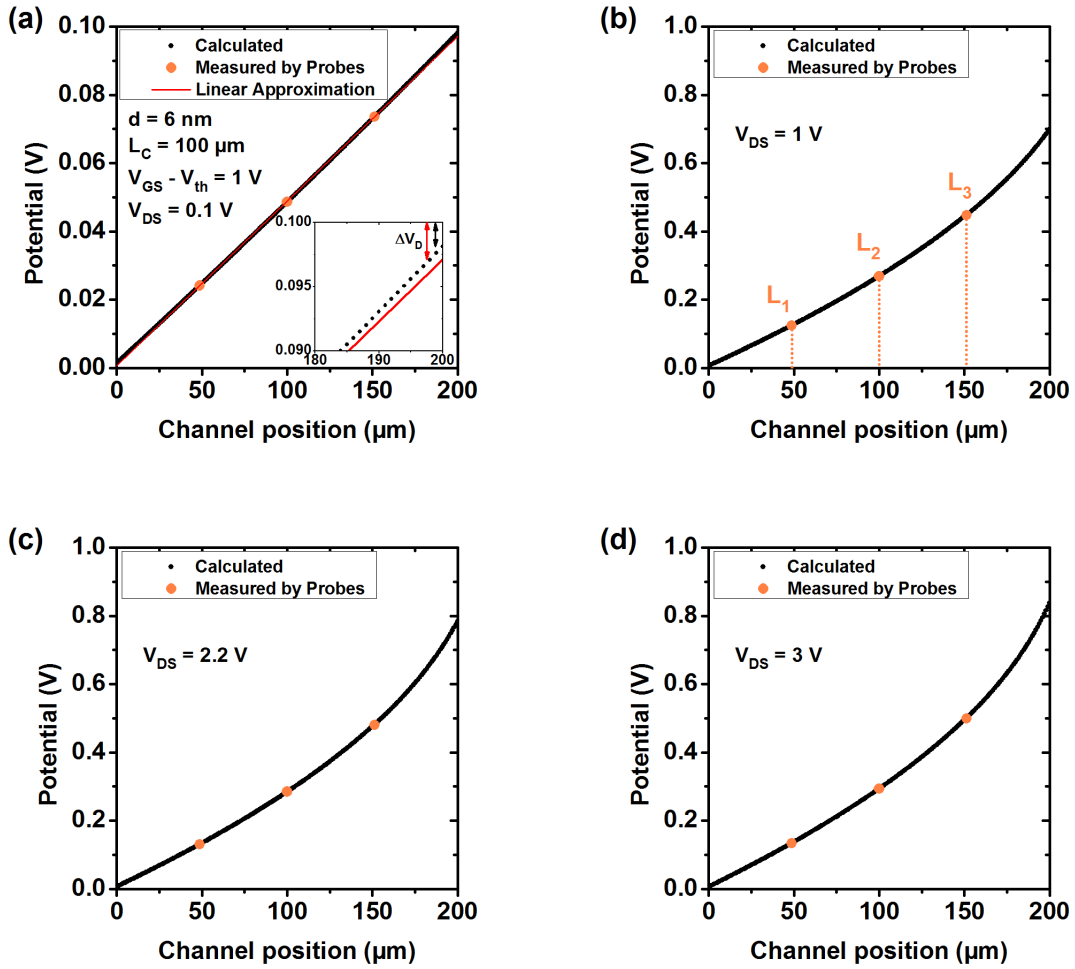


Figure 4.19: **Potential profiles for $d = 6$ nm.** Calculated channel potential profiles at a gate overdrive voltage of 1.0 V and at drain-source voltages of (a) 0.1 V, (b) 1.0 V, (c) 2.2 V and (d) 3.0 V. Potentials measured at the probe positions are shown for comparison. Inset in (a): Magnification of the channel region close to the drain, showing the difference between ΔV_D from the calculated profile and from the linear approximation (arrows).

semiconductor layers), the small deviations from linearity do not play a role anymore, and the linear approximation leads to almost the same source and drain resistances as the more accurate calculated potential profile.

From ΔV_S and ΔV_D, the V_{DS} dependence of the width-normalized source and drain resistances was extracted and plotted using a semilogarithmic scale in figure 4.20a. The source resistance is essentially independent of the drain-source voltage and is therefore ohmic in this voltage range. The drain resistance, on the other hand, increases by more than two orders of magnitude as V_{DS} is increased from 0.1 V to 3.0 V. An explanation for this significant drain-source voltage dependence of R_D may be the gate-field dependence of R_D, because an increase of the drain-source voltage results not only in a larger lateral

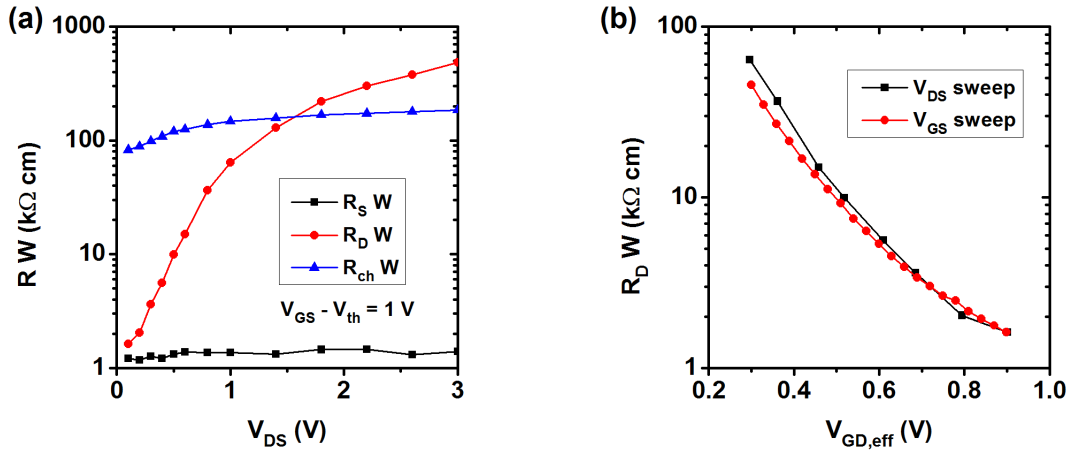


Figure 4.20: **Drain-source voltage dependence of the contact resistances for $d = 6$ nm.** (a) Width-normalized source, drain and channel resistance as a function of the drain-source voltage at $V_{GS} - V_{th} = 1$ V. (b) Width-normalized drain resistance as a function of the effective gate bias at the drain above threshold, obtained from a V_{DS} sweep and from a V_{GS} sweep at $V_{DS} = 0.1$ V.

field, but simultaneously reduces the gate-drain voltage $V_{GD} = V_{GS}$ - V_{DS}. Since the drain resistance was found to decrease strongly with increasing gate field at this nominal semiconductor thickness (6 nm, see figure 4.9a), the reduction of the gate-drain voltage may fully explain the observed increase of the drain resistance for increasing V_{DS}. To verify this, in figure 4.20b the width-normalized drain resistance obtained at different V_{DS} is compared with the one obtained from a single transfer curve measured at $V_{DS} = 0.1$ V. To have a good basis for the comparison, it is useful to define an effective gate-drain voltage above threshold $V_{GD,eff} = V_{GD} - V_{th} + \Delta V_D$, which is corrected for the potential drop across the drain contact. Using $V_{GD,eff}$ as the independent variable ensures that the voltage between the gate and the channel at the drain position is similar in both experiments, so that the drain resistances are compared at a similar number of accumulated charges present under the drain. A good agreement between the two measurements can be seen, indicating that the reduction of the gate field on the drain side and not the larger lateral field is indeed responsible for the observed V_{DS}-dependence of the drain resistance.
An interesting feature in figure 4.19d is the magnitude of the channel potential: even though the transistor is operated under saturation conditions ($V_{DS} = 3$ V), the channel potential is always smaller than the gate overdrive voltage. In other words, a pinch-off in the channel, which is expected at these bias conditions, is not reached due to the large potential drop at the drain contact, as depicted in figure 4.21. This can also be seen in figure 4.20a, where the drain resistance increases much more strongly with increasing V_{DS} than the channel resistance.

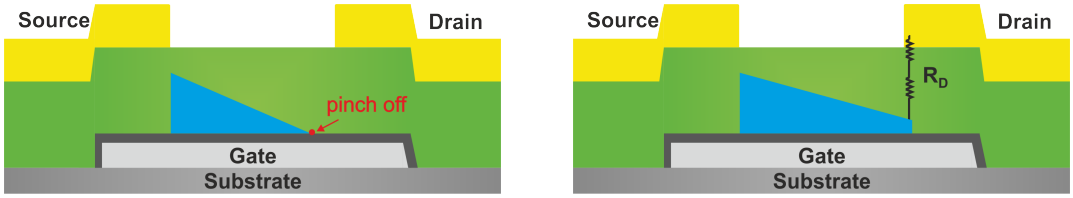


Figure 4.21: **Prevention of channel pinch-off due to the large drain resistance.** Cross sections of a TFT, illustrating the charge-carrier concentration in the channel (blue). Under saturation conditions ($V_{DS} > V_{GS} - V_{th}$), a pinch-off is expected in the channel (left). Due to the pronounced gate-field dependence of the contact resistances, the drain resistance increases strongly with increasing V_{DS} and prevents a pinch-off in the channel.

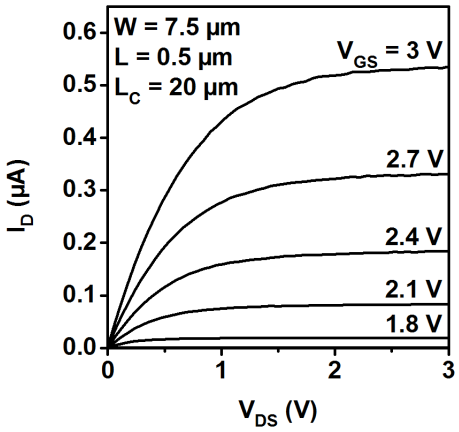


Figure 4.22: **Short-channel output characteristics for $d = 6$ nm.** Output curves for a transistor with $d = 6$ nm and a small channel length of $L = 0.5$ μm, showing excellent linearity at small V_{DS}.

Despite the lack of a pinch-off in the channel, the output characteristics have the expected shape with a pronounced drain current saturation, as was shown in figure 4.7 in section 4.2. A larger drain-source voltage is now compensated by a larger potential drop at the drain contact, as opposed to the channel region. However, the effect of V_{DS} compensation (saturation) is very similar, and since the drain resistance is dominant only at large V_{DS}, the unusual lack of a pinch-off in the channel under saturation conditions has only little influence on the electrical characteristics of the transistors.

The fact that the contacts are ohmic can be confirmed by looking at the output characteristics of a transistor with a very small channel length of $L = 0.5$ μm (figure 4.22). Despite the small channel length, the output curves show excellent linearity of the drain current at small drain-source voltages. Nonlinearities are a highly undesirable feature that is very common in short-channel organic transistors [84, 111, 165, 166].

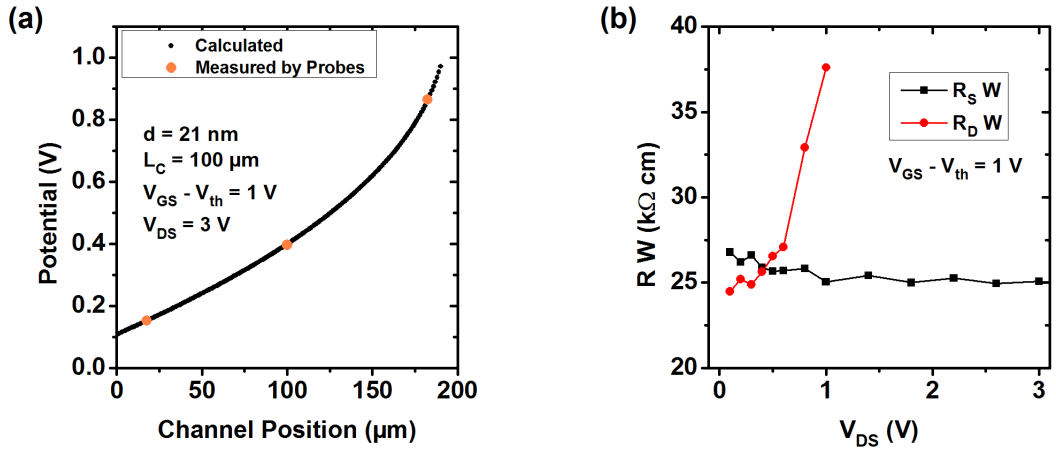


Figure 4.23: **Drain-source voltage dependence of the contact resistances for $d = 21$ nm.** (a) Calculated channel potential profiles at a gate overdrive voltage of 1.0 V and a drain-source voltage of 3.0 V. Potentials measured at the probe positions are shown for comparison. Due to the channel pinch-off, the potential profile close to the drain is not accessible. (b) Width-normalized source and drain resistances as a function of the drain-source voltage at a gate overdrive voltage of 1 V.

When the organic semiconductor is nominally 21 nm thick, the situation is different. The gate-bias dependence of R_D is now much weaker, so that the pinch-off occurs in the channel, as can be seen in the potential profile in figure 4.23a. The dependence of the source and drain resistances on the drain-source voltage for this nominal semiconductor thickness is plotted in figure 4.23b. The increase of R_D with increasing V_{DS} up to the pinch-off is much less pronounced in this case and the source resistance exhibits a slight decrease by about 7 % over the V_{DS} range from 0.1 V to 3.0 V.

The fact that the source resistance decreases with increasing V_{DS} indicates a non-ohmic behavior of the contact. This becomes clear in the current-voltage plots of the source contact, where the drain current is shown as a function of the voltage drop across the source contact for different contact lengths. Similar to $V_{GD,eff}$, an effective gate-source voltage above threshold $V_{GS,eff} = V_{GS} - V_{th} - \Delta V_S$ is defined, and all data points are at $V_{GS,eff} = 1$ V to have similar charge-carrier concentrations in the accumulation layer below the source.

The graph has a log-log scale, accordingly, if the relation $I_D \propto \Delta V_S^m$ is valid, the data are on a straight line and the slope gives the exponent m. For a contact length of 100 μm, m is close to unity at small ΔV_S, implying an ohmic behavior. However, at relatively large ΔV_S, the slope increases to approximately $m = 1.3$. This effect becomes more and more pronounced as the contact length is decreased, reaching an exponent of around 2.3 for very small L_C. However, in all cases, the drain current is linear with respect to the

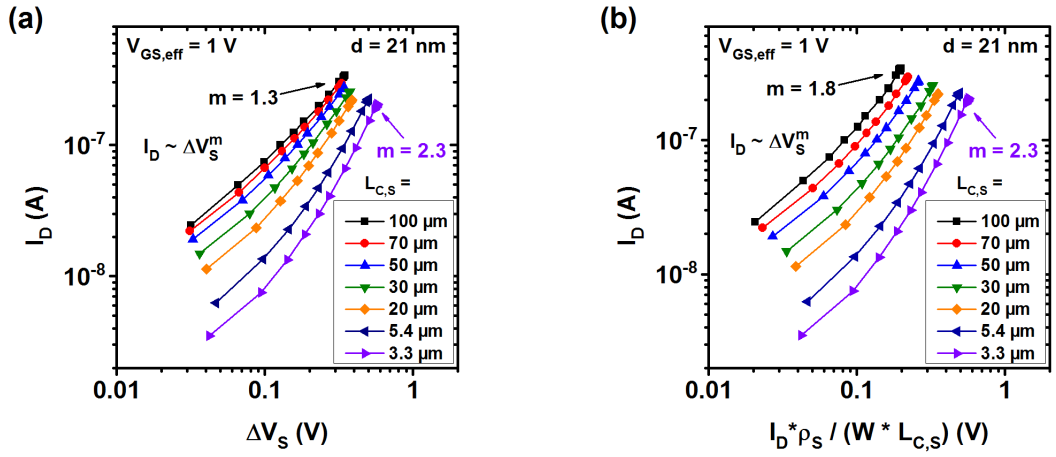


Figure 4.24: **Influence of the contact length on the current-voltage characteristics of the contacts.** The nominal semiconductor thickness is 21 nm and the data is shown in a log-log-plot for an effective gate-source voltage above threshold of 1 V. (a) Drain current as a function of the voltage drop across the source contact. At small ΔV_S, the current-voltage relation is almost linear, but becomes superlinear at larger voltage drops. The exponent m increases for smaller contact lengths. (b) Same data, but plotted as a function of the approximate voltage drop in the vertical direction. The difference in the values of m is decreased.

voltage across the source contact at small ΔV_S.

The observed dependence of the maximum slope on the contact length is again a consequence of the current crowding. Just like the V_{GS}-dependence of R_C, which was found to be different for different contact lengths (figure 4.18), the L_C dependence of the degree of nonlinearity in the contacts' current-voltage characteristics is caused by the different relative contributions of the sheet resistance at different contact lengths. For large $L_{C,S}$, R_{sheet} accounts for a larger fraction of the source resistance, and since R_{sheet} is ohmic, this reduces the nonlinearity of R_S.

Since the sheet resistance is ohmic and quite similar for all semiconductor thicknesses, the more interesting physical quantity is the source contact resistivity, i.e., the vertical component of the source resistance. To analyze the current-voltage characteristics corresponding to ρ_S, equation 2.23 was used to extract the source contact resistivity numerically. The voltage drop in the vertical direction can now be estimated as $I_D \cdot \rho_S/(W \cdot L_{C,S})$, the corresponding current-voltage curves are shown in figure 4.24b. It can be seen that the maximum slope in the log-log plot is similar to the previous case when looking at small contact lengths. The reason is that if the contact length is small compared to the transfer length, the resistor network is not effective, so the current flow is mainly in the vertical direction and R_S is already mostly determined by the contact resistivity (see equation 2.27).

For a contact length of 100 μm, however, the exponent m increases significantly to 1.8 (compared to 1.3), being much closer to, but still smaller than what is measured for small contact lengths. The reason is the inhomogeneous potential in the accumulation layer below the contacts in connection with the non-ohmic properties of the contact for that semiconductor thickness. Since ρ_S depends on the potential difference between the accumulation layer and the source contact and this potential difference decreases with increasing lateral distance from the source contact edge, ρ_S is not constant along the length of the contact, even for steady bias conditions. Instead, ρ_S increases when going away from the contact edge, and the calculated ρ_S can be thought of as an average of the contact resistivities present in the source contact, leading to a smaller exponent in the current-voltage characteristics.
In transistors having a contact length that is much smaller than the transfer length this is not a problem, because the potential in the accumulation layer below the contacts cannot vary considerably. Consequently, they are the best choice for the analysis of the physically important vertical component of the contact resistance.
The discussion above implies that the current crowding model with ohmic resistors (equation 2.23) cannot be simply used to calculate the contact-length dependence of the source resistance in the case of non-ohmic contacts, which were observed in PDI-FCN_2 transistors with relatively thick semiconductor layers and for sufficiently large voltage drops across the contact region. This is due to the contact-length dependence of the contact resistivity, for which two reasons are responsible. First, ρ_S can vary within the same transistor due to the inhomogeneous potential in the accumulation layer below the source, a behavior that is controlled by the contact length. Second, the contact length affects the magnitude of the source resistance, which in turn changes the voltage drop across the contact region and thereby the contact resistivity.
The consequences of these effects are illustrated in figure 4.25, where the width-normalized source resistance is plotted as a function of the contact length for different drain source voltages at $V_{GS,eff} = 1$ V. In addition, continuous lines show the relations calculated using equation 2.23; the parameters R_{sheet} and ρ_S were taken from the transistor with $L_C = 100$ μm. The nominal semiconductor thickness is 21 nm. The case of $V_{DS} = 0.1$ V is already known from section 4.4, and the experimental data reasonably agrees with the theoretical prediction. However, as the drain-source voltage is increased, the contact resistivity decreases. Due to the reasons explained above, this decrease is more pronounced and has a greater impact on the source resistance at smaller contact lengths. Consequently, the increase of the source resistance with decreasing contact length is reduced at larger V_{DS} and is weaker than what would be expected from equation 2.23 with a constant contact resistivity.
Having identified transistors with $L_C << L_T$ as most useful for the analysis of the con-

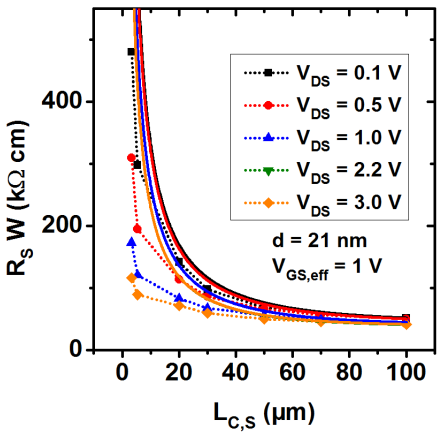


Figure 4.25: **Impact of the drain-source voltage on the contact-length dependence of the source resistance.** Width-normalized source contact resistance as a function of the contact length for different drain-source voltages at $V_{GS,eff} = 1$ V for $d = 21$ nm. Due to saturation, the graphs for $V_{DS} = 2.2$ V and $V_{DS} = 3.0$ V are almost identical. For comparison, the continuous lines show the relations calculated using equation 2.23, the parameters R_{sheet} and ρ_S were taken from the transistor with $L_C = 100$ μm.

tacts' current-voltage characteristics, a transistor with a source contact length of 2.4 μm and a drain contact length of 2.6 μm was chosen for a more detailed investigation. Figure 4.26a shows the measured drain current as a function of the voltage drop across the source or drain region at $V_{GS,eff} = V_{GD,eff} = 1$ V, again for a nominal semiconductor thickness of 21 nm. The measurements were performed in a cryostat under UHV conditions at a temperature of 90 K. Straight fit lines indicate the different slopes (exponents) at small and large voltages. There seems to be a crossover between ohmic and non-ohmic behavior at a voltage V_{CO} of approximately 0.2 V. It is obvious that the drain contact has the same properties as the source contact and the curves are just slightly shifted. The estimated maximum exponent m is approximately 2.6.

At room temperature and at $V_{GS,eff} = V_{GD,eff} = 1$ V, the range of available data barely extends beyond the crossover voltage, complicating a meaningful analysis. However, curves at different $V_{GS,eff}$ are parallel (as demonstrated below). Therefore, the ΔV_S range can be extended by using a higher $V_{GS,eff}$ without affecting m. The corresponding I-V characteristics for both room temperature and 90 K at $V_{GS,eff} = 1.4$ V are shown in figure 4.26b. Only the behavior of the source contact is shown, because at a high $V_{GD,eff}$ of 1.4 V the potential drop at the drain is barely accessible. At room temperature, an exponent of $m = 2$ is extracted. This is smaller than the low-temperature value and also smaller than the value measured in air ($m = 2.4$). For $T = 90$ K, the extended range results in a small correction of m to 2.8.

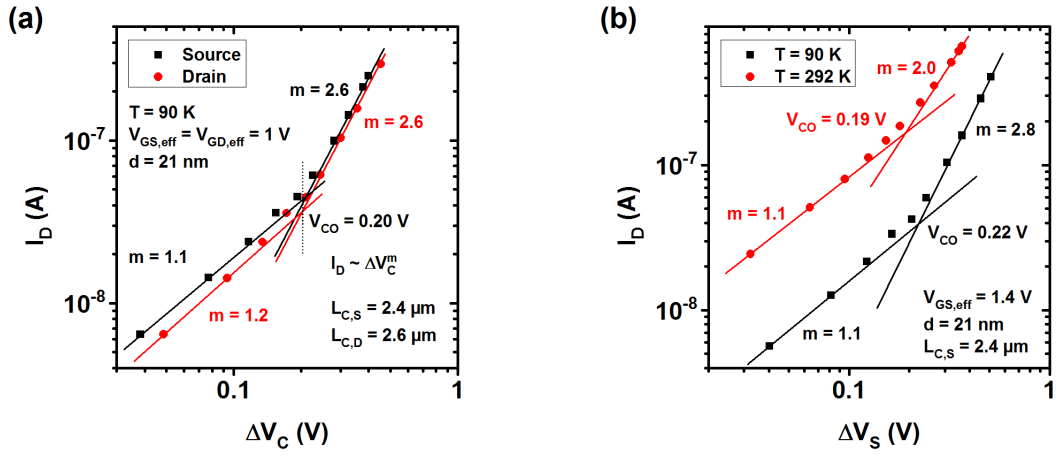


Figure 4.26: **Current-voltage characteristics of the contacts measured at different temperatures.** Log-log plots of the drain current as a function of the voltage drop across the contact for a transistor having $d = 21$ nm, $L_{C,S} = 2.4$ μm and $L_{C,D} = 2.6$ μm. Straight lines indicate the exponents at small and large voltages. The measurements were performed in an ultra-high vacuum. (a) Curves for both source and drain measured at $V_{GS,eff} = V_{GD,eff} = 1$ V and 90 K (b) I-V curves for the source contact at $V_{GS,eff} = 1.4$ V at room temperature and at 90 K.

So far, the current-voltage characteristics of the contact were mainly considered at $V_{GS,eff} = V_{GD,eff} = 1$ V. Figure 4.27a shows the drain current as a function of ΔV_S at different values of $V_{GS,eff}$ for a transistor having $d = 21$ nm, $L_{C,S} = 2.4$ μm and $L_{C,D} = 2.6$ μm. It is clearly visible that the curves are parallel and that the exponent m is not influenced by $V_{GS,eff}$. In addition, when increasing $V_{GS,eff}$ at a constant ΔV_S, the current decreases. This increase of the source (or drain) resistance with increasing gate voltage for transistors with a relatively thick organic semiconductor layer was already discussed for $V_{DS} = 0.1$ V and is again shown in figure 4.27b. However, due to the superlinear relation between I_D and ΔV_S at high ΔV_S, an interesting change in the apparent behavior occurs: the source resistance decreases with increasing $V_{GS,eff}$ at a drain-source voltage of 3.0 V. This can be explained as follows: at $V_{DS} = 3.0$ V, the transistor operates under saturation conditions and the channel is pinched off on the drain side. Hence, an increase of the gate-source voltage leads to a significant reduction of the channel resistance, and accordingly, the voltage drop across the source region increases. However, at larger ΔV_S, R_S is smaller, and this leads to the observed decrease of the source resistance with increasing $V_{GS,eff}$.

4.5.1 Origin of the nonlinearities

Nonlinear current-voltage characteristics in organic thin-film transistors are frequently reported in the literature, but a detailed analysis and experimentally confirmed explanations

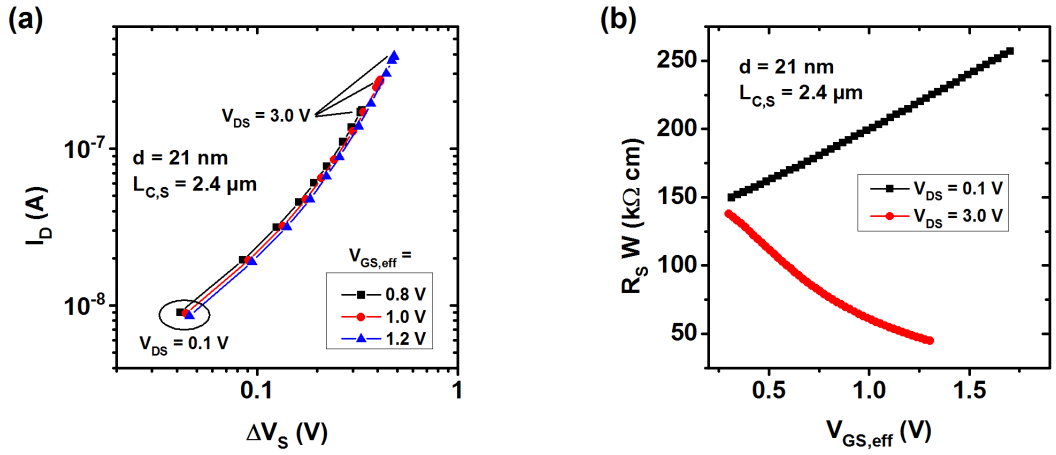


Figure 4.27: **Influence of the drain-source voltage on the gate-voltage dependence of the contact resistance for $d = 21$ nm.** (a) Current-voltage characteristics of the source contact for several effective gate-source voltages above threshold. (b) Width-normalized source resistance as a function of the effective gate-source voltage above threshold for $V_{DS} = 0.1$ V and $V_{DS} = 3.0$ V.

are rare. However, the extensive data reported above provide the basis for a well-founded discussion of possible effects.

First of all, the GFP analysis clearly shows that the nonlinearity is caused in the region at or below the source/drain contacts and is unrelated to the transistor channel. Often, nonlinear contact effects in organic transistors are associated with Schottky barriers at the metal/organic semiconductor interface [72, 167]. Assuming identical Schottky barriers at the source and the drain interfaces, the reverse-biased barrier at the source would limit the current flow in the transistor. The voltage-dependence of the current would be $\ln(I) \propto \sqrt{V}$ for the source (due to the Schottky effect) and $\ln(I) \propto V$ for the forward-biased drain [72]. However, as can be seen for example in figure 4.26a, the contact resistances at source and drain are very similar in magnitude and their voltage-dependence (which does not follow either of the two above-mentioned relations), so Schottky barriers can be safely ruled out as the origin of the observed nonlinearities. In the case of a phonon-assisted tunneling process, the conductivity would exponentially increase with the square of the voltage drop, $\ln(I/V) \propto V^2$ [58], but the experimental data do not follow this relation.

The nonlinearities are observed only for a nominal semiconductor thickness of at least 21 nm, but not for $d = 6$ nm. It is therefore reasonable to search for their cause in the bulk of the semiconductor where the charge has to flow from the metal/semiconductor interface to the accumulation layer or vice versa. The free charge-carrier density $n[y]$ in the bulk semiconductor is significantly smaller than in the accumulation layer and decreases

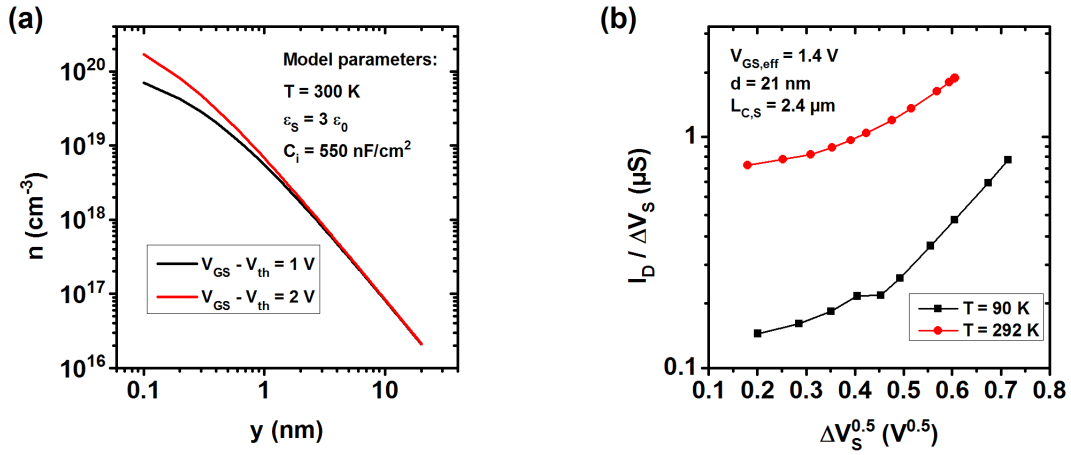


Figure 4.28: **Computed charge-carrier density function and verification of the Poole-Frenkel effect.** (a) Charge-carrier density as a function of the vertical distance from the gate dielectric/organic semiconductor interface calculated from equation 4.2. Model parameters are given in the graph. (b) Semilogarithmic plot of the source conductance as a function of the square root of the voltage drop at the source contact at $V_{GS,eff} = 1.4$ V.

with increasing distance y from the gate dielectric/organic semiconductor interface. $n[y]$ can be estimated by solving Poisson's equation; an approximate solution is given by [63]:

$$n[y] = \frac{C_i(V_{GS} - V_{th})}{2k_B T \varepsilon_S} \left(1 + \frac{y}{\sqrt{2}L_D}\right)^{-2}, \tag{4.2}$$

where ε_S is the permittivity of the organic semiconductor and L_D is the Debye length, which can be viewed as a rough estimate of the accumulation layer thickness [63] and which is given by:

$$L_D = \frac{\sqrt{2}k_B T \varepsilon_S}{eC_i(V_{GS} - V_{th})}. \tag{4.3}$$

The computed $n[y]$ is plotted in figure 4.28a, where the model parameters $T = 300$ K, $\varepsilon_S = 3\varepsilon_0$ with the vacuum permittivity ε_0 (typical value for an organic semiconductor [57]) and $C_i = 550$ nF/cm^2 have been used. Gate overdrive voltages of 1 V and 2 V were considered. Far away from the gate dielectric/organic semiconductor interface, the influence of the gate-source voltage on the charge-carrier density is small. Due to the molecular layer nature of the semiconductor, the function $n[y]$ is in reality not continuous, but probably resembles a staircase shape [63].

A well-known observation in semiconductors with a small free charge-carrier density and a small interface resistance at the injecting contact is the occurrence of space-charge-limited conduction. In staggered OTFTs, the existence of an SCLC regime in the contact region

has been treated theoretically [162, 163, 168], but without experimental proof. The shape of I-V curves in the SCLC regime (section 2.2.1) is similar to those shown in figure 4.26b: at low voltages, the current follows Ohm's law, but changes to a power-law behavior with an exponent $\geq$2 at higher voltages. In the simple picture of a trap-free SCLC, the crossover voltage that separates these two regions is given by [61]:

$$V_{CO} = \frac{4en_0d^2}{3\varepsilon_S}. \tag{4.4}$$

Using values of $d = 21$ nm and $\varepsilon_S = 3\varepsilon_0$, the free charge-carrier density n_0 necessary for a crossover voltage of around $V_{CO} = 0.2$ V can be estimated using equation 4.4 to around $5 \cdot 10^{16}$ cm^{-3}. Although n_0 is only a rough estimate, the good agreement with the charge-carrier densities calculated in the bulk semiconductor shown in figure 4.28a confirms the possibility of SCLC in the transistors investigated in this work. For $d = 6$ nm, the gate-induced charge-carrier density is greater than 10^{17} cm^{-3} throughout the entire thickness of the semiconductor, for which the estimated crossover voltage is in the order of 0.1 V. The fact that the measured voltage drop across the source contact was always smaller than 0.01 V for this nominal semiconductor thickness explains that in this case no nonlinear behavior is observed.

The charge-carrier mobility in the direction perpendicular to the dielectric interface can be estimated from the Mott-Gurney law (equation 2.10) to 10^{-5} cm^2/Vs, which is around four orders of magnitude smaller than the lateral field-effect mobility measured in the transistor channel. However, such a drastic difference is reasonable, since the upright-standing molecular orientation leads to a significantly smaller overlap of the molecular orbitals in the vertical direction. One reason for this smaller overlap are the long fluoroalkyl chains of the PDI-FCN$_2$ molecule.

While for room temperature and UHV conditions a maximum exponent of $m = 2$ was observed, which corresponds to the presence of no or shallow traps in the SCLC theory, m was larger when the measurements were performed in air or at cryogenic temperatures. Exponents larger than 2 can be explained with a distribution of trap states. While the presence of ambient molecules is likely responsible for the formation of deep trap states (see also chapter 5), equation 2.11 is able to explain the increase of m with decreasing temperature. From $m \approx 2.8$ at 90 K, the characteristic temperature T_C can be estimated to about 160 K. This is also consistent with $m = 2$ at room temperature, since for $T > T_C$, the situation simplifies to the shallow-trapping case with a power-law slope of 2 [61].

An alternative explanation for the nonlinearities would be the Poole-Frenkel effect. The predicted dependence of the current on the voltage is given by equation 2.8, meaning that a plot of $\ln(I/V)$ as a function of $\sqrt{V}$ should yield a straight line. Figure 4.28b shows such a plot for the source contact at room temperature and 90 K. The graph depicts

two regimes: a slowly increasing conductivity at low ΔV_S and a region that potentially follows the predicted Poole-Frenkel behavior at high ΔV_S. Poole-Frenkel behavior has been reported to be observable for electric fields in excess of 10^4 V/cm [169], which would be in rough agreement with a field strength of around 10^5 V/cm for a voltage of 0.2 V and a semiconductor thickness of 21 nm. However, the Poole-Frenkel parameters β calculated from equation 2.9 deviate by more than one order of magnitude from the values extracted from the slopes in figure 4.28b at high ΔV_S using $E = V/d$. In addition, the extracted values of β do not scale with the temperature as predicted by equation 2.9.
These contradictions raise doubts that the Poole-Frenkel effect alone can explain the nonlinear current-voltage characteristics of the contact. It is, however, possible that a space-charge-limited current is flowing in the bulk semiconductor where the charge-carrier mobility is modified by the Poole-Frenkel effect. Although for this combination no analytical solution exists that describes the dependence of the current on the voltage, an approximate solution for the trap-free case is given by [59]:

$$J \propto V^2 \exp\left(\frac{\gamma\sqrt{V}}{T}\right), \tag{4.5}$$

with a voltage-independent parameter γ. However, due to the limited data at voltages above V_{CO}, no clear statement can be made regarding the question whether a combination of SCLC and Poole-Frenkel effect yields a better description of the experimental data than either of the two effects alone.

4.6 Temperature dependence

Measuring the influence of the temperature on the behavior of physical quantities can provide considerable insight into the physical properties of a system. Particularly, different charge transport mechanisms are often characterized by a distinct temperature dependence of the resistance and can be identified or ruled out by measuring this dependence. In addition, the extent of the temperature dependence can also allow one to deduce information about relative energetic positions, trap distributions and energy barriers [134]. Electrical characterization at various temperatures was performed in a UHV environment and using LN_2 cooling. Although the PEN substrate is only 125 μm thick, great care was taken to ensure a thermal equilibrium during the measurement, because the thermal conductivity of PEN is quite small (≈0.1 W/(m·K), [170]). Therefore, after reaching a target temperature, electrical measurements were repeatedly performed for several minutes until the characteristics were stable. In addition, the characterization was done both during cooling and during subsequent heating to allow a comparison of the results.
First, measurements on a transistor with a nominal semiconductor thickness of 6 nm

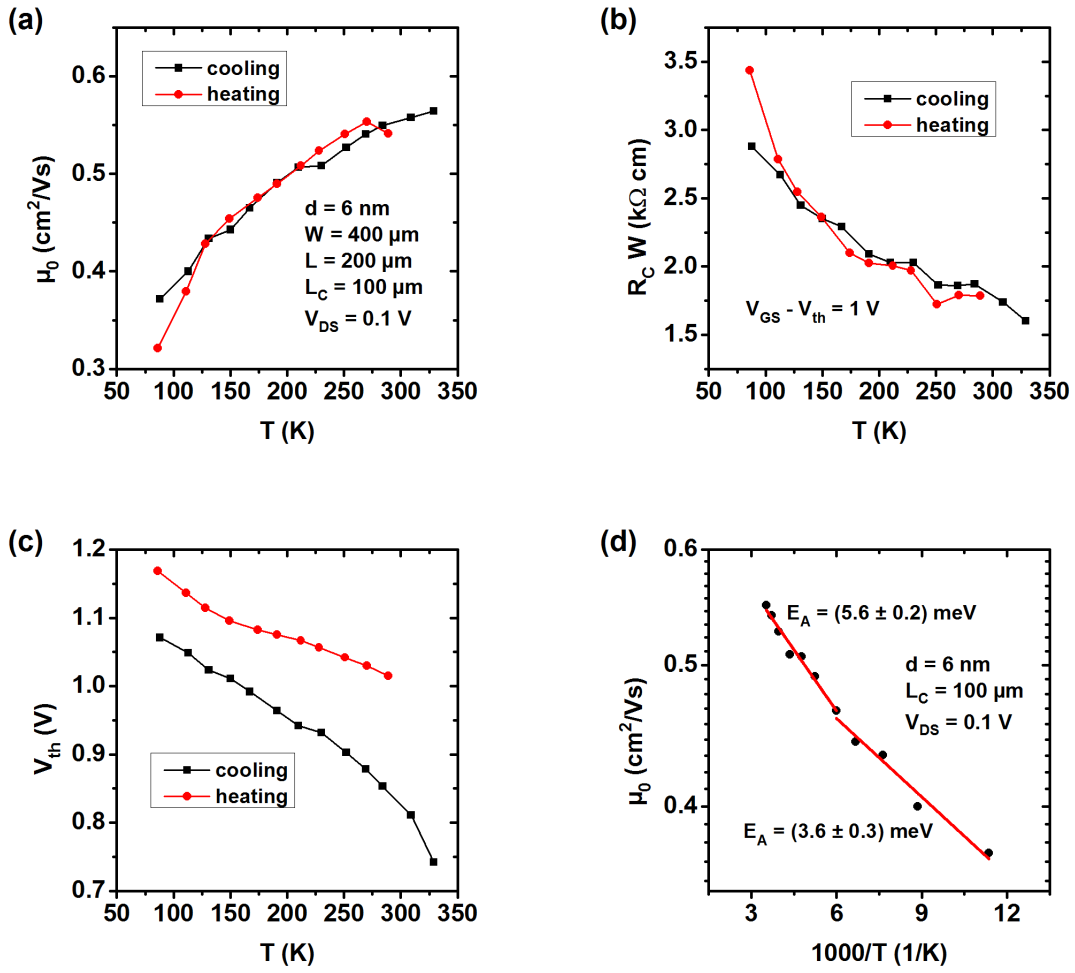


Figure 4.29: **Temperature dependence of transistor parameters for $d = 6$ nm.** (a) Intrinsic mobility, (b) width-normalized contact resistance and (c) threshold voltage as a function of the temperature at $V_{DS} = 0.1$ V for both cooling and heating. (d) Arrhenius plot of the intrinsic mobility, obtained during cooling. Straight lines are local exponential fits, the resulting activation energies are given next to the corresponding region.

will be discussed. To begin with, figures 4.29a and 4.29b plot the intrinsic mobility and the width-normalized contact resistance as a function of the temperature. Most values measured during cooling and heating agree very well, confirming the validity of the data and the stability of these parameters. Only for the lowest temperature there is a noticeable divergence between the data. This is possibly due to the fact that this temperature was held for some time in order to perform additional measurements before the temperature was raised again, and it is conceivable that these additional measurements caused bias-stress effects in the transistor. Indeed, a shift of the threshold voltage occurred between the end of the cooling sequence and the beginning of the heating sequence (figure 4.29c). Although the sensitivity to bias stress in vacuum and at room temperature was found to be very small (see section 5.2.2), this might be different at low temperatures, but this was not investigated more closely in order to not impair the temperature-dependent measurements. The following discussion is based on parameters that were extracted during the cooling sequence.

Both the intrinsic mobility and the contact resistance improve as the temperature is increased. The threshold voltage shifts towards more positive values as the temperature is lowered, probably because a larger fraction of the charge carriers is trapped in deep states due to the lower thermal energy.

Many thermally activated processes have an exponential dependence on the inverse temperature ($\propto \exp\left(-E_A/(k_B T)\right)$), and plotting the logarithm of the parameter under investigation as a function of the inverse temperature is then useful to obtain the corresponding activation energy E_A. Figure 4.29d shows such an Arrhenius plot of the intrinsic mobility. The resulting curve is not linear over the entire temperature range, but agrees reasonably well with linear fits applied separately to the low- and high-temperature regions with a transition at around 170 K. The resulting activation energy is about 3.6 meV at high temperatures and about 5.6 meV at low temperatures. These activation energies are quite small compared to literature values for organic TFTs, which are usually in the range of tens to hundreds of meV [49, 171–173].

The Arrhenius plot for the width-normalized source and drain resistance is shown in figure 4.30a. The same behavior with two different activation energies at high and low temperatures is visible, but the activation energies are now in the range of 3.5 meV to 9.4 meV, thus being slightly larger than those of the intrinsic mobility. The source and drain resistances show the same trend and exhibit very similar activation energies. As expected, the calculated activation energies of the source and drain contact resistivities are larger than those of the contact resistances due to the lack of an influence of the sheet resistance, as shown in figure 4.30b, but the general shape of the curves is unchanged.

The variable temperature measurements discussed so far were performed on a substrate with a nominal semiconductor thickness of 6 nm. The Arrhenius plots of the intrinsic mo-

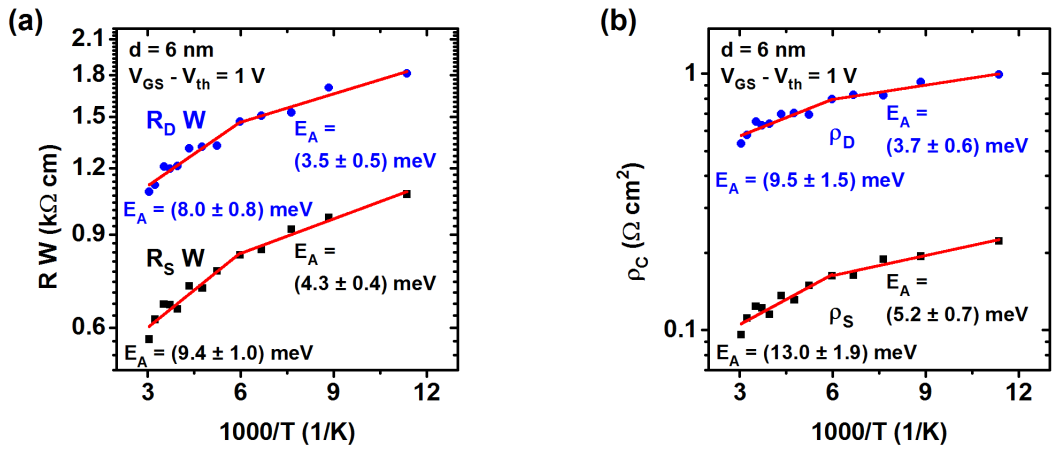


Figure 4.30: **Temperature dependence of the contact parameters for $d = 6$ nm.** Arrhenius plots of (a) the width-normalized source and drain resistances and (b) the source and drain contact resistivities. Straight lines are local exponential fits, and the resulting activation energies are given next to the corresponding region.

bility and the width-normalized source and drain resistances for $d = 21$ nm are presented in figure 4.31. As discussed in section 4.5, the behavior of the contact resistances directly reflects that of the contact resistivities, due to the small contact lengths of $L_{C,S} = 2.4$ μm and $L_{C,D} = 2.6$ μm. Again, a good agreement with an exponential behavior is observed for all parameters when treating high- and low-temperature regions separately. However, while the activation energies extracted for the intrinsic mobility are comparable to those obtained for $d = 6$ nm, the source and drain resistances exhibit a much stronger temperature dependence with activation energies that are approximately five times larger than those measured for a nominal semiconductor thickness of 6 nm.

4.6.1 Charge-transport mechanisms

The transistor properties deduced and discussed previously in this chapter provide insight into the charge-transport mechanisms in these TFTs. First, it is obvious that the intrinsic mobility is thermally activated over the entire temperature range and that there is no signature of band-like transport, as expected for a TFT. Some of the microscopy images of the semiconductor morphology (section 4.1) show island-like structures that resemble a well-ordered polycrystalline film, which is typical for vapor-deposited layers of small molecules [31]. In well-ordered organic semiconductor films, charge transport is often successfully described by the MTR model [43]. However, the relatively rough surface of the PEN substrate may induce sufficient disorder to invalidate the assumptions underlying the MTR model, and therefore the VRH model by Vissenberg and Matters, which is often

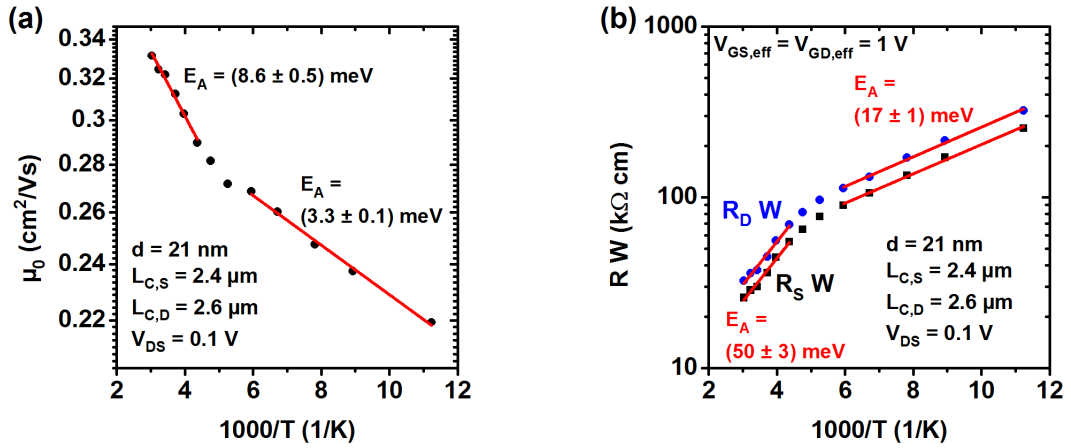


Figure 4.31: **Temperature dependence of transistor parameters for $d = 21$ nm.** Arrhenius plots of (a) the intrinsic mobility and (b) the width-normalized source and drain resistances of a transistor having $L_{C,S} = 2.4$ μm and $L_{C,D} = 2.6$ μm. Straight lines are local exponential fits, and the resulting activation energies are given next to the corresponding region.

used in the context of amorphous organic materials, will also be examined. In addition, the potentially polycrystalline nature of the film justifies the consideration of grain boundary models.

The MTR model, most grain boundary models and the VRH model by Vissenberg and Matters predict a temperature dependence of the intrinsic mobility that results in a straight (or almost straight) line in an Arrhenius plot for a constant charge-carrier density. Although such a behavior was not observed over the complete temperature range, it is visible when examining high- and low-temperature regions separately (figure 4.29d and 4.31b). Within the framework of grain boundary models the temperature regions with different activation energies can be explained by a change of the dominant site-to-site charge-transport mechanism within the grain boundary (e.g. from thermionic emission to thermally activated tunneling) [49, 57]. In films of polycrystalline polymers, a similar behavior was explained by assuming low-mobility states within the band-tail distribution [174]. Another explanation are temperature-induced structural changes in the molecular layer: different polymorphs in crystals of a molecule related to PDI-FCN_2 were recently observed [175].

Although the observed temperature dependence of the intrinsic mobility deviates from a normal Arrhenius-like behavior, it is in principle consistent with most common OTFT charge-transport models that assume such a behavior. Another important prediction of these models is the charge-carrier density dependence of the (differential) intrinsic mobility. Although for different reasons, both the MTR model and the VRH model by Vissenberg and Matters as well as grain boundary models predict an increase of the in-

trinsic mobility with increasing gate overdrive voltage, and the extent of this increase should be more pronounced at lower temperatures. However, for the transistors investigated in this work, no such increase was observed. In contrast, the intrinsic mobility always decreased slightly at large V_{GS}, possibly due to increased scattering or due to the presence of a region with lower mobility close to the dielectric/semiconductor interface [150]. In addition, transfer curves from the same transistor recorded at different temperatures exhibit exactly the same shape. It is imaginable that the increase of the intrinsic mobility with increasing gate overdrive voltage predicted by the models is present in our transistors, but is masked by the decrease at high V_{GS}. However, it is very unlikely that the process responsible for the decrease of the intrinsic mobility at high V_{GS} has exactly the same temperature dependence as the predicted mobility increase, meaning that the behavior should vary with temperature.

To investigate this in more detail, figure 4.32a shows Arrhenius plots of the sheet resistance for gate overdrive voltages ranging from 0.6 V to 1.6 V for $d = 6$ nm (similar results were obtained for $d = 21$ nm). An increase of the gate overdrive voltage elevates the Fermi energy in the accumulation layer, which should lead to a lowering of the activation energy. However, the curves for different $V_{GS} - V_{th}$ in figure 4.32a are almost exactly parallel, and very similar activation energies are extracted for different gate overdrive voltages. This is a surprising observation, since a reduction of the activation energy with increasing charge-carrier density is found in virtually all literature reports of variable temperature measurements where the mobility of the organic semiconductor is thermally activated, and is mostly connected with the validity of the Meyer-Neldel rule, meaning that Arrhenius plots measured at different $V_{GS} - V_{th}$ should intersect at a single crossing point [49, 132, 134, 172, 176–181]. The absence of these observations can conform with any of the above-mentioned models only if the Fermi level is pinned due to a large density of states close in energy and moves only marginally when the gate-source voltage is increased. The unusual behavior observed in these transistors indicates that probably none of the models commonly used to describe the charge transport in organic thin-film transistors is properly characterizing the physical transport mechanisms in the OTFTs investigated in this work.

If the Fermi level is not pinned, a possible explanation for the lack of a charge-carrier density dependence of both the intrinsic mobility and the activation energy would be hopping transport in a constant DOS as suggested by Mott (section 2.2.1). In such a case, the number of available states close to the Fermi level would be invariant to a shift of the Fermi level, hence all transport parameters would be unaffected by a change of the gate overdrive voltage. To test this hypothesis, the experimental data is compared to the temperature dependence predicted for Mott's VRH model (equation 2.5) by plotting the sheet resistance logarithmically against $T^{-1/3}$ for several $V_{GS} - V_{th}$ in figure 4.32b.

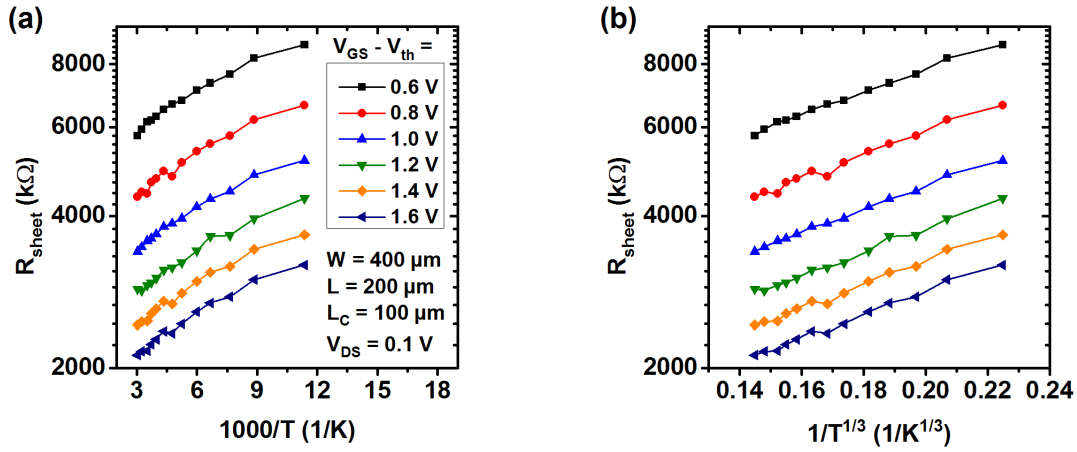


Figure 4.32: **Temperature dependence of the sheet resistance for various gate overdrive voltages.** Sheet resistance of a transistor with a nominal semiconductor thickness of 6 nm, plotted (a) in an Arrhenius plot and (b) as a function of $1/T^{1/3}$ for various gate overdrive voltages.

Straight lines are obtained, showing an excellent agreement with the model. It should be noted that the exponent 1/3 in equation 2.5 is obtained for hopping in two dimensions, which is presumably the case in a thin-film transistor, but plotting R_{sheet} as a function of $T^{-1/4}$ (3D-hopping) yields a similarly good agreement with the model. The curves for different $V_{GS} - V_{th}$ are parallel and a characteristic temperature of $T_1 = 145$ K can be extracted.

The picture of a constant density of states might seem unusual in view of the widespread assumption of a Gaussian or exponential DOS in organic semiconductors [182]. However, for the validity of Mott's VRH model the DOS only needs to be (fairly) constant in a restricted region around the fermi level. Recently, a Mott-type VRH regime was theoretically predicted for hopping transport in organic semiconductors with a Gaussian DOS at high charge-carrier densities and in a specific temperature range [183].

In order to verify the assumption of the constant DOS, direct measurements would be helpful. In principle, variable temperature measurements of the intrinsic mobility can be used to obtain information about the DOS. However, most methods that allow the calculation of the DOS $N[E]$ are of the form [184]:

$$N[E_A] \propto \left(\frac{\mathrm{d}E_A}{\mathrm{d}V_{GS}} \right)^{-1}, \tag{4.6}$$

which is not applicable in this case, since the activation energy E_A is not a function of V_{GS} in our TFTs.

The temperature dependence of the contact resistivity resembles that of the intrinsic mobility, i.e., the activation energy at high temperatures is larger than at low temperatures.

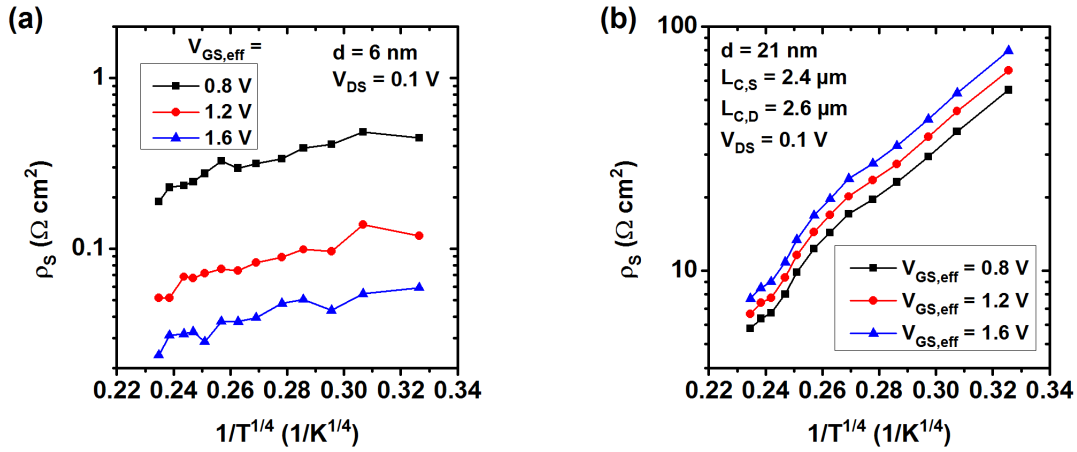


Figure 4.33: **Verification of Mott-like VRH transport at the contact.** Source contact resistivity for (a) $d = 6$ nm and (b) $d = 21$ nm as a function of $1/T^{1/4}$.

It is conceivable that the mechanism for the vertical transport through the bulk semiconductor (ρ_{bulk}) is similar to that for the lateral transport in the accumulation layer since the material is the same, although the charge-carrier density is substantially smaller. To verify this, the source contact resistivities for $d = 6$ nm and $d = 21$ nm are logarithmically plotted as a function of $T^{-1/4}$ in figure 4.33. Since the transport is now in the bulk, the transport is three-dimensional and the relevant exponent for the temperature in equation 2.5 is 1/4. In these plots, the contact parameters show a reasonable linearity and can therefore be described by Mott's VRH model. However, deviations, especially for $d = 21$ nm, indicate the presence of additional mechanisms.

4.7 Contact metal dependence

The contact resistivity is composed of contributions from the metal/organic semiconductor interface (ρ_{int}) and from the transport through the bulk semiconductor (ρ_{bulk}). At least for small nominal semiconductor thicknesses, where ρ_{bulk} is probably small, it is possible that the metal/organic semiconductor interface has a significant impact on the contact resistance. To investigate this, transistors with a nominal semiconductor thickness of 6 nm were fabricated that do not employ gold as the metal for the source/drain contacts, but instead silver, copper, titanium or aluminum. Like in the case of gold contacts, a 30 nm-thick layer of the metal was deposited by thermal evaporation, which was directly followed by a 15-nm-thick gold capping layer evaporated through the same stencil mask. The purpose of the capping layer is to protect the less noble metals from oxidation.
Figure 4.34 shows transfer characteristics of these transistors measured at a drain-source voltage of 0.1 V on a linear (left) and logarithmic scale (right). Except for the OTFT with

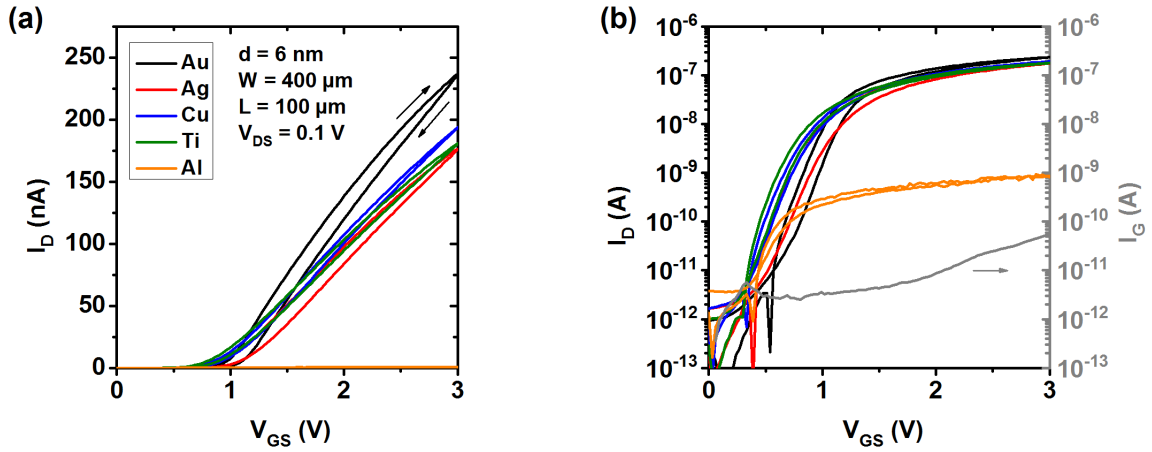


Figure 4.34: **Influence of the contact metal on the electrical characteristics.** Transfer curves of transistors with a nominal semiconductor thickness of $d = 6$ nm at $V_{DS} = 0.1$ V plotted on a (a) linear and (b) logarithmic scale.

aluminum contacts, the transfer curves are all very similar. However, in the case of aluminum contacts, the drain current in the on-state is about two orders of magnitude smaller than for the other contact metals, indicating a substantially inferior charge-transfer behavior. It is possible that Al reacts with the PDI-FCN_2 molecules, creating a heavily oxidized metal interface [185]. However, a more detailed investigation of the OTFTs with Al contacts was not possible, because the GFP potential information were not reliable.

On the substrate with titanium contacts, the contacts of most transistors were damaged. As can be seen in the photograph in figure 4.35b, the source and drain contacts peel off in the regions with an underlying semiconductor layer. Apparently, the adhesion between the PDI-FCN_2 and the titanium layers is very poor, and only a few transistors had proper contacts. All measurements on transistors with titanium contacts were therefore performed on devices with a contact length of 30 μm (instead of $L_C = 100$ μm for the other transistors in this section), but since the transfer length is well below 10 μm for gate overdrive voltages of 1 V or higher, this is not expected to influence the results.

The dependence of the contact resistivity on the gate overdrive voltage is plotted in figure 4.35a for the different contact metals at $V_{DS} = 0.1$ V. At large gate overdrive voltages, the contact resistivity is the smallest in transistors having gold contacts, but the gate-source voltage dependence of the contact resistivity is less pronounced for all other contact metals, so that copper and titanium contacts yield smaller values of R_C at small $V_{GS} - V_{th}$. The largest contact resistivity is observed with silver contacts, but even in this case R_C is relatively small. R_S and R_D were found to be similar for all contact metals and to be ohmic (not shown).

Most transport mechanisms across the metal/organic semiconductor interface exhibit a

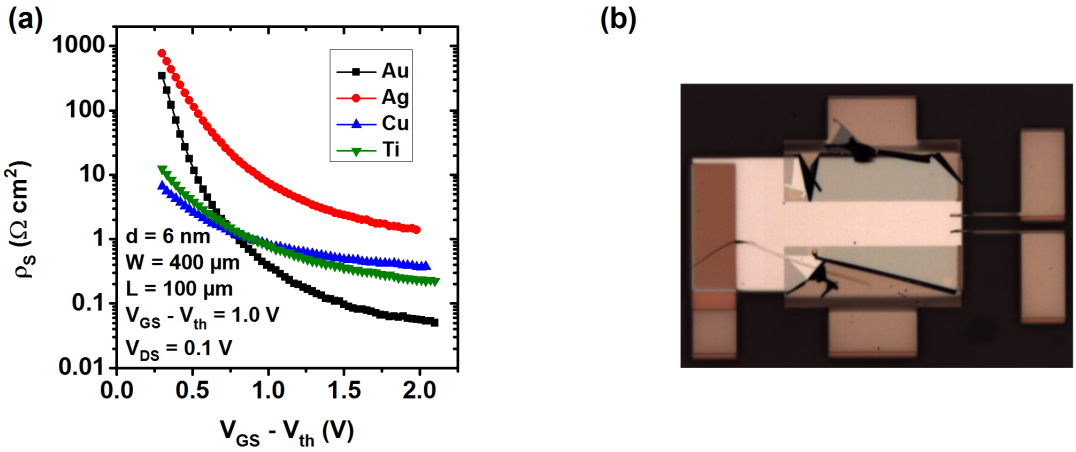


Figure 4.35: **Impact of the contact metal on the contact properties.** (a) Contact resistivity as a function of the gate overdrive voltage for different contact metals. (b) Photograph of a transistor with titanium contacts, showing the poor adhesion between PDI-FCN_2 and the titanium layer.

strong dependence on the energy barrier between the two materials (section 2.3.2). Therefore, figure 4.36 plots several transistor parameters as a function of the nominal work function of the contact metal. Data for the work functions was taken from [74]. As discussed in section 2.3.2, the nominal work functions do not necessarily determine the energy level alignment at the metal/organic semiconductor, but they could give a rough estimate.
The contact resistivities, extracted at $V_{GS} - V_{th} = 1$ V, are quite similar for gold, copper and titanium, despite the large differences in the nominal work function. Transistors having silver contacts exhibit a somewhat higher contact resistivity, but the range of measured values is quite large and overlaps with that measured for titanium contacts. The intrinsic mobility is similar for all contact metals, as expected, and the threshold voltage shows some variations, probably substrate-to-substrate fluctuations, but no clear dependence on the nominal work function of the contact metal.
In the literature, the reported influence of the contact material on the behavior of metal/organic semiconductor contacts is quite diverse, depending on the specific material combination, the type of device, the device geometry and the conditions during fabrication. Concerning organic thin-film transistors, the contact metal has been found to significantly influence the contact resistance [111, 186] or to have only little impact on it [132, 172]. In most cases, no correlation of the contact properties with the nominal work function of the contact metal was found. Kumatani et al. investigated pentacene OTFTs both ex-situ and in-situ (with or without any exposure to air during fabrication and characterization) and found a correlation between contact resistance and metal work function under in-situ conditions, but not under ex-situ conditions [187]. Instead, under ex-situ conditions (which were also used in this work), the contact resistance was found

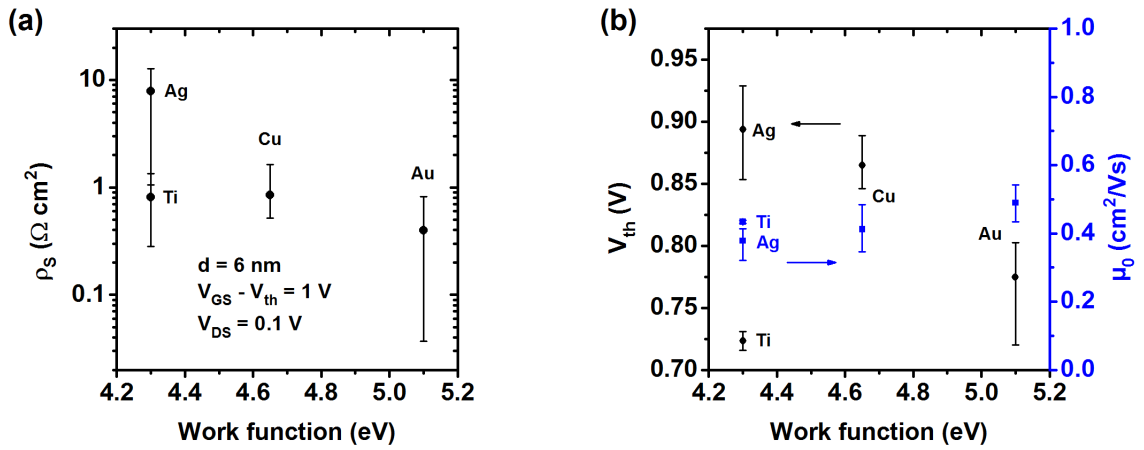


Figure 4.36: **Dependence of the transistor parameters on the nominal work function of the contact metal.** (a) Contact resistivity as a function of the nominal work function of the contact metal at a gate overdrive voltage of 1 V. (b) Threshold voltage and intrinsic mobility as a function of the nominal work function of the contact metal. Error bars show the full range of measured values.

to correlate with the standard electrode potential of the metal. No such correlation was found for the PDI-FCN_2 OTFTs. It should be noted that in [187] a gold capping layer was used as well, but the contacting metal had a thickness of only 2 nm.

Grobosch et al. investigated interfaces formed between the organic semiconductor α-sexithiophene (6T) and various metals using photoemission spectroscopy and found that while the hole injection barrier significantly varies for clean metals (all process steps done in UHV), it is essentially similar for all investigated contact metals if the metal was exposed to ambient atmosphere prior to the organic semiconductor deposition [188]. A similar situation may be present in the PDI-FCN_2 transistors investigated in this work, since the contact interface is in principle exposed to air before and after fabrication, despite the gold capping layer. Accordingly, the energy barrier at the interface and therefore the contact resistance would be similar for all metals, in accordance with the results presented in this section.

There are several alternative explanations for the lack of a relation between the contact metal and the contact resistance. For example, it is possible that the contact resistance is dominated by the transport through the bulk semiconductor, regardless of the semiconductor thickness of only 6 nm, due to the significant anisotropy of the charge-carrier mobility. In this case, the interface resistivity determined by the metal work function would be masked by the larger bulk resistivity. This would also be consistent with the observation that the source and drain resistances are virtually identical for all metals.

Another possibility is that the main transport mechanism across the interface is hopping

via in-gap states (path 2 in figure 2.10, section 2.3.2), thereby bypassing any energy barrier [132]. A third explanation is that the gate-induced charge-carrier concentration at the metal/organic semiconductor interface is sufficiently large to significantly decrease the width of any energy barrier, allowing efficient and ohmic tunneling for all contact metals [132]. This would be in line with the strong V_{GS} dependence of the contact resistance observed for this nominal semiconductor thickness (figure 4.10a).

4.8 Comparison with the transmission line method

The contact resistance analysis in this work was performed mainly using the gated four-probe method, due to the richness of detail it provides and the small number of assumptions it requires. However, since the most frequently used technique for this type of investigation is still the transmission line method, owing to its simplicity (both in terms of fabrication requirements and data analysis), this section provides a comparison of these two important methods.

In order to perform the TLM analysis, TFTs with channel widths of 400 μm and channel lengths ranging from 60 μm to 300 μm were utilized. In order to allow a direct comparison with the GFP results, all these transistors were equipped with potential probes using layout A. The contact resistance extraction was performed by extrapolating the total device resistance measured at $V_{DS} = 0.1$ V to zero channel length, as described in section 2.4.4. To obtain R_C as a function of the gate overdrive voltage, the threshold voltage must be known, and three different methods were used to obtain V_{th}. In the first method (in the following referred to as TLM A) V_{th} is extracted using the second derivative (SD) method from the as-measured data, thereby allowing transistor-to-transistor parameter variations in V_{th}, but not correcting for the shape-altering effect of the contact resistance on the transfer curve. In the second method (TLM B), the threshold voltage is initially not considered, and the analysis is performed as a function of V_{GS}. Afterwards, the inverse of the sheet resistance is plotted as a function of V_{GS}, yielding the threshold voltage from the intersection of a linear fit with the x-axis. V_{th} obtained in this way is conceptually similar to the intrinsic threshold voltage extracted from the GFP measurements, but since a single (average) value is obtained for all TFTs in the set, the parameter variations are not captured. In the third method (TLM C), the threshold voltage is taken from the GFP measurements. This would normally not be possible, but is at this point useful for the intended comparison.

Figure 4.37a shows the width-normalized contact resistance as a function of the gate overdrive voltage for a nominal semiconductor thickness of 6 nm, extracted using the GFP method for each transistor individually and using TLM with the different methods of threshold voltage extraction. For clarity, figure 4.37b shows the same graph, but with

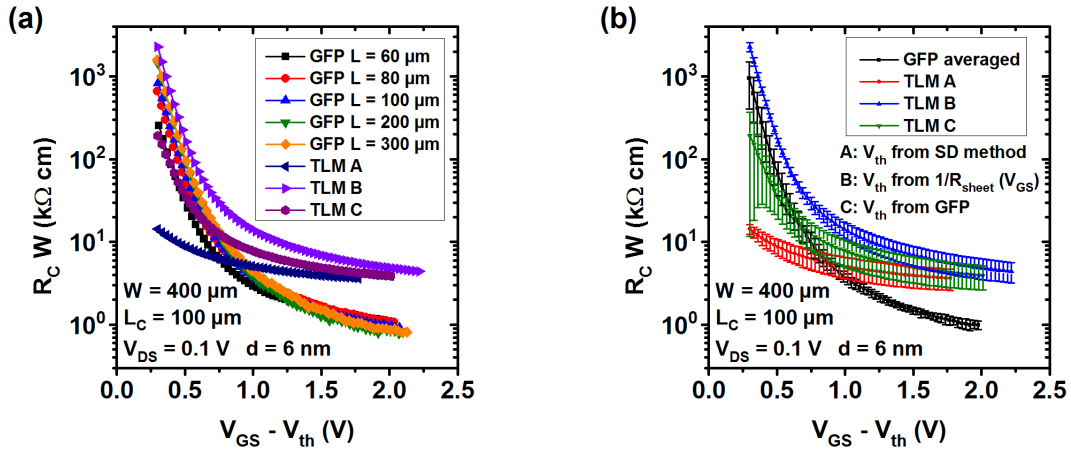


Figure 4.37: **Comparison of the contact resistance extracted from GFP and TLM for $d = 6$ nm.** (a) Width-normalized contact resistance as a function of $V_{GS}-V_{th}$ extracted from GFP measurements performed on transistors with various channel lengths and from TLM data using methods for determining V_{th}. (b) Same as (a), but with averaged GFP data. Error bars represent the standard error.

averaged GFP data and error bars representing the standard error of the statistics or of the linear fit. First of all, it is obvious that the contact resistance obtained from GFP is very similar for all channel lengths, again illustrating the accuracy of the GFP method. In contrast, the TLM results vary quite significantly depending on how the threshold voltage was determined. Using TLM C as a reference, the curve of TLM A is shifted to smaller gate overdrive voltages due to the larger threshold voltages determined by the SD method, while TLM B appears to be shifted to larger gate overdrive voltages.

Especially at high $V_{GS} - V_{th}$, TLM consistently yields larger contact resistances. This can be explained by the presence of fringe currents extending beyond the source/drain electrodes of the transistor, as illustrated in the inset of figure 4.38a. These fringe currents effectively increase the channel width and are more pronounced for smaller W/L ratios. Therefore, since all TFTs have the same channel width, transistors with longer channels are more severely affected, and the channel resistance is increasingly reduced with increasing channel length compared to the nominal value. This is illustrated in figure 4.38a, where the width-normalized total device resistance is plotted as a function of the channel length. The red line depicts the linear fit of the data, yielding the TLM results. The dotted line is the device resistance calculated from the contact and channel resistance obtained from the GFP measurement. As can be seen in figure 4.37a, the fringe currents do not influence the contact resistance extracted from the GFP method. Instead, the increasing contribution of the fringe currents for longer channels is reflected in the intrinsic mobility (or equivalently in the sheet conductance), which appears to increase

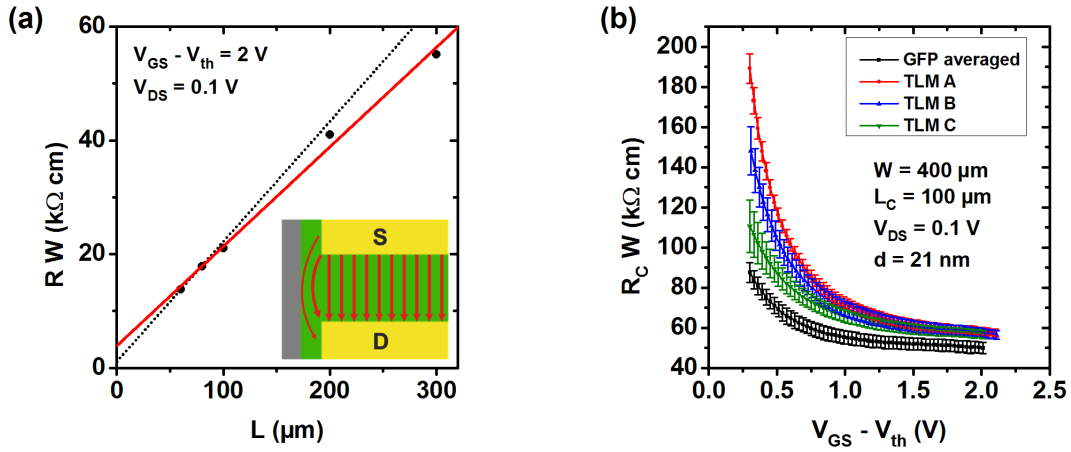


Figure 4.38: **Effect of fringe currents and comparison of GFP and TLM for $d = 21$ nm.** (a) Width-normalized device resistance as a function of the channel length for $d = 6$ nm and $V_{GS} - V_{th} = 2$ V. The red line is a linear fit of the TLM data, while the dotted line is the total resistance calculated from the GFP data, showing the effect of effectively wider channels for large channel lengths due to fringe currents. Inset: Schematic of the side of a transistor channel, illustrating the fringe currents. (b) Width-normalized contact resistance as a function of $V_{GS} - V_{th}$ for $d = 21$ nm averaged from GFP measurements performed on transistors with various channel lengths and from TLM data using different methods for determining V_{th}.

with increasing channel length according to the GFP data (not shown). Therefore, to calculate the dotted reference line in figure 4.38a, the sheet conductance from the transistor with $L = 60$ μm was taken, where the W/L ratio is largest. With increasing channel length, the deviation between the TLM fit line and the calculated dotted line increases. Due to the smaller slope, TLM overestimates both the intrinsic mobility and the contact resistance.

Figure 4.38b compares the width-normalized contact resistance as a function of the gate overdrive voltage measured using GFP and TLM for a nominal semiconductor thickness of 21 nm. As in the case of $d = 6$ nm, the TLM overestimates R_C. Relative to TLM B and TLM C, TLM A is now shifted to higher $V_{GS} - V_{th}$, due to the smaller threshold voltages obtained from the second derivative method.

In summary, contact resistances measured using the transmission line method can be significantly affected by fringe currents, while the GFP method is much more robust in this regard. If transistors with a constant W/L ratio were used, TLM would probably yield contact resistances similar to those from the GFP method for $d = 6$ nm (provided that parameter fluctuations are small), because the source and drain resistances are ohmic. For thicker semiconductor layers, this is true as well for small V_{DS} (which are necessary for TLM anyway) and for sufficiently large channel lengths (in order to limit the voltage

drop across the contact regions). However, an additional problem of TLM is the difficulty of a reliable determination of the threshold voltages, because conventional methods either disregard the influence of the contact resistance or do not capture device-to-device fluctuations. Due to these limitations and because the GFP method yields more detailed information (e.g., individual source and drain resistances and full V_{DS} range), the GFP method is to be preferred over TLM for measuring the contact resistance, if technically feasible.

4.9 Discussion of possible sources of error

The validity and accuracy of the GFP method used in this work was discussed in sections 4.3.2, 4.5 and 4.8, and the technique was found to be very reliable. Examinations using three potential probes verified the validity of calculated potential profiles at high gate overdrive voltages. At low $V_{GS} - V_{th}$, small deviations occur due to the nonlinear potential profile, which is why all data is only shown for $V_{GS} - V_{th} \geq 0.3$ V.
Contact resistance values are always given for a specific value of $V_{GS} - V_{th}$. Since the transfer curves were taken with a finite step size in V_{GS} (in this case 0.03 V) and the threshold voltages vary somewhat, data points are usually not taken exactly at the specified $V_{GS} - V_{th}$ and the deviation from that value can vary from data point to data point within the step size. This technical issue causes some data scattering, especially in cases where the V_{GS} dependence is strong.
A more important source of error is the air-induced evolution of some of the transistor parameters. Although the air stability of the transistors is relatively good, as will be discussed in the next chapter, changes in the transistor parameters during the course of all measurements performed on a substrate are unavoidable. This is especially problematic for comparative measurements that require long measurement times. An example are the GFP measurements on transistors with different contact lengths that take several hours. To minimize systematic errors, the measurement sequence in such cases was mixed and the parameter of interest (in this case L_C) was not changed monotonously.
Transistor parameters can also vary spatially across the same substrate or from substrate to substrate. While the former variation is usually small, the latter is often larger and can be significant. To quantify this, statistics of the contact resistance, the intrinsic mobility and the threshold voltage measured on six different samples with $d = 6$ nm and $L_C = 100$ μm, measured at $V_{DS} = 0.1$ V, have been compiled. The mean values and standard errors are $R_C = (5.5 \pm 2.1)$ kΩ cm, $\mu_0 = (0.41 \pm 0.09)$ cm^2/Vs and $V_{th} = (0.87 \pm 0.08)$ V. Although values from different substrates are quite similar, fluctuations are apparent and they are largest for the contact resistance. Due to the degradation of the device characteristics, the use of several different, but nominally identical substrates

is unavoidable. To minimize this problem, direct comparisons were always done using substrates fabricated within a short time frame. In addition, as far as measured, it was tested and verified that the functional dependencies reported in this work were similar for all nominally identical samples.

4.10 Conclusions and implications for the contact properties

High-performance n-channel organic thin-film transistors fabricated on flexible plastic substrates were analyzed by means of gated four-probe measurements. The method was found to give accurate, reliable and detailed information about the contact properties of the PDI-FCN_2 transistors and revealed that they are strongly affected by the thickness of the organic semiconductor film. In transistors with a thin semiconductor layer, the contact resistance can be extremely small ($\approx$0.6 kΩ cm) and is among the smallest values reported in the OTFT literature, despite the fact that the TFTs were operated in air and the lack of any contact treatment.
The following main properties of the contact resistance (and similarly of the contact resistivity, since the contact resistance can be well described by the current crowding model) were identified:

1. The parameter dependence and the magnitude of the source and drain contact resistances is identical for all semiconductor thicknesses.

2. The gate-source-voltage dependence of the contact resistance strongly depends on the thickness of the organic semiconductor layer, with a rapid decrease as V_{GS} increases for relatively thin films that turns into an increase for relatively thick films.

3. The contacts have an ohmic behavior in the case of small voltage drops across the contact regions. In TFTs with relatively thick semiconductor films, a nonlinear increase of the current with the voltage is observed for larger voltages. No nonlinearity is observed for relatively thin films, but the voltage drops across the contact regions are also limited to much smaller values in this case.

4. The temperature dependence of the contact resistivity is weak, with small activation energies in the range of 3 meV to 50 meV, assuming an Arrhenius-like behavior. However, the activation energies are larger than those of the sheet resistance in the accumulation layer and increase with the thickness of the organic semiconductor layer. The activation energies are not modulated by the gate-source voltage.

5. The source/drain contact metal has only a weak influence on the contact resistance.

These findings allow to draw conclusions about the mechanisms causing the contact resistance. Based on the fact that the source and drain resistances are similar in magnitude and behavior and based on the observations that the activation energies are small and the contact resistance is almost independent of the contact-metal, thermionic emission over an energy barrier at the metal/semiconductor interface can be ruled out as relevant process.
In the case of very thin semiconductor films, however, it is conceivable that the modulation of an energy barrier is involved in the charge transfer process in order to explain the observed significant V_{GS} dependence of the contact resistivity. Pesavento et al. suggested that if the metallic source or drain contact is in direct contact with the conducting channel, the gate-source-voltage-dependent charge-carrier density would modulate the width of any energy barrier at the metal/organic interface, yielding a strongly V_{GS}-dependent contact resistance and enabling efficient and ohmic tunneling at high V_{GS} as illustrated in figure 4.39a. In order to test the hypothesis of such a barrier modulation for the PDI-FCN_2 transistors, the shift of the potential ϕ due to these additional charges was calculated using the gate-induced charge-carrier density (equation 4.2 and figure 4.28a) and Poisson's equation:

$$\frac{\partial^2 \phi}{\partial y^2} = -\frac{n[y]e}{\varepsilon_S}. \tag{4.7}$$

The result is shown in figure 4.40a for a 6-nm-thick organic semiconductor film and for two different gate overdrive voltages. It is apparent that a significant difference in the potential shift is only obtained within the first two nanometers (about one molecular layer), further away from the gate dielectric/organic semiconductor interface the influence of $V_{GS} - V_{th}$ on the potential shift is very low due to screening. It should be noted that calculations with a stepwise charge-carrier density (accounting for the molecular layer nature) yield similar results. Therefore, a barrier modulation is not obtained in this scenario. However, several deviations from the above-mentioned simple consideration are possible. First, the organic semiconductor layer probably does not have a uniform thickness, and it is quite likely that at some positions the film is only one or two molecular layers thick. Second, the accumulation layer is not uniformly charged. The molecular density can be estimated to about 10^{21} cm^{-3} [98], while the charge-carrier density in the first molecular layer (the accumulation layer) is about 10^{19} cm^{-3} at a gate overdrive voltage of 1 V. This means that in both axes of the plane of the accumulation layer, on average only every tenth molecule is charged, so that the screening might not be effective everywhere and at all times.
Temperature-dependent measurements indicated the possibility of a significant contribution of hopping transport to the contact resistivity also for $d = 6$ nm (figure 4.33a).

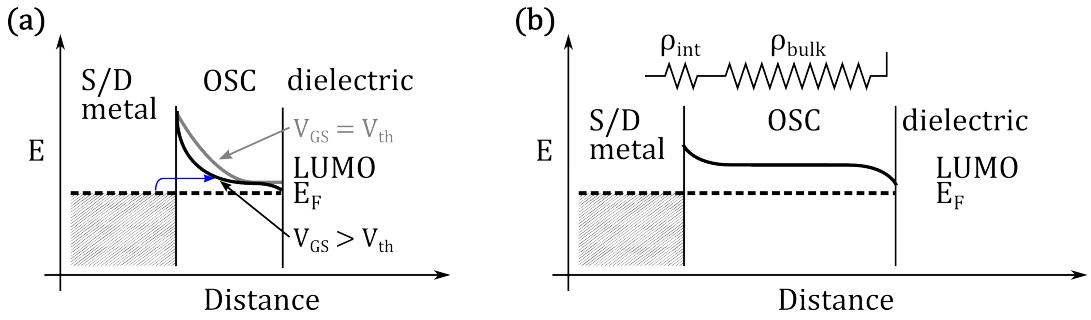


Figure 4.39: **Possible charge transfer mechanisms and energy level alignments.** (a) Simplified energy level diagram for the case of a thin organic semiconductor (OSC) layer. In this scenario, the gate-source voltage is able to significantly change the charge-carrier density near the source or drain metal/organic semiconductor interface, thereby modulating the tunneling barrier. (b) Simplified energy level diagram for the case of a thick organic semiconductor layer. Charge transfer is probably limited by the low-mobility transport through the bulk semiconductor.

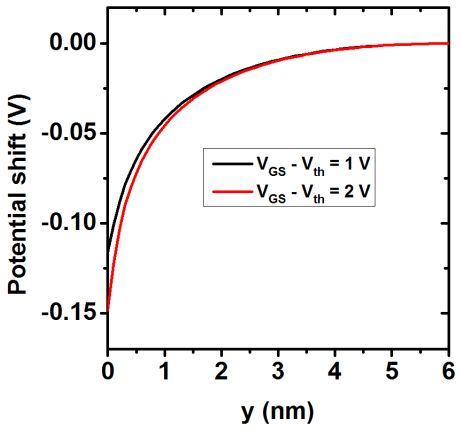


Figure 4.40: **Influence of the gate-source voltage on the potential in the semiconductor.** Shift of the electrostatic potential due to the gate-induced charge-carrier concentration as a function of the distance from the gate-dielectric/organic semiconductor interface, calculated from equations 4.2 and 4.7 for two values of the gate overdrive voltage.

However, it is more difficult to explain the strong V_{GS} dependence of the contact resistivity in this scenario. Possibly, vertical hopping transport is influenced by an energy barrier created by the insulating fluoroalkyl chains of the PDI-FCN_2 molecule, which may be modulated by the gate-source voltage.

In the case of relatively thick organic semiconductor films, the contact resistivity is probably dominated by the resistivity of the bulk semiconductor, as depicted in figure 4.39b.

The nonlinearity of the current-voltage characteristics observable at large potential drops across the contact region (figure 4.26) can be explained best by space-charge limited currents, possibly in combination with a Poole-Frenkel-modified charge-carrier mobility. In the proposed scenario, the interface resistivity is sufficiently small to be insignificant.
Since the charge-carrier density in the bulk is only weakly modulated by the gate-source voltage, a reduced gate-source voltage dependence of the contact resistance for increasing semiconductor thickness is reasonable. However, the partially observed increase of the contact resistance with increasing gate-source voltage is not understood so far. The larger contact resistance activation energies measured for transistors with thick organic semiconductor films might be related to the smaller charge-carrier density in the bulk that could result in larger energy-level spacings around the transport level. It is also conceivable that hopping transport in the vertical direction requires a larger thermal energy.

5 Stability of PDI-FCN_2 transistors

The stability of the electrical characteristics is an important aspect for practical applications of organic transistors. In this chapter, two types of stability of the PDI-FCN_2 transistors are investigated: the stability of the electrical characteristics during long-term storage under ambient conditions (shelf-life stability) and the steadiness under continuous operation (bias-stress stability). The stability of OTFTs (especially n-channel OTFTs) is often strongly influenced by chemical species from the ambient atmosphere, mainly oxygen and water. Therefore, both stabilities can often be improved by protecting the organic film from these molecules using an encapsulation layer. However, the fabrication of these layers can be quite difficult and costly, especially for flexible applications where rigid encapsulation layers are not possible. In addition, the encapsulation is never perfect or can be cheaper when the barrier requirements are more relaxed, so an intrinsic stability of the organic transistors is always beneficial and simplifies handling.
In addition to the changes in the mobility and threshold voltage, the temporal development of the contact resistance is also investigated in this work, a factor that is often ignored in the literature. The consideration of the contact resistance also guarantees that the mobility and the threshold voltage are determined in a reliable manner. The shelf-life stability of PDI-FCN_2 OTFTs is investigated in section 5.1. The bias-stress stability of the PDI-FCN_2 OTFTs, which will also be important in the discussion of the dynamic performance (chapter 6), is analyzed in section 5.2.

5.1 Shelf-life stability

The shelf-life stability of the PDI-FCN_2 OTFTs was investigated by storing the substrates in a cleanroom under ambient conditions (yellow light, a constant temperature of 19 °C and a humidity in the range of 30-70%). Occasionally, the substrates were taken to the probe station for a GFP measurement. Figure 5.1 shows the development of the transistor parameters measured at $V_{DS} = 0.1$ V over a period of 42 days in a semi-log plot for the different nominal semiconductor thicknesses. Exemplary transfer curves measured at various times for $d = 6$ nm are shown in figure 5.1d. Depending on the value of d, the threshold voltage shifts by approximately 0.1 V to 0.3 V towards more positive values within the first day and then displays sometimes strong fluctuations around that value.

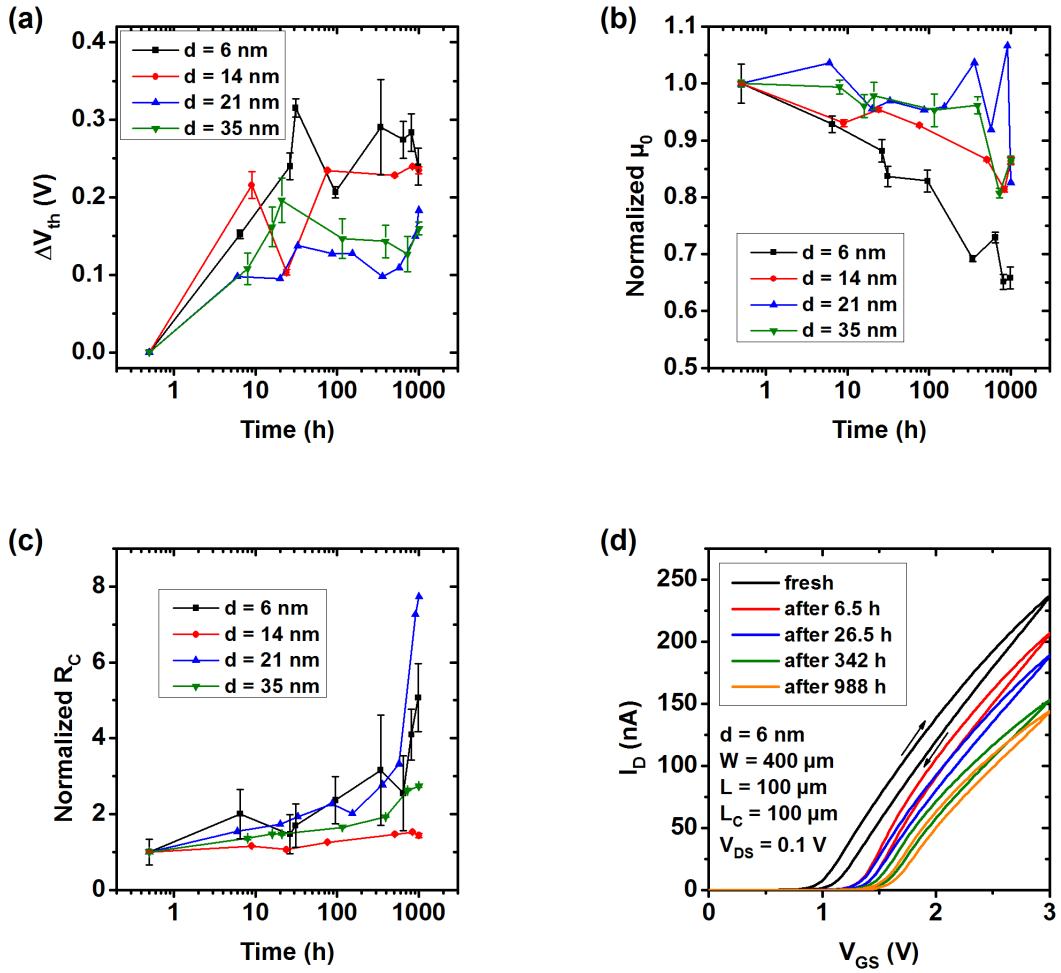


Figure 5.1: **Shelf-life stability of PDI-FCN$_2$ TFTs with different nominal semiconductor thicknesses.** All parameters were extracted and averaged from two transistors with $W = 400$ μm, $L = 100$ μm and $L_C = 100$ μm at $V_{DS} = 0.1$ V. For all thicknesses except $d = 21$ nm, error bars show the range of measured values from two devices. (a) Threshold voltage shift as a function of time. Most of the shift occurs within approximately one day. (b) Change of the intrinsic mobility over time normalized to its initial value. (c) Change of the contact resistance at $V_{GS} - V_{th} = 1$ V over time normalized to its initial value. (d) Development of the transfer curves over time for a transistor with $d = 6$ nm.

The shift seems to be somewhat larger for smaller semiconductor thicknesses.
The intrinsic mobility decreases continuously for $d = 6$ nm and $d = 14$ nm, with a more pronounced decrease for $d = 6$ nm. In contrast, for $d = 21$ nm and $d = 35$ nm μ_0 mostly shows fluctuations and no pronounced degradation within the first two weeks, but then eventually decreases. After 6 weeks, the intrinsic mobility has decreased to values between 65 % and 90 % of its initial value, depending on d. The contact resistance displays the most pronounced changes, with values up to almost 800 % of the initial value after 6 weeks, but showing no clear correlation with the semiconductor thickness. The fact that the change of R_C is larger than that of μ_0 is surprising, because the gold contacts are expected to partially protect the underlying organic semiconductor from the ambient atmosphere [115]. A possible explanation for this behavior is a degradation of the contact metal/organic semiconductor interface. Alternatively, the bulk mobility or the mobility under the contacts may degrade more rapidly than the channel mobility.
When compared with other n-channel OTFTs from the literature [189], the TFTs investigated in this work exhibit a good air stability, especially when considering that many n-channel OTFTs can only be operated in vacuum or an inert atmosphere.
The degradation mechanism in n-channel organic TFTs can be very complex. It is, however, believed that changes in the chemical composition, which were observed in pentacene [190], do not play an important role for most n-channel OTFTs [32, 115]. Instead, the instability probably arises from charge-carrier trapping induced by oxygen or water [32, 91, 92, 189]. Nicolai et al. observed a universal trap level in several electron-transporting semiconducting polymers centred at an energy of ≈3.6 eV below the vacuum level, which might be caused by the presence of hydrated oxygen complexes [93]. Consequently, the high air stability of the PDI-FCN_2 TFTs is probably due to the following factors. First, the LUMO energy of PDI-FCN_2 is well below 3.6 eV and thus has a significant energetic difference from these trap states. In addition, the large van der Waals radius of fluorine reduces the available spacing between the *N,N'* chains, thus preventing the intrusion of oxygen and water [91, 191]. Finally, the pronounced hydrophobicity of the SAM-covered gate-dielectric surface may also play an important role for the air stability by repelling water from the dielectric/organic interface.
Compared with previous investigations of the air stability of PDI-FCN_2 TFTs, the stability determined in this work is not quite as good as in [91, 104], but somewhat better than in [100, 108]. However, the process conditions were different in all studies. In addition, the rougher substrate used in this study might lead to additional grain boundaries that have been shown to be important for the air-induced degradation process [108].

5.2 Bias-stress stability

First, the bias-stress stability of the PDI-FCN$_2$ OTFTs under ambient conditions in a cleanroom (for details see section 5.1) is analyzed. The yellow light of the cleanroom present during the measurements was found to not affect the bias-stress behavior in a reference measurement. During a bias-stress measurement, the transistor is operated continuously at fixed V_{GS} and V_{DS} and the drain current is monitored. At certain times, the bias stress was briefly interrupted for about 40 s to allow the recording of transfer curves including GFP data at $V_{DS} = 0.1$ V. Transfer curves were also measured before and after each bias stress experiment.

Figure 5.2 illustrates the development of the electrical characteristics and parameters during continuous bias stress at $V_{GS} = 3$ V and $V_{DS} = 0.1$ V for transistors with different nominal semiconductor thicknesses with the specifications $W = 400$ μm, $L = 100$ μm and $L_C = 100$ μm. The evolution of the drain current is shown in figure 5.2a. Except for $d = 21$ nm where the drain current initially increases, the drain current drops essentially monotonically as the transistors are stressed. This drop is more pronounced for smaller semiconductor thicknesses and leads to a reduction of the drain current to less then 40 % of the initial value after about 37 min of stress for $d = 6$ nm. The brief interruptions of the bias stress for the transfer curve measurements produce apparent discontinuities in the drain current. However, upon continuation of the bias stress, the drain current quickly returns to its previous value and follows the former trend, indicating a memory effect for the stress behavior. Consequently, the brief interruptions probably have no or little influence on the overall bias-stress behavior of the OTFTs.

To analyze the cause of the reduction in the drain current, the individual transistor parameters were extracted from the transfer curves measured prior to, during and after each bias-stress experiment. These electrical characteristics are plotted in figure 5.3 for $d = 6$ nm and $d = 35$ nm. Figure 5.2b illustrates the shift of the threshold voltage as the transistors are being stressed. A significant increase of V_{th} occurs already during the first minutes, and this is most pronounced for $d = 6$ nm and least pronounced for $d = 21$ nm. The increase of the threshold voltage is also evident in figure 5.3 and manifests itself as a shift of the transfer curves to larger gate-source voltages.

A shift of the threshold voltage under constant operation in the direction of the applied gate-source voltage is the most commonly observed effect in bias-stress experiments [23, 192–195]. This shift is usually attributed to charge trapping into localized states: the trapped charges contribute to the charge balance of the gate capacitor, but no longer contribute to the charge transport from source to drain. The trap states can be located in the semiconductor, in the gate dielectric or at the semiconductor/dielectric interface.

In figure 5.2c, the evolution of the intrinsic mobility during stress is shown. A significant

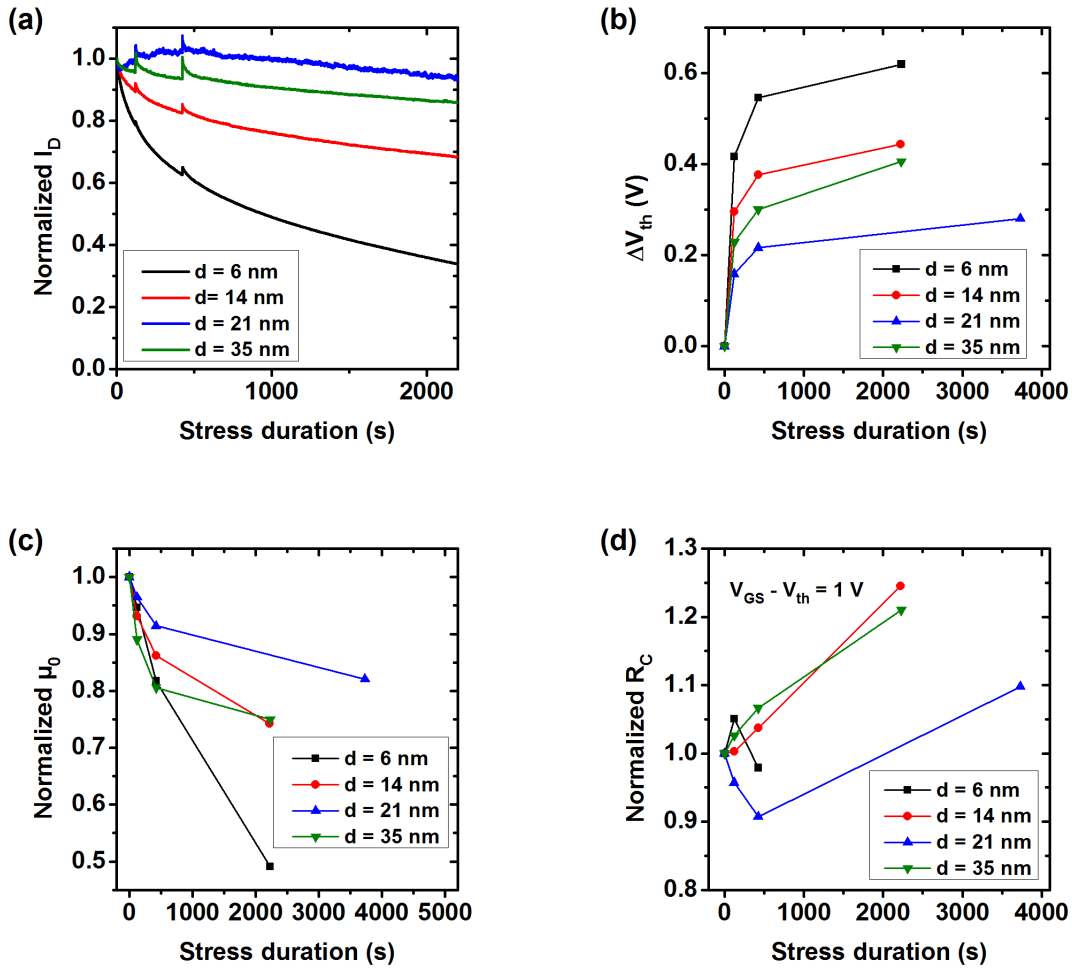


Figure 5.2: **Bias-stress stability of PDI-FCN$_2$ TFTs with different nominal semiconductor thicknesses.** All data were taken from transistors with $W = 400$ μm, $L = 100$ μm and $L_C = 100$ μm. A constant bias of $V_{GS} = 3$ V and $V_{DS} = 0.1$ V was applied and briefly interrupted at certain times in order to measure transfer curves at $V_{DS} = 0.1$ V for parameter extraction. (a) Drain current as a function of stress time. The brief interruptions are visible as discontinuities in the drain current. (b) Threshold-voltage shift as a function of stress time. Most of the shift takes place during the first few minutes. (c) Development of the intrinsic mobility over stress time normalized to its initial value. A continuous decrease is visible. (d) Development of the contact resistance over stress time normalized to its initial value. For $d = 6$ nm, the fast relaxation after long stress times prevented the reliable determination of R_C.

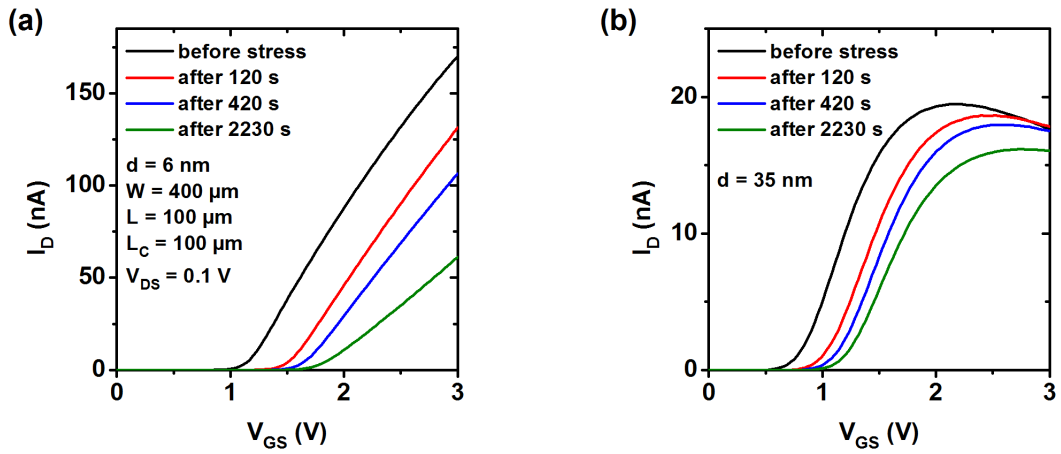


Figure 5.3: **Effect of bias stress on the transfer curves.** Linear transfer characteristics after different durations of bias-stress at $V_{GS} = 3$ V and $V_{DS} = 0.1$ V. The transistor dimensions are $W = 400$ μm, $L = 100$ μm, $L_C = 100$ μm and the nominal semiconductor thickness is (a) 6 nm and (b) 35 nm.

drop of μ_0 is evident for all values of d, but is again most pronounced for $d = 6$ nm. The decrease of μ_0 is also visible in figure 5.3a as a reduced slope of the transfer curve after stressing. The change in the contact resistance during bias stress is smaller than that of the mobility (figure 5.2d). For $d = 21$ nm, R_C initially decreases for unknown reasons, causing an initial increase of the drain current.
Observations of a degradation of the effective mobility during bias stress in OTFTs are rare [194–196]. However, except for [196], the evolution of the contact resistance was not monitored simultaneously, so that it is not clear whether the drop of μ_{eff} in these reports is caused by a reduction of the intrinsic mobility or an increase of the contact resistance.

5.2.1 Influence of the gate and drain biases and recovery

A common observation in organic TFTs is that the bias-stress stability is affected by the gate-source and drain-source biases. In general, the stability is lower for larger V_{GS} and smaller V_{DS}, probably because the number of charge carriers trapped during a certain time frame increases if their density in the channel is larger [194, 195, 197, 198]. To investigate this effect for the PDI-FCN$_2$ transistors, the bias stress was analyzed for two values of V_{GS}, each at $V_{DS} = 0.1$ V and for $V_{DS} = V_{GS}$, on transistors with a nominal semiconductor thickness of 6 nm. For each bias voltage combination, a fresh (i.e., not previously stressed) transistor was used. The bias stress was frequently interrupted to measure transfer curves at $V_{DS} = 0.1$ V, from which the electrical parameters were extracted. After the bias stress, the transistors were stored without bias under ambient conditions and occasionally measured to investigate the recovery behavior. It should be

noted that the air-induced degradation due to storage in ambient atmosphere is expected to interfere with the recovery process.

The temporal development of the threshold voltage is plotted in figure 5.4a. It is obvious that the magnitude of the drain-source voltage has only a small influence on the bias-stress behavior, which is in accordance with the fact that for $d = 6$ nm the influence of the drain-source voltage on the charge carrier concentration in the channel is reduced due to the large voltage drop at the drain contact (section 4.5). On the other hand, the impact of the gate-source voltage is substantial. In particular, the threshold voltage prior to the bias stress is already larger by about 0.13 V when using a V_{GS} of 3.2 V instead of 2.6 V due to the initial short application of a larger V_{GS}. The threshold voltage then shifted by about 1.0 V and 1.2 V towards higher values during the complete bias-stress sequence at $V_{GS} = 2.6$ V and $V_{GS} = 3.2$ V, respectively. After the bias stress, the threshold voltage slowly recovered, approaching the initial value after about two days.

The development of the intrinsic mobility during bias stress and recovery is shown in figure 5.4b. In this case, the behavior is similar for all bias conditions. Again, a recovery of the degraded mobility is visible, but it is much less pronounced than that of the threshold voltage, indicating that the origin of the mobility degradation is more complex.

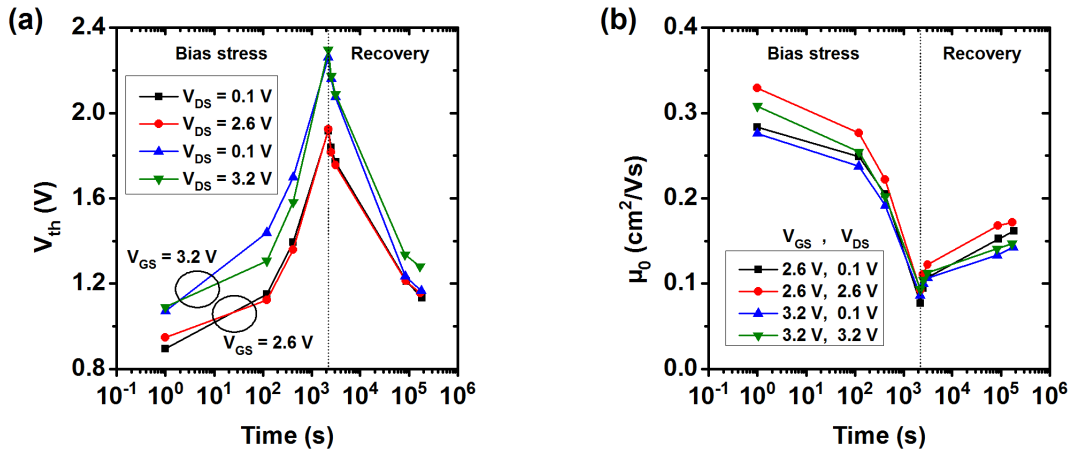


Figure 5.4: **Influence of the applied voltages on the bias-stress stability for transistors with $d = 6$ nm.** Development of the (a) threshold voltage and (b) intrinsic mobility over time during bias stress and recovery for various applied gate-source and drain-source voltages. The dotted line marks the transition between bias stress and recovery.

5.2.2 Influence of the atmosphere

Degradation due to bias stress in OTFTs is usually related to charge trapping in the organic transistor. Charge traps can be air-induced, as discussed in section 5.1, but can also be intrinsically present, for example in the gate dielectric [66] or at the grain boundaries in the organic semiconductor [199].
Therefore, in this section the bias-stress behavior of PDI-FCN$_2$ TFTs in vacuum ($\approx 10^{-8}$ mbar) and in different atmospheres is analyzed for $d = 6$ nm. First, the change of the electrical characteristics upon transfer of the transistors from air into vacuum is shown in figure 5.5a. After pumping, the intrinsic mobility increases slightly by around 30 % and the contact resistance simultaneously decreases by around 20 %. In addition, the hysteresis almost vanishes, indicating a reduction of trap states.

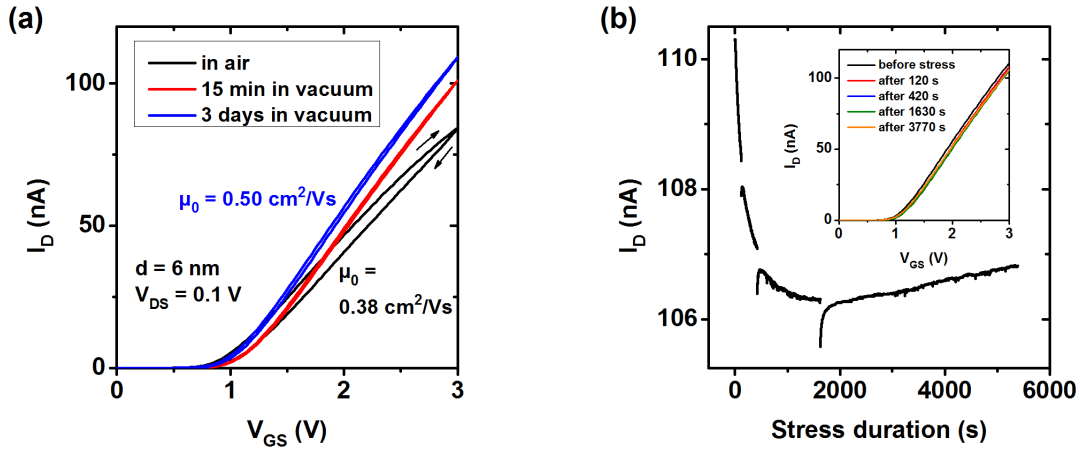


Figure 5.5: **Electrical behavior of PDI-FCN$_2$ TFTs with $d = 6$ nm in vacuum.** (a) Transfer curves measured in air, after 15 min in vacuum and after 3 days in vacuum. In vacuum, the intrinsic mobility increases and the hysteresis decreases. The transistor dimensions are $W = 400$ μm, $L = 200$ μm and $L_C = 100$ μm, and the measurement was performed at $V_{DS} = 0.1$ V (b) Bias-stress measurement performed on the same transistor at $V_{GS} = 3$ V and $V_{DS} = 0.1$ V, showing the drain current as a function of stress duration. Inset: Evolution of the linear transfer curves under bias stress in vacuum.

The evolution of the drain current under bias stress in vacuum at $V_{GS} = 3$ V and $V_{DS} = 0.1$ V is plotted in figure 5.5b. The degradation of the drain current is obviously much smaller than in air, with a reduction of the drain current to about 96 % of the initial value after 2200 s of bias stress (compared to 34 % in air). At the end, the drain current shows a slight increase, possibly due to self-heating. The inset shows the transfer curves measured before, during and after the bias-stress experiment, and it can be seen that there is almost no change during stress.

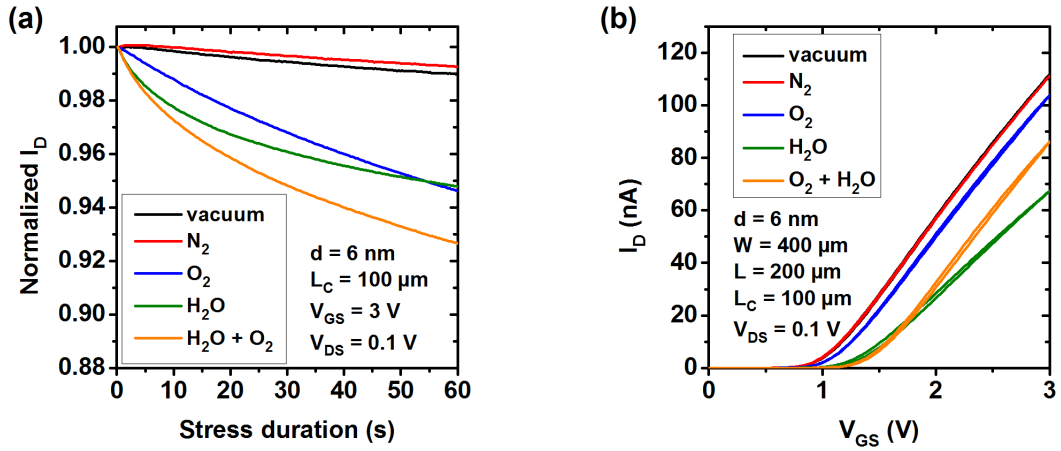


Figure 5.6: **Influence of the atmosphere on the bias-stress stability of a transistor with $d = 6$ nm.** (a) Evolution of the drain current during bias stress at $V_{GS} = 3$ V and $V_{DS} = 0.1$ V in different atmospheres. (b) Linear transfer characteristics measured in different atmospheres.

Apparently, the sensitivity to bias stress is almost completely due to trap states that are generated by airborne species. In order to obtain more insight into this process, bias-stress measurements in different atmospheres were performed. For measurements in nitrogen or oxygen, the vacuum chamber was flooded with gases of 99.999 % purity until a pressure of about 1 bar was reached. A water atmosphere was created by opening the valve between a flask of pure water and the evacuated vacuum chamber, creating a water vapor with a pressure of about 23 mbar. A mixed water/oxygen atmosphere was established by adding oxygen gas to a water atmosphere until a pressure of 1 bar was reached. In between measurements in different atmospheres, the chamber was evacuated for several minutes, flushed with nitrogen and evacuated again. Prior to the bias stress measurements, the system was allowed to equilibrate in the new atmosphere for 5 minutes. Stress durations were limited to 60 s in order to minimize the stress history for the measurements in the following atmospheres.

The evolution of the drain current with stress time in all atmospheres and in vacuum for a transistor with $d = 6$ nm is shown in figure 5.6a. While the stress behavior in a dry nitrogen atmosphere is very similar to that in vacuum, the presence of dry oxygen, water vapor or a combination of both leads to much more pronounced bias-stress-induced degradations of the drain current, with the most severe degradation in a wet oxygen atmosphere. The transfer characteristics measured 5 min after filling the chamber with the corresponding gas, but prior to bias stress are shown in figure 5.6b. In both the water vapor and the wet oxygen atmosphere, the threshold voltage is shifted to higher values. In addition, the charge-carrier mobility is smaller in the water atmosphere.

In single-crystal PDI-FCN_2 transistors, Barra et al. observed a remarkable bias-stress

stability in vacuum as well as in ambient air, with a decrease of the drain current by only 10 % after one week of stressing in air [107]. In the context of the stress measurements discussed above, this excellent bias stress stability in air is probably due to the fact that in these single-crystal transistors, the interface between the gate dielectric and the semiconductor (and hence the carrier channel) is protected from the atmosphere by the approximately 1-μm-thick semiconductor crystal.

Figure 5.7a illustrates the influence of different atmospheres on the development of the drain current under bias stress for a transistor with a nominal semiconductor thickness of 21 nm and contact lengths of $L_{C,S} = 2.4$ μm and $L_{C,D} = 2.6$ μm. In vacuum, dry nitrogen and dry oxygen, the behavior is similar to that of the transistor with $d = 6$ nm. However, in a water atmosphere, the drain current features an unexpected and significant increase during bias stress. As can be seen in the transfer characteristics measured before and after bias stress in figure 5.7b, a normal shift of the threshold voltage is observed after the bias stress. However, as depicted in the inset, there is a simultaneous and uniform decrease of the contact resistance over the entire $V_{GS} - V_{th}$ range to approximately half of the initial value. In the subsequent bias stress experiment in a mixed water/oxygen atmosphere, no such contact resistance reduction was observed.

The origin of this behavior may be chemical doping of the bulk semiconductor by water molecules. Since the gate-field-induced charge-carrier density far away from the dielectric/semiconductor interface is small, the amount of charge carriers in that region would be significantly increased by doping, thereby decreasing the contact resistivity. This would also explain why such a behavior was not observed for $d = 6$ nm, since the gate-field-induced charge-carrier density is relatively large throughout the small thickness of the film. In a mixed water/oxygen atmosphere, the water content might be too small to see this phenomenon.

5.3 Conclusion

The shelf-life and bias-stress stability of flexible PDI-FCN$_2$ transistors was analyzed. The transistors can be operated in air and show a shelf-life stability that is relatively good for n-channel organic TFTs. Nevertheless, the threshold voltage, the intrinsic mobility and the contact resistance were found to degrade during long-term storage in ambient atmosphere. The strongest degradation was observed for TFTs with thinner semiconductor films, which is probably due to the protective effect of additional PDI-FCN$_2$ layers against the penetration and diffusion of ambient molecules to the accumulation layer.

PDI-FCN$_2$ transistors were found to be quite sensitive to bias stress, again with higher sensitivity for thinner semiconductor films. Both the threshold voltage and the intrinsic mobility degrade during bias stress, but recover slowly once the bias is removed. While

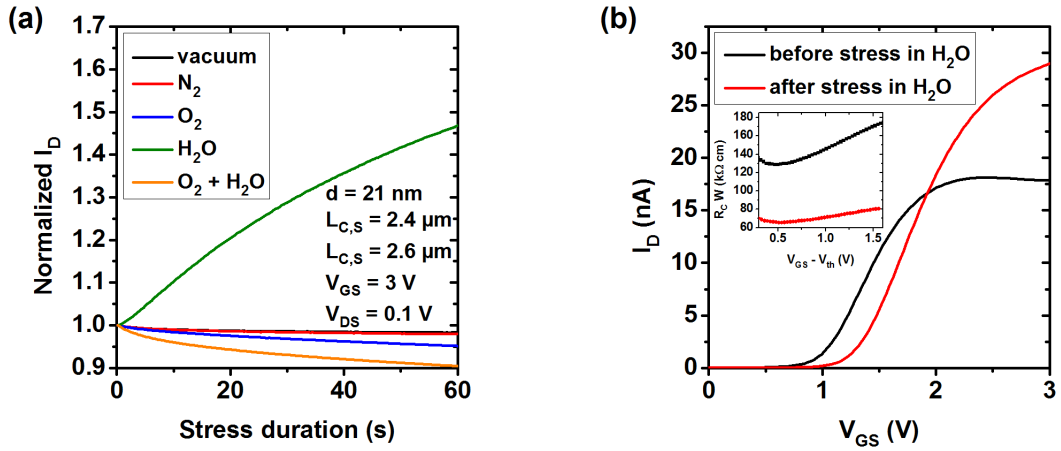


Figure 5.7: **Influence of the atmosphere on the bias-stress stability of a transistor with d = 21 nm.** (a) Evolution of the drain current during bias stress at V_{GS} = 3 V and V_{DS} = 0.1 V in different atmospheres. (b) Transfer curve measured in a water atmosphere before and after bias stress. Inset: Width-normalized contact resistance as a function of the gate overdrive voltage before and after bias stress in water vapor.

the initial threshold voltage is nearly restored within two days, the recovery of the intrinsic mobility is slower and its degradation is probably not completely reversible. The threshold-voltage shift was found to be more pronounced at higher gate-source voltages, but to be independent of the drain-source voltage. No distinct bias dependence of the degradation of the intrinsic mobility was observed.

Bias-stress measurements in different atmospheres have revealed the origin of the bias-stress sensitivity: while the PDI-FCN_2 transistors are very stable in vacuum and in a nitrogen atmosphere, bias stress in oxygen and water atmospheres has a significant impact on the transistor performance. Apparently, the trap states responsible for the bias-stress sensitivity are generated by oxygen and water molecules that diffuse into the organic layer. In transistors with relatively thick organic semiconductor films, an unusual increase of the drain current during bias stress in water vapor was observed, caused by a significant reduction of the contact resistance. More experiments are necessary to understand this phenomenon.

6 Dynamic characterization of integrated circuits

The GFP analysis of the PDI-FCN_2 thin-film transistors revealed various fascinating contact properties. Ultimately, the contact resistance is most important in transistors with small channel lengths, where it can become dominant over the channel resistance and limit the device performance. Transistors with reduced channel lengths are necessary to enable high switching frequencies during dynamic operation, and optimized contact resistances are essential to reach this goal.
In chapter 4 it was shown that very small contact resistances are achievable in the n-channel PDI-FCN_2 transistors. Since n-channel transistors are generally the limiting part in complementary organic transistor circuits, these transistors are therefore ideal candidates to realize high-frequency operation in such circuits.
The performance of such circuits, namely complementary inverters and ring oscillators, is analyzed in this chapter. The corresponding p-channel transistors, necessary for complementary logic, were realized by using DNTT as the organic semiconductor. DNTT transistors have already shown excellent performance in terms of charge-carrier mobility, contact resistance and stability [16, 84, 146, 154, 194].
Complementary ring oscillators based on PDI-FCN_2 (d = 6 nm) and DNTT TFTs are demonstrated in section 6.1, and the dependence of the oscillation frequency on the channel and contact lengths is explored. Section 6.2 presents a comparison with circuit simulations based on SPICE to explore the suitability of this standard simulation tool for organic circuits.

6.1 Ring oscillator performance

The dynamic performance of TFTs can be analyzed in stand-alone transistors using S-parameter measurements [135, 136], admittance characterization [200] and the unity-gain method [201]. An alternative approach is the fabrication and characterization of ring oscillators, which are circuits composed of an odd number n_{st} of inverter stages arranged in a closed loop, as depicted in figure 6.1a. An inverter is a basic building block of digital circuits, a logic gate that performs the negation on a single input variable. A circuit

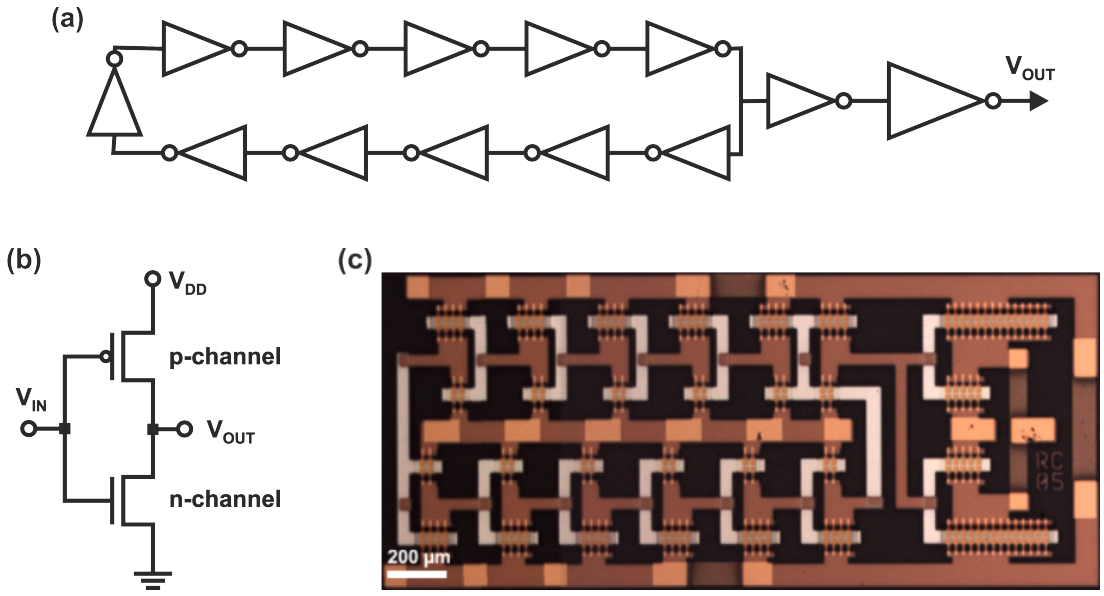


Figure 6.1: **Complementary inverter and ring oscillator.** (a) Circuit diagram of an 11-stage complementary ring oscillator with two additional inverters for decoupling and driving of the output capacitance. (b) Circuit diagram of a complementary inverter. (c) Photograph of an 11-stage complementary ring oscillator based on organic TFTs.

diagram of a complementary inverter is shown in figure 6.1b; a detailed description of the operation principle can be found in [81]. In short, the output voltage V_{OUT} is high and equal to the supply voltage V_{DD} at low input voltages V_{IN} around 0 V, but close to 0 V at high input voltages around V_{DD}. Since high voltages represent the logic value ”1” and low voltages represent the logic value ”0”, the inverter’s output is the logical NOT of the input.

The static voltage transfer characteristics of an organic complementary inverter with channel lengths of 2 μm and contact lengths of 10 μm is shown in figure 6.2a, measured for supply voltages of 1 V, 2 V and 3 V. The input voltage at which the inverter switches is not representive for the ring oscillators discussed later, because it is shifted to higher values due to bias stress, but the shape of the transfer curve is still representative. The inverter exhibits a full output voltage swing between 0 V and V_{DD} and a sharp transition with a small-signal gain (slope of the voltage transfer characteristics) of up to 27 (figure 6.2b). An image of the inverter is shown in the inset of figure 6.2b. The (total) channel width is 40 μm for the p-channel and 80 μm for the n-channel transistor to compensate for the smaller mobility in the n-channel devices. Due to technical reasons related to the mechanical stability of the stencil mask, the source and drain contacts are divided into parallel fingers with a width of 20 μm.

Due to the odd number of inverter stages in a ring oscillator n_{st}, the output of the last

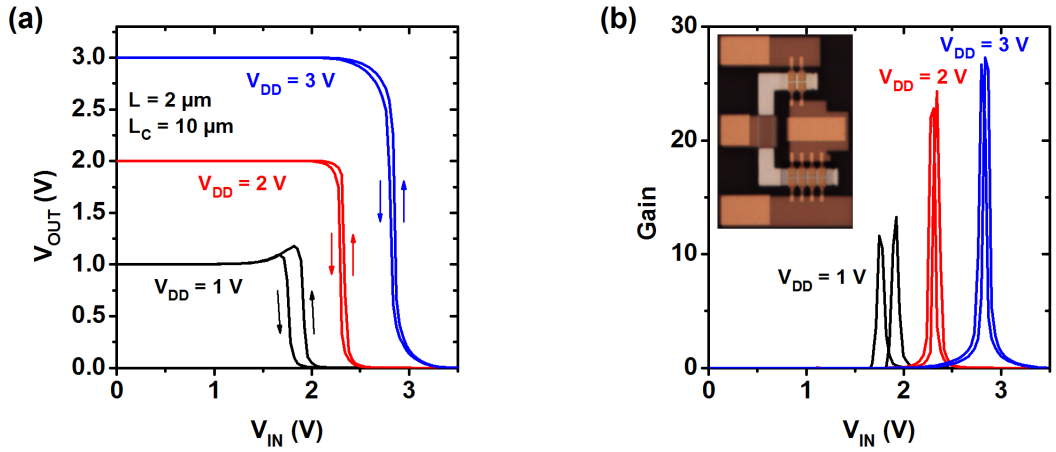


Figure 6.2: **Voltage transfer characteristics of a complementary inverter.** (a) Output voltage as a function of the input voltage of a complementary organic inverter, employing PDI-FCN_2 and DNTT transistors with channel lengths of 2 μm. (b) Corresponding small-signal gain as a function of the input voltage. Inset: Photograph of the inverter.

inverter is the opposite of the former input of the first inverter, and the feedback causes an oscillation that starts spontaneously above a certain supply voltage. The frequency f_{osc} of this oscillation is a function of the capacitance of each inverter stage that is charged or discharged by the output of the last inverter, delaying the signal propagation in the loop by a time τ. Since a phase shift of 2π is necessary for a self-sustained oscillation, the signal travels through the ring twice, leading to a total oscillation period of $2n_{st}\tau$. Accordingly, the oscillation frequency of the ring oscillator can be expressed by [81]:

$$f_{osc} = \frac{1}{2n_{st}\tau}, \tag{6.1}$$

where $n_{st} = 11$ in this work.

In principle, inverters and ring oscillators can also be realized in the unipolar design (using only n-channel or p-channel transistors), but the complementary architecture is superior in terms of steady-state power-dissipation, noise immunity, gain and output voltage swing range [31, 81].

The optical microscopy image in figure 6.1c shows one of the organic complementary ring oscillators investigated in this work. As also depicted in the circuit diagram in figure 6.1a, two additional inverters are added between the loop and the output. The first one has the same geometric dimensions as the inverters in the loop and is used to decouple the signal in the loop from the output load. The second inverter is significantly larger, with total channel widths of 560 μm for the n-channel and 200 μm for the p-channel transistors, to preserve the full output voltage swing in the case of (relatively) large output capacitances

connected with the oscilloscope and the cables. This large second inverter is divided into two parallel parts to allow operation in case of damages by simply separating one part by scratching.

Several organic complementary ring oscillators were fabricated on a flexible PEN substrate. The signal delay per stage measured as a function of the supply voltage is shown in figure 6.3 for various channel and contact lengths. All ring oscillators start oscillating at small supply voltages of 1 V. The dynamic performance of the ring oscillators is observed to improve at higher supply voltages and at both reduced channel and contact lengths, in agreement with the expectations (section 2.5). Increased supply voltages lead to higher drain currents of the individual transistors, allowing a faster charging of the load capacitance of an inverter stage, which is the parasitic capacitance of the following inverter stage. The drain currents also benefit from smaller channel lengths, although this is partially compensated by a decrease of the effective mobility due to an increased influence of the contact resistances. However, as shown in table 6.1, this decrease is small due to the low contact resistances, so that the effective mobility in the n-channel transistors drops by only about 20 % when the channel length is reduced from 8 μm to 2 μm. A reduced channel length also decreases the parasitic capacitances, just like a reduced contact length. In both cases, the dynamic performance is enhanced.

The minimum signal delay per stage obtained is 6 μs for a channel length of 4 μm, a contact length of 2 μm and a supply voltage of 3.6 V. This is smaller or comparable to the minimum literature values reported for flexible organic complementary ring oscillators [115, 202–205].

A main issue preventing even smaller signal delays per stage is bias stress. Figure 6.4a plots the development of the oscillation frequency of a ring oscillator with $L = 4$ μm and $L_C = 10$ μm as a function of the operation time at $V_{DD} = 3.6$ V. After 80 s, the frequency dropped below 80 % of the initial value. The reason for this is bias stress that degrades the threshold voltage and intrinsic mobility of the n-channel TFTs (see section 5.2). The p-channel DNTT transistors cannot be responsible for this effect, because bias stress appears to have only little influence on these transistors. As illustrated in figure 6.4b, bias stress at V_{GS} = -3 V and V_{DS} = -0.1 V in the DNTT TFTs even results in a small initial increase of the drain current due to a reduced absolute value of the threshold voltage. The reason for this unexpected shift in the direction opposite of the applied voltage is unknown so far, but GFP investigations (not shown here) revealed that indeed the intrinsic threshold voltage is affected, i.e., contact effects are not responsible. In order to minimize the bias stress for the following measurements, the measurements were done using ascending supply voltages. However, this leads to an increasing bias-stress as V_{DD} is raised, resulting in a lower performance at high supply voltages.

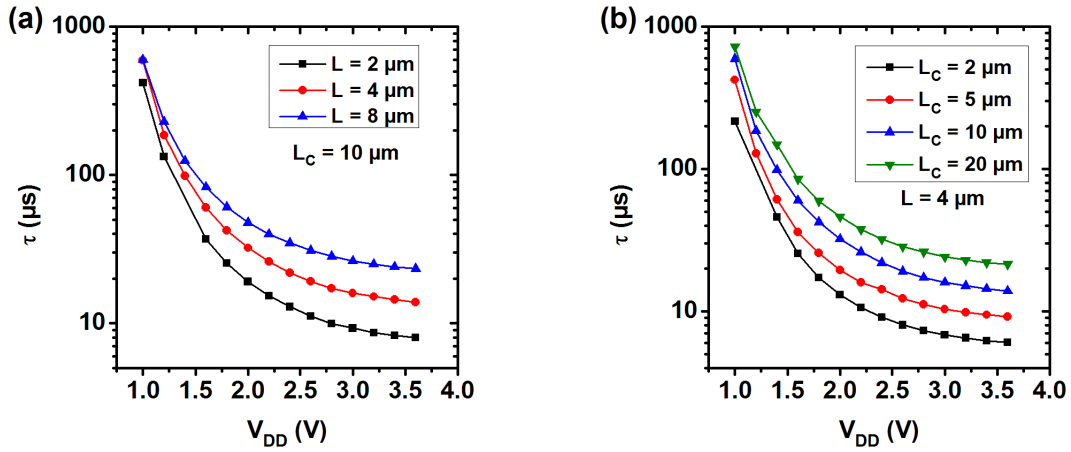


Figure 6.3: **Impact of channel and contact length on the ring oscillator performance.** Signal delay per stage measured as a function of the supply voltage for complementary organic ring oscillators employing transistors with various (a) channel lengths and (b) contact lengths. The ring oscillators operate with supply voltages as low as 1 V and reach signal delays per stage as small as 6 μs.

6.2 SPICE modeling

SPICE (Simulation Program with Integrated Circuit Emphasis) is an open-source general purpose circuit simulator. This sections contains a comparison of the ring oscillator experimental data with simulation results obtained from SPICE modeling. This is useful for two reasons: One is that a comparison of experimental data with analytical models is difficult due to the complex and dynamic nature of the system. Equations 2.30 and 2.31 only estimate the cutoff frequency of single unipolar transistors in one region of operation. The other reason is that SPICE is very widely used both in the microelectronics industry and in educational institutions, meaning that the possibility of a reliable SPICE simulation is important for circuit design.

The inset of figure 6.5a depicts the circuit diagram of the inverter model used for the SPICE simulations. A simple model was used in which all parasitic capacitances that are not part of the ideal transistors are summarized in C_n and C_p and are added to the source and drain capacitances of the n-channel and p-channel transistors. C_n and C_p are composed of the fringe capacitances beyond the edges of the channel defined by the width of the source/drain contacts where an organic semiconductor/gate dielectric/gate layer stack exists. The fringe capacitances are present in between the parallel fingers of the transistor (5 μm separation) and outside the fingers, because the organic semiconductor layer extends beyond the periphery of the source/drain contacts by 20 μm on each side in order to simplify the alignment. C_n and C_p also include the overlap capacitances C_{ov}. For

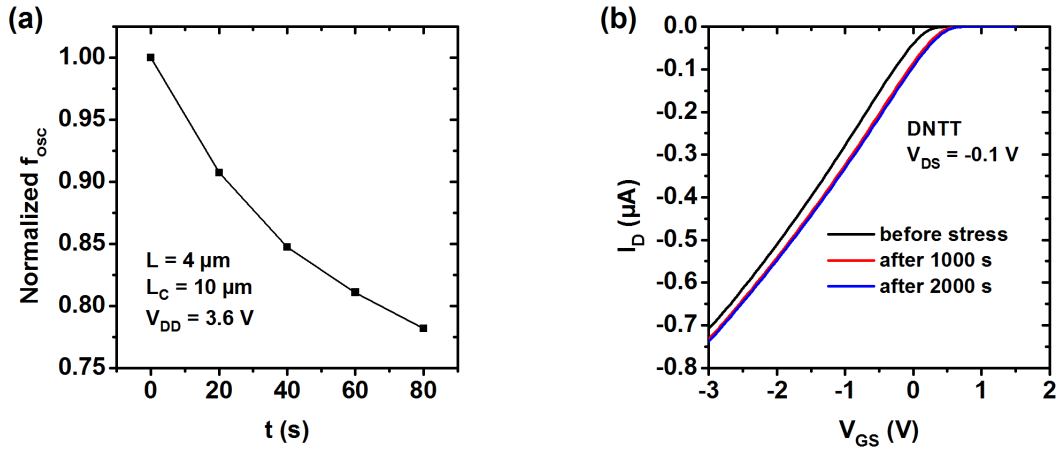


Figure 6.4: **Bias-stress effects in complementary ring oscillators.** (a) Normalized oscillation frequency at V_{DD} = 3.6 V measured over time on a ring oscillator with L = 4 μm and L_C = 10 μm. (b) Transfer curves in the linear regime of operation (V_{DS} = -0.1 V) of DNTT transistors before and after bias stress measured at V_{GS} = -3 V and V_{DS} = -0.1 V. A threshold-voltage shift in the direction opposite of the applied bias is observed.

the transistors, the standard SPICE MOSFET model level 1 was incorporated (identical results were obtained for level 3) that treats the channel capacitance according to Meyer's model, which was recently found to be valid in OTFTs [200]. Transistor parameters for the SPICE simulation were obtained from measurements on individual reference transistors that were fabricated next to the ring oscillators using the same geometries and dimensions as in the ring oscillators. Effective threshold voltages and mobilities at V_{DS} = 3 V were used for this purpose; the measured values averaged over two devices are given in table 6.1.

		n-channel		p-channel	
L (μm)	L_C (μm)	μ_{eff} (cm^2/Vs)	$V_{th,eff}$ (V)	μ_{eff} (cm^2/Vs)	$V_{th,eff}$ (V)
8	10	0.46	1.40	1.30	0.06
4	10	0.41	1.48	0.94	0.04
2	10	0.36	1.67	0.84	0.02
4	20	0.43	1.56	1.12	0.05
4	5	0.40	1.61	0.85	0.13
4	2	0.42	1.65	0.88	0.12

Table 6.1: **Transistor parameters as reference for the ring oscillators.** Summary of the effective mobility and effective threshold voltage of the reference transistors. Measurements were performed at V_{DS} = 3 V. All parameters were averaged over two devices.

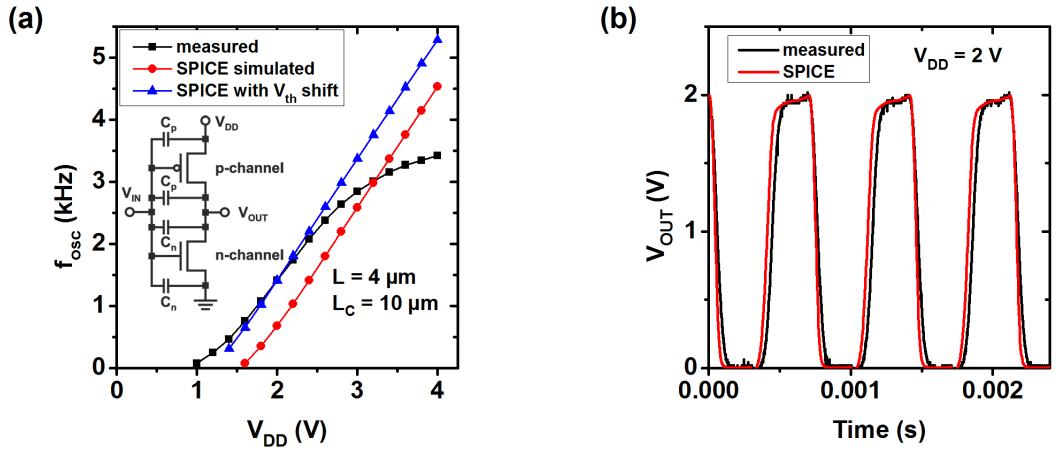


Figure 6.5: **Ring oscillator performance and SPICE simulation.** (a) Oscillation frequency of a complementary ring oscillator with a channel length of 4 μm and a contact length of 10 μm measured as a function of the supply voltage. A comparison with values obtained from a SPICE simulation using the parameters of table 6.1 and with shifted threshold voltage is shown. Inset: Circuit diagram of the inverter model used in the SPICE simulations. (b) Output signal of the ring oscillator at $V_{DD} = 2$ V. A full swing between 0 V and V_{DD} is observed. The shape of the output signal is very similar to the one obtained by a SPICE simulation with a shifted threshold voltage.

The oscillation frequency measured as a function of the supply voltage is shown in figure 6.5a for a ring oscillator with a channel length of 4 μm and a contact length of 10 μm. The measured data shows a start of the oscillation at a supply voltage of around 1 V, followed by a superlinear increase of the oscillation frequency with V_{DD}, probably due to subthreshold operation of at least one transistor. At higher V_{DD}, the slope of the curve continuously decreases due to bias-stress effects (see above). The simulated curve is shifted with respect to the measured one. This is probably because the transfer curves measured to extract the effective threshold voltages listed in table 6.1 were obtained using a V_{GS} sweep range of 3 V, resulting in a higher threshold voltage compared to a device operated at lower voltages (section 5.2.1). To account for that and to allow a better comparison, the value of the threshold voltage of the n-channel transistors that is used as a simulation parameter was therefore reduced by 0.35 V, so that the two curves coincide at a supply voltage of 2 V, which is the voltage at which the slope of the measured curve has its maximum. The increase of f_{osc} with V_{DD} for both the measured and the simulated curve is comparable in this region, indicating that the simple model is applicable. A comparison of a measured and a simulated (with V_{th} shift) output signal at $V_{DD} = 2$ V in figure 6.5b indicates a very similar shape of both curves, with a full swing between 0 V and V_{DD}. Using these results, it is possible to further investigate the dependence of the oscillation

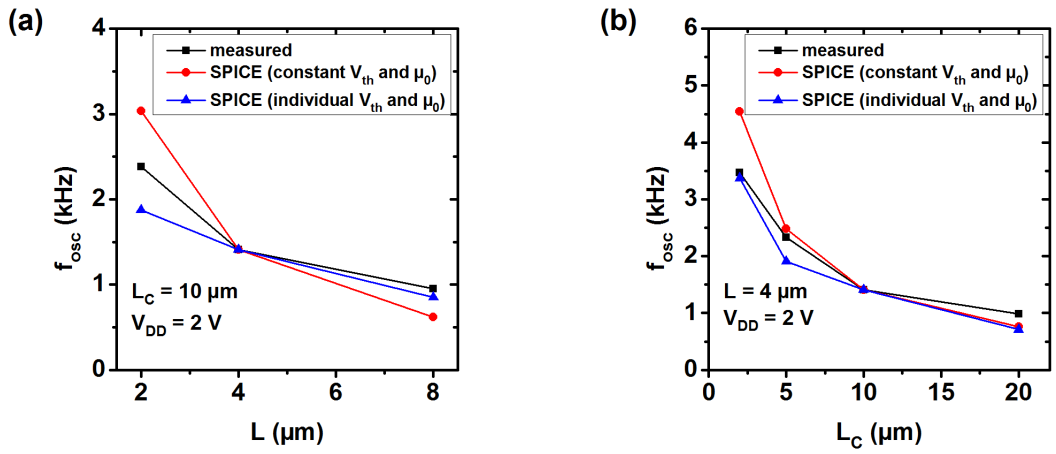


Figure 6.6: **Channel and contact length dependence of the oscillation frequency and comparison with SPICE results.** Measured oscillation frequency of the organic complementary ring oscillators at a supply voltage of 2 V as a function of the (a) channel length and (b) contact length (black data points). A comparison with SPICE simulation results is shown for a constant threshold voltage and mobility obtained from measurements on the reference transistors with the dimensions $L = 4$ μm and $L_C = 10$ μm (red data points) and with varying device parameters according to table 6.1 (blue data points). In both cases, all threshold voltages were reduced by 0.35 V.

frequency on the lateral dimensions. Figure 6.6 illustrates the impact of the channel and contact lengths on the oscillation frequency at a supply voltage of 2 V. As was seen in figure 6.3, the ring oscillators switch faster when the TFTs have smaller channel and contact lengths. A comparison with SPICE simulation results is also shown to investigate whether the the oscillation frequency scales in accordance with the standard MOSFET theory. One set of SPICE simulations was performed using a constant threshold voltage and mobility obtained from the reference transistor with the dimensions $L = 4$ μm and $L_C = 10$ μm, while another set of simulations is based on the individual parameters from table 6.1. In both cases, all threshold voltages were reduced by 0.35 V to match experimental and simulation results for $L = 4$ μm and $L_C = 10$ μm.

In the simulations with constant threshold voltages and effective mobilities, the oscillation frequency varies too rapidly with the channel or contact length. Due to the influence of the contact resistance, reduced channel and contacts lengths generally degrade the effective mobility and threshold voltage, partly compensating the positive effect of the lower parasitic capacitances. Considering this effect by the use of individual device parameters leads to a much better matching of the simulation results with the experimental data.

6.3 Conclusion

Organic complementary circuits on flexible substrates were fabricated and their dynamic performance was analyzed in air. Ring oscillators with various channel and contact lengths down to 2 μm were realized, having signal delays per stage as small as 6 μs. Even faster operation speeds would be achievable by using further reduced channel lengths, which is in principle possible using the silicon stencil mask technique [146, 154]. Bias-stress effects in the n-channel transistors were found to be a major problem of the complementary circuits, causing an unstable oscillation frequency. Effective encapsulation might solve this problem since PDI-FCN_2 transistors were found to have a high bias-stress stability when they are protected from the ambient atmosphere. Experimental results of the ring oscillators were compared with SPICE simulations using a simple model. A good agreement was observed when comparing the dependence of the oscillation frequency on the supply voltage, channel length and contact length, indicating that the organic circuits behave similar to standard MOSFET devices and that the design of organic circuits via standard tools like SPICE is possible.

7 Summary and outlook

High-mobility, low-voltage, air-stable organic thin-film transistors (TFTs) were fabricated on flexible plastic substrates and characterized by various techniques. The transistors are based on the small-molecule organic semiconductor N,N'-bis-(1H,1H-heptafluorobutyl)-1,7-dicyano-perylene-3,4:9,10-tetracarboxylic diimide (PDI-FCN_2) and operate as n-channel devices. A powerful method was used for a deep analysis of the contact properties, revealing the impact of various factors on the contact resistance. The stability of the transistors while stored or operated continuously in air was investigated. Since high-performance organic n-channel TFTs are essential for the realization of low-power complementary circuits, 11-stage complementary organic ring oscillators were fabricated, and their excellent dynamic performance has been demonstrated.

Various methods are available for the contact-resistance analysis in organic TFTs, and all of them have advantages and drawbacks. The simplest techniques in terms of experimental effort are based on the modeling of the electrical characteristics of individual transistors. However, the reliability of these procedures is impaired by the assumptions and simplifications that are necessary for the applicability of the models. The most popular technique for the contact-resistance extraction is the transmission line method (TLM) that requires a set of transistors with different channel lengths. Problematic for TLM are transistor parameter fluctuations and nonlinear contact resistances. Kelvin probe force microscopy (KPFM) is the most detailed technique, but it is also the experimentally most challenging method and it requires relatively long measurement times, which can be problematic for transistors with a high sensitivity towards bias stress. In this work, the gated four-probe (GFP) method was employed. It requires a special transistor layout, but needs only a few basic assumptions and the electrical characteristics of a single transistor, thus making it very reliable. The source resistance and the drain resistance can be analyzed separately, and the use of a slightly adapted version of an advanced GFP method introduced by Richards et al. [114] gives access to the contact resistance at high drain-source voltages.

The organic TFTs were fabricated in a staggered architecture, which usually allows smaller contact resistances than the coplanar architecture [80, 111]. High-resolution patterning of all layers was accomplished using silicon stencil masks. Low-voltage transistor operation was realized by using a thin hybrid gate dielectric consisting of oxygen-plasma-grown aluminum oxide and a self-assembled monolayer (SAM) of phosphonic acid molecules

with a fluorinated alkyl chain. TFTs with various nominal thicknesses of the organic semiconductor layer were fabricated and considered in the contact-resistance analysis. The quality of the organic films was investigated using atomic force microscopy (AFM) and scanning electron microscopy (SEM). The set of desirable properties present in the TFTs, namely high charge-carrier mobility, low-voltage operation, air stability, n-channel operation and mechanical flexibility of the substrate, provides a meaningful environment for the contact-resistance analysis.

Using the gated four-probe method, the contact properties were explored by examining the dependence of internal and external factors on the contact resistance. First, the gate-source voltage dependence of the contact resistance was investigated. A rapid decrease of the contact resistance with increasing gate-source voltage was found for transistors with a thin organic semiconductor layer, which gradually weakens and finally turns into an increase as the semiconductor film is made thicker. The observation that various, often quite different dependencies of the contact resistance on the gate-source voltage are possible is important and has significant and general consequences for the electrical analysis of organic transistors. Parameters of organic TFTs are usually determined from transfer curves. An undetermined gate-source voltage dependence of the contact resistance can alter the shape of the transfer curve in a quite arbitrary way. If contact effects are not carefully considered, which is often the case in the literature, it is unforeseeable if the extracted parameters are overestimations or underestimations of the intrinsic values, greatly impairing the usefulness, comparability and physical meaning of these parameters. The lowest contact resistances are obtained for transistors with a very thin organic semiconductor layer of only 6 nm thickness. As can be seen in the literature, this is not generally true for organic transistors [17, 206], but it highlights the importance of a careful thickness optimization of the organic film. In this case, the optimization led to a very small width-normalized contact resistance of only about 0.6 $k\Omega\,cm$, which is one of the best values for organic n-channel transistors, especially when considering that no special contact treatment was performed and that the transistors were operated in air.

The current crowding model proved to be very useful for the analysis of staggered TFTs, since it can explain various effects simply by disentangling the various contact resistance components. By investigating the contact-length dependence of the contact resistance over a wide range, the current crowding model was found to be valid for all nominal semiconductor thicknesses, provided the voltage drop across the contact regions is small. Larger voltage drops across the contact regions can be present when using large drain-source voltages. Under such conditions, the contact resistance remains ohmic in the case of a small semiconductor thickness. In TFTs with a thick organic semiconductor layer, however, large voltage drops across the contacts lead to nonlinear current-voltage characteristics. Schottky barriers can be ruled out as the origin of this behavior, also because

the source and drain resistances are identical in magnitude and parameter dependence. Instead, the nonlinear behavior is probably caused by space-charge-limited currents that occur due to the small charge-carrier density in the bulk semiconductor.
Variable-temperature measurements of the channel and contact resistances revealed a weak temperature dependence. Assuming an Arrhenius-like behavior, small activation energies in the range of 3 meV to 50 meV were extracted. Contact-resistivity activation energies are larger than those of the channel resistance and increase with the thickness of the organic semiconductor layer. The gate-source voltage has no impact on the activation energies. Together with other results, the temperature-dependent measurements make it possible to draw conclusions about the charge-transport mechanisms in the transistors. The best agreement with experimental observations is obtained for Mott's Model that describes variable-range hopping in a constant density of states. The most common charge-transport models for organic TFTs deviate in several essential predictions.
Based on the contact-resistance analysis, conclusions were drawn about the responsible mechanisms. In the case of TFTs with a very thin organic semiconductor layer, it is proposed that the gate-source voltage-induced charge carriers modulate either the energy barrier at the metal/semiconductor interface and/or that of hopping transport in the direction perpendicular to the gate dielectric/organic semiconductor interface. Thermionic emission over significant energy barriers at the metal/semiconductor interface can be ruled out as relevant process. In the case of TFTs with a relatively thick organic semiconductor layer, the interface resistivity is believed to be insignificant. Instead, the transport through the bulk semiconductor is supposed to be the limiting process due to the probably small carrier mobility in the vertical direction.
Stability is a serious issue in potential organic transistor applications. The PDI-FCN_2 TFTs were stored in a cleanroom or subjected to a constant bias in order to investigate the shelf-life and bias-stress stability. In both cases the degradation is smaller for thicker organic semiconductor films, indicating a protective effect of additional semiconductor material. While the shelf-life stability is good, the transistors are quite susceptible to bias stress. Measurements in various atmospheres showed that bias-stress effects are caused by oxygen and water. Since very stable operation is possible in vacuum or an inert atmosphere, effective encapsulation layers may be helpful for improving the bias-stress stability of the transistors.
The dynamic performance of the transistors was analyzed using flexible organic integrated circuits. Low-voltage 11-stage complementary ring oscillators were realized using DNTT transistors as the p-channel counterparts. A full swing of the output voltage between 0 V and the supply voltage was observed. Ring oscillators with a channel length of 4 μm and a contact length of 2 μm have a signal delay per stage of 6 μs at a supply voltage of 3.6 V, which is smaller than or similar to the minimum literature values reported for

flexible organic complementary ring oscillators operated at supply voltages below 10 V. An even better performance should be possible by employing smaller channel lengths and by reducing bias-stress effects. The response of the ring oscillators was successfully simulated using a simple SPICE model. The dependence of the oscillation frequency on the channel and contact length is in accordance with standard MOSFET theory.

Further insight into the contact properties of PDI-FCN_2 TFTs may be obtained using transistors in the bottom-gate, bottom-contact (inverted coplanar) configuration, which is in principle compatible with the fabrication technology used in this work. Coplanar transistors usually have larger contact resistances, but they allow a more direct investigation of the source and drain metal/organic semiconductor interface, since there is no additional contribution from the transport through the bulk semiconductor. In addition, novel surface treatments that are only available in the bottom-contact geometry greatly reduce detrimental effects of the underlying source/drain metal on the semiconductor morphology and allow a good and well-defined control over the work function of the source/drain contacts [207–209].

Device simulations can be helpful to understand the physical mechanisms in the transistors by comparing and adjusting simulation results with experimental data. Therefore, in cooperation with the University of Ilmenau, two-dimensional numerical simulations of the PDI-FCN_2 transistors are ongoing in order to gain further insight into their contact properties.

In silicon technology, contact resistances are effectively reduced by doping. Contact doping in organic semiconductors is demanding and poorly understood, especially in n-channel devices. Preliminary attempts of contact doping in PDI-FCN_2 transistors showed no improvement of the contact properties. However, major improvements in the technological understanding and in the material development of organic semiconductor dopants were recently reported, raising hopes that controlled doping may become a standard process in organic transistor technology [83, 85, 210]. Therefore, future attempts to reduce the contact resistance of organic n-channel transistors should include contact doping with novel dopants.

Bibliography

[1] J. E. Lilienfeld. *Method and apparatus for controlling electric currents* (1930). US Patent 1745175.

[2] O. Heil. *Improvements in or relating to electrical amplifiers and other control arrangements and devices* (1935). British Patent 439457.

[3] D. Kahng. *Electric field controlled semiconductor device* (1963). US Patent 3102230.

[4] P. K. Weimer. *The TFT a new thin-film transistor.* Proc. IRE **50**, 1462 (1962).

[5] W. Brütting, S. Berleb, and A. G. Mückl. *Device physics of organic light-emitting diodes based on molecular materials.* Org Electron. **2**, 1 (2001).

[6] J. H. Burroughes, D. D. C. Bradley, A. R. Brown, R. N. Marks, K. Mackay, R. H. Friend, P. L. Burns, and A. B. Holmes. *Light-emitting diodes based on conjugated polymers.* Nature **347**, 539 (1990).

[7] Y.-J. Cheng, S.-H. Yang, and C.-S. Hsu. *Synthesis of conjugated polymers for organic solar cell applications.* Chem. Rev. **109**, 5868 (2009).

[8] S. Günes, H. Neugebauer, and N. S. Sariciftci. *Conjugated polymer-based organic solar cells.* Chem. Rev. **107**, 1324 (2007).

[9] K. M. Coakley and M. D. McGehee. *Conjugated polymer photovoltaic cells.* Chem. Mater. **16**, 4533 (2004).

[10] G. H. Heilmeier and L. A. Zanoni. *Surface studies of α-copper phthalocyanine films.* J. Phys. Chem. Solids **25**, 603 (1964).

[11] D. F. Barbe and C. R. Westgate. *Surface state parameters of metal-free phthalocyanine single crystals.* J. Phys. Chem. Solids **31**, 2679 (1970).

[12] A. Tsumura, H. Koezuka, and T. Ando. *Macromolecular electronic device: Field-effect transistor with a polythiophene thin film.* Appl. Phys. Lett. **49**, 1210 (1986).

[13] A. Tsumura, H. Koezuka, and T. Ando. *Polythiophene field-effect transistor: Its characteristics and operation mechanism.* Synth. Met. **25**, 11 (1988).

[14] G. Horowitz, D. Fichou, X. Peng, Z. Xu, and F. Garnier. *A field-effect transistor based on conjugated alpha-sexithienyl.* Solid State Commun. **72**, 381 (1989).

[15] Y.-Y. Lin, D. J. Gundlach, S. F. Nelson, and T. N. Jackson. *Stacked pentacene layer organic thin-film transistors with improved characteristics.* IEEE Electron Dev. Lett. **18**, 606 (1997).

[16] U. Zschieschang, F. Ante, D. Kälblein, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Someya, J. Blochwitz-Nimoth, and H. Klauk. *Dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) thin-film transistors with improved performance and stability.* Org. Electron. **12**, 1370 (2011).

[17] R. Hofmockel, U. Zschieschang, U. Kraft, R. Rödel, N. H. Hansen, M. Stolte, F. Würthner, K. Takimiya, K. Kern, J. Pflaum, and H. Klauk. *High-mobility organic thin-film transistors based on a small-molecule semiconductor deposited in vacuum and by solution shearing.* Org. Electron. **14**, 3213 (2013).

[18] Y. Yuan, G. Giri, A. L. Ayzner, A. P. Zoombelt, S. C. B. Mannsfeld, J. Chen, D. Nordlund, M. F. Toney, J. Huang, and Z. Bao. *Ultra-high mobility transparent organic thin film transistors grown by an off-centre spin-coating method.* Nat. Commun. **5** (2014).

[19] P. Lin and F. Yan. *Organic Thin-Film Transistors for Chemical and Biological Sensing.* Adv. Mater. **24**, 34 (2012).

[20] J. E. Anthony, D. L. Eaton, and S. R. Parkin. *A road map to stable, soluble, easily crystallized pentacene derivatives.* Org. Lett. **4**, 15 (2002).

[21] I. Yagi, N. Hirai, Y. Miyamoto, M. Noda, A. Imaoka, N. Yoneya, K. Nomoto, J. Kasahara, A. Yumoto, and T. Urabe. *A flexible full-color AMOLED display driven by OTFTs.* J. Soc. Inf. Display **16**, 15 (2008).

[22] G. H. Gelinck, H. Huitema, E. van Veenendaal, E. Cantatore, L. Schrijnemakers, J. van der Putten, T. Geuns, M. Beenhakkers, J. Giesbers, B. Huisman, E. J. Meijer, E. M. Benito, F. J. Touwslager, A. W. Marsman, B. J. E. van Rens, and D. M. de Leeuw. *Flexible active-matrix displays and shift registers based on solution-processed organic transistors.* Nat. Mater. **3**, 106 (2004).

[23] H. Sirringhaus. *25th Anniversary Article: Organic Field-Effect Transistors: The Path Beyond Amorphous Silicon.* Adv. Mater. **26**, 1319 (2014).

[24] T. Someya, Y. Kato, T. Sekitani, S. Iba, Y. Noguchi, Y. Murase, H. Kawaguchi, and T. Sakurai. *Conformable, flexible, large-area networks of pressure and thermal*

sensors with organic transistor active matrixes. Proc. Nat. Acad. Sci. U.S.A **102**, 12321 (2005).

[25] S. C. B. Mannsfeld, B. C. K. Tee, R. M. Stoltenberg, C. V. H. H. Chen, S. Barman, B. V. O. Muir, A. N. Sokolov, C. Reese, and Z. Bao. *Highly sensitive flexible pressure sensors with microstructured rubber dielectric layers.* Nat. Mater. **9**, 859 (2010).

[26] M. L. Hammock, A. Chortos, B. C.-K. Tee, J. B.-H. Tok, and Z. Bao. *25th Anniversary Article: The Evolution of Electronic Skin (E-Skin): A Brief History, Design Considerations, and Recent Progress.* Adv. Mater. **25**, 5997 (2013).

[27] S. R. Forrest. *The path to ubiquitous and low-cost organic electronic appliances on plastic.* Nature **428**, 911 (2004).

[28] K. Myny, S. Steudel, S. Smout, P. Vicca, F. Furthner, B. van der Putten, A. K. Tripathi, G. H. Gelinck, J. Genoe, W. Dehaene, and P. Heremans. *Organic RFID transponder chip with data rate compatible with electronic product coding.* Org. Electron. **11**, 1176 (2010).

[29] E. Cantatore, T. C. T. Geuns, G. H. Gelinck, E. van Veenendaal, A. F. A. Gruijthuijsen, L. Schrijnemakers, S. Drews, and D. M. de Leeuw. *A 13.56-MHz RFID system based on organic transponders.* IEEE J. Solid-State Circuits **42**, 84 (2007).

[30] V. Subramanian, P. C. Chang, J. B. Lee, S. E. Molesa, and S. K. Volkman. *Printed organic transistors for ultra-low-cost RFID applications.* IEEE Trans. Components Packag. Technol. **28**, 742 (2005).

[31] H. Klauk. *Organic thin-film transistors.* Chem. Soc. Rev. **39**, 2643 (2010).

[32] Y. Zhao, Y. Guo, and Y. Liu. *25th Anniversary Article: Recent Advances in n-Type and Ambipolar Organic Field-Effect Transistors.* Adv. Mater. **25**, 5372 (2013).

[33] A. Kekulé. *Ueber einige Condensationsproducte des Aldehyds.* Liebigs Ann. Chem. **162**, 77 (1872).

[34] I. Kymissis. *Organic Field Effect Transistors: Theory, Fabrication and Characterization.* Integrated Circuits and Systems (Springer, 2008).

[35] J. E. Anthony. *Functionalized acenes and heteroacenes for organic electronics.* Chem. Rev. **106**, 5028 (2006).

[36] H. Sirringhaus. *Charge Transport Physics of Solution-Processed Organic Field-Effect Transistors.* In Z. Bao and J. Locklin (editors) *Organic Field-Effect Transistors*, Optical Science and Engineering, chapter 2.3 (CRC Press, 2007).

[37] D. M. DeLongchamp and R. J. Kline. *Characterization of Order and Orientation in Semiconducting Polymers.* In H. Klauk (editor) *Organic Electronics II: More Materials and Applications*, chapter 2 (Wiley-VCH, 2012).

[38] A. Facchetti. *Semiconductors for organic transistors.* Mater. Today **10**, 28 (2007).

[39] W. Warta and N. Karl. *Hot holes in naphthalene: High, electric-field-dependent mobilities.* Phys. Rev. B **32**, 1172 (1985).

[40] R. Noriega and A. Salleo. *Charge Transport Theories in Organic Semiconductors.* In H. Klauk (editor) *Organic Electronics II: More Materials and Applications*, chapter 3 (Wiley-VCH, 2012).

[41] N. H. Hansen, F. May, D. Kälblein, T. Schmeiler, C. Lennartz, A. Steeger, C. Burschka, M. Stolte, F. Würthner, J. Brill, and J. Pflaum. *Anisotropic electron mobility studies on Cl2-NDI single crystals and the role of static and dynamic lattice deformations upon temperature variation.* arXiv preprint arXiv:1501.01856 (2015).

[42] V. Podzorov. *Charge Carrier Transport in Single-Crystal Organic Field-Effect Transistors.* In Z. Bao and J. Locklin (editors) *Organic Field-Effect Transistors*, Optical Science and Engineering, chapter 2.1 (CRC Press, 2007).

[43] G. Horowitz. *Charge Transport in Oligomers.* In Z. Bao and J. Locklin (editors) *Organic Field-Effect Transistors*, Optical Science and Engineering, chapter 2.2 (CRC Press, 2007).

[44] E. Silinsh and V. Cápek. *Organic molecular crystals: interaction, localization, and transport phenomena* (American Institute of Physics, New York, 1994).

[45] V. Coropceanu, J. Cornil, D. A. da Silva Filho, Y. Olivier, R. Silbey, and J.-L. Brédas. *Charge transport in organic semiconductors.* Chem. Rev. **107**, 926 (2007).

[46] A. Troisi. *Charge transport in high mobility molecular semiconductors: classical models and new theories.* Chem. Soc. Rev. **40**, 2347 (2011).

[47] P. G. Le Comber and W. E. Spear. *Electronic transport in amorphous silicon films.* Phys. Rev. Lett. **25**, 509 (1970).

[48] G. Horowitz, R. Hajlaoui, and P. Delannoy. *Temperature dependence of the field-effect mobility of sexithiophene. Determination of the density of traps.* J. Phys. III France **5**, 355 (1995).

[49] G. Horowitz, M. E. Hajlaoui, and R. Hajlaoui. *Temperature and gate voltage dependence of hole mobility in polycrystalline oligothiophene thin film transistors.* J. Appl. Phys. **87**, 4456 (2000).

[50] N. Tessler, Y. Preezant, N. Rappaport, and Y. Roichman. *Charge Transport in Disordered Organic Materials and Its Relevance to Thin-Film Devices: A Tutorial Review.* Adv. Mater. **21**, 2741 (2009).

[51] A. Miller and E. Abrahams. *Impurity conduction at low concentrations.* Phys. Rev. **120**, 745 (1960).

[52] N. F. Mott and W. D. Twose. *The theory of impurity conduction.* Adv. Phys. **10**, 107 (1961).

[53] N. F. Mott and E. A. Davis. *Electronic Processes in Non-Crystalline Materials* (OUP Oxford, 2012).

[54] C. Godet and J.-P. Kleider. *Disorder and localization in bandtail hopping transport: experiments and concepts.* J. Mater. Sci.: Mater. Electron. **17**, 413 (2006).

[55] V. Ambegaokar, B. I. Halperin, and J. S. Langer. *Hopping conductivity in disordered systems.* Phys. Rev. B **4**, 2612 (1971).

[56] M. C. J. M. Vissenberg and M. Matters. *Theory of the field-effect mobility in amorphous organic transistors.* Phys. Rev. B **57**, 12964 (1998).

[57] G. Horowitz. *Tunneling Current in Polycrystalline Organic Thin-Film Transistors.* Adv. Funct. Mater. **13**, 53 (2003).

[58] S. D. Ganichev, E. Ziemann, W. Prettl, I. N. Yassievich, A. A. Istratov, and E. R. Weber. *Distinction between the Poole-Frenkel and tunneling models of electric-field-stimulated carrier emission from deep levels in semiconductors.* Phy. Rev. B **61**, 10361 (2000).

[59] P. N. Murgatroyd. *Theory of space-charge-limited current enhanced by Frenkel effect.* J. Phys. D: Appl. Phys. **3**, 151 (1970).

[60] A. Rose. *Space-charge-limited currents in solids.* Phys. Rev. **97**, 1538 (1955).

[61] M. A. Lampert and P. Mark. *Current injection in solids.* Electrical science series (Academic Press, 1970).

[62] D. M. DeLongchamp, S. Sambasivan, D. A. Fischer, E. K. Lin, P. Chang, A. R. Murphy, J. M. J. Fréchet, and V. Subramanian. *Direct Correlation of Organic Semiconductor Film Structure to Field-Effect Mobility.* Adv. Mater. **17**, 2340 (2005).

[63] G. Horowitz. *Organic Transistors*. In H. Klauk (editor) *Organic Electronics: Materials, Manufacturing, and Applications*, chapter 1 (Wiley-VCH, 2006).

[64] J. R. Brews. *A charge-sheet model of the MOSFET*. Solid-State Electron. **21**, 345 (1978).

[65] D. I. James., J. Smith, M. Heeney, T. D. Anthopoulos, A. Salleo, and I. McCulloch. *Organic Semiconductor Materials for Transistors*. In H. Klauk (editor) *Organic Electronics II: More Materials and Applications*, chapter 1 (Wiley-VCH, 2012).

[66] S. D. Brotherton. *Introduction to Thin Film Transistors: Physics and Technology of TFTs* (Springer, 2013).

[67] S. M. Sze and K. K. Ng. *Physics of Semiconductor Devices* (Wiley, 2007).

[68] H.-S. Wong, M. H. White, T. J. Krutsick, and R. V. Booth. *Modeling of transconductance degradation and extraction of threshold voltage in thin oxide MOSFET's*. Solid-State Electron. **30**, 953 (1987).

[69] D. Boudinet, G. L. Blevennec, C. Serbutoviez, J.-M. Verilhac, H. Yan, and G. Horowitz. *Contact resistance and threshold voltage extraction in n-channel organic thin film transistors on plastic substrates*. J. Appl. Phys. **105**, 084510 (2009).

[70] H. Ishii, K. Sugiyama, E. Ito, and K. Seki. *Energy level alignment and interfacial electronic structures at organic/metal and organic/organic interfaces*. Adv. Mater. **11**, 605 (1999).

[71] S. Braun, W. R. Salaneck, and M. Fahlman. *Energy-Level Alignment at Organic/Metal and Organic/Organic Interfaces*. Adv. Mater. **21**, 1450 (2009).

[72] D. Natali and M. Caironi. *Charge Injection in Solution-Processed Organic Field-Effect Transistors: Physics, Models and Characterization Methods*. Adv. Mater. **24**, 1357 (2012).

[73] J. Hwang, A. Wan, and A. Kahn. *Energetics of metal–organic interfaces: new experiments and assessment of the field*. Mater. Sci. Eng.: R **64**, 1 (2009).

[74] C. Calandra, G. Chiarotti, U. Gradmann, K. Jacobi, F. Manghi, A. A. Maradudin, S. Y. Tong, and R. F. Wallis. *Physics of Solid Surfaces: Electronic and Vibrational Properties*. In G. Chiarotti (editor) *Landolt-Börnstein - New Series III/24b* (Springer, 1994).

[75] L. Mariucci, M. Rapisarda, A. Valletta, S. Jacob, M. Benwadih, and G. Fortunato. *Current spreading effects in fully printed p-channel organic thin film transistors with Schottky source–drain contacts.* Org. Electron. **14**, 86 (2013).

[76] V. Vinciguerra, M. L. Rosa, D. Nicolosi, G. Sicurella, and L. Occhipinti. *Modeling the gate bias dependence of contact resistance in staggered polycrystalline organic thin film transistors.* Org. Electron. **10**, 1074 (2009).

[77] J. J. Brondijk, F. Torricelli, E. C. P. Smits, P. W. M. Blom, and D. M. de Leeuw. *Gate-bias assisted charge injection in organic field-effect transistors.* Org. Electron. **13**, 1526 (2012).

[78] M. Rapisarda, A. Valletta, A. Daami, S. Jacob, M. Benwadih, R. Coppard, G. Fortunato, and L. Mariucci. *Analysis of contact effects in fully printed p-channel organic thin film transistors.* Org. Electron. **13**, 2017 (2012).

[79] M. Gruber, F. Schürrer, and K. Zojer. *Relation between injection barrier and contact resistance in top-contact organic thin-film transistors.* Org. Electron. **13**, 1887 (2012).

[80] M. J. Panzer and C. D. Frisbie. *Contact Effects in Organic Field-Effect Transistors.* In Z. Bao and J. Locklin (editors) *Organic Field-Effect Transistors*, Optical Science and Engineering, chapter 2.4 (CRC Press, 2007).

[81] S. M. Kang and Y. Leblebici. *CMOS Digital Integrated Circuits* (McGraw-Hill, 2005).

[82] D. Khim, K.-J. Baeg, M. Caironi, C. Liu, Y. Xu, D.-Y. Kim, and Y.-Y. Noh. *Control of Ambipolar and Unipolar Transport in Organic Transistors by Selective Inkjet-Printed Chemical Doping for High Performance Complementary Circuits.* Adv. Funct. Mater. (2014).

[83] B. Lüssem, M. L. Tietze, H. Kleemann, C. Hoßbach, J. W. Bartha, A. Zakhidov, and K. Leo. *Doped organic transistors operating in the inversion and depletion regime.* Nat. Commun. **4** (2013).

[84] F. Ante, D. Kälblein, U. Zschieschang, T. W. Canzler, A. Werner, K. Takimiya, M. Ikeda, T. Sekitani, T. Someya, and H. Klauk. *Contact Doping and Ultrathin Gate Dielectrics for Nanoscale Organic Thin-Film Transistors.* Small **7**, 1186 (2011).

[85] B. Lüssem, M. Riede, and K. Leo. *Doping of organic semiconductors.* Phys. Status Solidi A **210**, 9 (2013).

[86] I. Salzmann, G. Heimel, S. Duhm, M. Oehzelt, P. Pingel, B. M. George, A. Schnegg, K. Lips, R.-P. Blum, A. Vollmer, and N. Koch. *Intermolecular hybridization governs molecular electrical doping.* Phys. Rev. Lett. **108**, 035502 (2012).

[87] A. Mityashin, Y. Olivier, T. Van Regemorter, C. Rolin, S. Verlaak, N. G. Martinelli, D. Beljonne, J. Cornil, J. Genoe, and P. Heremans. *Unraveling the mechanism of molecular doping in organic semiconductors.* Adv. Mater. **24**, 1535 (2012).

[88] D. A. da Silva Filho, E.-G. Kim, and J.-L. Brédas. *Transport properties in the rubrene crystal: electronic coupling and vibrational reorganization energy.* Adv. Mater. **17**, 1072 (2005).

[89] A. Facchetti. *Conjugated Semiconductors for Organic n-Channel Transistors and Complimentary Circuits.* In H. Klauk (editor) *Organic Electronics II: More Materials and Applications*, chapter 1 (Wiley-VCH, 2012).

[90] B. A. Jones, M. J. Ahrens, M. H. Yoon, A. Facchetti, T. J. Marks, and M. R. Wasielewski. *High-Mobility Air-Stable n-Type Semiconductors with Processing Versatility: Dicyanoperylene-3, 4: 9, 10-bis (dicarboximides).* Angew. Chem. Int. Ed. **43**, 6363 (2004).

[91] B. A. Jones, A. Facchetti, M. R. Wasielewski, and T. J. Marks. *Tuning orbital energetics in arylene diimide semiconductors. Materials design for ambient stability of n-type charge transport.* J. Am. Chem. Soc. **129**, 15259 (2007).

[92] D. M. De Leeuw, M. M. J. Simenon, A. R. Brown, and R. E. F. Einerhand. *Stability of n-type doped conducting polymers and consequences for polymeric microelectronic devices.* Synth. Met. **87**, 53 (1997).

[93] H. T. Nicolai, M. Kuik, G. A. H. Wetzelaer, B. De Boer, C. Campbell, C. Risko, J. L. Brédas, and P. W. M. Blom. *Unification of trap-limited electron transport in semiconducting polymers.* Nat. Mater. **11**, 882 (2012).

[94] H. Jung, T. Lim, Y. Choi, M. Yi, J. Won, and S. Pyo. *Lifetime enhancement of organic thin-film transistors protected with organic layer.* Appl. Phys. Lett. **92**, 163504 (2008).

[95] C. Pannemann, T. Diekmann, U. Hilleringmann, U. Schuermann, M. Scharnberg, V. Zaporojtchenko, R. Adelung, and F. Faupel. *PTFE encapsulation for pentacene based organic thin film transistors.* Mater. Sci.-Poland **25** (2007).

[96] Y. Qiu, Y. Hu, G. Dong, L. Wang, J. Xie, and Y. Ma. *H_2O effect on the stability of organic thin-film field-effect transistors.* Appl. Phys. Lett. **83**, 1644 (2003).

[97] C. R. Newman, C. D. Frisbie, D. A. da Silva Filho, J. L. Brédas, P. C. Ewbank, and K. R. Mann. *Introduction to organic thin film transistors and design of n-channel organic semiconductors.* Chem. Mater. **16**, 4436 (2004).

[98] R. Colle, G. Grosso, A. Cassinese, and R. Centore. *Structural, electronic and vibrational properties of N, N'-1H, 1H-perfluorobutyl dicyanoperylenecarboxydiimide (PDI-FCN$_2$) crystal.* J. Chem. Phys. **139**, 114507 (2013).

[99] B. A. Jones, A. Facchetti, M. R. Wasielewski, and T. J. Marks. *Effects of Arylene Diimide Thin Film Growth Conditions on n-Channel OFET Performance.* Adv. Funct. Mater. **18**, 1329 (2008).

[100] R. T. Weitz, K. Amsharov, U. Zschieschang, E. B. Villas, D. K. Goswami, M. Burghard, H. Dosch, M. Jansen, K. Kern, and H. Klauk. *Organic n-channel transistors based on core-cyanated perylene carboxylic diimide derivatives.* J. Am. Chem. Soc. **130**, 4637 (2008).

[101] U. Zschieschang, K. Amsharov, R. T. Weitz, M. Jansen, and H. Klauk. *Low-voltage organic n-channel thin-film transistors based on a core-cyanated perylene tetracarboxylic diimide derivative.* Synth. Met. **159**, 2362 (2009).

[102] M. Sejfić. Ph.D. thesis, University of Munich, in preparation.

[103] J. Soeda, T. Uemura, Y. Mizuno, A. Nakao, Y. Nakazawa, A. Facchetti, and J. Takeya. *High Electron Mobility in Air for N,N'-1H,1H-Perfluorobutyldicyanoperylene Carboxydi-imide Solution-Crystallized Thin-Film Transistors on Hydrophobic Surfaces.* Adv. Mater. **23**, 3681 (2011).

[104] C. Piliego, D. Jarzab, G. Gigli, Z. Chen, A. Facchetti, and M. A. Loi. *High Electron Mobility and Ambient Stability in Solution-Processed Perylene-Based Organic Field-Effect Transistors.* Adv. Mater. **21**, 1573 (2009).

[105] N. A. Minder, S. Ono, Z. Chen, A. Facchetti, and A. F. Morpurgo. *Band-Like Electron Transport in Organic Transistors and Implication of the Molecular Structure for Performance Optimization.* Adv. Mater. **24**, 503 (2012).

[106] A. S. Molinari, H. Alves, Z. Chen, A. Facchetti, and A. F. Morpurgo. *High electron mobility in vacuum and ambient for PDIF-CN$_2$ single-crystal transistors.* J. Am. Chem. Soc. **131**, 2462 (2009).

[107] M. Barra, F. V. Di Girolamo, N. A. Minder, I. G. Lezama, Z. Chen, A. Facchetti, A. F. Morpurgo, and A. Cassinese. *Very low bias stress in n-type organic single-crystal transistors.* Appl. Phys. Lett. **100**, 133301 (2012).

[108] R. T. Weitz, K. Amsharov, U. Zschieschang, M. Burghard, M. Jansen, M. Kelsch, B. Rhamati, P. A. van Aken, K. Kern, and H. Klauk. *The Importance of Grain Boundaries for the Time-Dependent Mobility Degradation in Organic Thin-Film Transistors.* Chem. Mater. **21**, 4949 (2009).

[109] S. Ono, N. Minder, Z. Chen, A. Facchetti, and A. F. Morpurgo. *High-performance n-type organic field-effect transistors with ionic liquid gates.* Appl. Phys. Lett. **97**, 143307 (2010).

[110] I. Yagi, K. Shigeto, K. Tsukagoshi, and Y. Aoyagi. *Alignment-free top-contact formation for organic thin film transistors with submicron-length channel.* Jpn. J. Appl. Phys. **44**, L479 (2005).

[111] D. J. Gundlach, L. Zhou, J. A. Nichols, T. N. Jackson, P. V. Necliudov, and M. S. Shur. *An experimental study of contact effects in organic thin film transistors.* J. Appl. Phys. **100**, 024509 (2006).

[112] I. Kymissis, C. D. Dimitrakopoulos, and S. Purushothaman. *High-performance bottom electrode organic thin-film transistors.* IEEE Trans. Electron Dev. **48**, 1060 (2001).

[113] D. K. Schroder. *Semiconductor Material and Device Characterization* (Wiley, 2006).

[114] T. J. Richards and H. Sirringhaus. *Analysis of the contact resistance in staggered, top-gate organic field-effect transistors.* J. Appl. Phys. **102**, 094510 (2007).

[115] R. Rödel, F. Letzkus, T. Zaki, J. N. Burghartz, U. Kraft, U. Zschieschang, K. Kern, and H. Klauk. *Contact properties of high-mobility, air-stable, low-voltage organic n-channel thin-film transistors based on a naphthalene tetracarboxylic diimide.* Appl. Phys. Lett. **102**, 233303 (2013).

[116] H. H. Berger. *Contact resistance and contact resistivity.* J. Electrochem. Soc. **119**, 507 (1972).

[117] C.-H. Shim, F. Maruoka, and R. Hattori. *Structural analysis on organic thin-film transistor with device simulation.* IEEE Trans. Electron Dev. **57**, 195 (2010).

[118] C.-S. Chiang, S. Martin, J. Kanicki, Y. Ugai, T. Yukawa, and S. Takeuchi. *Top-gate staggered amorphous silicon thin-film transistors: Series resistance and nitride thickness effects.* Jpn. J. Appl. Phys. **37**, 5914 (1998).

[119] G. Horowitz, P. Lang, M. Mottaghi, and H. Aubin. *Extracting Parameters from the Current-Voltage Characteristics of Organic Field-Effect Transistors.* Adv. Funct. Mater. **14**, 1069 (2004).

[120] G. Ghibaudo. *New method for the extraction of MOSFET parameters.* Electron. Lett. **24**, 543 (1988).

[121] Y. Xu, T. Minari, K. Tsukagoshi, J. A. Chroboczek, and G. Ghibaudo. *Direct evaluation of low-field mobility and access resistance in pentacene field-effect transistors.* J. Appl. Phys. **107**, 114507 (2010).

[122] D. Natali, L. Fumagalli, and M. Sampietro. *Modeling of organic thin film transistors: Effect of contact resistances.* J. Appl. Phys. **101**, 014501 (2007).

[123] A. Cerdeira, M. Estrada, R. Garcıa, A. Ortiz-Conde, and F. J. Garcıa Sánchez. *New procedure for the extraction of basic a-Si:H TFT model parameters in the linear and saturation regions.* Solid-State Electron. **45**, 1077 (2001).

[124] C. H. Kim, Y. Bonnassieux, and G. Horowitz. *Compact DC Modeling of Organic Field-Effect Transistors: Review and Perspectives.* IEEE Trans. Electron Dev. **61**, 278 (2014).

[125] J. A. J. Tejada, J. A. L. Villanueva, P. L. Varo, K. M. Awawdeh, and M. J. Deen. *Compact Modeling and Contact Effects in Thin Film Transistors.* IEEE Trans. Electron Dev. **61**, 266 (2014).

[126] P. V. Necliudov, M. S. Shur, D. J. Gundlach, and T. N. Jackson. *Modeling of organic thin film transistors of different designs.* J. Appl. Phys. **88**, 6594 (2000).

[127] L. Bürgi, H. Sirringhaus, and R. H. Friend. *Noncontact potentiometry of polymer field-effect transistors.* Appl. Phys. Lett. **80**, 2913 (2002).

[128] L. Bürgi, T. J. Richards, R. H. Friend, and H. Sirringhaus. *Close look at charge carrier injection in polymer field-effect transistors.* J. Appl. Phys. **94**, 6129 (2003).

[129] K. P. Puntambekar, P. V. Pesavento, and C. D. Frisbie. *Surface potential profiling and contact resistance measurements on operating pentacene thin-film transistors by Kelvin probe force microscopy.* Appl. Phys. Lett. **83**, 5539 (2003).

[130] J. A. Nichols, D. J. Gundlach, and T. N. Jackson. *Potential imaging of pentacene organic thin-film transistors.* Appl. Phys. Lett. **83**, 2366 (2003).

[131] F. Lüttich, D. Lehmann, M. Friedrich, Z. Chen, A. Facchetti, C. von Borczyskowski, D. R. T. Zahn, and H. Graaf. *Interface properties of OFETs based on an air-stable n-channel perylene tetracarboxylic diimide semiconductor.* Phys. Status Solidi A **209**, 585 (2012).

[132] P. V. Pesavento, R. J. Chesterfield, C. R. Newman, and C. D. Frisbie. *Gated four-probe measurements on pentacene thin-film transistors: Contact resistance as a function of gate voltage and temperature.* J. Appl. Phys. **96**, 7312 (2004).

[133] P. V. Pesavento, K. P. Puntambekar, C. D. Frisbie, J. C. McKeen, and P. P. Ruden. *Film and contact resistance in pentacene thin-film transistors: Dependence on film thickness, electrode geometry, and correlation with hole mobility.* J. Appl. Phys. **99**, 094504 (2006).

[134] R. J. Chesterfield, J. C. McKeen, C. R. Newman, C. D. Frisbie, P. C. Ewbank, K. R. Mann, and L. L. Miller. *Variable temperature film and contact resistance measurements on operating n-channel organic thin film transistors.* J. Appl. Phys. **95**, 6396 (2004).

[135] T. Zaki, R. Rödel, F. Letzkus, H. Richter, U. Zschieschang, H. Klauk, and J. N. Burghartz. *S-parameter characterization of submicrometer low-voltage organic thin-film transistors.* IEEE Electron Device Lett. **34**, 520 (2013).

[136] T. Zaki, R. Rödel, F. Letzkus, H. Richter, U. Zschieschang, H. Klauk, and J. N. Burghartz. *AC characterization of organic thin-film transistors with asymmetric gate-to-source and gate-to-drain overlaps.* Org. Electron. **14**, 1318 (2013).

[137] F. Letzkus, J. Butschke, B. Höfflinger, M. Irmscher, C. Reuter, R. Springer, A. Ehrmann, and J. Mathuni. *Dry etch improvements in the SOI wafer flow process for IPL stencil mask fabrication.* Microelectron. Eng. **53**, 609 (2000).

[138] U. Zschieschang, F. Ante, M. Schlörholz, M. Schmidt, K. Kern, and H. Klauk. *Mixed Self-Assembled Monolayer Gate Dielectrics for Continuous Threshold Voltage Control in Organic Transistors and Circuits.* Adv. Mater. **22**, 4489 (2010).

[139] R. Luschtinetz, A. F. Oliveira, J. Frenzel, J.-O. Joswig, G. Seifert, and H. A. Duarte. *Adsorption of phosphonic and ethylphosphonic acid on aluminum oxide surfaces.* Surf. Sci. **602**, 1347 (2008).

[140] R. Luschtinetz, A. F. Oliveira, H. A. Duarte, and G. Seifert. *Self-assembled Monolayers of Alkylphosphonic Acids on Aluminum Oxide Surfaces - A Theoretical Study.* Z. Anorg. Allg. Chem. **636**, 1506 (2010).

[141] H. Klauk, U. Zschieschang, J. Pflaum, and M. Halik. *Ultralow-power organic complementary circuits.* Nature **445**, 745 (2007).

[142] I. Horcas, R. Fernandez, J. M. Gomez-Rodriguez, J. Colchero, J. Gómez-Herrero, and A. M. Baro. *WSXM: a software for scanning probe microscopy and a tool for nanotechnology.* Rev. Sci. Instrum. **78**, 013705 (2007).

[143] G. Horowitz and M. E. Hajlaoui. *Mobility in polycrystalline oligothiophene field-effect transistors dependent on grain size.* Adv. Mater. **12**, 1046 (2000).

[144] S. Oh, J.-S. Yu, J. Lim, M. Jadhav, T.-M. Lee, D. Kim, and C. Kim. *Highly Flexible Magnetoelectronic Device Integrated With Embedded Ag Nanoparticle Electrode.* IEEE Sens. J. **13**, 3957 (2013).

[145] G. Horowitz and M. E. Hajlaoui. *Grain size dependent mobility in polycrystalline organic field-effect transistors.* Synth. Met. **122**, 185 (2001).

[146] U. Kraft, M. Sejfić, M. J. Kang, K. Takimiya, T. Zaki, F. Letzkus, J. N. Burghartz, E. Weber, and H. Klauk. *Flexible Low-Voltage Organic Complementary Circuits: Finding the Optimum Combination of Semiconductors and Monolayer Gate Dielectrics.* Adv. Mater. **27**, 207 (2015).

[147] C.-H. Wang, C.-W. Su, S. W. Chan, L.-J. Fan, M.-C. Chen, and Y.-W. Yang. *Damaging Effect of Hot Metal Atoms on Organic Semiconducting Films during Top Contact Formation.* J. Phys. Chem. C **119**, 14593 (2015).

[148] S. Scholz, Q. Huang, M. Thomschke, S. Olthof, P. Sebastian, K. Walzer, K. Leo, S. Oswald, C. Corten, and D. Kuckling. *Self-doping and partial oxidation of metal-on-organic interfaces for organic semiconductor devices studied by chemical analysis techniques.* J. Appl. Phys. **104**, 104502 (2008).

[149] J. H. Cho, D. H. Kim, Y. Jang, W. H. Lee, K. Ihm, J.-H. Han, S. Chung, and K. Cho. *Effects of metal penetration into organic semiconductors on the electrical properties of organic thin film transistors.* Appl. Phys. Lett. **89**, 132101 (2006).

[150] M. Mottaghi and G. Horowitz. *Field-induced mobility degradation in pentacene thin-film transistors.* Org. Electron. **7**, 528 (2006).

[151] L. Ma, Y. Guo, Y. Wen, Y. Liu, and X. Zhan. *High-mobility, air stable bottom-contact n-channel thin film transistors based on N, N'-ditridecyl perylene diimide.* Appl. Phys. Lett. **103**, 203303 (2013).

[152] O. Acton, M. Dubey, T. Weidner, K. M. O'Malley, T.-W. Kim, G. G. Ting, D. Hutchins, J. E. Baio, T. C. Lovejoy, A. H. Gage, D. G. Castner, H. Ma, and A. K.-Y. Jen. *Simultaneous Modification of Bottom-Contact Electrode and Dielectric*

Surfaces for Organic Thin-Film Transistors Through Single-Component Spin-Cast Monolayers. Adv. Funct. Mater. **21**, 1476 (2011).

[153] N.-K. Kim, D. Khim, Y. Xu, S.-H. Lee, M. Kang, J. Kim, A. Facchetti, Y.-Y. Noh, and D.-Y. Kim. *Solution-Processed Barium Salts as Charge Injection Layers for High Performance n-Channel Organic Field-Effect Transistors.* ACS Appl. Mater. Interfaces **6**, 9614 (2014).

[154] F. Ante, D. Kälblein, T. Zaki, U. Zschieschang, K. Takimiya, M. Ikeda, T. Sekitani, T. Someya, J. N. Burghartz, K. Kern, and H. Klauk. *Contact resistance and megahertz operation of aggressively scaled organic transistors.* Small **8**, 73 (2012).

[155] B. Stadlober, U. Haas, H. Gold, A. Haase, G. Jakopic, G. Leising, N. Koch, S. Rentenberger, and E. Zojer. *Orders-of-Magnitude Reduction of the Contact Resistance in Short-Channel Hot Embossed Organic Thin Film Transistors by Oxidative Treatment of Au-Electrodes.* Adv. Funct. Mater. **17**, 2687 (2007).

[156] C.-Y. Chen and J. Kanicki. *Origin of series resistances in a-Si:H TFTs.* Solid State Electron. **42**, 705 (1998).

[157] W. Hu and R. L. Peterson. *Molybdenum as a contact material in zinc tin oxide thin film transistors.* Appl. Phys. Lett. **104**, 192105 (2014).

[158] R. A. Vega, V. C. Lee, and T.-J. K. Liu. *The effect of random dopant fluctuation on specific contact resistivity.* IEEE Trans. Electron Dev. **57**, 273 (2010).

[159] S. Luan and G. W. Neudeck. *An experimental study of the source/drain parasitic resistance effects in amorphous silicon thin film transistors.* J. Appl. Phys. **72**, 766 (1992).

[160] S. D. Wang, T. Minari, T. Miyadera, K. Tsukagoshi, and Y. Aoyagi. *Contact-metal dependent current injection in pentacene thin-film transistors.* Appl. Phys. Lett. **91**, 203508 (2007).

[161] C.-Y. Chen and J. Kanicki. *Gated-four-probe a-Si:H TFT structure: a new technique to measure the intrinsic performance of a-Si:H TFT.* IEEE Electron Dev. Lett. **18**, 340 (1997).

[162] C.-W. Sohn, T.-U. Rim, G.-B. Choi, and Y.-H. Jeong. *Analysis of contact effects in inverted-staggered organic thin-film transistors based on anisotropic conduction.* IEEE Trans. Electron Dev. **57**, 986 (2010).

[163] M. N. Islam and B. Mazhari. *An analytical model for current crowding and source contact resistance in top-contact organic thin-film transistors.* Semicond. Sci. Technol. **23**, 125027 (2008).

[164] S. Scheinert and G. Paasch. *Interdependence of contact properties and field-and density-dependent mobility in organic field-effect transistors.* J. Appl. Phys. **105**, 014509 (2009).

[165] M. Leufgen, U. Bass, T. Muck, T. Borzenko, G. Schmidt, J. Geurts, V. Wagner, and L. W. Molenkamp. *Optimized sub-micron organic thin-film transistors: the influence of contacts and oxide thickness.* Synt. Met. **146**, 341 (2004).

[166] B. H. Hamadani and D. Natelson. *Extracting Contact Effects in Organic FETs.* Proceedings of the IEEE **93**, 1306 (2005).

[167] M. Caironi, C. Newman, J. R. Moore, D. Natali, H. Yan, A. Facchetti, and H. Sirringhaus. *Efficient charge injection from a high work function metal in high mobility n-type polymer field-effect transistors.* Appl. Phys. Lett. **96**, 183303 (2010).

[168] S. D. Wang, Y. Yan, and K. Tsukagoshi. *Understanding contact behavior in organic thin film transistors.* Appl. Phys. Lett. **97**, 063307 (2010).

[169] D. L. Pulfrey, A. H. M. Shousha, and L. Young. *Electronic conduction and space charge in amorphous insulating films.* J. Appl. Phys. **41**, 2838 (1970).

[170] K. R. Sarma. *Amorphous Silicon: Flexible Backplane and Display Application.* In W. S. Wong and A. Salleo (editors) *Flexible Electronics: Materials and Applications*, Electronic Materials: Science & Technology, chapter 4 (Springer, 2009).

[171] D. Knipp, R. A. Street, and A. R. Völkel. *Morphology and electronic transport of polycrystalline pentacene thin-film transistors.* Appl. Phys. Lett. **82**, 3907 (2003).

[172] R. J. Chesterfield, J. C. McKeen, C. R. Newman, P. C. Ewbank, D. A. da Silva Filho, J.-L. Brédas, L. L. Miller, K. R. Mann, and C. D. Frisbie. *Organic thin film transistors based on N-alkyl perylene diimides: charge transport kinetics as a function of gate voltage and temperature.* J. Phy. Chem. B **108**, 19281 (2004).

[173] J. A. Letizia, J. Rivnay, A. Facchetti, M. A. Ratner, and T. J. Marks. *Variable Temperature Mobility Analysis of n-Channel, p-Channel, and Ambipolar Organic Field-Effect Transistors.* Adv. Funct. Mater. **20**, 50 (2010).

[174] R. A. Street, J. E. Northrup, and A. Salleo. *Transport in polycrystalline polymer thin-film transistors.* Phys. Rev. B **71**, 165202 (2005).

[175] T. He, M. Stolte, C. Burschka, N. H. Hansen, T. Musiol, D. Kälblein, J. Pflaum, X. Tao, J. Brill, and F. Würthner. *Single-crystal field-effect transistors of new Cl2-NDI polymorph processed by sublimation in air.* Nat. Commun. **6** (2015).

[176] D. Guo, T. Miyadera, S. Ikeda, T. Shimada, and K. Saiki. *Analysis of charge transport in a polycrystalline pentacene thin film transistor by temperature and gate bias dependent mobility and conductance.* J. Appl. Phys. **102**, 023706 (2007).

[177] E. J. Meijer, M. Matters, P. T. Herwig, D. M. de Leeuw, and T. M. Klapwijk. *The Meyer–Neldel rule in organic thin-film transistors.* Appl. Phys. Lett. **76**, 3433 (2000).

[178] M. Ullah, I. I. Fishchuk, A. Kadashchuk, P. Stadler, A. Pivrikas, C. Simbrunner, V. N. Poroshin, N. S. Sariciftci, and H. Sitter. *Dependence of Meyer–Neldel energy on energetic disorder in organic field effect transistors.* Appl. Phys. Lett. **96**, 213306 (2010).

[179] W. B. Jackson. *Connection between the Meyer-Neldel relation and multiple-trapping transport.* Phys. Rev. B **38**, 3595 (1988).

[180] S. R. Saudari and C. R. Kagan. *Electron and hole transport in ambipolar, thin film pentacene transistors.* J. Appl. Phys. **117**, 035501 (2015).

[181] J. Cho, Y. Akiyama, T. Kakinuma, and T. Mori. *Trap density of states in n-channel organic transistors: variable temperature characteristics and band transport.* AIP Advances **3**, 102131 (2013).

[182] H. Bässler. *Charge transport in disordered organic photoconductors a Monte Carlo simulation study.* Phys. Status Solidi B **175**, 15 (1993).

[183] I. P. Zvyagin. *A percolation approach to the temperature and charge carrier concentration dependence of the hopping conductivity in organic materials.* Phys. Status Solidi C **5**, 725 (2008).

[184] W. L. Kalb and B. Batlogg. *Calculating the trap density of states in organic field-effect transistors from experiment: A comparison of different methods.* Phys. Rev. B **81**, 035327 (2010).

[185] Y. Hirose, A. Kahn, V. Aristov, P. Soukiassian, V. Bulovic, and S. Forrest. *Chemistry and electronic properties of metal-organic semiconductor interfaces: Al, Ti, In, Sn, Ag, and Au on PTCDA.* Phys. Rev. B **54**, 13748 (1996).

[186] H. Wada, K. Shibata, Y. Bando, and T. Mori. *Contact resistance and electrode material dependence of air-stable n-channel organic field-effect transistors using dimethyldicyanoquinonediimine (DMDCNQI).* J. Mater. Chem. **18**, 4165 (2008).

[187] A. Kumatani, Y. Li, P. Darmawan, T. Minari, and K. Tsukagoshi. *On Practical Charge Injection at the Metal/Organic Semiconductor Interface.* Sci. Rep. **3** (2013).

[188] M. Grobosch and M. Knupfer. *Charge-Injection Barriers at Realistic Metal/Organic Interfaces: Metals Become Faceless.* Adv. Mater. **19**, 754 (2007).

[189] Y.-C. Chang, M.-Y. Kuo, C.-P. Chen, H.-F. Lu, and I. Chao. *On the air stability of n-channel organic field-effect transistors: a theoretical study of adiabatic electron affinities of organic semiconductors.* J. Phys. Chem. C **114**, 11595 (2010).

[190] F. De Angelis, M. Gaspari, A. Procopio, G. Cuda, and E. Di Fabrizio. *Direct mass spectrometry investigation on pentacene thin film oxidation upon exposure to air.* Chem. Phys. Lett. **468**, 193 (2009).

[191] H. E. Katz, A. J. Lovinger, J. Johnson, C. Kloc, T. Siegrist, W. Li, Y.-Y. Lin, and A. Dodabalapur. *A soluble and air-stable organic semiconductor with high electron mobility.* Nature **404**, 478 (2000).

[192] W. H. Lee, H. H. Choi, D. H. Kim, and K. Cho. *25th Anniversary Article: Microstructure Dependent Bias Stability of Organic Transistors.* Adv. Mater. **26**, 1660 (2014).

[193] P. A. Bobbert, A. Sharma, S. G. J. Mathijssen, M. Kemerink, and D. M. de Leeuw. *Operational Stability of Organic Field-Effect Transistors.* Adv. Mater. **24**, 1146 (2012).

[194] S. Bisoyi, U. Zschieschang, M. J. Kang, K. Takimiya, H. Klauk, and S. P. Tiwari. *Bias-stress stability of low-voltage p-channel and n-channel organic thin-film transistors on flexible plastic substrates.* Org. Electron. **15**, 3173 (2014).

[195] R. A. Street, M. L. Chabinyc, F. Endicott, and B. Ong. *Extended time bias stress effects in polymer transistors.* J. Appl. Phys. **100**, 114518 (2006).

[196] T. Richards and H. Sirringhaus. *Bias-stress induced contact and channel degradation in staggered and coplanar organic field-effect transistors.* Appl. Phys. Lett. **92**, 023512 (2008).

[197] U. Zschieschang, R. T. Weitz, K. Kern, and H. Klauk. *Bias stress effect in low-voltage organic thin-film transistors.* Appl. Phys. A. **95**, 139 (2009).

[198] H.-W. Zan and S.-C. Kao. *The effects of drain-bias on the threshold voltage instability in organic TFTs.* IEEE Electron Device Lett. **29**, 155 (2008).

[199] M. Tello, M. Chiesa, C. M. Duffy, and H. Sirringhaus. *Charge trapping in intergrain regions of pentacene thin film transistors.* Adv. Funct. Mater. **18**, 3907 (2008).

[200] T. Zaki, S. Scheinert, I. Hörselmann, R. Rödel, F. Letzkus, H. Richter, U. Zschieschang, H. Klauk, and J. N. Burghartz. *Accurate Capacitance Modeling and Characterization of Organic Thin-Film Transistors.* IEEE Trans. Electron Dev. **61**, 98 (2014).

[201] Y.-Y. Noh, N. Zhao, M. Caironi, and H. Sirringhaus. *Downscaling of self-aligned, all-printed polymer thin-film transistors.* Nat. Nanotechnol. **2**, 784 (2007).

[202] W. Smaal, C. Kjellander, Y. Jeong, A. Tripathi, B. van der Putten, A. Facchetti, H. Yan, J. Quinn, J. Anthony, K. Myny, W. Dehaene, and G. Gelinck. *Complementary integrated circuits on plastic foil using inkjet printed n-and p-type organic semiconductors: Fabrication, characterization, and circuit analysis.* Org. Electron. **13**, 1686 (2012).

[203] K.-J. Baeg, S.-W. Jung, D. Khim, J. Kim, D.-Y. Kim, J. B. Koo, J. R. Quinn, A. Facchetti, I.-K. You, and Y.-Y. Noh. *Low-voltage, high speed inkjet-printed flexible complementary polymer electronic circuits.* Org. Electron. **14**, 1407 (2013).

[204] T.-H. Ke, R. Müller, B. Kam, M. Rockele, A. Chasin, K. Myny, S. Steudel, W. D. Oosterbaan, L. Lutsen, J. Genoe, L. van Leuken, B. van der Putten, and P. Heremans. *Scaling down of organic complementary logic gates for compact logic on foil.* Org. Electron. **15**, 1229 (2014).

[205] M. Benwadih, A. Aliane, S. Jacob, J. Bablet, R. Coppard, and I. Chartier. *Integration of a graphene ink as gate electrode for printed organic complementary thin-film transistors.* Org. Electron. **15**, 614 (2014).

[206] M. Kano, T. Minari, K. Tsukagoshi, and H. Maeda. *Control of device parameters by active layer thickness in organic field-effect transistors.* Appl. Phys. Lett. **98**, 073307 (2011).

[207] C.-H. Kim, H. Hlaing, J.-A. Hong, J.-H. Kim, Y. Park, M. M. Payne, J. E. Anthony, Y. Bonnassieux, G. Horowitz, and I. Kymissis. *Decoupling the Effects of Self-Assembled Monolayers on Gold, Silver, and Copper Organic Transistor Contacts.* Adv. Mater. Interfaces **2** (2015).

[208] Y. Zhou, C. Fuentes-Hernandez, J. Shim, J. Meyer, A. J. Giordano, H. Li, P. Winget, T. Papadopoulos, H. Cheun, J. Kim, F. Fenoll, A. Dindar, W. Haske, E. Najafabadi, T. M. Khan, H. Sojoudi, S. Barlow, S. Graham, J.-L. Brédas, S. R. Marder, A. Kahn, and B. Kippelen. *A universal method to produce low-work function electrodes for organic electronics.* Science **336**, 327 (2012).

[209] W. E. Ford, D. Gao, N. Knorr, R. Wirtz, F. Scholz, Z. Karipidou, K. Ogasawara, S. Rosselli, V. Rodin, G. Nelles, and F. von Wrochem. *Organic Dipole Layers for Ultralow Work Function Electrodes.* ACS Nano **8**, 9173 (2014).

[210] M. L. Tietze, P. Pahner, K. Schmidt, K. Leo, and B. Lüssem. *Doped Organic Semiconductors: Trap-Filling, Impurity Saturation, and Reserve Regimes.* Adv. Funct. Mater. **25**, 2701 (2015).

Curriculum Vitae

Personal information

Name	Reinhold Rödel
Date of birth	24.06.1985
Place of birth	Halle (Saale), Germany
Nationality	German

Education

since August 2011	Max Planck Institute for Solid State Research, Stuttgart, Germany
	Research staff
	École Polytechnique Fédérale de Lausanne, Switzerland
	PhD student
2005 - 2010	University of Würzburg, Germany
	Diploma degree in Nanotechnology
1996 - 2005	Georg-Cantor-Gymnasium in Halle, Germany
	Abitur

Publications

- T. Zaki, R. Rödel, F. Letzkus, H. Richter, U. Zschieschang, H. Klauk, and J. N. Burghartz, *S-Parameter Characterization of Submicrometer Low-Voltage Organic Thin-Film Transistors*, IEEE Electron. Dev. Lett. **34**, 520 (2013)

- U. Zschieschang, R. Hofmockel, R. Rödel, U. Kraft, M. J. Kang, K. Takimiya, T. Zaki, F. Letzkus, J. Butschke, H. Richter, J. N. Burghartz, and H. Klauk, *Megahertz operation of flexible low-voltage organic thin-film transistors*, Org. Electron. **14**, 1516 (2013)

- T. Zaki, R. Rödel, F. Letzkus, H. Richter, U. Zschieschang, H. Klauk, and J. N. Burghartz, *AC characterization of organic thin-film transistors with asymmetric gate-to-source and gate-to-drain overlaps*, Org. Electron. **14**, 1318 (2013)

- R. Rödel, F. Letzkus, T. Zaki, J. N. Burghartz, U. Kraft, U. Zschieschang, K. Kern, and H. Klauk, *Contact properties of high-mobility, air-stable, low-voltage organic n-channel thin-film transistors based on a naphthalene tetracarboxylic diimide*, Appl. Phys. Lett., **102**, 233303 (2013)

- R. Hofmockel, U. Zschieschang, U. Kraft, R. Rödel, N. H. Hansen, M. Stolte, F. Würthner, K. Takimiya, K. Kern, J. Pflaum, and H. Klauk, *High-mobility organic thin-film transistors based on a small-molecule organic semiconductor deposited in vacuum and by solution shearing*, Org. Electron. **14**, 3213 (2013)

- T. Zaki, S. Scheinert, I. Hörselmann, R. Rödel, F. Letzkus, H. Richter, U. Zschieschang, H. Klauk, and J. N. Burghartz, *Accurate Capacitance Modeling and Characterization of Organic Thin-Film Transistors*, IEEE Trans. Electron. Dev. **61**, 98 (2014)

- S. Scheinert, T. Zaki, R. Rödel, I. Hörselmann, H. Klauk, and J. N. Burghartz, *Numerical analysis of capacitance compact models for organic thin-film transistors*, Org. Electron. **15**, 1503 (2014)

- J. Milvich, T. Zaki, M. Aghamohammadi, R. Rödel, U. Kraft, H. Klauk, and J. N. Burghartz, *Flexible low-voltage organic phototransistor based on air-stable*

dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT), Org. Electron. **20**, 63 (2015)

- M. Aghamohammadi, R. Rödel, U. Zschieschang, C. Ocal, R. T. Weitz, E. Barrena, and H. Klauk, *Threshold-Voltage Shifts in Organic Transistors Due to Self-Assembled Monolayers at the Dielectric: Evidence for Electronic Coupling and Dipolar Effects*, accepted for publication in ACS Appl. Mater. Interfaces

- S. Bisoyi, R. Rödel, U. Zschieschang, M. J. Kang, K. Takimiya, H. Klauk, and S. P. Tiwari, *Charge trapping in field-effect devices based on four different organic semiconductors and four different contact metals evaluated by displacement current measurements*, submitted to Semicond. Sci. Technol.

Acknowledgements

At this point I would like to thank the following people who contributed to this work:

I am grateful to Prof. Klaus Kern for supervising my thesis and giving me the possibility to receive my PhD degree from the EPF Lausanne.
I am thankful to Dr. Hagen Klauk for giving me the opportunity to conduct my work in his research group. I am also grateful for guidance, support and the freedom to realize my ideas.
I would like to thank Prof. Cécile Hébert, Prof. Holger Frauenrath, Prof. Jana Zaumseil and Prof. Jens Pflaum for being part of my PhD jury.
My special thanks go to Dr. Ute Zschieschang for introducing me to the cleanroom facility and for taking care of the technical equipment.
I am thankful to my colleagues Ulrike Kraft, Mirsada Sejfić, Mahdieh Schmidt and Sibani Bisoyi and my former colleagues Dr. Daniel Kälblein, Dr. Frederik Ante, Dr. Hyeyeon Ryu, Robert Hofmockel and Muriel de Pauli for the friendly atmosphere, interesting scientific and non-scientific discussions and diverse social activities. In addition, I am grateful to Mahdieh Schmidt for kindly providing the AFM data of the bare PEN surface.
A special word of thanks goes to Dr. Tarek Zaki for performing the admittance measurements and for various interesting discussions. I also acknowledge support from the IMS CHIPS, namely Prof. Joachim Burghartz, Dr. Florian Letzkus and Dr. Harald Richter.
I am grateful to Dr. Jürgen Weis for interesting and insightful discussions.
My thanks go to PD Dr.- Ing. Susanne Scheinert for the work on device simulations.
I appreciate continuous technical support, especially from Bernhard Fenk with the SEM, from Marion Hagel with sample bonding and ALD processing and from Wolfgang Winter with uncomplicated and fast help.
I am indebted to Sabine Birtel for the support in paperwork and organization.
I appreciate the invitations of Prof. Klaus von Klitzing to diverse social events and the annual group meeting at Ringberg Castle.
My thanks go to all members of the MPI-FKF for providing a friendly, supportive and pleasant working atmosphere.
I appreciate partial funding of this work by the German Research Foundation (DFG) under Grant KL 2223/5-1 and KL 2223/5-2.

Finally, I would like to thank my family and especially Anne for their continuous support.