ADVANCED ELECTRONIC MATERIALS
www.advelectronicmat.de

Tailoring the Dielectric Layer Structure for Enhanced Carrier Mobility in Organic Transistors: The Use of Hybrid Inorganic/Organic Multilayer Dielectrics

*Muriel de Pauli, Ute Zschieschang, Ingrid D. Barcelos, Hagen Klauk, and Angelo Malachias**

The combination of inorganic and organic insulating layers to create gate dielectrics that simultaneously provide a smooth surface, a small surface energy, and negligible gate leakage has been well reported in the literature as a key aspect in the fabrication of organic thin-film transistors (TFTs).[1] Such hybrid bilayer dielectrics are generally composed of an inorganic metal oxide layer, ideally one with a large dielectric constant (e.g., SiO_2, Al_2O_3, HfO_2, ZrO_2), and an organic self-assembled monolayer (SAM) composed of amphiphilic molecules. This arrangement can significantly improve crucial device performance parameters, and it can be exploited to tune the threshold voltage of the TFTs,[2–6] produce low-voltage operating TFTs,[7] control the charge-carrier density,[2] and reduce the gate leakage current.[8] However, the interaction between the inorganic layer and the SAM in such hybrid dielectrics is still poorly explored. Here we show that the use of a hybrid multilayer dielectric (HMD) obtained by stacking successive Al_2O_3/SAM bilayers can tailor interface phenomena and thereby significantly improve the charge-carrier mobility and operational stability of organic TFTs. While Yoon et al.,[9] DiBenedetto et al. [10] and Ha et al. [11] have previously shown that hybrid inorganic/organic multilayer dielectrics are a powerful approach to producing gate dielectrics that cover a wide range of thicknesses (5–12 nm) and capacitances (100–700 nF cm^{-2}), the influence of the number of inorganic/organic bilayers on the charge-carrier mobility and operational stability of the transistors was not explored in these previous studies. Through the use of alkylphosphonic acid SAMs with different chain lengths, we have furthermore revealed a threshold for the Al_2O_3/SAM surface roughness; when the surface roughness is below this threshold, additional Al_2O_3/SAM bilayers enhance the carrier mobility, otherwise additional bilayers will reduce the mobility.

In preparing HMDs one has to aim for an inorganic dielectric that can be deposited at low temperatures and provides atomically smooth interfaces. Thanks to modern atomic layer deposition (ALD) methods it is possible to fulfill these requirements using precursors that undergo strongly exothermic reactions with exposed surfaces at mild temperatures.[12,13] This is the case for Al_2O_3, obtained by the reaction of $Al(CH_3)_3$ (trimethyl-aluminum) and water. Alkylphosphonic acids (PAs) are known to form high-quality self-assembled monolayers on the surface of atomic-layer-deposited Al_2O_3 films.[14]

Figure 1a shows a schematic view of the TFT structure fabricated using an HMD. In this work all devices were fabricated on doped silicon substrates, which also serve as the gate electrodes of the TFTs. Alkylphosphonic acid molecules with three distinct alkyl chain lengths of 1.3 nm (HC_{10}-PA), 1.7 nm (HC_{14}-PA), and 2.1 nm (HC_{18}-PA) [15] were investigated in order to optimize the quality of the dielectric. Our HMDs consist of an intercalation of atomic-layer-deposited Al_2O_3 films with a thickness of 9 nm grown at a temperature of 60 °C and solution-processed SAMs.[16] The alkyl chain length not only determines the thickness of the SAM, but also greatly influences the molecular packing within the SAM.[17–20] Therefore, the assembly behavior of the molecules studied here can drive the system into distinct multilayer structural properties due to a dependence of the resulting interface roughness with the presence of defects on the supramolecular packing (long-range order).[17,21] Samples with a different number of Al_2O_3/SAM bilayers stacked on top of each other were prepared, with the number of bilayers ranging from 1 to 6. 25 nm thick films of the small-molecule organic semiconductor dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT), which has previously shown high carrier mobilities and good air stability,[22] were deposited onto the HMDs. Source and drain contacts were finally deposited onto the DNTT layer using shadow masks. Details of the sample preparation procedure are described in the Experimental Section.

The performance of DNTT TFTs with HMDs was evaluated and compared to devices fabricated with a single Al_2O_3/SAM bilayer dielectric. Measurements of the gate-dielectric capacitance, the transfer and output characteristics and the bias-stress behavior of the TFTs were performed on all samples (see Figures S1–S3, Supporting Information). Figure 1b shows the carrier mobility in TFTs with different numbers of stacked Al_2O_3/SAM bilayers in which the SAMs are based on either HC_{10}-PA (blue squares), HC_{14}-PA (red circles), or HC_{18}-PA (green triangles). The carrier mobilities were determined by fitting the measured transfer curves to the standard FET equation (see the Experimental Section) using the value of the gate-dielectric capacitance measured at a frequency of 100 Hz (see Figure S1,

Dr. M. de Pauli, Dr. I. D. Barcelos, Prof. A. Malachias
Physics Department
Universidade Federal de Minas Gerais
ICEx
Av. Antonio Carlos, 6627, Belo Horizonte
CEP 30123-970, Brazil
E-mail: angelomalachias@gmail.com
Dr. U. Zschieschang, Dr. H. Klauk
Max Planck Institute for Solid State Research
Heisenbergstr. 1, 70569 Stuttgart, Germany

DOI: 10.1002/aelm.201500402

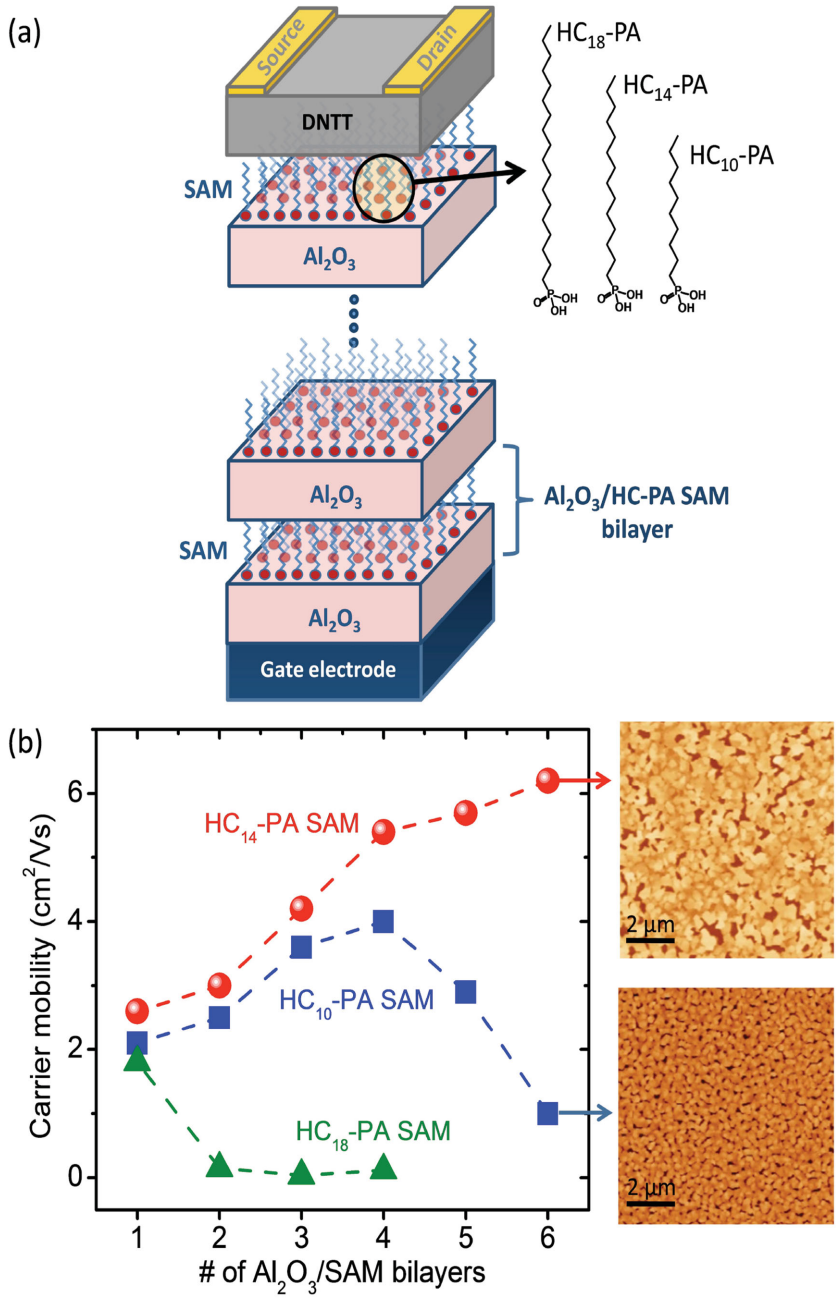

Figure 1. a) Schematic view of an organic TFT fabricated using a hybrid multilayer dielectric (HMD) composed of atomic-layer-deposited Al_2O_3 layers with a thickness of 9 nm and alkylphosphonic acid SAMs. The molecular structures of the alkylphosphonic acids HC_{10}-PA, HC_{14}-PA and HC_{18}-PA are also depicted. The number of stacked Al_2O_3/SAM bilayers ranges from 1 to 6. b) Charge-carrier mobility measured in TFTs as a function of the number of stacked Al_2O_3/SAM bilayers in the HMD. Distinct dependencies of the carrier mobility on the number of Al_2O_3/SAM bilayers are observed. In this plot, the error bars are smaller than the data points. The inset shows AFM images of the thin-film morphology of the organic semiconductor (DNTT) in the TFTs with six Al_2O_3/HC_{14}-PA SAM or six Al_2O_3/HC_{10}-PA SAM bilayers. The z-scale maximum was set to 90 nm in both images.

Supporting Information). In the TFTs with the Al_2O_3/HC_{14}-PA SAM bilayer dielectrics, the carrier mobility increases monotonically with the number of Al_2O_3/SAM bilayers, from 2.6 cm^2 Vs^{-1} for one bilayer to 6.2 cm^2 Vs^{-1} for six bilayers, which is by far the largest carrier mobility that has been reported so far for DNTT TFTs. In contrast, in the TFTs with the Al_2O_3/HC_{10}-PA SAM bilayers, the carrier mobility increases up to 4 cm^2 Vs^{-1} for four bilayers, but shows a pronounced drop when the number of bilayers is increased to five and six. Finally, in the TFTs with the Al_2O_3/HC_{18}-PA SAM bilayers, the carrier mobility decreases monotonically and significantly as the number of bilayers is increased beyond one. To account for the fact that the TFTs with the large number of stacked Al_2O_3/SAM bilayers have a larger gate-dielectric capacitance, these TFTs had to be operated with larger gate-source voltages in order to produce similar electric fields and similar charge-carrier densities in the semiconductor channel. To check whether the observed dependence of the carrier mobility on the number of stacked Al_2O_3/SAM bilayers can be explained as a field-dependent carrier mobility in the context of multiple trapping and release (MTR) model[23], we fabricated and characterized a reference sample based on a single hybrid Al_2O_3/SAM bilayer consisting of a 62 nm thick layer of Al_2O_3 and an HC_{14}-PA SAM, thus having the same total dielectric thickness as in the TFTs with six Al_2O_3 (9 nm)/HC_{14}-PA SAM bilayers. A mobility of 3.3 cm^2 Vs^{-1} was measured in these TFTs. As discussed in reference[6] , the carrier mobility for a single hybrid Al_2O_3/HC_{14}-PA SAM bilayer is essentially independent of the Al_2O_3 thickness. Therefore, we believe that the characteristic dependence of the carrier mobility on the number of hybrid Al_2O_3/SAM bilayers observed in Figure 1b is not related to the total dielectric thickness or to the applied gate field, but to the number of inorganic/organic interfaces. The carrier mobilities shown in Figure 1b are averages of measurements performed on 25 TFTs per sample, and the error bars are smaller than the data points.

In order to clarify why the dependence of the carrier mobility on the number of Al_2O_3/SAM bilayers is so different for the three phosphonic acids, we have used atomic force microscopy (AFM) to study the thin-film morphology of the organic semiconductor films deposited onto the different HMDs. Indeed, the differences in the DNTT grain size observed in these measurements are directly related to the differences in the carrier mobility. The inset of Figure 1b shows AFM topography maps of the surface of DNTT layers deposited onto six Al_2O_3/HC_{14}-PA SAM bilayers as well as onto six Al_2O_3/HC_{10}-PA SAM bilayers.

The two different trends observed for the dependence of the carrier mobility of the Al_2O_3/HC_{10}-PA SAM TFTs on

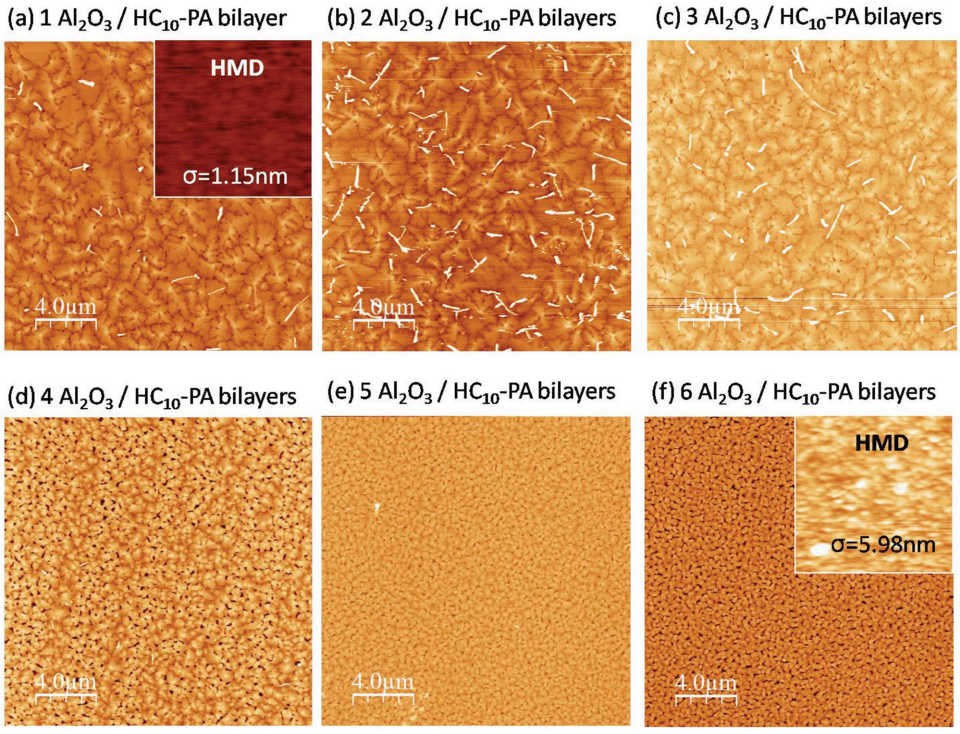

Figure 2. Topography of nominally 25-nm-thick DNTT layers deposited onto HMDs composed of one to six Al_2O_3/HC_{10}-PA SAM bilayers. The dielectric surface roughness, depicted in the insets of images (a) and (f), increases with the number of bilayers, resulting in a very small DNTT grain size on five and six Al_2O_3/SAM bilayers. The z-scale was set to 90 nm (4.8 nm for the inset images).

the number of bilayers (mobility increases from one to four bilayers, but decreases for five and six bilayers) makes these six samples particularly interesting for an AFM investigation. The topography images shown in **Figure 2** reveal that the DNTT grain size is relatively large (about 2 μm) in the samples with up to three Al_2O_3/SAM bilayers, but substantially smaller (about 200 nm) in the samples with five and six Al_2O_3/SAM bilayers. The HMD topmost surface roughness was also evaluated prior to the DNTT deposition. As shown in the insets of Figure 2a,f, the HMD topmost surface roughness is relatively small (1.15 nm) in the sample with one bilayer, but significantly larger (5.98 nm) in the sample with six bilayers. The smaller grain size and smaller carrier mobility in the samples with five and six bilayers are therefore related to the larger dielectric/semiconductor interface roughness in these samples; such a correlation between dielectric roughness, grain size, and mobility has been reported many times for various materials.[24–28] The smaller mobility observed on HMDs of Al_2O_3/HC_{18}-PA SAM (compared to HMDs with HC_{14}-PA or HC_{10}-PA SAMs) is also related to the larger HMD surface roughness and consequently smaller DNTT grain size.[17] For a single Al_2O_3/HC_{18}-PA SAM bilayer, we measured a surface roughness of 2.6 nm and a DNTT grain size of 2 μm, while for two bilayers the surface roughness is 11.2 nm and the DNTT grain size is less than 200 nm (see Figure S4, Supporting Information).

As discussed above, stacking more bilayers into an HMD substantially modifies the carrier mobility in the organic semiconductor layer deposited onto the HMD. An improvement in mobility is observed up to four Al_2O_3/SAM bilayers in the case of the HC_{10}-PA SAM, while for the HC_{14}-PA SAM, the HMD surface roughness remains small (3.5 nm) and the DNTT grain size remains large (about 1.2 μm; see inset of Figure 1b) even for six bilayers. Such small roughness is unexpected for such a large number of stacked inorganic/organic bilayers.

In order to understand the high carrier mobility in TFTs with multiple Al_2O_3/HC_{14}-PA SAM bilayer dielectrics, bias-stress measurements were carried out. To allow meaningful comparisons of the bias-stress data, the gate-source and drain-source voltages applied during the bias-stress measurements were chosen so that similar initial drain currents (−3 μA) were obtained for all TFTs, i.e., the channel sheet resistance is similar in all measurements.[29] **Figure 3** shows the measured drain current as a function of bias-stress time for TFTs in which the number of bilayers ranges from 1 to 5. (Results from bias-stress measurements on TFTs with Al_2O_3/HC_{10}-PA SAM and Al_2O_3/HC_{18}-PA SAM HMDs are shown in Figure S5, Supporting Information). It is known that charge trapping in the dielectric or at the semiconductor/dielectric interface results in a decrease in drain current.[30–32] Hence, a monotonic decrease of the drain current would be expected for our TFTs. This behavior is clearly observed in the TFT with a single Al_2O_3/HC_{14}-PA SAM bilayer. However, the introduction of HMDs with more than one Al_2O_3/HC_{14}-PA SAM bilayer causes an initial increase of the drain current during bias stress, followed by a decay that is slower for stacks with a larger number of Al_2O_3/HC_{14}-PA SAM bilayers. In the sample with five Al_2O_3/HC_{14}-PA SAM bilayers, the drain current continues to increase for the entire duration of the bias-stress measurement (60 min).

The observed drain-current increase during bias stress in TFTs based on Al_2O_3/HC_{14}-PA SAM HMDs can be ascribed

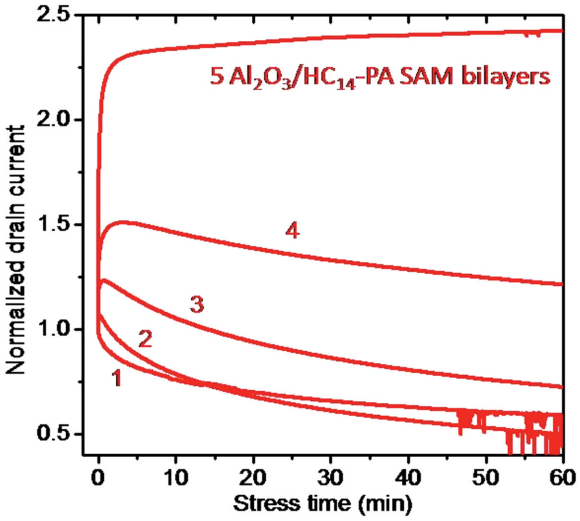

Figure 3. Bias-stress measurements performed on DNTT TFTs with HMDs composed of one to five Al_2O_3/HC_{14}-PA SAM bilayers. To allow meaningful comparisons of the bias-stress dynamics, the gate-source, and drain-source voltages were chosen to obtain similar initial drain currents (–3 μA).

either to dielectric polarization or to charge injection from the gate.[31,32] Since the gate current is very small in our devices (<10^{-11} A; see Figure S6, Supporting Information), charge injection from the gate can be ruled out, so polarization effects must be the main reason for the observed drain-current increase. Such polarization may be enhanced by the presence of highly dipolar groups in the dielectric originating from incomplete chemical reactions during ALD, due to the low ALD growth temperatures.[31–33] During the first few minutes of bias stress, the orientation of these dipolar groups with respect to the applied gate field may change, thus maximizing the polarization, which would explain the observed drain-current increase at the beginning of the bias-stress measurements. A larger number of inorganic/organic interfaces would further enhance the polarization due to the amphiphilic character of the phosphonic acids. To rule out that the effect is related to the organic semiconductor, we performed the same measurements on TFTs fabricated using a different organic semiconductor (2,9-didecyl-DNTT; C_{10}-DNTT; [34] see Figure S7, Supporting Information), and the result was very similar (drain-current increase during the first few minutes of bias stress), which reinforces our hypothesis that polarization in the HMD layers is responsible for the improved stability of our devices.

Figure 4 shows the measured transfer characteristics of DNTT TFTs with HMDs composed of four Al_2O_3/SAM bilayers based on each of the three alkylphosphonic acids. The largest mobility (5.6 cm^2 Vs^{-1}) is obtained with the HC_{14}-PA SAMs, as already discussed above. One also notices that the TFT with the HC_{14}-PA SAMs has a smaller threshold voltage than the TFTs with the HC_{10}-PA and HC_{18}-PA SAMs. The smaller threshold voltage obtained with the HC_{14}-PA SAMs indicates a smaller degree of charge trapping in these TFTs, as discussed previously.[30,35] Also, the transfer curves of the TFT with the HC_{14}-PA SAMs displays a small hysteresis, which may be an indication of dielectric polarization.[31] We take this combination of large carrier mobility and hysteresis as an additional indication of dielectric polarization in this HMD.

In order to obtain physical insight into the electrical device characteristics we have evaluated the interface roughness within the HMDs of all samples by X-ray reflectivity (XRR), which is a well-known technique for investigating the structure and interface quality of dielectric layers. These measurements were performed prior to the semiconductor deposition, and the results are shown in **Figure 5**. The measured reflectivity intensity is plotted as a function of the vertical momentum transfer vector, $q_z = 4\pi \sin(2\theta/2)$. The curves are displaced for better visualization. As can be seen in Figure 5, increasing the number of Al_2O_3/SAM bilayers leads to the appearance of satellite peaks in the XRR curves (indicated by arrows). The Δq_z intervals between the satellite peaks are related to the bilayer thickness d by $\Delta q_z = 2\pi/d$. Additionally, short-period oscillations δq_z are observed due to the interference of scattering from the top interface (HMD/air) with scattering from the bottom interface (HMD/Si substrate). These features provide the total HMD thickness D by $\delta q_z = 2\pi/D$. All measured HMD thicknesses are in agreement with the nominal thicknesses. For the Al_2O_3/HC_{10}-PA SAM HMDs [Figure 5a], one notices that the satellite peaks are broad and that the short-period oscillations vanish for $q_z > 0.3$ Å^{-1}. This is also observed for the Al_2O_3/HC_{18}-PA SAM HMDs [Figure 5c]. In contrast, the reflectivity curves measured on the Al_2O_3/HC_{14}-PA SAM HMDs [Figure 5b] exhibit narrower satellite peaks, and the short-period oscillations are observed up to larger q_z values.

The preservation of the short-period oscillations as well as the narrowing of the satellites indicate that the average roughness at the interfaces between adjacent bilayers within the

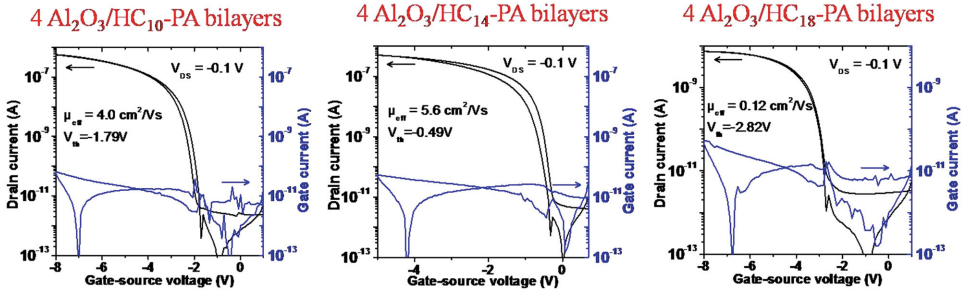

Figure 4. Transfer curves of DNTT TFTs with HMDs composed of four Al_2O_3/SAM bilayers based on each of the three alkylphosphonic acids. The carrier mobility and the threshold voltage are given in the graphs.

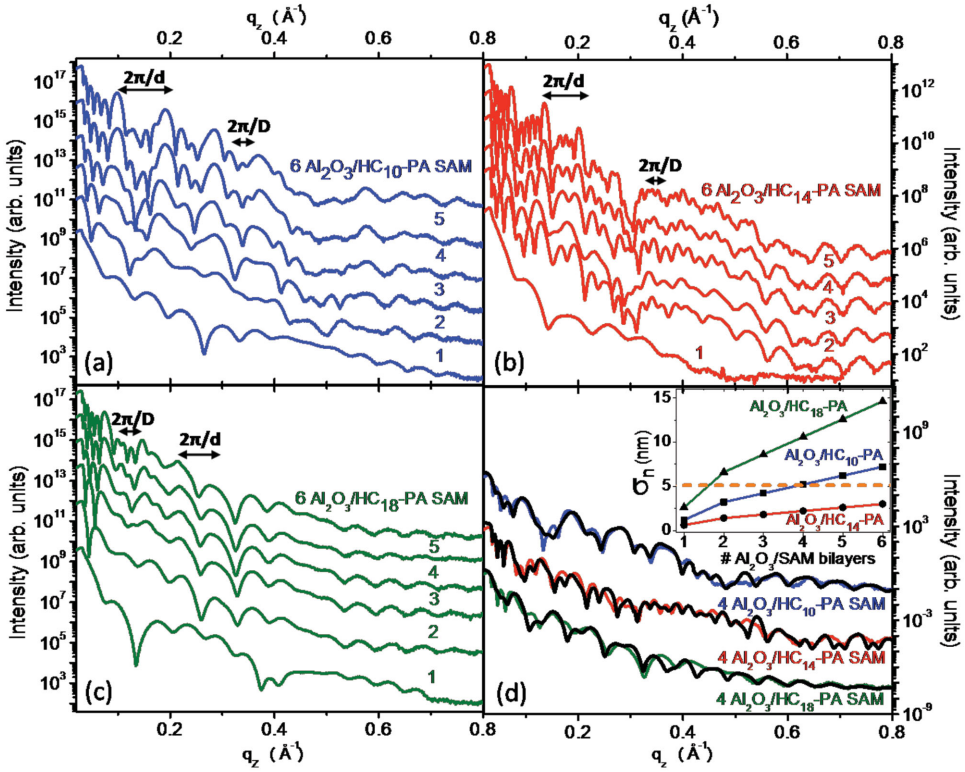

Figure 5. X-ray reflectivity measured on all HMDs studied in this work. a) Al_2O_3/HC_{10}-PA SAM HMDs; b) Al_2O_3/HC_{14}-PA SAM HMDs; c) Al_2O_3/HC_{18}-PA SAM HMDs. d) The reflectivity curves measured on the samples with four Al_2O_3/SAM bilayers (represented as blue, red, and green lines) were fitted with a modified Parratt model (depicted as black lines). The inset depicts how the interface roughness increases with the number of stacked Al_2O_3/SAM bilayers, with a slope that depends critically on the alkyl chain length of the phosphonic acid. A roughness threshold of 5 nm for the topmost dielectric surface is indicated by the dashed line.

Al_2O_3/HC_{14}-PA SAM HMDs is smaller than that in the HMDs based on the other two phosphonic acids. In order to obtain the interfacial roughness, theoretical fits were performed using the Parratt model.[36–38] In Figure 5d, we show fits obtained for HMDs consisting of four Al_2O_3/SAM bilayers with each of the three phosphonic acids. By fitting the reflectivity curves we have found a dependence of the interfacial roughness on the number of Al_2O_3/SAM bilayers. For simplification, we have introduced a linear roughness variation across the stack, where the upper interfaces have larger roughness than the lower interfaces. In the modified Parratt model used here, the interfacial bilayer roughness is given by $\sigma_n = \sigma_n + (n-1)^*\delta\sigma$, where n denotes the interface ($n = 1$ for the bottom interface) and $\delta\sigma$ the additional interface roughness obtained with each additional Al_2O_3/SAM bilayer. Using this assumption we observed the vanishing of short-period oscillations as well as the disappearance of the satellite peaks for $q_z > 0.3$ Å^{-1} in the HC_{10}-PA and HC_{18}-PA samples. The inset of Figure 5d shows the interface roughness along the stack retrieved from our simulations. This figure shows that the increase in interface roughness with each additional Al_2O_3/SAM bilayer is most pronounced when the SAM consists of HC_{18}-PA and least pronounced for the HC_{14}-PA SAM. By combining the information from Figure 1b with those from the inset of Figure 5d, we can define for our DNTT-based TFTs a threshold for the surface roughness of the topmost dielectric surface of about 5 nm, indicated by the dashed line in the inset of Figure 5d. As long as the surface roughness of the topmost dielectric layer is smaller than this threshold, the addition of another Al_2O_3/SAM bilayer enhances the carrier mobility in the organic semiconductor, whereas when the surface roughness of the topmost dielectric layer is larger than such threshold, additional bilayers will lead to smaller mobility. The mobility-roughness trend discussed above is expected to have general validity, and the value of the surface roughness threshold will depend on the properties of the organic semiconductor, e.g., its molecular size, crystal structure, orbital overlap, etc.

The roughness and polarization effects discussed in the previous paragraphs are the key factors for correlating the structural and electrical characteristics in order to provide a physical scenario that explains the observed enhancement in carrier mobility and operational stability of the TFTs with the Al_2O_3/HC_{14}-PA SAM HMDs. In all TFTs we fabricated, a significant difference between the capacitance behavior of HMDs with one and two bilayers was observed. Average permittivity values of 5.1, 3.4, and 5.0 ε_0 were measured for capacitors with one Al_2O_3/SAM bilayer based on HC_{10}-PA, HC_{14}-PA, and HC_{18}-PA, respectively (values are expressed in terms of $\varepsilon_0 = 8.85 \times 10^{-12}$ $C^2N^{-1}m^{-2}$). For two bilayers, all systems exhibit permittivities above 8 ε_0. For four bilayers, permittivities of 11.1 ε_0 (HC_{10}-PA), 9.6 ε_0 (HC_{14}-PA), and 9.8 ε_0 (HC_{18}-PA) were obtained. This indicates a higher degree of polarization in the HMD as the

number of bilayers is increased. On the other hand, the increase in interface roughness with increasing number of bilayers leads to smaller semiconductor grain size,[24–28] which is known to have a detrimental effect on the carrier mobility. Therefore, although the capacitances measured for four bilayers are similar for all three alkylphosphonic acids, the resulting carrier mobility will be smaller in HMDs in which the interface roughness is greater than the threshold of 5 nm discussed above, compared to HMDs with small interface roughness. Finally, larger interface roughness is also known to cause charge trapping,[30–32] which has a detrimental effect on the operational stability of the TFTs. In this scenario, the combination of polarization effects in the dielectric and a small degree of charge trapping (due to small interface roughness) leads to an improved carrier mobility in combination with improved bias-stress stability.

From the data analysis and the experimental results discussed so far, we have thus identified the interface roughness as the major factor determining the carrier mobility of our TFTs. The discussed effects of dielectric polarization and charge trapping arising from the interface roughness are illustrated in **Figure 6**.

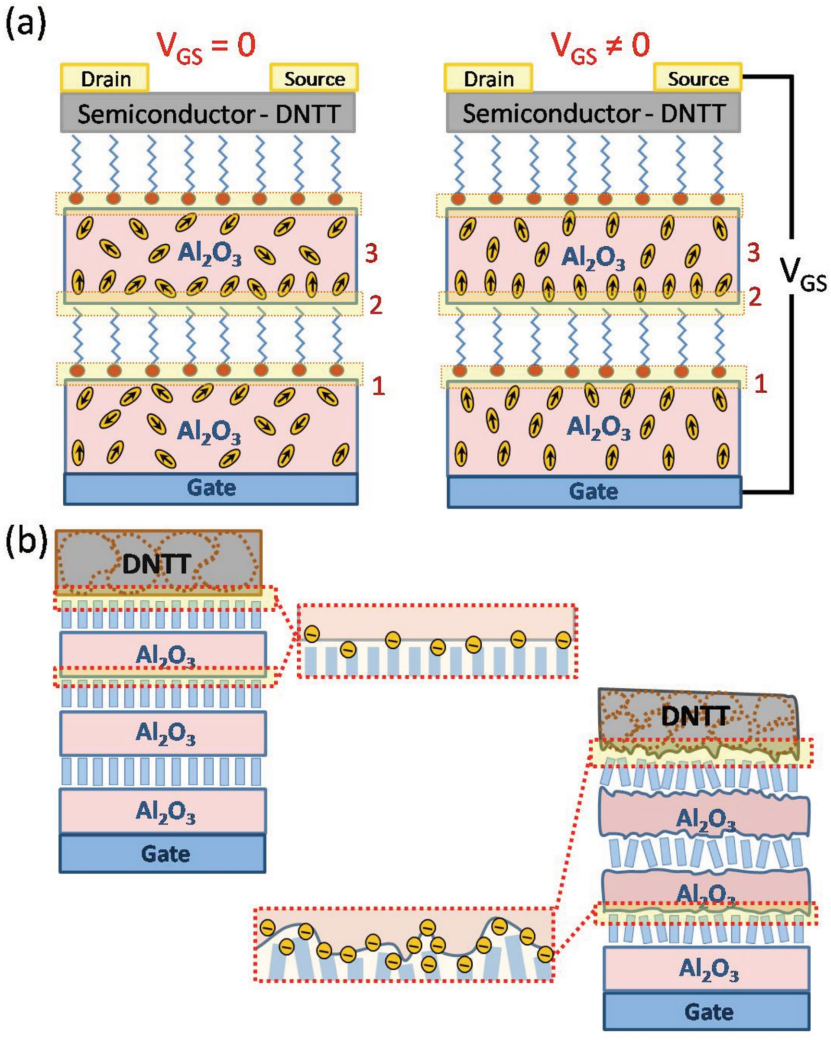

Figure 6. a) Illustration of the effect of the electric field-induced orientation of dipolar groups in the Al_2O_3 layers under an applied gate-source voltage (V_{GS}). b) For rougher interfaces, the charge trapping is more effective, as sketched in the image. TFTs based on HMDs with smaller interface roughness also exhibit enhanced carrier mobility due to structural effects on the DNTT layer. Dotted lines in the semiconductor layer indicate the observed grain size, which depends on interface roughness.

In the following lines, we will describe the polarization effects in more detail. All Al_2O_3 layers inside our HMDs were deposited at a relatively low temperature of 60 °C, so that the TFTs can in principle be fabricated on substrates that do not withstand high process temperatures (e.g., flexible plastics or paper). ALD of Al_2O_3 at this temperature is known to lead to the incorporation of a relatively large concentration of hydrogen (20% in atomic species) compared to Al_2O_3 films grown at higher temperatures (about 5% hydrogen in films grown at 200 °C).[13] Such large hydrogen concentration suggests the presence of dipolar groups stemming from the aluminum precursor, as well as OH groups from water. We believe that incomplete polar precursor groups, such as Al(OH) and $Al(OH)_2$, may also be present. Although these groups would not present translational degrees of freedom within the Al_2O_3 films, they could be able to locally polarize under applied bias. Once a gate-source voltage (V_{GS}) is applied in the TFTs, remnant precursor groups align their dipole moment, as depicted in Figure 6a, inducing a more effective polarization whenever a larger number of Al_2O_3/SAM bilayers are stacked.

The presence of dipolar groups in the bulk of the Al_2O_3 alone cannot fully explain the observed dependence of the carrier mobility on the number of Al_2O_3/SAM bilayers. We believe the polarization of remnant precursor groups is more effective at the Al_2O_3/SAM interfaces (regions 1 and 2 in Figure 6 a) than in the Al_2O_3 bulk and therefore results in a more pronounced effect for a larger number of Al_2O_3/SAM interfaces, i.e., for a larger number of stacked bilayers. Alkylphosphonic acid SAMs have a dipole moment [6,39] and the deposition of Al_2O_3 on top of each SAM creates conditions that allow for a larger density of remnant groups at the inorganic/organic interfaces, thus enhancing polarization in these regions. A less pronounced dipole effect can occur inside the Al_2O_3 layers [region 3 of Figure 6a]. The orientation of dipolar groups at the Al_2O_3/SAM interfaces and within the Al_2O_3 layers before and after the application of a gate-source voltage is illustrated in Figure 6a.

A complete explanation of the observed scenario can be provided based on the interface roughness analysis. The interface roughness in the HMDs has a direct influence on the quality of the organic semiconductor layer, as sketched in Figure 6b.[11] In our systems, a reduced interface roughness allows for better molecular ordering in the organic semiconductor layer, which

leads to improved electronic interactions between neighboring molecules and thus reduces carrier scattering in the semiconductor. Rougher interfaces favor charge trapping, thereby affecting the operational stability of the TFTs. Both our X-ray reflectivity data evaluation (buried interfaces) as well as the AFM measurements (only topmost surface) show that the HMDs based on the HC_{14}-PA SAM have the smallest interface roughness, which is consistent with earlier reports.[17] Since the capacitance of the HMDs is only weakly affected by the choice of the alkylphosphonic acid (see Figure S1), the mobility enhancement seen in Figure 1 must be indirectly related to the interface roughness via the semiconductor grain size.

In summary, hybrid multilayer dielectrics composed of alternating layers of Al_2O_3 prepared by atomic layer deposition and alkylphosphonic acid SAMs prepared from solution were employed as the gate dielectric of organic thin-film transistors. The small interface roughness and polarization phenomena lead to a larger charge-carrier mobility and better operational stability compared with TFTs based on simpler gate dielectrics. Our results show that polarization occurs at the inorganic/organic interfaces of the hybrid multilayer dielectrics and is more pronounced as the number of bilayers is increased. Reduced charge trapping effects are observed in devices with smoother interfaces, leading to improved operational stability. A 5 nm roughness threshold was found as the maximum value that allows for large DNTT grain size and provides mobility enhancement on our HMD-based TFTs. This optimal dielectric surface roughness range is applicable to DNTT-based devices, while a similar trend is expected to be found on other systems and must be investigated whenever the use of HMDs is envisaged for improving device performance.

Experimental Section

Device Fabrication: All TFTs were fabricated on doped silicon substrates (also serving as the gate electrode of the TFTs) covered with native silicon dioxide (approximately 2 nm thick). The gate dielectric is a hybrid multilayer dielectric (HMD) consisting of alternating layers of aluminum oxide (Al_2O_3) and alkylphosphonic acid self-assembled monolayers (SAMs). The Al_2O_3 layers were grown by atomic layer deposition (ALD) in a Cambridge Nanotech Savannah 100 reactor with pulse and purge intervals of 0.015 s/20 s for trimethylaluminum (TMA) and 0.015 s/30 s for H_2O. The first Al_2O_3 layer was deposited at a temperature of 250 °C, while all additional layers were deposited at 60 °C. Each Al_2O_3 layer has a thickness of 9 nm. After the deposition of each Al_2O_3 layer, an oxygen plasma treatment was performed to produce reactive groups at the Al_2O_3 surface (oxygen flow rate: 30 sccm, oxygen partial pressure: 10 mTorr, plasma power: 200 W, plasma duration: 20 s). SAMs were prepared by immersing the substrate into a 2-propanol solution of one of three alkylphosphonic acids, namely HC_{10}-PA [$CH_3(CH)_9PO(OH)_2$], HC_{14}-PA [$CH_3(CH)_{13}PO(OH)_2$], or HC_{18}-PA [$CH_3(CH)_{17}PO(OH)_2$], followed by drying with compressed nitrogen and annealing on a hot plate at a temperature of 100 °C for 10 min. In order to obtain samples with a distinct number of Al_2O_3/SAM bilayers, the deposition of Al_2O_3 layers by ALD and the preparation of alkylphosphonic acid SAMs were alternated in cycles. After the preparation of the last Al_2O_3/SAM bilayer, a 25 nm thick layer of the organic semiconductor dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) was deposited in vacuum, with the substrate held at a temperature of 60 °C and using a fixed deposition rate of 0.2 Å s^{-1}. Finally, 30 nm thick Au source and drain contacts were deposited by thermal evaporation using a shadow mask. All transistors have a channel length of 100 µm and a channel width of 200 µm.

Structural Characterization: Dielectric and semiconductor topographies were investigated by atomic force microscopy (AFM) using a Veeco microscope in contact mode. In order to investigate the structure of the multilayer dielectric, X-ray reflectivity measurements were performed at the XRD2 beamline of the Brazilian Synchrotron Light Laboratory (LNLS). The beamline is placed after a bending magnet source and is equipped with a cylindrically bent Rh-coated mirror, a sagittal focusing Si(111) double-crystal monochromator and a 4+2 axis diffractometer. All measurements were performed with a fixed energy of 8 keV.

Electrical Characterization: The current–voltage characteristics and the bias-stress behavior of the TFTs were measured using an Agilent 4156C parameter analyzer. The capacitance-frequency measurements were performed using a function generator, a low-noise current amplifier and a lock-in amplifier on dedicated silicon/dielectric/metal capacitors (without semiconductor). The charge-carrier mobility of the TFTs was calculated by fitting the measured transfer curves to the following equation

$$I_D = \frac{\mu C_{diel} W}{L}\left((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right) \quad (1)$$

where µ is the carrier mobility, C_{diel} is the dielectric capacitance (see Figure S1, Supporting Information), W is the channel width (200 µm), L is the channel length (100 µm), V_{GS} is the gate-source voltage, V_{DS} is the drain-source voltage (–0.1 V), and V_{th} is the threshold voltage.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

The authors acknowledge CNPq, FAPEMIG, and CAPES for financial support. The Brazilian Synchrotron Light Laboratory (LNLS—via XRD2 beamline proposals) and MCTI are gratefully acknowledged. M. de Pauli would like to thank the people from Max Planck Institute for Solid State Research (MPI—Stuttgart), Marion Hagel for the assistance in the Al_2O_3 deposition, Ulrike Kraft for the help with the capacitance measurements, and Reinhold Rödel, Mahdieh Aghamohammadi, and Sibani Bisoyi for the discussion and help in this work. Prof. Gustavo Safar from Universidade Federal de Minas Gerais is acknowledged for scientific discussions.

Received: November 19, 2015
Revised: January 17, 2016
Published online: February 11, 2016

[1] H. Dong, L. Jiang, W. Hu, *Phys. Chem. Chem. Phys.* **2012**, *14*, 14165.
[2] S. Kobayashi, T. Nishikawa, T. Takenobu, S. Mori, T. Shimoda, T. Mitani, H. Shimotani, N. Yoshimoto, S. Ogawa, Y. Iwasa, *Nat. Mater.* **2004**, *3*, 317.
[3] K. P. Pernstich, A. N. Rashid, S. Haas, G. Schitter, D. Oberhoff, C. Goldmann, D. J. Gundlach, B. Batlogg, *J. Appl. Phys.* **2004**, *96*, 6431.
[4] S. K. Possanner, K. Zojer, P. Pacher, E. Zojer, F. Schuerrer, *Adv. Funct. Mater.* **2009**, *19*, 958.
[5] U. Zschieschang, F. Ante, M. Schlörholz, M. Schmidt, K. Kern, H. Klauk, *Adv. Mater.* **2010**, *22*, 4489.
[6] M. Aghamohammadi, R. Rödel, U. Zschieschang, C. Ocal, H. Boschker, R. T. Weitz, E. Barrena, H. Klauk, *Appl. Mater. Interfaces* **2015**, *7*, 22775.

[7] P. H. Wöbkenberg, J. Ball, F. B. Kooistra, J. C. Hummelen, D. M. de Leeuw, D. D. C. Bradley, T. D. Anthopoulos, *Appl. Phys. Lett.* **2008**, *93*, 013303.
[8] H. Klauk, U. Zschieschang, J. Pflaum, M. Halik, *Nature* **2007**, *445*, 745.
[9] M. H. Yoon, A. Facchetti, T. J. Marks, *Proc. Natl. Acad. Sci. U.S.A.* **2005**, *102*, 4678.
[10] S. A. DiBenedetto, D. Frattarelli, A. Facchetti, M. A. Ratner, T. J. Marks, *J. Am. Chem. Soc.* **2009**, *131*,11080.
[11] Y. G. Ha, J. D. Emery, M. J. Bedzyk, H. Usta, A. Facchetti, T. J. Marks, *J. Am. Chem. Soc.* **2011**, *133*, 10239.
[12] S. M. George, *Chem. Rev.* **2010**, *110*, 111.
[13] M. D. Groner, F. H. Fabreguette, J. W. Elam, S. M. George, *Chem. Mater.* **2004**, *16*, 639.
[14] R. Luschtinetz, A. F. Oliveira, J. Frenzel, J.-O. Joswig, G. Seifert, H. A. Duarte, *Surf. Sci.* **2008**, *602*, 1347.
[15] A. Jedaa, M. Burkhardt, U. Zschieschang, H. Klauk, D. Habich, G. Schmid, M. Halik, *Org. Electronics* **2009**, *10*, 1442.
[16] Y. Chung, B. Murmann, S. Selvarasah, M. R. Dokmeci, Z. Bao, *Appl. Phys. Lett.* **2010**, *96*, 133306.
[17] K. Fukuda, T. Hamamoto, T. Yokota, T. Sekitani, U. Zschieschang, H. Klauk, T. Someya, *Appl. Phys. Lett.* **2009**, *95*, 203301.
[18] M. de Pauli, M. C. Prado, M. J. S. Matos, G. N. Fontes, C. A. Perez, M. S. C. Mazzoni, B. R. A. Neves, A. Malachias, *Langmuir* **2012**, *28*, 15124.
[19] M. de Pauli, C. A. Perez, M. C. Prado, D. H. C. Araujo, B. R. A. Neves, A. Malachias, *Synth. Metals* **2012**, *161*, 2521.
[20] D. M. Spori, N. V. Venkataraman, S. G. P. Tosatti, F. Durmaz, N. D. Spencer, S. Zurcher, *Langmuir* **2007**, *23*, 8053.
[21] M. de Pauli, R. Magalhães-Paniago, A. Malachias, *Phys. Rev. E* **2013**, *87*, 052402.
[22] U. Zschieschang, F. Ante, D. Kälblein, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Someya, J. Blochwitz- Nimoth, H. Klauk, *Org. Electronics* **2011**, *12*, 1370.
[23] G. Horowitz, M. E. Hajlaoui, R. J. Hajlaoui, *J. Appl. Phys.* **2000**, *87*, 4456.
[24] S. Steudel, S. De Vusser, S. De Jonge, D. Janssen, S. Verlaak, J. Genoe, P. Heremans, *Appl. Phys. Lett.* **2004**, *85*, 4400.
[25] S. E. Fritz, T. W. Kelley, C. D. Frisbie, *J. Phys. Chem. B* **2005**, *109*, 10574.
[26] K. Suemori, S. Uemura, M. Yoshida, S. Hoshino, N. Takada, T. Kodzasa, T. Kamata, *Appl. Phys. Lett.* **2008**, *93*, 033308.
[27] W. H. Lee, C. C. Wang, *J. Vac. Sci. Technol. B* **2009**, *27*, 1116.
[28] G. Lin, Q. Wang, L. Peng, M. Wang, H. Lu, G. Zhang, G. Lv, L. Qiu, *J. Phys. D: Appl. Phys.* **2015**, *48*, 105103.
[29] B. Hekmatshoar, S. Wagner, J. C. Sturm, *Appl. Phys. Lett.* **2009**, *95*, 143504.
[30] S. G. J. Mathijssen, M. Kemerink, A. Sharma, M. Colle, P. A. Bobbert, R. A. J. Janssen, D. M. de Leeuw, *Adv. Mater.* **2008**, *20*, 975.
[31] M. Egginger, S. Bauer, R. Schwödiauer, H. Neugebauer, N. S. Sariciftci, *Monatsh. Chem.* **2009**, *140*, 735.
[32] D. K. Hwang, C. Fuentes-Hernandez, J. Kim, W. J. Potscavage Jr., S.-J. Kim, B. Kippelen, *Adv. Mater.* **2011**, *23*, 1293.
[33] Y.-S. Li, B.-L. Yeh, M.-R. Tsai, H.-L. Cheng, S.-J. Liu, F.-C. Tang, W.-Y. Chou, *J. Appl. Phys.* **2015**, *117*, 104507.
[34] R. Hofmockel, U. Zschieschang, U. Kraft, R. Rödel, N. H. Hansen, M. Stolte, F. Würthner, K. Takimiya, K. Kern, J. Pflaum, H. Klauk, *Org. Electronics* **2013**, *14*, 3213.
[35] Y. R. Liu, R. Liao, P. T. Lai, R. H. Yao, *IEEE Trans. Dev. Mat. Reliability* **2012**, *12*, 58.
[36] L. G. Parratt, *Phys. Rev.* **1954**, *95*, 359.
[37] S. K. Sinha, E. B. Sirota, S. Garoff, *Phys. Rev. B* **1988**, *38*, 2297.
[38] M. de Pauli, A. Malachias, H. WestfahlJr., J. Bettini, A. Ramirez, G. S. Huang, Y. F. Mei, O. G. Schmidt, *J. Appl. Phys.* **2011**, *109*, 063524.
[39] M. Salinas, C. M. Jager, A. Y. Amin, P. O. Dral, T. Meyer-Friedrichsen, A. Hirsch, T. Clark, M. Halik, *J. Am. Chem. Soc.* **2012**, *134*, 12648.

WILEY-VCH

Supporting Information

Tailoring the Dielectric Layer Structure for Enhanced Carrier Mobility in Organic Transistors: The Use of Hybrid Inorganic/Organic Multilayer Dielectrics

Muriel de Pauli[1], *Ute Zschieschang*[2], *Ingrid David Barcelos*[1], *Hagen Klauk*[2] *and Angelo Malachias*[1*]

[1]Universidade Federal de Minas Gerais, Physics Department, ICEx, Av. Antonio Carlos, 6627, Belo Horizonte, CEP 30123-970, Brazil
[2] Max Planck Institute for Solid State Research, Heisenbergstr. 1, 70569, Stuttgart, Germany

1. Dielectric capacitance measurements.
2. Transfer characteristics of the TFTs
3. Output characteristics of the TFTs
4. AFM
5. Bias-stress measurements on TFTs with Al_2O_3/HC_{10}-PA SAM and Al_2O_3/HC_{18}-PA SAM HMDs
6. Gate current during bias-stress measurements
7. Bias-stress measurements on TFTs based on C_{10}-DNTT as the semiconductor

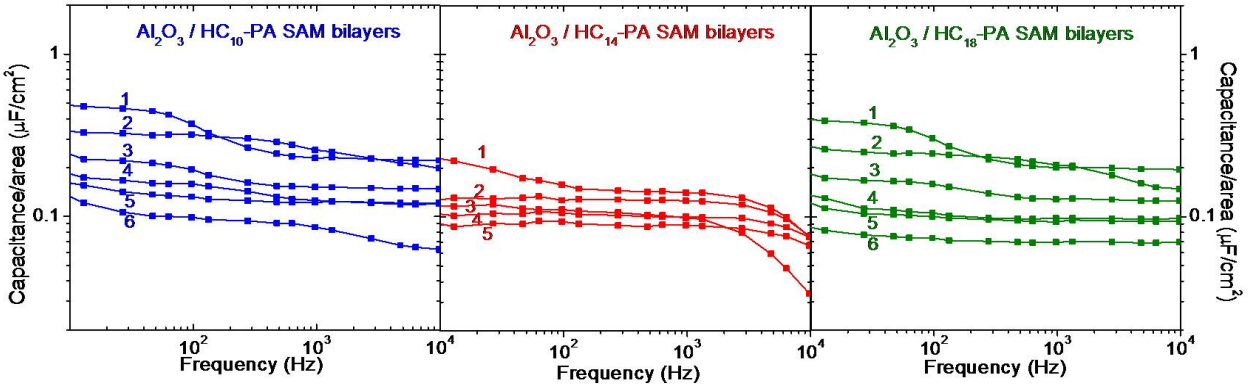

Figure S1. Dielectric capacitance measured as a function of frequency for HMDs composed of 9-nm-thick layers of Al_2O_3 and SAMs of either (a) HC_{10}-PA, (b) HC_{14}-PA or (c) HC_{18}-PA, with the number of Al_2O_3/SAM bilayers ranging from 1 to 6. The measurements were performed on dedicated silicon/dielectric/metal capacitors without semiconductor.

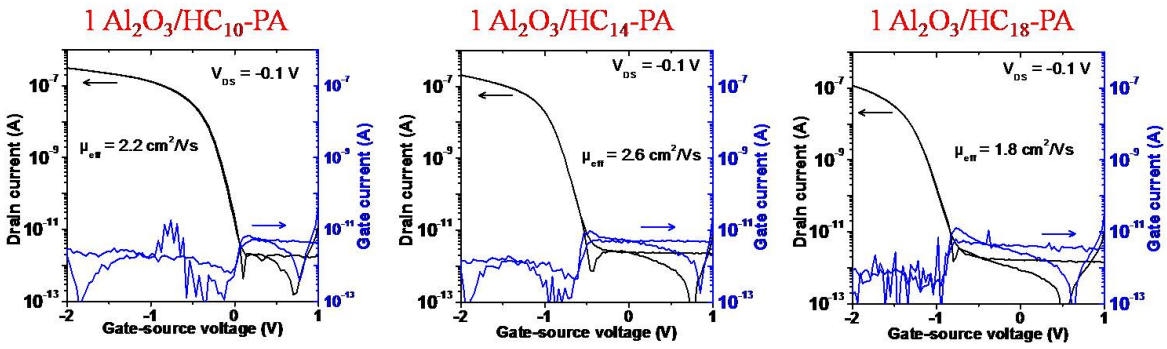

Figure S2. Transfer characteristics of DNTT TFTs with HMDs composed of 1 Al_2O_3/SAM bilayer based on each of the three alkylphosphonic acids.

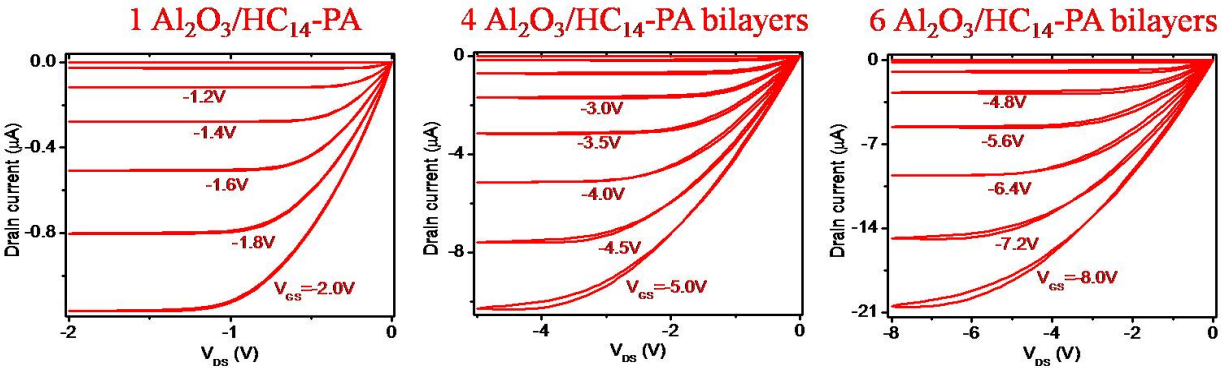

Figure S3. Output characteristics of DNTT TFTs with HMDs composed of 1, 4 or 6 Al_2O_3/HC_{14}-PA SAM bilayers.

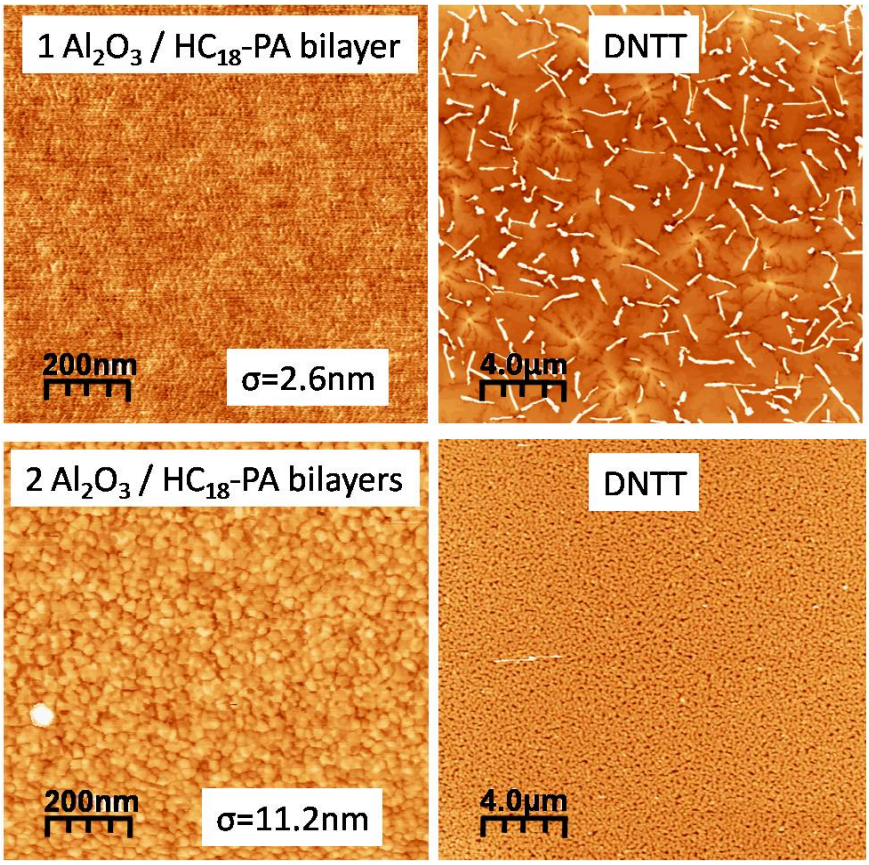

Figure S4. Topography of HMDs composed of 1 or 2 Al_2O_3/HC_{18}-PA SAM bilayers (left images) and of nominally 25-nm-thick DNTT layers deposited onto these HMDs (right images). For an average roughness of 2.6nm and 11.2nm were retrieved for the dielectric surface after 1 and 2 bilayer repetitions, respectively.

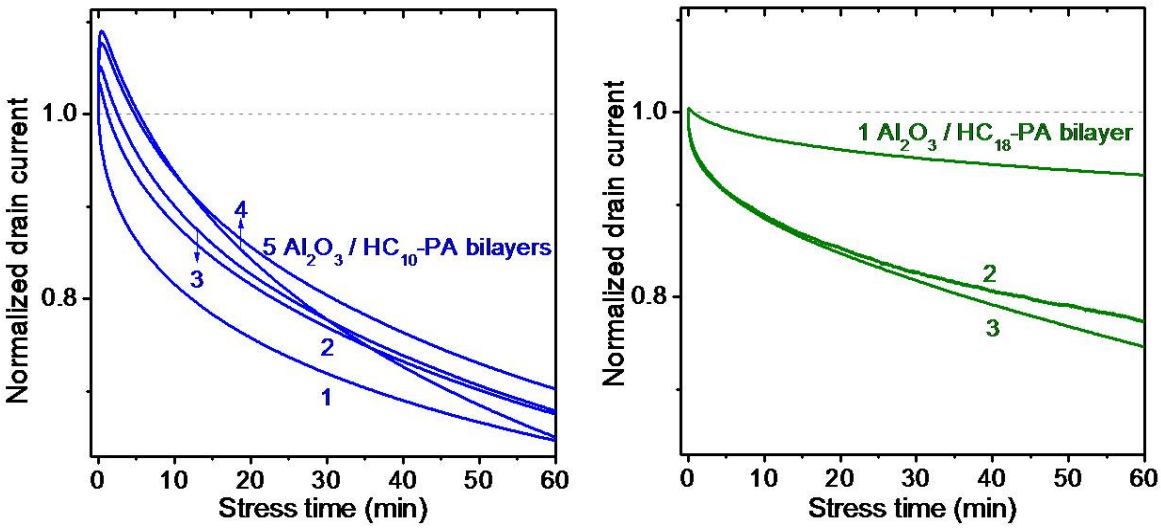

Figure S5. Bias-stress measurements on DNTT TFTs with HMDs composed of Al_2O_3/HC_{10}-PA SAM and Al_2O_3/HC_{18}-PA SAM bilayers. For the TFTs with the Al_2O_3/HC_{18}-PA SAM HMDs as well as for the TFT with a single Al_2O_3/HC_{10}-PA SAM bilayer, the drain current deceases immediately from the start of the bias-stress measurement and continues to decrease monotonically during the entire duration of the measurement. In contrast, for the TFTs with HMDs composed of 2 to 5 Al_2O_3/HC_{10}-PA SAM bilayers, the drain current initially increases before it begins to decrease. The initial increase of the drain current in the case of the Al_2O_3/HC_{10}-PA SAM HMDs is ascribed to the polarization discussed in the text.

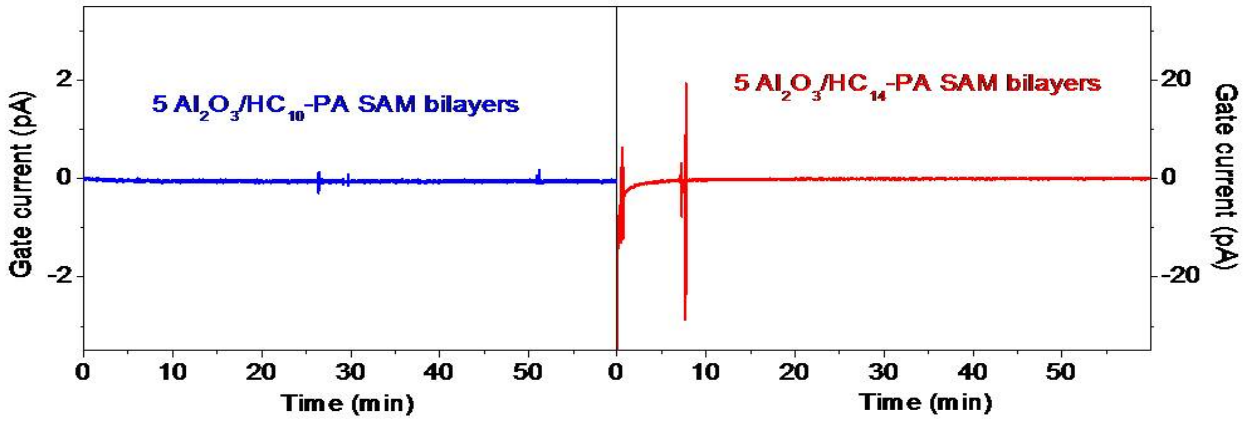

Figure S6. Gate current measured during the bias-stress measurements. As can be seen, the gate current is very small, so that charge injection from the gate can be ruled out as the reason for the observed increase of the drain current during bias stress.

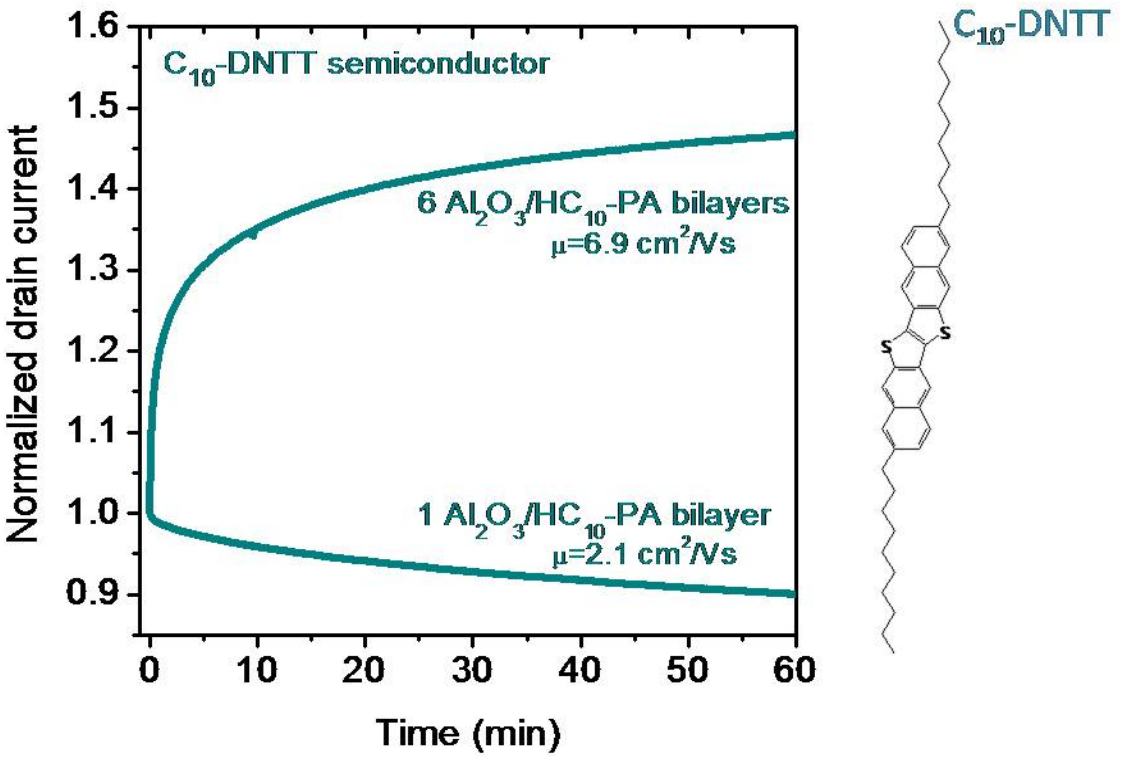

Figure S7. Bias-stress measurements on TFTs based on C_{10}-DNTT as the semiconductor. The gate dielectric consists of 1 or 6 Al_2O_3/HC_{10}-PA SAM bilayers. For the TFT with a single Al_2O_3/HC_{10}-PA SAM bilayer, the drain current deceases immediately from the start of the bias-stress measurement and continues to decrease monotonically during the entire duration of the measurement. In contrast, for the TFT with 6 Al_2O_3/HC_{10}-PA SAM bilayers, the drain current increases monotonically. This behavior is identical to the behavior observed for the DNTT TFTs (see Figure 3), which confirms that the polarization does not occur in the semiconductor, but in the gate dielectric.