High voltage surface potential measurements in ambient conditions: Application to organic thin-film transistor injection and transport characterization

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A scanning surface potential measurement technique suited for thin-film devices operating under high voltages is reported. A commercial atomic force microscope has been customized to enable a feedback-controlled and secure surface potential measurement based on phase-shift detection under ambient conditions. Measurements of the local potential profile along the channel of bottom-gate organic thin-film transistors (TFTs) are shown to be useful to disentangle the contributions from the channel and contacts to the device performance. Intrinsic contact current-voltage characteristics have been measured on bottom-gate, top-contact (staggered) TFTs based on the small-molecule semiconductor dinaphtho[2,3-b:2′,3-f]thieno[3,2-b]thiophene (DNTT) and on bottom-gate, bottom-contact (coplanar) TFTs based on the semiconducting polymer polytriarylamine (PTAA). Injection has been found to be linear in the staggered DNTT TFTs and nonlinear in the coplanar PTAA TFTs. In both types of TFT, the injection efficiency has been found to improve with increasing gate bias in the accumulation regime. Contact resistances as low as 130 Ω cm have been measured in the DNTT TFTs. A method that eliminates the influence of bias-stress-induced threshold-voltage shifts when measuring the local charge-carrier mobility in the channel is also introduced, and intrinsic channel mobilities of $1.5 \, \mathrm{cm^2 \, V^{-1} \, s^{-1}}$ and $1.1 \times 10^{-3} \, \mathrm{cm^2 \, V^{-1} \, s^{-1}}$ have been determined for DNTT and PTAA. In both semiconductors, the mobility has been found to be constant with respect to the gate bias. Despite its simplicity, the Kelvin probe force microscopy method reported here provides robust and accurate surface potential measurements on thin-film devices under operation and thus paves the way towards more extensive studies of particular interest in emerging fields of solid-state electronics. © 2016 AIP Publishing LLC. [http://dx.doi.org/10.1063/1.4944884]

I. INTRODUCTION

Within the past two decades, significant efforts have been devoted to improving our understanding of the charge-transport physics of organic semiconductors employed in electronic devices, in particular, in organic thin-film transistors (TFTs).[1,2] Atomic Force Microscopy (AFM) has been shown to be an efficient tool in this field. Its various operating modes have enabled the investigation of a wide range of properties of electronic materials and devices.[3–5] This work will focus on AFM-based surface potential measurements, often called Kelvin Probe Force Microscopy (KPFM),[6] of electronic devices under normal operating conditions, i.e., in the presence of applied voltages. Driven by the rapid development of organic light emitting diodes,[7] organic TFTs are widely studied and their performance is continuously being improved.[2] However, in a constant effort to improve the performance of organic TFTs in order to address increasingly demanding applications, it appears necessary to more clearly identify performance bottlenecks imposed either by intrinsic materials properties or by the device architecture. Current-voltage characterization is by far the most common technique to compare various technologies. From the measured transfer characteristics, an effective carrier mobility can be extracted, together with a number of other useful parameters, such as the threshold voltage and the subthreshold slope.[8] These data are effective (as opposed to intrinsic) in the sense that most extraction protocols refer to an ideal transistor current-voltage model, which real devices deviate more or less substantially from, and the extracted values are thus often modified by parasitic effects. Attempts to obtain corrected values are widely discussed in the literature,[9–11] but the task is difficult whenever the device characteristics are influenced by multiple effects simultaneously. For example, both a field activation of the mobility and an injection barrier at the source contact tend to produce the same characteristic S-shape in the output characteristics of organic TFTs.[12,13] In this particular example, an improvement of the device performance may require one of two entirely different strategies, depending on which of the two phenomena is responsible. Accessing local and intrinsic materials or device properties is therefore an important step towards a better understanding of real performance bottlenecks.

KPFM significantly contributes to this effort. Improved quantitative knowledge of the source and drain contacts and of the intrinsic mobility of organic TFTs was demonstrated by Bürgi and co-workers using KPFM.[14,15] Despite the

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evident importance of this pioneering work, KPFM surprisingly did not break through as a commonly used characterization technique. A few reasons may explain this. First, many commercial AFM/KPFM setups allow only qualitative, but no quantitative measurements. This has been attributed mainly to the parasitic cantilever interaction with the sample surface when relying on inappropriate measurement modes.[16,17] Second, application of the KPFM technique to devices during operation (i.e., while biased from external power supplies) requires a number of setup modifications depending on the targeted measurement conditions. This work describes a KPFM setup addressing these issues, hopefully contributing to its wider application. The setup is first described in detail, in particular, in those aspects related to robust measurements at high operating voltages under ambient conditions. Application of the technique to the characterization of bottom-gate, top-contact, and bottom-gate, bottom-contact organic TFTs is presented next, which demonstrates that the proposed KPFM measurement method is, indeed, a quantitative and reliable materials and device characterization tool. Examples of linear and non-linear contact characterization are given, allowing the accurate determination of their internal properties and direct observation of their detrimental effects on the characteristics of the organic TFTs. Finally, an intrinsic mobility extraction procedure is described and illustrated.

II. REQUIREMENTS FOR ACCURATE KPFM MEASUREMENTS

AFM-based potential measurement methods exploit the tip-to-sample electrostatic force.[18] A conductive tip connected to a voltage source and hovering above a surface will reach an electrostatic equilibrium in which a density of surface charges σ will appear on the tip, creating an electrostatic force. Measuring this force will provide information on the electrostatic interaction between the tip and the surface. Considering an electrically conducting sample surface with a constant potential V_{surf} in total interaction with the tip, the electrostatic force is always attractive, and its vertical axis component modulus F_{el} depends on the potential difference between the tip and the surface as follows:[16]

$$F_{el} = \frac{1}{2}\frac{\partial C}{\partial z}(V_{tip} - V_{surf})^2, \quad (1)$$

where z is the distance along the vertical axis, C is the tip-to-surface capacitance, and V_{tip} is the tip potential. The electrostatic force vanishes when the tip potential equals the surface potential, $V_{tip} = V_{surf}$. Measuring this voltage is the principle of the KPFM measurement. Various implementations of this measurement have been proposed in the literature and by instrument manufacturers.[16,19] An efficient detection method relies on bringing the cantilever into forced oscillations and on measuring modifications of these oscillations induced by the electrostatic force.

Understanding the KPFM measurement requires an understanding of the various contributions to the potential difference $V_{tip} - V_{surf}$. Indeed, Equation (1) assumes a constant surface potential, which is far from reality for most samples. First, bringing two different conducting materials

into equilibrium will give rise to a contact potential difference between them (U_{CPD}) that is equal to their work function difference. This applies to metals and semiconductors and is the basis of metal-work-function measurements using KPFM.[20,21] This measurement can be difficult under ambient conditions, since surface metal work functions are sensitive to environment and sample history. The contact potential difference is a first contribution to the measured surface potential. It is determined on the unbiased device and then subtracted from further measurements.[22]

For quantitative and local surface potential measurements, it is mandatory to emphasize the contribution of the tip apex compared to that of the cantilever. To do so, one must use a measurement method sensitive to the force gradient rather than to the force itself.[23] This is possible by using a configuration in which the cantilever is brought into oscillations using a piezoelectric element attached to it. One then measures the oscillation phase or frequency shift produced by the electrostatic interaction with respect to free oscillations. It can be shown that small phase shifts $\Delta\phi$ can be approximated by[24]

$$\Delta\phi = -\frac{Q}{2k}\frac{dF_{el}}{dz} = -\frac{Q}{2k}\left(\frac{d^2C}{dz^2}\right)(V_{tip} - V_{surf})^2, \quad (2)$$

where Q is the quality factor and k is the spring constant of the cantilever. The phase shift is zeroed when the tip potential equals the surface potential. Monitoring the phase shift while applying a DC voltage to the tip will allow the determination of the surface potential. Figure 1 compares the surface potential profiles measured using a force-sensitive method (Bruker D3100 NanoMan V) and a force-derivative-sensitive method on a validation sample. This sample consists in a highly doped silicon substrate with a 230-nm-thick thermally grown silicon dioxide layer (SiO$_2$). Metal contacts consisting of a 10-nm-thick indium tin oxide (ITO) adhesion
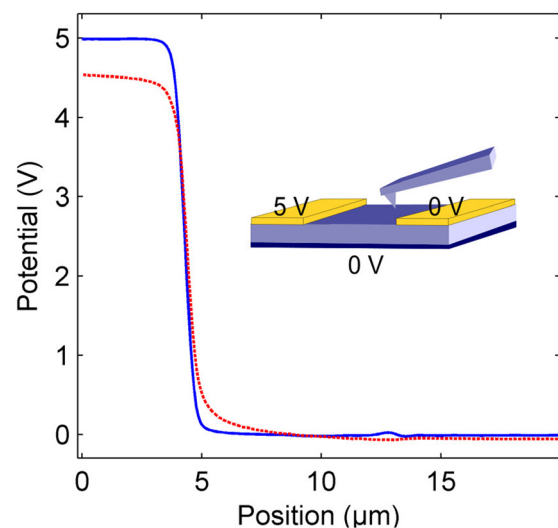

FIG. 1. Comparison of the results of two surface potential measurements, one performed using a force-sensitive method (dashed red line) and the other using the force-gradient-sensitive method described in this study (blue line). Only the force-gradient-sensitive method provides an accurate measurement of the contact potential.

layer and a 30-nm-thick Au layer were defined on the SiO_2 surface by photolithography, vacuum deposition, and lift-off. The contact spacing is $10\,\mu m$. These substrates are commercially available from the Fraunhofer Institute for Photonic Microsystems (Dresden, Germany), but a custom contact design was used here. The doped silicon substrate is used as a gate electrode, and the two metal contacts can be biased separately. Thanks to the gradient sensitive method, a quantitative determination of the voltages actually applied to the contacts on the test sample is achieved, as illustrated in Figure 1.

In the following, a simple implementation of the gradient-sensitive method is presented, allowing accurate and robust surface potential measurements on biased samples under ambient conditions.

III. METHOD FOR KPFM MEASUREMENTS ON BIASED DEVICES

Some issues must be addressed in order to obtain reliable and robust measurements, in particular, with regard to the large electrostatic force that may occur when high voltages are applied to the device. For simplicity, accuracy, and robustness, the proposed implementation uses the same equipment for both standard current-voltage measurements and KPFM measurements. The setup is illustrated in Figure 2.

The AFM is a Bruker D3100 NanoMan V. The phase difference between the photodiode AC response and the applied AC signal driving the cantilever piezoelectric element is available as an analog voltage output from the AFM. The tip is a commercial SCM-PIT from Bruker with a nominal apex radius of $20\,nm$. All DC voltage sources, voltmeters and ammeters are provided by a Keysight Technologies Precision IV Analyzer E5270B. The potentials to the source and drain contacts are applied using probe tips. Since the TFTs were fabricated on doped silicon substrates that also serve as a common gate electrode, the gate potential is applied through the chuck (100 mm diameter). (For TFTs fabricated on insulating substrates, the gate potential would be applied using another probe tip.) No dicing or bonding of the TFTs is required. To synchronize the biasing of the sample and the tip with the AFM scans, the end-of-line TTL output signals from the AFM are used. The TTL signals are detected using an Arduino Uno electronic board. An automation software has been developed, and the overall setup is synchronized with the help of an electronic board. All feedback loops are provided through software control. The AFM is operated in dual-pass mode. In this

mode, a first scan (back and forth) is performed to determine the sample topography in intermittent contact mode. During a second scan (also back and forth), the surface potential is measured. This second scan is performed with the tip maintained at a constant height above the sample surface. Compared with a single-pass acquisition in which potential and topography are measured simultaneously,[23] the dual-pass mode provides greater stability, especially when the measurement is performed under ambient conditions, when high voltages are applied, and when the sample presents a rough surface, which is often the case in organic TFTs with vacuum-deposited semiconductor layers.[25,26] When the surface topography is recorded, it is important to cancel any electrostatic interaction between the tip and the sample, in particular, in dual-pass mode. Failure to this rule could lead to a distortion of the topography measurements by several tens of nanometers, as illustrated in the supplementary material,[27] thereby impacting the subsequent surface potential measurement. Ziegler *et al.* proposed a solution where the tip bias continuously follows the previously recorded potential profile,[28] thereby canceling the electrostatic forces. This method is particularly well-suited for mapping measurements where the sample bias is kept constant. In the present work, however, the device under study is intended to be biased at various operating points during the measurements in order to obtain intrinsic contact current-voltage characteristics, as discussed in the following. In this case, for the sake of safe and robust measurements, it is preferred to zero the sample and the tip voltages during the topography measurement.[29]

Methods for surface potential measurements have already been reported. The phase variation is measured using a fixed voltage range applied to the tip,[21,24] extending over the voltage range applied to the sample for an accurate measurement of the phase parabola at all times. Therefore, when applying a wide range of voltages, strong interaction forces will occur between the tip and the sample surface while scanning, so that the above-mentioned approaches cannot be employed. Knowledge of the surface potential in real time is mandatory in order to be able to adjust the tip bias close to that of the local surface potential at any time.

The phase shift control loop is based on the following algorithm: In order to initialize the algorithm, at the very beginning of the first potential scan (trace line) a limited bias sweep is applied to the tip, centered on the expected surface potential (for example, $-1.5\,V +/-3\,V$, as illustrated in Figure 3). A first phase shift parabola is measured accordingly. At this initial stage, some points do not satisfy the
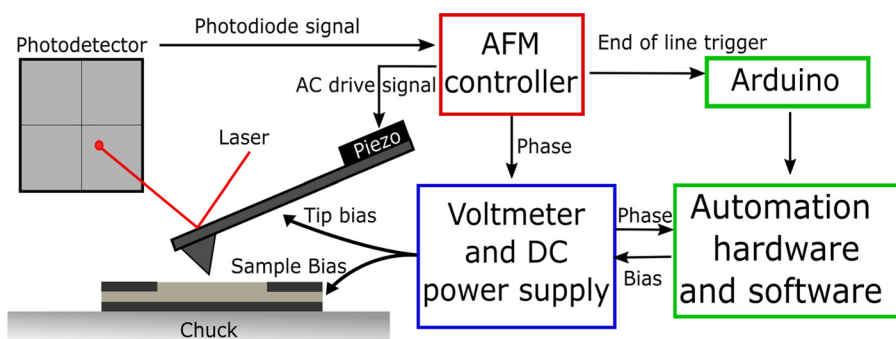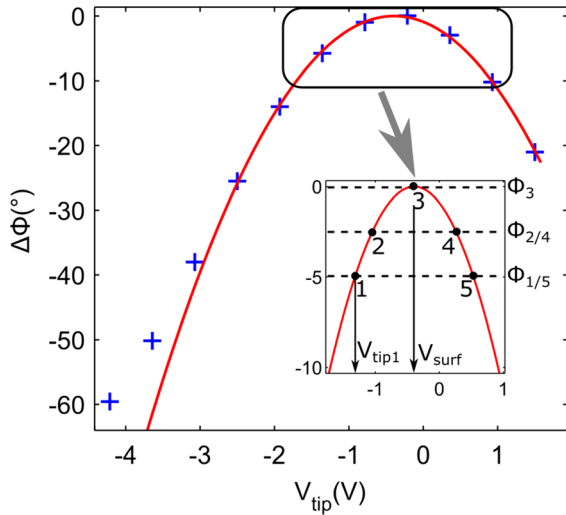

FIG. 2. Schematic of the KPFM setup.

FIG. 3. Initially measured phase shifts versus tip bias (+) and initial parabolic fit (line). The rectangle at the apex of the parabola indicates a restricted area where the phase shift will be maintained during the tracking to satisfy the small-angle approximation under which Equation (3) is valid. Within this restricted area, a set of targeted phase shifts is defined.

low-angle approximation and do not follow a parabolic approximation. Within a restricted area, however, as indicated in the inset of Figure 3, the phase locations are very close to a parabola, and a fit of the data using Equation (3) provides three coefficients describing the parabola, namely, the parabola opening $\frac{Q}{2k}(\frac{d^2C}{dz^2})$, the surface potential V_{surf} and the maximum phase shift ϕ_{max}

$$\phi = -\frac{Q}{2k}\left(\frac{d^2C}{dz^2}\right)(V_{tip} - V_{surf})^2 + \phi_{max}. \qquad (3)$$

In order to prevent any influence of the fluctuation of the free oscillation phase, in particular, due to tip apex aging, the maximum value of the parabola ϕ_{max} will be left as a free parameter during the KPFM experiment.

From this initial figure, a set of points (V_{tip_i}, ϕ_i) is defined, as shown in the inset of Figure 3. Five points are typically used. Along the entire length of the scan, this fixed number of points is updated in order to track the parabola evolution. The parabola coefficients are fitted along the length of the tip scan, and from the coefficients the surface potential and the second derivative profiles of the tip-to-surface capacitance can be determined.

Due to the continuous tip motion over the sample surface, it is not possible to update the complete set of (V_{tip_i}, ϕ_i) points instantaneously at each tip location along the scan. This is inherent to any feedback process, either digital or analog, and could lead to measurement errors if not appropriately accounted for in the design of the feedback process. To guaranty an efficient feedback, the speed of the feedback loop must be high compared to the evolution rate of the data to be controlled, here the phase parabola. Fortunately, the evolution rate of the surface potential and the parabola opening are both governed by the tip scan speed, which can be reduced down to very small values. The accuracy of the feedback process is controlled through the measured phase: The phase must not escape the restricted area in which

Equation (3) applies, typically within ±5° of the parabola maximum. If the phase is measured outside this range, the scan speed must be reduced and the experiment restarted.

To follow the parabola evolution, the phase points are updated one by one in the following way: Aiming at a phase target ϕ_i from the initially defined set, a tip bias V_{tip_i} is calculated using the following equation:

$$V_{tip\_i} = \pm \sqrt{\frac{\phi_{max} - \phi_i}{\frac{Q}{2k}\left(\frac{d^2C}{dz^2}\right)}} + V_{surf}, \qquad (4)$$

where the sign is taken negative for points located on the left side of the parabola maximum and positive for the others. The real phase shift is then measured, and it may of course differ from the targeted value. The new point replaces the old one in the set and a new parabola equation is determined. From the fitting parameters, the surface potential and the parabola opening are determined at the given tip position. During the scan, the points are updated one by one from the left to the right of the parabola, and so on.

The second derivative of the capacitance is sensitive to structure parameters other than the surface potential, such as the charge location depth, the tip shape, and the material's permittivity. Unlike the surface potential, the opening of the parabola is very sensitive to the scan height, and can thus be used as a control parameter.

Monitoring (i.e., targeting) the phase rather than the tip potential is preferred, since the phase shift is strongly dependent on the electrostatic force. Doing so keeps the force from increasing too much while describing the parabola, since the voltage range applied to the tip is automatically adapted to the parabola opening in a restricted phase range of typically ±5°. For example, in the case of a rough sample surface the parabola opening can significantly and rapidly vary during the scan. In such situations, keeping a constant voltage swing would cause failure of the small-phase approximation (as illustrated in Figure 3), and the phase shift would not follow a parabolic shape. Consequently, the calculation of the potential would not be accurate.

As mentioned above, the scan must be kept slow compared to the feedback sequence to ensure measurement accuracy and stability. Also, very importantly, a time delay must be set between the tip bias application and the phase measurement in order to enable system stabilization.[30] This delay must be measured on each system, as it may be originating from numerous factors, such as cable capacitance or probe tip relaxation time. On the present setup, the relaxation time is a few milliseconds and cannot be neglected.

IV. LATERAL RESOLUTION

Before studying active devices, it is important to determine the lateral measurement resolution, or at least its order of magnitude, under ambient conditions. Many studies have addressed the lateral resolution of KPFM, both from theoretical[31,32] and experimental[33] points of view. Unfortunately, there is no agreement on the exact definition of the lateral KPFM resolution, probably because the interaction between

the tip and the sample is a truly three-dimensional problem. The lateral resolution depends on the scan height, but it is also highly sensitive to the shape and condition of the tip. The sample topography cannot be ignored either. It seemed appropriate in this study to rely on an experimental determination of the lateral resolution, measured under conditions similar to those in the intended devices. A validation sample similar to that depicted in Figure 1 is thus employed, but here the SiO$_2$ surface was treated so as to be slightly conducting, thus offering a smooth potential slope between the two contacts and a sharp potential step at each contact edge. In order to increase the potential steps at the contact edges, the contacts were biased (3 V). The potential profile measured across the edge of one of the two contacts is shown in Figure 4. The lift height is 40 nm to provide robust measurement conditions (see supplementary material[27]), and the measurement was performed in ambient air at room temperature. Worth mentioning is that the lift height differs from the average tip-to-sample surface distance, as the tip oscillates over the surface. Using the procedure described by Riedel *et al.*[34] with parameters typically applied to a Bruker SCM-PIT probe (the typical amplitude setpoint is 110 mV in tapping mode), the additional height due to the tip oscillations was found to be between 6 and 10 nm. Therefore, a 40 nm lift height corresponds to an average tip-to-sample height of about 46–50 nm.

The measured surface potential profile has been fitted to a Gaussian function convolved with a potential step. The Gaussian function approximates the point spread function of the tip integrated along the axis perpendicular to the scan direction. The KPFM resolution is then defined as the full width at half maximum (FWHM) of the Gaussian function. From this procedure, a FWHM of 120 nm is deduced. This gives on order of magnitude of the present KPFM lateral resolution when the scan is performed about 50 nm above the sample surface. The true shape of the probe point spread function is certainly not a Gaussian, and this may partly
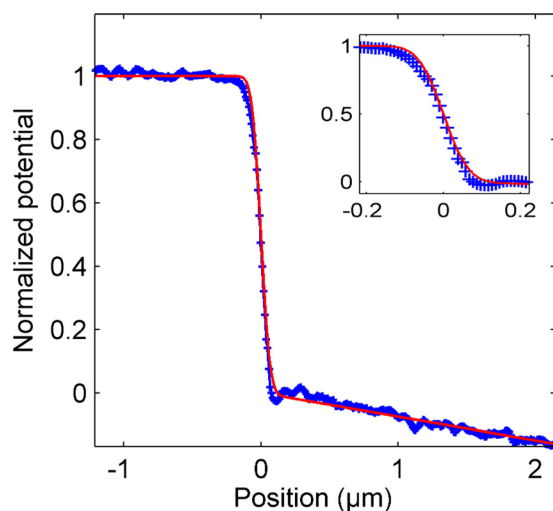
explain some slight discrepancy between the measurement and the fitting curve. Other fitting functions could have been used to obtain a better agreement. However, one must keep in mind that not all AFM tips will have the exact same point spread function. Using a simple generic function thus seemed more relevant for comparing different approaches to evaluate the measurement resolution.

To assess whether the measurement resolution degrades during the experiment due to any changes in the tip condition, it can be useful to monitor either the contact potential difference between the tip and a gold electrode or the second derivative of the tip-to-substrate capacitance. The latter signal (capacitance second derivative) is particularly sensitive to the tip condition. In our experiments, no degradation of the tip caused by the biasing of the tip was observed, and we were able to perform the experiments continuously over a period of several hours.

V. KPFM MEASUREMENTS ON ORGANIC TFTS DURING OPERATION

The contact and channel potential profiles of bottom-gate, bottom-contact (coplanar) organic TFTs have been measured. The TFTs were fabricated on a highly doped silicon substrate that also serves as the gate electrode, coated with a 230-nm-thick SiO$_2$ gate dielectric and photolithographically patterned ITO/Au source and drain contacts. The SiO$_2$ surface was passivated with a thin layer of hexamethyldisilazane (HMDS), which was deposited from the vapor phase at low pressure and at room temperature. The semiconductor, polytriarylamine (PTAA), was purchased from Sigma-Aldrich and deposited by spin-coating from a 10 mg ml^{-1} toluene solution. The resulting PTAA films have a thickness of 60 nm and a surface roughness of 1.8 nm, as measured by AFM. Results are presented in Figure 5 for a PTAA transistor with a channel length of 2 μm after contact potential correction. Due to the sensitivity of the PTAA to ambient moisture and in order to maintain stable transistor operation during the KPFM experiment, the measurements were performed in a slightly dried atmosphere of about 10% relative humidity (ambient temperature and light).

Scanning along the slow AFM axis is disengaged during the measurements at various applied voltages, resulting in repeated scans along the same single line along the transistor channel. Accurate measurement of the applied voltages on the source and drain contacts is achieved without any scaling of the data. Moreover, flat potential profiles on the source contact are obtained regardless of the applied drain bias, indicating that the contribution of the cantilever to the measurement is negligible. As explained above, this is due to the use of a measurement method that is sensitive to the force derivative, rather than to the force itself. High voltages, here up to −35 V, can thus be applied without damage. The high bias limit is mainly imposed by the speed of the phase feedback loop that allows close tracking of the high and rapidly varying potential drop near the drain contact. A high potential drop at the source contact edge is also seen in the measured potential profiles shown in Figure 5. This potential drop is not due to the intrinsic transistor operation, but rather to an

FIG. 4. Surface potential profile measured across the edge of a biased metal contact on a slightly conducting SiO$_2$ surface (blue data points). From the fit to the measurement data (red line), the lateral resolution of the KPFM setup can be determined; in this case the resolution is about 120 nm FWHM. The inset is a closer view of the potential step.
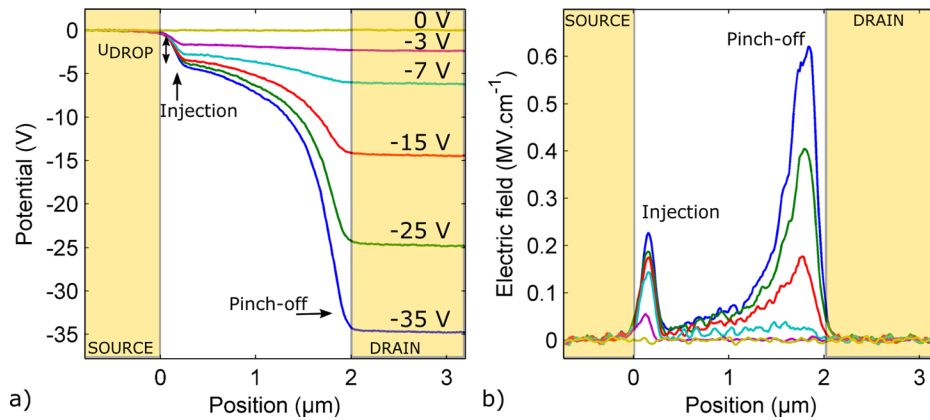
FIG. 5. (a) Measured potential profile and (b) deduced electric field in the channel of a polytriarylamine (PTAA) thin-film transistor with a channel length of $2\,\mu m$ measured at gate-source voltages of $-10\,V$.

imperfect source contact. After this initial drop, the potential evolves according to the intrinsic transistor operation regime, in agreement with theory.[35] At low drain bias, the transistor is in the linear regime where the potential profile is close to linear. When the drain bias is increased, the potential profile becomes nonlinear and may vary more and more rapidly as the tip approaches the drain contact. This is due to the pinch-off process where the gate-channel potential difference approaches or even drops below the threshold voltage in the vicinity of the drain contact. In this region, the carrier density is very small and the electric field in the channel must increase in order to drain a constant current into the drain contact. As shown in Figure 5(b), the electric field increases with increasing drain bias and reaches $0.6\,MV\,cm^{-1}$. Along most of the channel, the electric field can be determined accurately from the potential derivative. However, close to the contacts the potential may vary rapidly compared to the measurement resolution. Therefore, the peak electric fields are underestimated. This is particularly true at the source contact where it was found from a number of experiments that the potential drop can be very abrupt. In combination with the simultaneous measurement of the drain current, surface potential profiling along the TFT channel makes it possible to study the intrinsic transport properties and parasitic contact effects.

A. Intrinsic source contact characteristics

From the analysis of the potential profile, the intrinsic source contact characteristics can be obtained from the measurement of the potential drop at the source contact edge (U_{DROP}) and from the knowledge of the drain current (I_{DS}) measured along each scan line. The evolution of U_{DROP} with the drain bias, therefore with drain current, is illustrated in Figure 5, and details on the extraction procedure are given in the supplementary material.[27] In the following, examples are given for the bottom-gate, bottom-contact (coplanar) PTAA transistors described above, as well as for bottom-gate, top-contact (staggered) TFTs based on the small-molecule semiconductor dinaphtho[2,3-b:2′, 3′-f]thieno[3,2-b]thiophene (DNTT), which were fabricated as described previously.[25] Since DNTT provides good stability in air,[36] the KPFM measurements were performed under ambient conditions (air, temperature, and light). The intrinsic source contact characteristics were found

to be linear in the staggered DNTT transistors and nonlinear in the coplanar PTAA devices, and a more detailed analysis of these characteristics will be described in the following.

First, the characteristics of the top-contact DNTT TFTs are used to illustrate the measurement of an intrinsic ohmic contact resistance. The intrinsic source contact current-voltage characteristics measured for three different gate-source voltages ($-10\,V$, $-15\,V$, $-20\,V$) are shown in Figure 6. KPFM measurements where performed over the entire range of operating voltages (U_{DS} from 0 to $-20\,V$ and U_{GS} from 0 to $-20\,V$). The resulting U_{DROP} range is limited to less than $1\,V$ due to the small contact resistances.

The intrinsic source contact characteristics are linear over the entire transistor operating bias range. Accurate, intrinsic source resistances normalized to the channel width $R_S W$ can be obtained from a linear fit. The contact resistance is found to vary with the gate bias. This is expected for organic TFTs fabricated in the staggered device structure, since the sheet resistance below the source contact decreases with increasing accumulated charge density in the semiconductor.[37] The contact resistance decreases from $225\,\Omega\,cm$ at

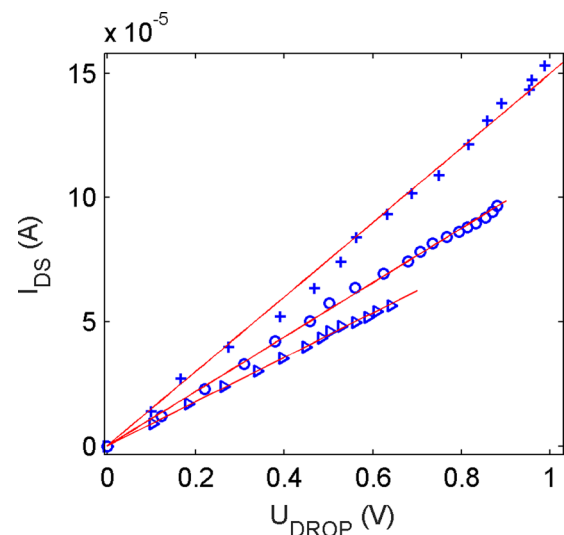

FIG. 6. Intrinsic source contact characteristics of a bottom-gate, top-contact (staggered) DNTT TFT with a channel length of $10\,\mu m$ measured at gate-source voltages of $-10\,V$ (Δ), $-15\,V$ (o), and $-20\,V$ (+). Each data set can be well approximated by a linear fit.

a gate-source voltage of $-10\,$V to $131\,\Omega\,$cm at a gate-source voltage of $-20\,$V.

Improvements in the contact performance are required in order to take advantage of emerging high-mobility organic semiconductors.[38,39] Analysis of the transistor's small-signal equivalent circuit shows that the source resistance R_S acts as a feedback that reduces the effective transconductance g_m by a factor $(1 + R_S\,g_m)$. Thus, in order for the device performance not to be limited by the source resistance, it is important that $R_S\,g_m \ll 1$. From the equation for the drain current in the saturation regime, the transconductance can be expressed as

$$g_m = \frac{\partial I_{DS}}{\partial U_{GS}} = \frac{W}{L}\mu C_i(U_{GS} - U_T), \tag{5}$$

where C_i is the gate-insulator capacitance per unit area, W is the channel width, L is the channel length, U_{GS} is the gate-source voltage, U_T is the threshold voltage, and μ is the mobility. The width-normalized source contact resistance should therefore not exceed

$$R_S W \ll \frac{L.d_i}{\mu\varepsilon_i(U_{GS} - U_T)}, \tag{6}$$

where ε_i and d_i are the gate-insulator permittivity and thickness, respectively. To give a figure: For an overdrive voltage $(U_{GS} - U_T)$ of $-10\,$V, a gate-insulator thickness of $100\,$nm, a relative permittivity of 3.9 (SiO$_2$), a channel length of $10\,\mu$m and a carrier mobility of $1.5\,$cm^2 V^{-1} s^{-1}, the contact resistance should be well below $2\,$kΩ cm. The contact resistance measured for the DNTT TFTs is an order of magnitude smaller than this target, so the source contact does not have a significant effect on the TFT performance. However, to reduce the operating voltage and increase the cutoff frequency of the TFTs, it will be required to scale both the gate-insulator thickness and the channel length.[40,41] To give numbers: Reducing both the channel length and the insulator thickness by a factor of ten without introducing contact limitations will require a contact resistance well below $200\,\Omega$ cm. This can be quite challenging, even for today's state-of-the-art organic TFTs, and reliable measurements of the intrinsic contact resistance are therefore an important contribution to the advancement of organic TFT for real applications.

In contrast to the staggered DNTT TFTs, the bottom-gate, bottom-contact (coplanar) PTAA TFTs were found to have nonlinear contact characteristics. The intrinsic current-voltage characteristics of a PTAA TFT with a channel length of $10\,\mu$m are shown in Figure 7. In this coplanar configuration, the effective carrier injection surface from the source contact into the channel is limited to the contact edge, which typically results in nonlinear TFT characteristics.[42] Again, the injection efficiency is improved when the gate bias is increased, because increasing the carrier concentration in the channel enhances the carrier injection process.

Considering the energy alignment between the Fermi level of the Au contacts and the highest occupied molecular orbital (HOMO) of PTAA,[43] a significant injection barrier

would not be expected. Deviations from this ideal picture can be caused by various types of defects that modify the Fermi energy of the contact, which might explain the observed contact injection limitation.[44] The local derivative of the contact current-voltage curves yields an apparent width-normalized contact resistance on the order of $1\,$MΩ cm. This value must be considered in view of the small channel mobility.[45] In order to appreciate how detrimental this contact resistance can be, the source contact potential drop U_{DROP} has been compared to the total voltage across the channel, U_{DS}. Results are shown in Figure 7 (inset). More than 10% of the applied bias is lost at the source contact even at high gate bias, and this fraction can increase up to 50% when the electric field at the source contact is lower. Worth noticing is that this large influence of the contact resistance is not immediately visible in the output characteristics of the TFT, shown in Figure 7(b). This illustrates how powerful intrinsic measurements are for improving our knowledge of the device physics.

B. Intrinsic channel mobility

The channel carrier mobility is probably the most important parameter of thin-film transistors. Indeed, most of the TFT performance parameters, such as their drive current and their cutoff frequency, are dependent on the mobility with a first order dependence. The mobility is usually extracted from the measured current-voltage characteristics, but as mentioned in the introduction, the extraction methods may suffer from various parasitics, first and foremost from the contact resistance.[46] Measuring the intrinsic channel mobility is therefore of great importance. The proposed method is adapted from that proposed by Bürgi *et al.*,[22] in order to account for threshold-voltage variations during current-voltage and KPFM measurements.

Neglecting the very limited contribution of the diffusion current compared to the drift current,[22] the drain current of a p-channel field-effect transistor can be expressed as

$$I_{DS} = -WQ_{acc}\mu E, \tag{7}$$

where Q_{acc} is the accumulated surface charge density and E is the electric field. Above the threshold voltage U_T, the density of holes accumulated in the channel can be well approximated by the well-known equation $Q_{acc} = -C_i(U_{GC} - U_T)$, where U_{GC} is the gate-to-channel voltage at a given position along the channel.[47] This equation applies along the entire channel length, except close to the drain contact (where the channel may be pinched off depending on the gate and drain biases) and close to the source contact (where an injection barrier may modify the charge density). Using the source as a reference potential, one has $U_{GC} = U_{GS} - U_{CS}$, where U_{CS} is the channel potential referenced to the source contact. Where applicable, the drain current can be written as

$$I_{DS} = WC_i(U_{GS} - U_T - U_{CS})\mu\frac{dU_{CS}}{dx}. \tag{8}$$

In this equation, I_{DS} is the drain current measured at all time, U_{CS} is directly available from the KPFM potential
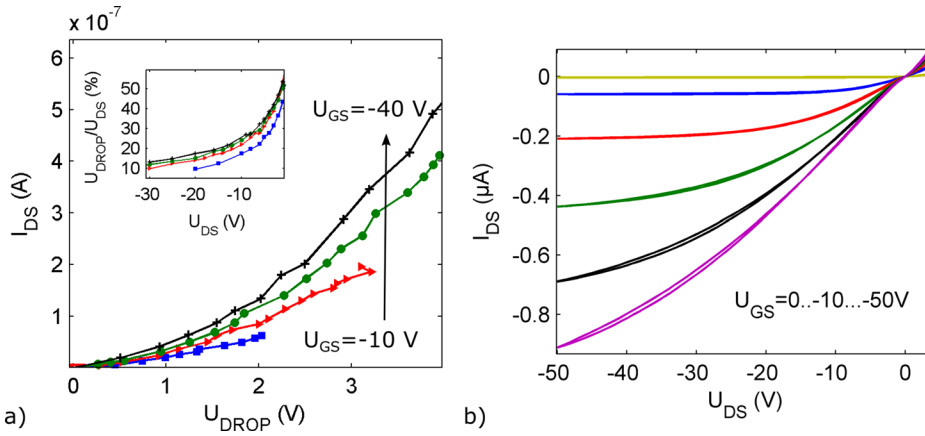
FIG. 7. (a) Nonlinear intrinsic source contact characteristics of a bottom-gate, bottom-contact (coplanar) PTAA TFT with a channel length of $10\,\mu m$ measured at gate-source voltages of $-40\,V$, $-30\,V$, $-20\,V$, and $-10\,V$. The inset shows the fraction of the drain-source voltage lost in the source contact (U_{DROP}/U_{DS}) as a function of the applied drain-source voltage U_{DS}. (b) Output characteristics of the transistor.

profile measurement, and $E = -\frac{dU_{CS}}{dx}$ is the longitudinal electric field extracted from the derivative of the measured potential. To eliminate the influence of any threshold-voltage shifts, a differential method is used where the threshold voltage is extracted simultaneously. At any channel location, the channel sheet resistance can be expressed as $R_{sheet} = 1/\sigma d$, where σ is the local channel conductivity and d the semiconductor film thickness. Given the current density $I_{DS}/(Wd) = \sigma E$, one can write $I_{DS}/(WE) = 1/R_{sheet}$. The intrinsic channel mobility can then be expressed as

$$\mu_{intrinsic} = \frac{1}{C_i}\frac{\partial(1/R_{sheet})}{\partial U_{GC}}. \tag{9}$$

This intrinsic mobility extraction method is illustrated in Figure 8 for both the coplanar PTAA transistors and the staggered DNTT transistors. Potential profiles were measured at various gate-source voltages, so that several data points are reported for the same U_{GC}, showing some fluctuations. Also, one should keep in mind that the extraction procedure is not valid close to the threshold voltage, due to the fact that the expression for the accumulated charge is only approximated.

In disordered semiconductors, the mobility may vary with both the carrier concentration and the electric field.[48] To guarantee a limited field variation within the mobility plot, the extraction procedure is performed within a restricted field range, i.e., at slightly different locations along the channel, depending on the applied gate-source and drain-source voltages. Regions close to the source and drain contacts must be ignored, as mentioned above. For the present

transistors with a channel length of $10\,\mu m$, the available field range was between 5 and $10\,kV\,cm^{-1}$. From the results shown in Figure 8, it appears that the sheet conductance varies linearly with the gate bias, indicating that the intrinsic channel mobility is constant with respect to the gate bias. Consequently, the mobility appears to be independent of the carrier concentration, at least in the explored gate bias range. Worth mentioning is that the intrinsic mobility extracted from the KPFM measurements is slightly higher than the maximum effective mobility extracted from the transfer (I_{DS} vs. U_{GS}) characteristics (see insets in Figure 8) for both the PTAA and the DNTT transistors. The difference can be attributed to parasitic contact effects which affect the current-voltage extraction method, but not the KPFM method.

VI. CONCLUSION

An efficient, robust, and accurate implementation of KPFM measurements on thin-film transistors during operation with high voltages has been described. Measurements are performed under ambient conditions directly on the transistor substrates using conventional probe needles to bias the transistors. The technique is based on phase-shift measurement and tracking. It uses an external feedback loop and a simple algorithm allowing real-time tracking of the surface potential profile. Many of the intrinsic and parasitic device properties can be accessed directly from the potential profile measurement, opening the way to systematic improvements in the device performance. The measured potential profiles
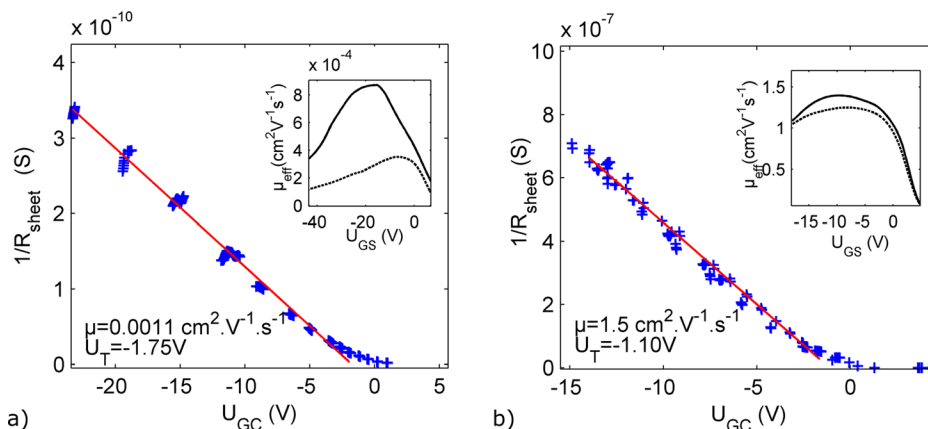

FIG. 8. Extraction of the intrinsic carrier mobility from KPFM measurements applied to (a) the coplanar PTAA transistors and (b) the staggered DNTT transistors. For comparison, the insets show the effective mobilities as extracted from the measured transfer characteristics in the linear regime (dashed line) and in the saturation regime (solid line).

have been exploited to gain a better understanding of the intrinsic contact and materials properties of organic thin-film transistors, i.e., of the injection and transport properties of these devices. In particular, linear or nonlinear intrinsic current-voltage characteristics were obtained, and contact resistances were accurately measured. The injection efficiency was shown to depend on the gate bias for both the coplanar PTAA and the staggered DNTT thin-film transistors under study. Finally, the intrinsic carrier mobility in the channel was accurately measured using an improved extraction method that is more tolerant with respect to threshold-voltage shifts. The present KPFM implementation may be applied to other emerging electronic devices, thus facilitating the identification of intrinsic and extrinsic bottlenecks and contributing to technology improvements.

ACKNOWLEDGMENTS

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