High-Performance ZnO Nanowire Transistors with Aluminum Top-Gate Electrodes and Naturally Formed Hybrid Self-Assembled Monolayer/AlO_x Gate Dielectric

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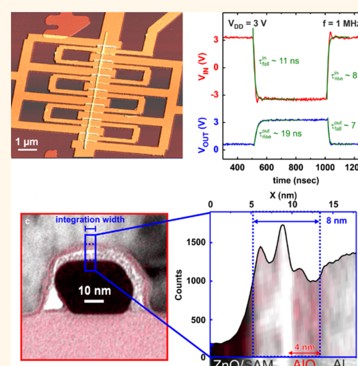
ABSTRACT A method for the formation of a low-temperature hybrid gate dielectric for high-performance, top-gate ZnO nanowire transistors is reported. The hybrid gate dielectric consists of a self-assembled monolayer (SAM) and an aluminum oxide layer. The thin aluminum oxide layer forms naturally and spontaneously when the aluminum gate electrode is deposited by thermal evaporation onto the SAM-covered ZnO nanowire, and its formation is facilitated by the poor surface wetting of the aluminum on the hydrophobic SAM. The hybrid gate dielectric shows excellent electrical insulation and can sustain voltages up to 6 V. ZnO nanowire transistors utilizing the hybrid gate dielectric feature a large transconductance of 50 μS and large on-state currents of up to 200 μA at gate-source voltages of 3 V. The large on-state current is sufficient to drive organic light-emitting diodes with an active area of 6.7 mm^2 to a brightness of 445 cd/m^2. Inverters based on ZnO nanowire transistors and thin-film carbon load resistors operate with frequencies up to 30 MHz.



KEYWORDS: zinc oxide · nanowire transistors · hybrid dielectric · organic light-emitting diodes

Field-effect transistors (FETs) based on individual[1−4] or thin films[5−7] of semiconducting nanowires are potentially useful for high-performance electronics on flexible polymeric substrates.[8] One promising target application is to replace thin-film transistors (TFTs) in active-matrix organic light-emitting diode (AMOLED) displays.[9−11] Compared to TFTs based on hydrogenated amorphous silicon or organic semiconductors, single-crystal-nanowire FETs provide larger charge-carrier mobilities and therefore permit faster pixel charging. Further, the smaller footprint of nanowire FETs compared to TFTs potentially provides a larger aperture ratio since a larger portion of the pixel area is available for the organic LED. In order to benefit from high-performance FETs based on semiconducting nanowires on flexible plastic substrates, it is important that the temperature during the FET fabrication process is below ~150 °C. Although the synthesis of single-crystalline semiconductor nanowires often involves high temperatures ($T \gg 150$ °C) that are not compatible with plastic substrates, it is in general possible to transfer the nanowires from a temperature-compatible sacrificial growth substrate to the low-temperature target substrate.[8]

To fabricate the gate dielectric, low-temperature atomic layer deposition (ALD) is often utilized.[12,13] This process allows the fabrication of thin dielectric layers that provide excellent electrical insulation and a large capacitance per unit area[14−16] at low process temperatures (~150 °C). However, while ALD offers precise control of the dielectric film thickness, control in the lateral dimension is more difficult. Standard lithographic patterning techniques, such as electron-beam lithography, are usually not applicable because the ALD films also

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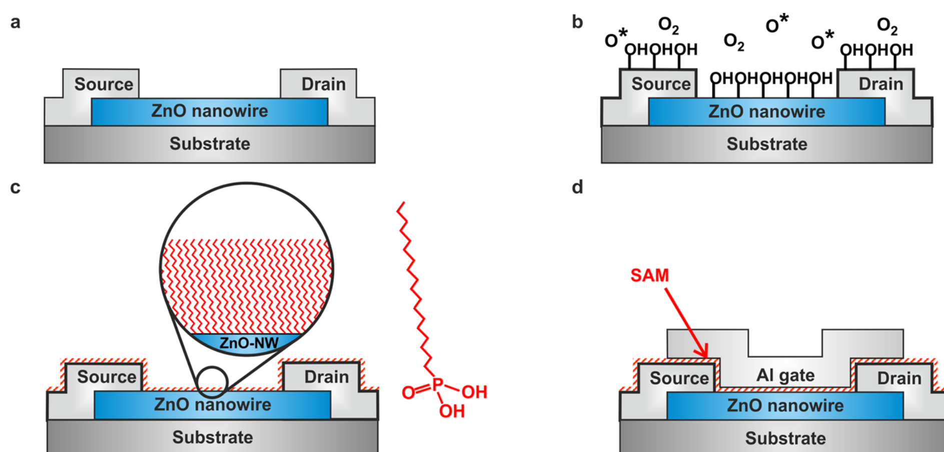

Figure 1. Fabrication of top-gate ZnO nanowire transistors. (a) Source and drain contacts are patterned on randomly dispersed ZnO nanowires by electron-beam lithography and thermal evaporation of 80 nm thick aluminum. Immediately prior to the aluminum evaporation, the contact regions are exposed to an argon-plasma treatment to increase the conductivity of the ZnO nanowire below the contacts. (b) ZnO nanowire and the aluminum contacts are exposed to a soft oxygen plasma (30 sccm O_2, 10 mTorr, 50 W, 20 s) to clean the surfaces and increase the density of hydroxyl groups. (c) Sample is immersed into a solution of 2-propanol containing 1 mmol of octadecylphosphonic acid. The self-assembled monolayer readily forms on the surfaces of the aluminum contacts and the ZnO nanowire. (d) Top-gate electrode is patterned by electron-beam lithography and thermal evaporation of 80 nm thick aluminum.

nucleate on the side walls of the resist masks, making the lift-off process difficult. Therefore, an additional patterning step and a subtractive process are usually required to control the lateral dimensions of ALD films. Here we demonstrate an alternative approach for the formation of a high-quality, high-capacitance gate dielectric in a top-gate FET configuration that can be fabricated at a low temperature (100 °C) to be fully compatible with flexible plastic substrates and without the need for subtractive dielectric patterning. In a previous report, we demonstrated the fabrication of low-voltage ZnO nanowire transistors and circuits with a very thin gate dielectric consisting of an organic self-assembled monolayer (SAM) and patterned gold top-gate electrodes.[17] While these transistors showed excellent static and dynamic performance, a significant increase of the gate current was observed when the gate-source voltage was increased above 0.5 V, making it difficult to integrate these transistors with organic LEDs for active-matrix displays.

Here we show that by replacing the gold top-gate electrode with aluminum, the thickness of the gate dielectric increases by a few nanometers due to the spontaneous formation of an interfacial aluminum oxide (AlO_x) layer at the interface between the SAM-covered ZnO nanowire and the aluminum top-gate electrode. This hybrid organic/inorganic (SAM/AlO_x) gate dielectric shows significantly improved insulation compared to the SAM-only dielectric in our previous study.[17] This makes it possible to apply larger voltages to the transistors and hence to accumulate a larger density of charge carriers in the channel and to obtain a larger transconductance and a larger cutoff frequency while maintaining low gate currents of about 1 pA. Since the aluminum oxide forms naturally during the deposition of the aluminum top-gate electrode, no additional patterning step to remove the gate dielectric layer in undesired locations is required. We demonstrate that the aluminum top-gate FETs are fully compatible with organic LEDs and operate at frequencies up to 30 MHz.

RESULTS AND DISCUSSION

The ZnO nanowires are synthesized by a wet-chemical approach utilizing a metallic zinc foil as the growth substrate.[18] The as-grown nanowires have a large charge-carrier density in the range of 10^{19} cm^{-3}, due to dopants that are unintentionally incorporated during the nanowire synthesis. Transistors based on as-grown nanowires have field-effect mobilities in the range of 20–40 cm^2/Vs, but the large charge-carrier concentration makes it difficult to modulate the drain current with the gate-source voltage. In order to reduce the charge-carrier density, a thermal anneal at 600 °C for 15 min in air is required, as described in our previous study.[17] The field-effect mobility of transistors based on wet-chemically synthesized and post-growth-annealed ZnO nanowires in a global back-gate geometry is usually around 50 cm^2/Vs.

Figure 1 shows the fabrication process for the top-gate ZnO nanowire transistors. The ZnO nanowires are randomly dispersed on the device substrate (heavily doped silicon with 100 nm thick thermally grown SiO_2 or glass) and located by microscopy with respect to predefined unique alignment markers. Next, the source and drain contacts are patterned using electron-beam lithography (EBL), vacuum evaporation of 80 nm thick aluminum, and lift-off (Figure 1a). Immediately prior to the evaporation of the aluminum source and drain contacts, the contact regions of the nanowires

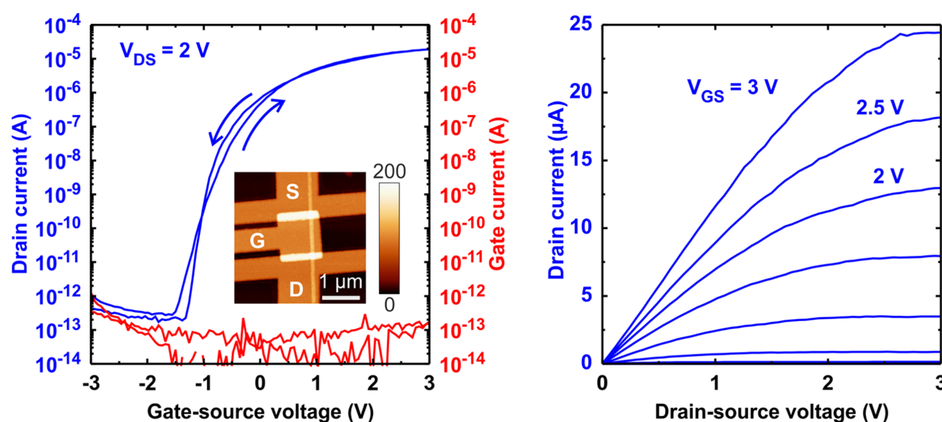

Figure 2. Transfer and output characteristics of a ZnO nanowire transistor with an aluminum top-gate electrode. The inset shows an AFM image (*z*-scale: 0−200 nm) of the transistor, based on a nanowire with a thickness of 35 nm and having a channel length of 1 μm. The transistor has a transconductance of 7 μS, an on/off ratio 10^7, and a subthreshold slope of 150 mV/dec. The gate current is below 1 pA for -3 V < V_{GS} < 3 V.

are briefly exposed to an argon plasma (30 sccm Ar, 10 mTorr, 100 W, 15 s). This argon-plasma treatment cleans the surface of the nanowires and is known to increase the surface conductivity of the ZnO nanowires due to preferential sputtering of oxygen from the ZnO lattice.[19,20] During this argon-plasma treatment, the channel region of the nanowires is protected by electron-beam resist (poly(methyl methacrylate), PMMA). In the next step, the sample is again spin-coated with PMMA, and the regions for the gate electrodes are defined by EBL. After the resist is developed, the substrate is exposed to a soft oxygen plasma (30 sccm O_2, 10 mTorr, 50 W, 20 s). The purpose of the oxygen-plasma treatment is to increase the density of hydroxyl groups on the surface of the ZnO nanowire channel and on the surface of the aluminum source and drain contacts in the area of the gate electrode (Figure 1b). Immediately after the oxygen-plasma treatment, the sample is immersed into a solution of octadecylphosphonic acid molecules in 2-propanol, which leads to the formation of a self-assembled monolayer on the ZnO nanowire and on the aluminum contacts (Figure 1c). After 1 h, the substrate is removed from the solution, rinsed with 2-propanol, and baked on a hot plate at 100 °C for 10 min to evaporate excess solvent and improve the quality of the SAM. Finally, 80 nm thick aluminum is deposited by thermal evaporation to form the metal gate electrode, followed by the lift-off of excess metal (Figure 1d).

Figure 2 shows the transfer and output characteristics of a ZnO nanowire transistor with an aluminum top-gate electrode and a channel length of 1 μm. The thickness of the nanowire measured by atomic force microscopy (AFM) is 35 nm (see inset in Figure 2). The transistor has an on/off current ratio of 10^7, a subthreshold slope of 150 mV/dec, and a peak transconductance of 7 μS. The gate current of the transistor is no greater than ~0.1 pA over the entire gate-source voltage range.

In our previous study, we investigated the insulating properties of SAMs of alkylphosphonic acid molecules in ZnO nanowire transistors with top-gate electrodes made of gold instead of aluminum.[17] This study showed that the SAM gate dielectric effectively reduces the gate current of gold top-gate ZnO nanowire transistors by 3 orders of magnitude compared to gold top-gate ZnO nanowire MESFETs where the SAM gate dielectric was omitted. However, the gate current of the gold top-gate transistors with SAM gate dielectric still increased considerably for positive gate-source voltages exceeding 0.5 V, which means that these FETs cannot be integrated with organic LEDs for displays since organic LEDs typically require voltages of about 3 V.[21] The observed increase in gate current for positive voltages was attributed to the diminishing height of the Schottky barrier that forms between the gold gate electrode and the ZnO nanowire. Based on these observations for ZnO nanowire transistors with gold top-gate electrodes, an even larger gate current for positive voltages would be expected when the gold is substituted by aluminum because the work function difference between aluminum and ZnO ($\Phi_{ZnO\text{-}Al}$ < 0.1 eV) is even smaller compared to that between gold and ZnO ($\Phi_{ZnO\text{-}Au}$ ~ 0.65 eV).[22,23] However, as can be seen from Figure 2, ZnO nanowire transistors that employ an aluminum top-gate electrode withstand much higher voltages up to V_{GS} = 3 V without showing a significant increase of the gate current.

In order to investigate the composition of the gate dielectric of aluminum top-gate ZnO nanowire transistors, the transistor cross section has been investigated by transmission electron microscopy (TEM). With the help of a focused ion beam, nominally 50 nm thick slices of the transistor cross section have been cut out and transferred to the TEM. Figure 3a shows the TEM image of the nanowire cross section cut out from the channel region of the transistor. In this region, the nanowire was covered with an octadecylphosphonic acid SAM prior to the deposition of the aluminum gate electrode. For comparison, Figure 3b shows the cross

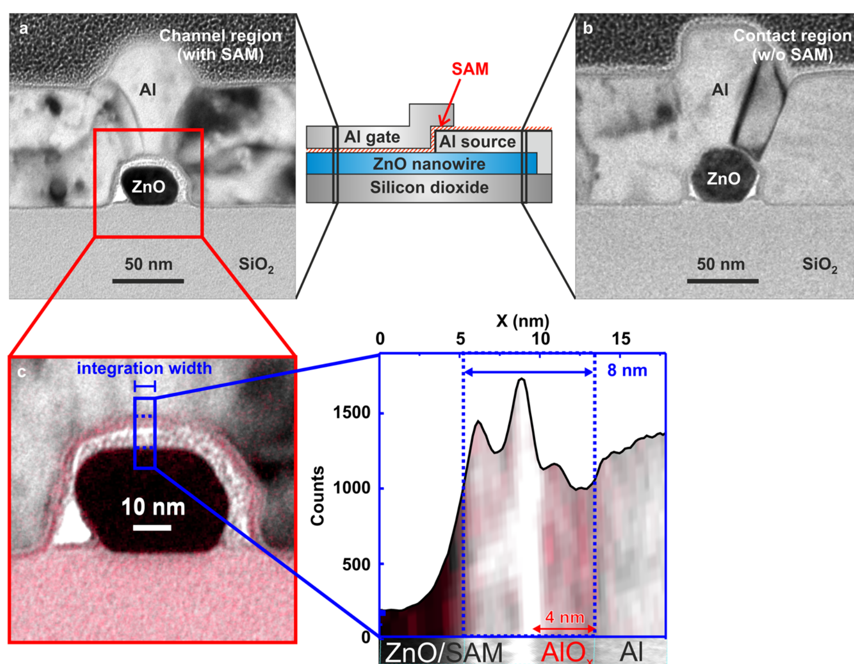

Figure 3. Transmission electron microscopy analysis of transistor cross sections. TEM cross-sectional image of (a) the channel region and (b) the contact region of a ZnO nanowire transistor with an aluminum top-gate electrode. In the channel region, the ZnO nanowire has been covered with a SAM prior to the aluminum evaporation. A bright shell is recognized around the circumference of the ZnO nanowire, separating it from the aluminum gate electrode. Further, a dark region is found at the bottom interface of the aluminum gate electrode near the nanowire. In contrast, the aluminum is in intimate contact with the ZnO nanowire in the contact region. (c) Superposition of the bright-field TEM image of the channel cross section and the oxygen elemental map (colored in red) acquired by energy-filtered transmission electron microscopy. The dark region at the bottom interface of the aluminum gate electrode is identified as aluminum oxide (AlO_x). To quantify the thickness of the bright shell and the aluminum oxide layer, the profile of the interface between the top facet of the SAM-covered ZnO nanowire and the aluminum gate electrode is investigated. The profile is obtained by integration of the bright-field image parallel to the top facet of the ZnO nanowire over the indicated integration width (5 nm). The thickness of the aluminum oxide layer and of the bright shell is estimated to 4 nm in this region. Since the thickness of the SAM is expected to be no more than 2.1 nm, the bright shell is thicker than expected, indicating a poor wetting of the aluminum on the SAM-covered ZnO nanowire.

section of another ZnO nanowire cut out from the source/drain contact region of a transistor. In this region, the ZnO nanowire has been exposed to a short argon-plasma treatment prior to the evaporation of the aluminum contact (no SAM). The cross sections of the channel and the contact regions show significant structural differences. In the contact region, the aluminum is in intimate contact with the ZnO nanowire, which allows excellent charge-carrier injection. In contrast, in the channel region, the aluminum gate electrode appears to be separated from the SAM-covered nanowire. A bright shell is recognized around the ZnO nanowire, and a darker region is found at the bottom interface of the aluminum gate electrode near the nanowire. Figure 3c shows a superposition of the bright-field TEM image with the elemental map of oxygen obtained from the energy-filtered transmission electron microscopy (EFTEM) image. For clarity, the elemental map of oxygen has been colored in red. As can be seen, a pronounced oxygen signal is found in the dark regions at the bottom interface of the aluminum gate electrode, which indicates the formation of an aluminum oxide (AlO_x) layer. It is important to note that no attempts were made to induce the formation of this AlO_x layer. For both the deposition of the aluminum contacts and the deposition of the aluminum gate electrode, the evaporation chamber was evacuated to a pressure of $<4 \times 10^{-6}$ mbar (evaporation rate $\sim$10 Å/s). The presence of the spontaneously formed AlO_x layer indicates that atmospheric oxygen can diffuse into the SAM/Al interface. Similar observations have recently been reported for the interface between graphene and vacuum-deposited aluminum.[24]

It is further interesting to note that the distance between the AlO_x layer and the surface of the ZnO nanowire appears to vary around the circumference of the nanowire. The thickness of the bright shell separating the AlO_x layer from the ZnO nanowire varies between 2 and 6 nm around the circumference of the ZnO nanowire. As an example, Figure 3c shows the profile obtained by integrating the bright-field TEM image parallel to the top facet of the ZnO nanowires over the indicated integration width (5 nm). The thickness of the AlO_x layer as well as the thickness of the bright shell are estimated from the TEM profile to be both 4 nm. The interpretation of the bright layer on the basis of the TEM image is difficult. A straightforward assumption is to conclude that the bright shell represents

the SAM. However, the thickness of the SAM should be no more than 2.1 nm (ref 25) and is expected to be constant around the circumference of the nanowire. It is therefore believed that the bright region indicates that the AlO_x layer is not in intimate contact with the SAM-covered ZnO nanowire. The bright shell might correspond to hollow regions that form at the interface as a consequence of a poor surface wetting of the aluminum on the SAM-covered ZnO nanowire. This hypothesis is supported by Supporting Information Figure S1, which shows TEM cross sections of oxygen- and argon-plasma-treated ZnO nanowires, without SAM, covered with aluminum. In both cases, good wetting of the aluminum on the ZnO surface and intimate Al/ZnO contact are observed, without any indication of a bright shell.

Our hypothesis regarding the formation of hollow regions is further supported by a comparison between the TEM cross sections of aluminum deposited onto a SAM-covered ZnO nanowire and aluminum deposited onto a flat SAM-covered aluminum film (see Figure 4b). The thickness of the bright shell is found to vary only when aluminum is deposited onto the SAM-covered ZnO nanowires but not when aluminum is deposited onto a flat SAM-covered surface, which we believe is due to the larger surface of the ZnO nanowire compared to the flat aluminum film. The formation of hollow regions at the interface to the ZnO nanowire may also facilitate the penetration of atmospheric oxygen and may thereby support the spontaneous formation of the AlO_x layer. The TEM cross sections of three additional ZnO nanowire channel regions are shown in Figure S2. All of them show a varying thickness of the bright shell around the circumference of the SAM-covered ZnO nanowire.

The TEM analysis therefore provides an explanation for the strongly reduced gate current of ZnO nanowire transistors with an aluminum top-gate electrode, compared to ZnO nanowire transistors with a gold top-gate electrode. The hybrid gate dielectric consisting of the SAM and the spontaneously formed AlO_x layer provides a much more stable dielectric than the SAM alone.

To analyze the influence of the SAM and the spontaneously formed AlO_x layer on the leakage current density and the capacitance per unit area, large-area leakage current test structures are fabricated with the help of polyimide shadow masks. (The details of the fabrication process can be found in the Supporting Information.) Figure 4a shows a photograph of the test structures and the schematic cross section of the investigated dielectrics (Al/Au, Al/SAM/Au, Al/SAM/Al). For all test structures, the aluminum bottom electrodes are exposed to a soft oxygen-plasma treatment (30 sccm, 10 mTorr, 50 W, 20 s) before the deposition of the top electrode (Al or Au) or before the immersion into the SAM solution (Al/SAM/Au, Al/SAM/Al).

It is important to note that the test structures (Al/SAM/Al) resemble the gate dielectric stack only in the overlap region of the source/drain contacts and the gate electrode of the nanowire FETs. In the channel region of the nanowire FETs, the gate dielectric stack is different due to the poor wetting of the aluminum on the SAM-covered ZnO nanowire. The poor wetting is not observed in the Al/SAM/Al test structure, as can be seen from the TEM cross section in Figure 4b. Nevertheless, the experiment shows the important influence of the spontaneously grown aluminum oxide on the insulating properties of the gate dielectric.

As can be seen from Figure 4c, the spontaneously formed AlO_x layer has a significant effect on the leakage current density through the test structure. While the addition of the SAM reduces the leakage current density by around 1 order of magnitude (compare green and red curves), the current density is reduced by 2 to 3 orders of magnitude when the gold top electrode is replaced by aluminum (compare red and blue curves). This is especially pronounced for negative voltages where the reduction is even larger than 3 orders of magnitude. (Please note that the leakage current for the junctions with gold top electrode (red curves) is larger compared to the value reported in ref 25. However, this can be attributed to the milder oxygen plasma conditions utilized in the current study.) Simultaneously, the capacitance per unit area (Figure 4d) decreases from 1900 nF/cm^2 (Al/Au) to 680 nF/cm^2 (Al/SAM/Au) to 560 nF/cm^2 (Al/SAM/Al).

Based on the values obtained for the capacitance per unit area of the different dielectrics, the capacitance per unit area of the SAM in combination with the spontaneously oxidized aluminum in the channel region of the nanowire FET can be estimated to be ~790 nF/cm^2, although this value only gives an upper limit for the true capacitance since the hollow regions identified in the channel region may reduce the actual capacitance in the channel region. Based on this estimation of the gate dielectric capacitance per unit area, the field-effect mobility of the ZnO nanowire FET shown in Figure 2 can be calculated using the following equation:

$$\mu_{sat} = \frac{2L}{\pi r C}\left(\frac{d\sqrt{I_D}}{dV_{GS}}\right)^2$$

where it has been assumed that the channel width of the nanowire FET is one-half of the nanowire circumference. The field-effect mobility of the ZnO nanowire shown in Figure 2 is calculated to be 50 cm^2/Vs, which is almost identical to the mobilities which we measured for ZnO nanowire FETs realized in the global back-gate configuration on Si/SiO_2 substrates based on the same nanowire material.

Please note again that the spontaneous formation of the AlO_x layer occurs only in the channel region of the transistors (oxygen-plasma treatment and hydrophobic SAM) but not in the contact regions (argon-plasma treatment, no SAM), ensuring efficient charge injection at the contacts.

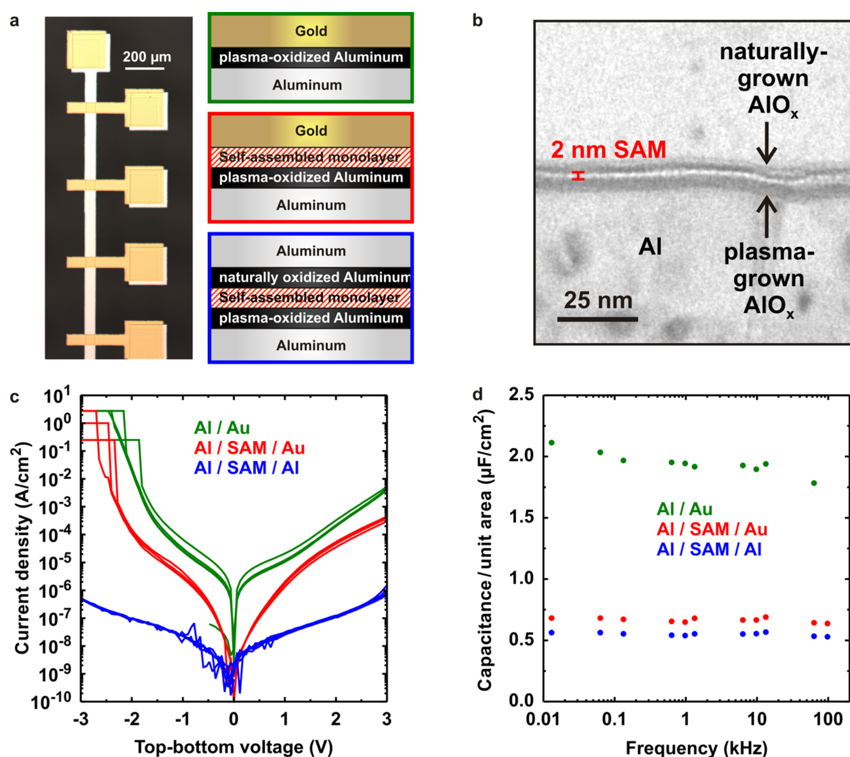

Figure 4. Leakage current through dielectric test structures. (a) Photograph of leakage current test structures with an aluminum bottom electrode and a gold top electrode. Schematic cross sections of the investigated dielectrics with different composition: Al/Au; Al/SAM/Au; Al/SAM/Al. (b) TEM cross-sectional image of an Al/SAM/Al leakage current test structure. The thickness of the bright shell is only 2 nm and hence coincides with the estimated thickness of the SAM. Further, the thickness of the SAM is constant along the interface. This observation supports the assumption of a poor surface wetting of the aluminum on the SAM-covered ZnO nanowire. (c) Leakage current density as a function of the voltage applied between top and bottom electrode across the different dielectric layers. A dramatic reduction of the leakage current density of around 3 orders of magnitude is observed when the gold top electrode is replaced by aluminum (compare red and blue curves). This is attributed to the spontaneous formation of the additional AlO_x layer at the interface between aluminum and SAM. (d) Capacitance per unit area of the different dielectrics obtained from leakage current test structures with an overlap area of 3600 μm^2. To obtain the capacitance, a sine-wave signal with an amplitude of 0.1 V was applied to the top electrode. A lock-in amplifier was used to record the alternating current at the bottom electrode.

Given the small leakage current densities through the hybrid dielectric, we believe that this gate dielectric may also be interesting for the fabrication of thin-film transistors based on ZnO,[26−29] where the overlap areas between gate electrode and semiconductor are much larger compared to transistors based on ZnO nanowires.

The small gate current and the potential to tolerate voltages above 3 V make it possible to operate ZnO nanowire transistors with aluminum top-gate electrodes with much larger overdrive voltages compared to the previously investigated gold top-gate ZnO nanowire transistors and to integrate them with organic LEDs. Figure 5a,b shows the transfer and output characteristics of a transistor with a channel length of 1 μm. In order to obtain a large drain current and a large transconductance, the source and drain contacts have been designed in a comb-like pattern, with a total of nine contact fingers (see inset in Figure 5a for a microscopy image and Figure 5c for a schematic). The transistor has an on/off current ratio of 10^8, a subthreshold slope of 100 mV/dec, and a peak transconductance of 50 μS. From the output characteristics, a slightly nonlinear increase of the drain current with increasing V_{DS} can be observed for small V_{DS} at large V_{GS}. This can be attributed to the small width of the contact fingers of only 500 nm, which might introduce a non-negligible contact resistance at large overdrive voltages.[30] The maximum drain current at V_{GS} = 3 V and V_{DS} = 3 V is 125 μA. The large drain current can be used to drive an organic LED to a sufficiently high brightness for practical display applications. The transistor is connected to an organic LED, as depicted in Figure 5c. The organic LED is a green phosphorescent device manufactured by Novaled (Dresden, Germany). It has a luminous efficiency of 31 cd/A and an active area of 6.7 mm^2. Figure 5d shows four photographs of the green organic LED driven by the ZnO nanowire transistor at a drain potential of V_2 = 5.5 V and gate potentials of V_1 = 0, 3.5, 4.5, and 5.5 V. As expected, the FET is capable of modulating the brightness of the LED with increasing gate potential. For a gate potential of 0 V, the current driven through the LED is smaller than 1 pA. This is a particularly critical requirement for FETs intended for active-matrix display backplanes since these FETs must

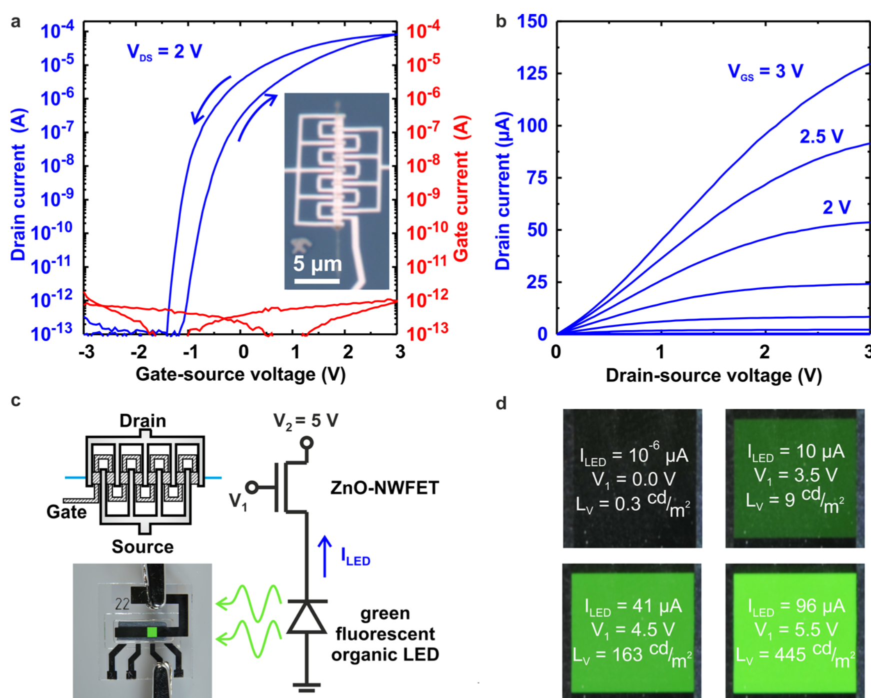

Figure 5. Organic LED driven by a ZnO nanowire transistor. (a) Transfer and (b) output characteristics of a ZnO nanowire transistor with aluminum top-gate electrode with source and drain contacts realized in a comb-like pattern. For a drain-source voltage of 2 V, the transistor has a peak transconductance of 50 μS, an on/off ratio of 10^8, and a subthreshold slope of 100 mV/dec The inset shows a photograph of the transistor. (c) Schematic of the comb-like pattern, photograph of the green organic LED, and circuit schematic. (d) Photographs of the light-emitting area (6.7 mm^2) of the green organic LED for different gate potentials V_1. For V_1 = 5.5 V, a current of 96 μA flows through the organic LED which is sufficient to drive the organic LED to a brightness of 445 cd/m^2.

provide not only large on-state currents but also extremely small off-state currents, which further underlines the importance of a small doping concentration. For a gate potential of 5.5 V, a current of 96 μA is driven through the LED, producing a brightness of 445 cd/m^2. This demonstrates the general feasibility of the presented approach based on a hybrid top-gate dielectric for the application in AMOLED displays. However, in order to design the comb-like pattern for the source and drain contacts of the ZnO nanowire FET demonstrated in Figure 5a, the use of electron-beam lithography is essential. Certainly, electron-beam lithography is not a suitable patterning technique for flat-panel displays, but taking into account that a typical display subpixel area is only around 10^{-4} cm^2, and hence around 2 orders of magnitude smaller compared to the organic LED used in this demonstration, the transistor geometry in an actual pixel could be much more relaxed. We therefore expect that the patterning with electron-beam lithography could eventually be readily replaced by photolithography (as shown, for example, in ref 9) while maintaining the performance necessary to drive organic LEDs to sufficient brightness.

To estimate the dynamic performance of the aluminum top-gate ZnO nanowire transistors, inverters based on a ZnO nanowire transistor and a load resistor based on a patterned thin film of carbon are fabricated on insulating glass substrates. The fabrication of the thin-film carbon resistors is detailed in ref 31. Again, a comb-like pattern has been chosen for the source and drain contacts of the ZnO nanowire FETs in order obtain a large transconductance. An AFM image of the transistor based on a 60 nm thick ZnO nanowire is depicted in Figure 6a. The transistor has a channel length of 0.5 μm and a total of eight contact fingers. Figure 6b shows the circuit schematic and a microscopy image of the inverter with a thin-film carbon load resistor that has a total width of 35 μm and a length of 1 μm.

The resistance of the thin-film carbon resistor is 50 kΩ. The load curve of the resistor together with the output curves of the transistor is shown in Figure S4a. The dynamic response of the inverter is characterized using an active probe needle (GGB Industries Picoprobe 19C) with a total capacitance of $C_{pico} \sim 150$ fF. Figure 6c shows the dynamic response of the inverter to a square-wave input signal with a frequency of 1 MHz at supply voltage of 3 V. The extracted time constants are obtained from exponential fits to the input and output signals (see Supporting Information). Due to the large transconductance of the transistor (50 μS), charging the output node from high potential to low potential happens almost instantaneously, as confirmed by the extracted time constants: $\tau_{rise}^{in} = 8$ ns and $\tau_{fall}^{out} = 7$ ns. In contrast, charging the output node from low to high potential through the 50 kΩ load resistor occurs with a delay; that is, the time constant of the output signal $\tau_{rise}^{out} = 19$ ns is larger than the time

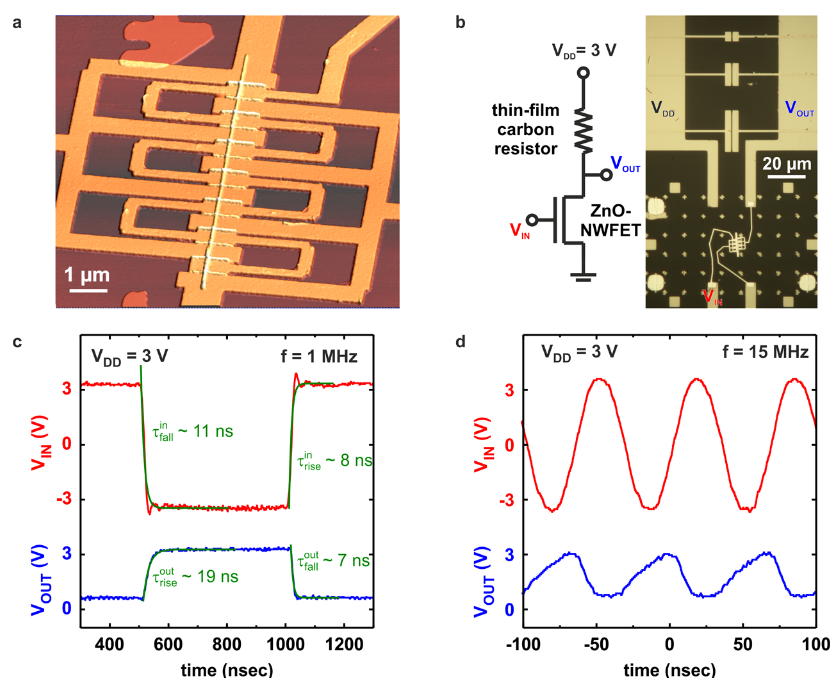

Figure 6. Inverter with thin-film carbon resistor and dynamic characterization. (a) Tilted atomic force microscopy image of a ZnO nanowire transistor with a comb-like pattern for the source and drain contacts. The transistor has a channel length of 0.5 μm, and the thickness of the ZnO nanowire is 60 nm. (b) Circuit schematic and photograph of an inverter based on a ZnO nanowire transistor and a thin-film carbon load resistor on a glass substrate. AuPd electrodes were patterned on the thin-film carbon by electron-beam lithography. The resistor has a width of 35 μm and a length of 1 μm, providing a resistance of 50 kΩ. (c) Exponential fits (green) to the square-wave input signal (red) and to the dynamic response of the inverter (blue) at a frequency of 1 MHz. As can be seen from the extracted time constants, charging the output node from low potential to high potential through the 50 kΩ load resistor introduces a delay, while charging the output node from high to low potential through the transistor happens instantaneously. (d) Dynamic response of the inverter with a frequency of 15 MHz to a sine-wave input signal at a supply voltage of 3 V.

constant of the input signal τ_{fall}^{in} = 11 ns. Figure 6d shows the dynamic response of the inverter to a sine-wave input signal with a frequency of 15 MHz at a supply voltage of 3 V. For a transconductance of g_m = 50 μS, this frequency is close to the calculated cutoff frequency

$$f_T = g_m/(2\pi C_{pico})$$

of 50 MHz. (Figure S4b–d illustrates the dynamic response for frequencies up to 30 MHz.) It should be noted that the switching frequency is limited by the capacitance of the active probe needle (150 fF). Based on the estimated gate capacitance per unit area, the total device capacitance is expected to be around 10 fF, so a cutoff frequency near 750 MHz is projected for this transistor.

CONCLUSION

In conclusion, we have demonstrated high-performance top-gate field-effect transistors based on ZnO nanowires and a hybrid organic/inorganic gate dielectric consisting of a self-assembled monolayer and aluminum oxide. The hybrid dielectric forms naturally when aluminum is thermally evaporated onto a SAM-covered ZnO nanowire since atmospheric oxygen can penetrate the interface between the SAM and aluminum. Cross-sectional TEM images indicate that the aluminum gate electrode is only poorly wetting the SAM-covered ZnO nanowire which is beneficial for the penetration of atmospheric oxygen. The transistors have an on/off current ratio of 10^8, a subthreshold swing of 100 mV/dec, and a transconductance of 50 μS. The hybrid gate dielectric allows operating the transistors at voltages up to 3 V, making them fully compatible with organic LEDs. Inverters based on ZnO nanowire transistors with hybrid gate dielectric operate at frequencies up to 30 MHz. As the maximum temperature during the fabrication of the hybrid gate dielectric is 100 °C, the developed process is compatible with flexible polymeric substrates.

METHODS

The hydrothermally synthesized ZnO nanowires were randomly dispersed onto a glass substrate or onto a heavily doped silicon substrate covered with 100 nm thick thermally grown SiO_2 and located by microscopy with respect to a marker array. The source and drain contacts were patterned by electron-beam lithography, vacuum evaporation of 80 nm thick aluminum, and lift-off. Immediately prior to the evaporation of the aluminum contacts, the contact regions of the nanowires were briefly exposed to an argon plasma (30 sccm Ar, 10 mTorr, 100 W, 15 s) to clean the nanowire surface and increase the ZnO

surface conductivity by preferential sputtering of oxygen. Next, the regions for the gate electrodes were defined by EBL, followed by exposing the substrate to a soft oxygen plasma (30 sccm O_2, 10 mTorr, 50 W, 20 s) to increase the density of hydroxyl groups on the surface of the ZnO nanowire channel and on the surface of the aluminum source and drain contacts in the area of the gate electrode. The sample was then immersed into a solution of octadecylphosphonic acid in 2-propanol to form a self-assembled monolayer on the ZnO nanowire and on the aluminum contacts. After 1 h, the substrate was removed from the solution, rinsed with 2-propanol, and baked on a hot plate at 100 °C for 10 min to evaporate excess solvent and improve the quality of the monolayer. Finally, 80 nm thick aluminum was deposited by thermal evaporation to form the metal gate electrode, followed by the lift-off of excess metal.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: TEM cross sections of the ZnO/Al, ZnO/SAM/Al, and Al/SAM/Al interfaces and additional information on the fabrication of the leakage current test structures, on the breakdown voltage tests, and on the dynamic performance of ZnO-nanowire-based inverters. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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