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A digital library for a flexible low-voltage organic thin-film transistor technology

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ABSTRACT

This paper presents the design, fabrication and characterization of digital logic gates, flip-flops and shift registers based on low-voltage organic thin-film transistors (TFTs) on flexible plastic substrates. The organic transistors are based on the p-channel organic semiconductor dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) and have channel lengths as short as 5 μm and gate-to-contact overlaps of 20 μm. The organic TFT is modeled which allows us to simulate different logic gate architectures prior to the fabrication process. In this study, the zero-VGS, biased-load and pseudo-CMOS logic families are investigated, where their static and dynamic operations are modeled and measured. The inverter and NAND gates use channel length of 5 μm and operate with a supply voltage of 3 V. Static and dynamic master-slave flip-flops based on biased-load and pseudo-CMOS logic are designed, fabricated and characterized. A new design for biased-load dynamic flip-flops is proposed, where transmission gate switches are implemented using only p-channel transistors. 1-stage shift registers based on the new design and fabricated using TFTs with a channel length of 20 μm operate with a maximum frequency of about 3 kHz.

1. Introduction

Organic electronics paves the way for novel applications utilizing its compatibility with large-area and flexible substrates such as plastics, paper and fabric. Organic thin-film transistors (TFTs) have also been integrated with other technologies, such as ultra-thin silicon chips and printed sensors, in a hybrid system-in-foil (HySiF) [1,2]. In this system, the complementary advantages of the large-area and room-temperature-fabricated organic and printed electronics are combined with the high-performance silicon technology on a single flexible foil as a demonstration of a smart electronic skin for robotic applications.

Previous work has demonstrated the realization of organic-TFT-based complex circuits, such as shift registers (operating at frequencies as high as 10 kHz at a supply voltage of 20 V [3]), analog-to-digital converters (signal-to-noise ratio of 26.5 dB [4]), digital-to-analog converters (resolution 6 bits and update rate 100 kS/s [5]), voltage generator (10 μA driving current), binary counter (14 bit) [6] and digital processors (40 instructions per second [?]). However, these circuits usually require high voltages to operate, which is a serious issue in mobile or wearable systems powered by small batteries. In this work, a digital library comprising basic combinational and sequential building blocks is developed, and circuits based on low-voltage organic TFTs are fabricated and characterized. A 1-stage shift register based on a new biased-load dynamic flip-flop design and fabricated using organic TFTs with a channel length of 20 μm operate with a maximum clock frequency of 3 kHz at a supply voltage of 2.2 V.

2. Fabrication

The organic TFTs and circuits are fabricated using high-resolution silicon stencil masks which provide a minimum resolution of a few microns [5,7]. The substrate is a stack of

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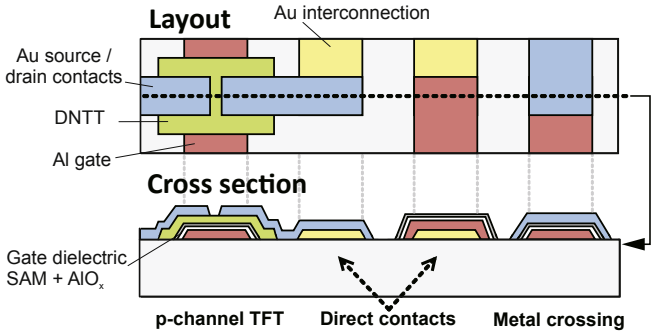

Fig. 1. Schematic showing the top and cross-sectional views of the inverted staggered (bottom-gate, top-contact) organic TFTs and the circuit interconnects. The gate electrode is aluminum (Al) and the source/drain contacts are gold (Au). The gate dielectric is a combination of AlO_x and an alkylphosphonic acid self-assembled monolayer (SAM). The organic semiconductor is dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT).

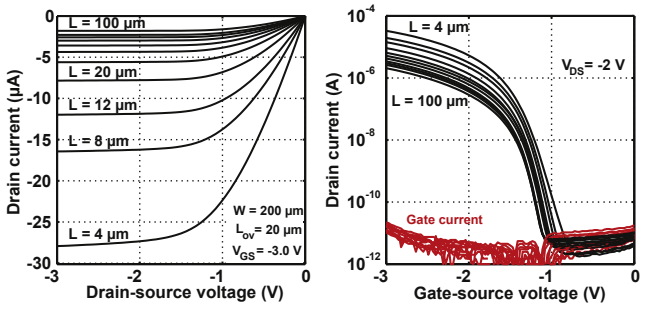

Fig. 2. Measured static output and transfer characteristics of organic TFTs with channel lengths (L) ranging from 100 μm to 4 μm fabricated on a flexible PI/BCB substrate. All TFTs have a channel width (W) of 200 μm and gate-contact-overlaps (L_{ov}) of 20 μm.

Table 1
Extracted transistor parameters.

Parameter	Value
Threshold voltage V_{th}	−1 V
Mobility μ_0	1.3 cm^2/Vs
Contact resistance R_c	0.2 kΩ cm
Sheet resistance R_{sh}	666 kΩ/□
On/off current ratio	10^6

polyimide (PI) and benzocyclobutene (BCB) with a total thickness of about 40–50 μm previously developed for a hybrid system-in-foil [1].

Fig. 1 shows the structure of the inverted staggered (bottom-gate, top-contact) organic TFTs. First, 30-nm-thick layers of gold and aluminum are deposited by thermal evaporation in vacuum through the first and second stencil masks to define the interconnects and the gate electrodes. The gate dielectric is a combination of a 3.6-nm-thick oxygen-plasma-grown AlO_x layer and a 1.7-nm-thick solution-processed tetradecylphosphonic acid self-assembled monolayer (SAM). The capacitance of the hybrid gate dielectric (C_I) is about 700 $nFcm^{-2}$ [8] which allows the organic TFTs to operate at low supply voltages. A 25-nm-thick layer of the small-molecule organic semiconductor dinaphtho[2,3-b:2′,3′-f] thieno [3,2-b]thiophene (DNTT) [9] is then deposited by sublimation in vacuum through the third mask. Finally, 25-nm-thick gold is deposited for the source/drain contacts through the fourth mask.

3. Organic TFT characterization and modeling

Fig. 2 shows the measured static output and transfer characteristics of organic TFTs with channel lengths ranging from 100 μm to 4 μm fabricated on the flexible PI/BCB substrate. The transmission line method (TLM) is used to extract the threshold voltage V_{th}, the intrinsic channel mobility μ_0 and the contact and sheet resistances R_c and R_{sh} [7,10]; the extracted values are summarized in Table 1.

In order to properly design an organic integrated circuit and simulate its behavior, a SPICE model is needed. Various organic TFT models have been proposed [7,11]. However, a model which is mature, fast, simple and suitable for circuit simulation with large number of TFTs was required in this work. The industry-standard Berkeley Short-channel IGFET Model (BSIM3) is chosen here to model the organic TFT behavior. Note that BSIM is used to model 4-terminal silicon-based transistors. However it is used herein to model 3-terminal organic TFTs, which does not result in accurate or physical modeling rather than behavior modeling that is enough for organic TFT digital design. The measured static output and transfer characteristics of the TFTs are used to extract the device parameters. Fig. 3 shows the measurement data of our organic TFTs plotted against the simulated data using the BSIM3 model, showing good agreement between the measurements and the simple simulation model.

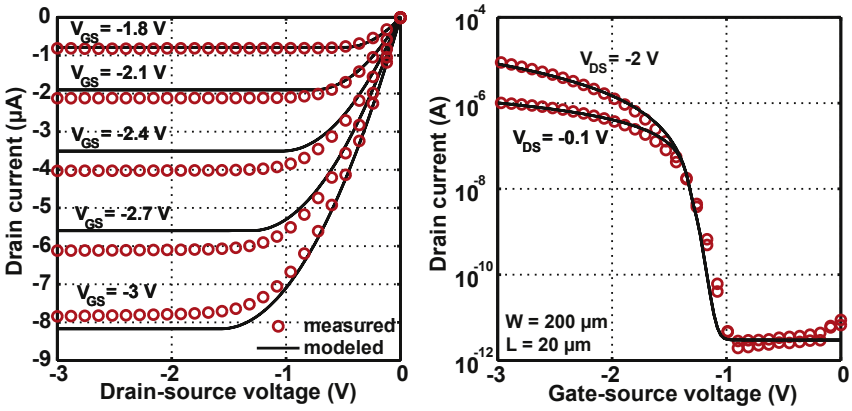

Fig. 3. Comparison of measured and modeled static output and transfer characteristics of an organic TFT with a channel length of 20 μm.

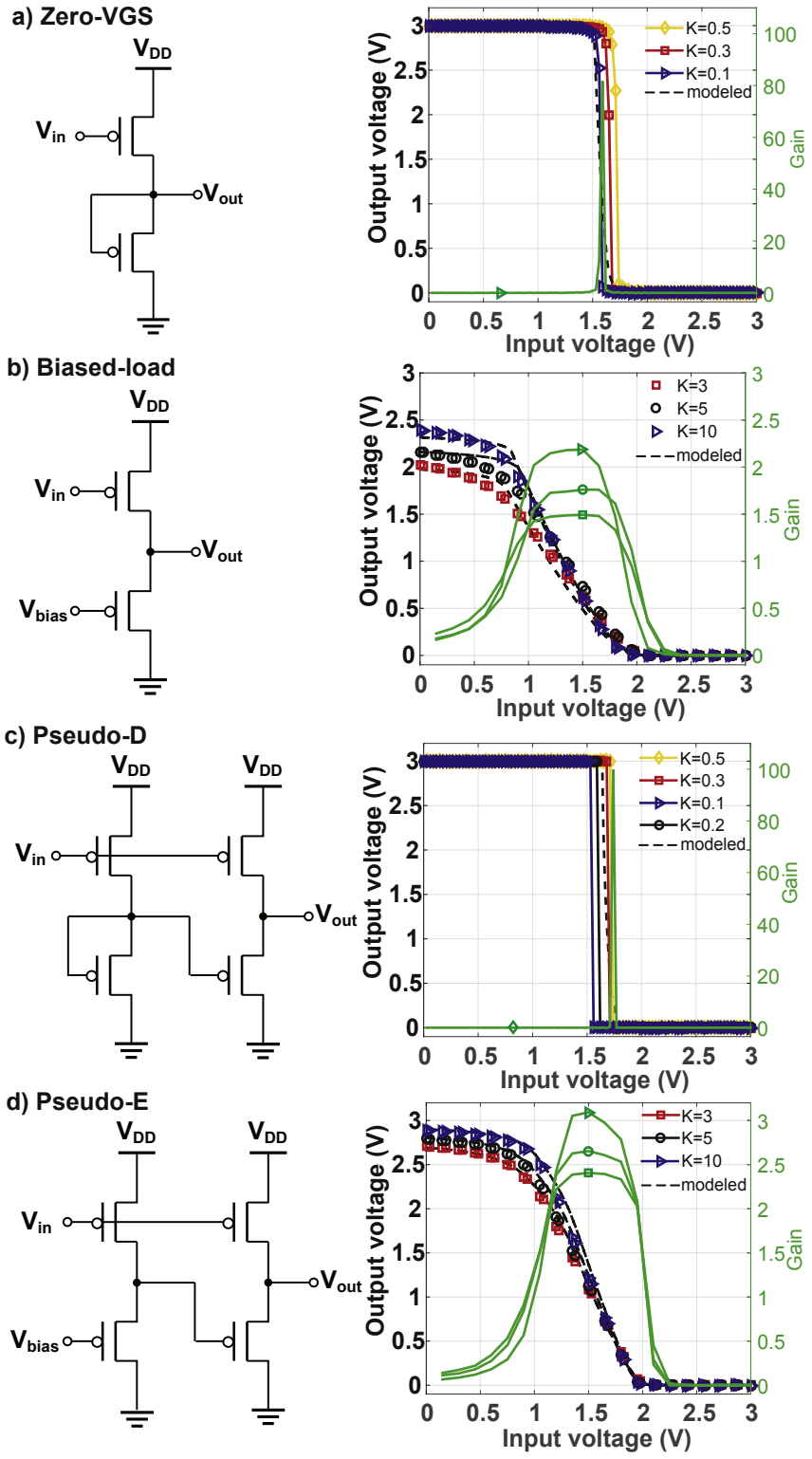

Fig. 4. Schematics and static modeled and measured voltage transfer characteristics of inverters based on the (a) zero-VGS, (b) biased-load, (c) pseudo-D and (d) pseudo-E design. All TFTs have a channel length of 5 μm and gate-to-contact overlaps of 20 μm. In zero-VGS and pseudo-D logic, the load transistors have a channel width of 100 μm and the driver transistors have channel widths of 50, 33, 20 or 10 μm (channel-width ratio K = 0.5, 0.33, 0.2 and 0.1). In the biased-load and pseudo-E logic, the bias voltage is −1.5 V and the driver transistors have a channel width of 100 μm and the load transistors have channel widths of 50, 33, 20 or 10 μm (channel-width ratio K = 2, 3, 5 and 10).

This model is then used to simulate the behavior of the organic logic gates and flip-flops.

4. Organic logic gates

The complementary logic design, which utilizes both n-channel

and p-channel transistors, is generally preferable, due to the low power consumption and rail-to-rail output voltage swing [12]. However, the performance and stability of organic n-channel TFTs is still inferior to that of organic p-channel TFTs, so we have used only p-channel TFTs in this study.

The characteristics of four different logic designs have been investigated, namely zero-VGS, biased-load, pseudo-D and pseudo-E. Fig. 4 (a)-(d) shows the schematics and the measured static voltage transfer characteristics of inverters based on each of these four designs. While the zero-VGS and the biased-load designs require two transistors per inverter, four transistors per inverter are required in the pseudo-CMOS designs.

In the zero-VGS design, the gate and the source of the load transistor are connected, hence the term zero-VGS [13]. Depending on the threshold voltage, the channel width of the load transistor should be larger than that of the driver transistor in order to enhance its pull-down behavior. For this purpose, we define the parameter K as the ratio between the channel width of the driver transistor and that of the load transistor (normally $K < 1$). Zero-VGS inverters generally provide large small-signal gain, as demonstrated in Fig. 4a. However, when the threshold voltage of the transistors is negative, which is the case in our technology, the load transistor is always switched off, which has the benefit of rail-to-rail output swing, but the drawback of poor dynamic characteristics, especially when the output voltage is discharging through the load transistor.

In the biased-load design, the load transistor is designed to be always turned on in order to provide rapid discharging of the output node, which is accomplished with the help of the external bias voltage V_{bias}. As a result, when the input voltage is high and the driver transistor is off, the output voltage discharges rapidly through the conducting load transistor. When the input voltage is low and the driver transistor is on, it pulls up the output voltage. However, because the load transistor is conducting, there is a finite voltage drop across the load transistor so that the output voltage will not reach the supply voltage. To increase the output voltage in this situation, the driver transistor is designed to have a larger channel width than the load transistor ($K > 1$) in order to provide a stronger pull. The effect of K on the pull-up behavior can be clearly seen in Fig. 4b: a larger channel width of the driver transistor (i.e., a larger K) produces a larger maximum output voltage and hence a larger output voltage swing. The biased-load design consumes more static power but provides superior dynamic characteristics compared to the zero-VGS inverter. Also, the possibility of tuning the transconductance of the load transistor with the help of the external bias voltage is useful to account for process variations and to realize the optimum compromise between signal delay and power consumption.

In addition to the zero-VGS and biased-load designs, we have also investigated two variants of pseudo-CMOS logic, which provides rail-to-rail output voltage swing at the expense of a larger transistor count [14]. Pseudo-CMOS inverters are comprised of two stages. The first stage of the pseudo-D inverter is a zero-VGS inverter, while the first stage of the pseudo-E inverter is a biased-load inverter. The second stage is identical in both variants. In both variants, the driver transistors of the first and second stages have their gate electrodes connected to the input node of the inverter, while the load transistor of the second stage has its gate electrode connected to the output node of the first stage. When the threshold voltage of the transistors is negative, the pseudo-D design has the same drawback as the zero-VGS design, namely poor dynamic performance. The signal delay of the pseudo-E design is comparable to that of the biased-load design (slightly larger due to the additional delay of the second stage). However, the pseudo-E inverter provides a larger output voltage swing than the biased-load inverter, because when the input voltage is low, the output of the first stage is high while the pull-down transistor of the second stage is off, thereby preventing any direct current flow from the supply-voltage node to the ground node.

Table 2
Extracted static and dynamic parameters of the inverters.

Parameter	Zero-VGS	Biased-load	Pseudo-D	Pseudo-E
NMH (V)	1.3	0.4	1.3	1.1
NML (V)	1.4	0.4	1.5	0.3
Gain	81	2	100	3
Rise time (μs)	43	29	53	61
Fall time (μs)	368	144	345	147

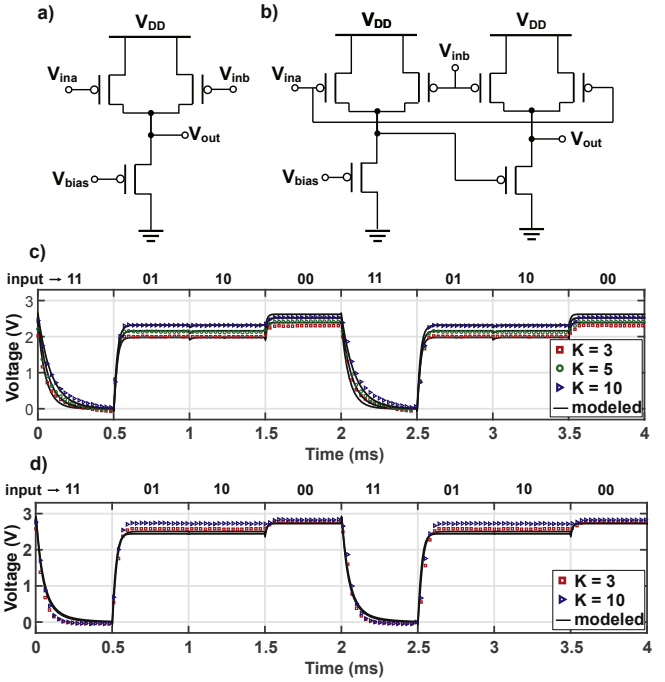

Fig. 5. Schematic and transient modeling and measurement results of 2-input NAND gates based on the (a) and (c) biased-load and (b) and (d) pseudo-E designs. All TFTs have a channel length of 5 μm and gate-to-contact overlaps of 20 μm. The driver TFTs have a channel width of 100 μm, and the load TFTs have channel widths of 33, 20 or 10 μm (channel-width ratio $K = 3$, 5 and 10). The bias voltage is −1.5 V. The binary input values are indicated above the graphs. The minimum load at the output node is the oscilloscope impedance, which is 1 MΩ in parallel with 16 pF.

Table 2 summarizes the measured static and dynamic performance parameters of organic inverters based on each of the four designs. The noise margin high (NMH) and low (NML) are calculated using a graphical approach [15]. Fig. 5 shows the schematics and the transient modeled and measured behavior of 2-input NAND gates based on the biased-load and pseudo-E designs for different channel-width ratios (K) measured at an input-signal frequency of 1 kHz. For the biased-load design it can be seen that the fall time decreases as K increases from 3 to 10, while the rise time is independent of K. This is due to the fact that the output node is pulled up through the driver transistor, which is identical in all three designs, but pulled down through the load transistor, which

has a different channel width in each of the three designs (33, 20 or 10 μm).

5. Flip-flops and shift registers

A complete library of basic combinational and sequential digital blocks must include a flip-flop. In this section, three flip-flops and two shift registers are presented using a channel length of 20 μm. This channel length is chosen to ensure minimum effect of the fabrication process variations and lower static power consumption for the biased-load designs (at the same gate bias for the load transistor, longer channel length results in lower static current and power consumption). Fig. 6 shows the schematic and the transient measurement results of a 1-stage shift register based on a static positive-edge-triggered master-slave flip-flop using the biased-load design. The measurement was performed with a clock frequency of 1 kHz and bias voltage of −1.5 V. The flip-flop consists of two latches, and each latch consists of three biased-load inverters and two pass transistors, so the total transistor count is 16 per flip-flop. The pass transistors are operated with complementary clock signals applied to the gate electrodes in order to switch between the feed-forward and feed-back paths of the latch. The main drawback of this design is that it requires clock signals with both positive and negative voltages in order to switch the pass transistors completely off and completely on, respectively. In technologies in which p-channel and n-channel transistors are available, this situation can be avoided by combining one p-channel and one n-channel transistor into a transmission gate switch that can be operated with a unipolar clock signal [12]. The fact that clock signals with positive and negative voltages are required here means that this circuit may not be immediately compatible with other components in a hybrid system operated with a single unipolar power supply [1].

An alternative to the static logic approach is the dynamic approach which provides the general advantage of a smaller signal delay. However, robustness of dynamic logic is inferior to that of static logic, and problems like charge sharing and charge leakage are critical. In addition, dynamic flip-flops can usually be designed with only one pass transistor and two cascaded inverters in each latch, which would significantly reduce the transistor count compared to the static approach [12]. However, with only p-channel TFTs being available, this would again require clock signals with positive and negative voltages, as explained above. In order to be able to operate the circuit with a unipolar clock signal (i.e., a clock signal that switches between 0 V and the supply voltage), we propose the design shown in Fig. 7. This design is based on the fact that when the clock signal is zero, the p-channel pass transistors are not able to pass a logic low signal, but they are able to pass a logic high signal without problem. Therefore, the proposed design consists of two parallel paths. In the primary path, the signal is passed through the pass transistor directly, whereas in the secondary path, the signal is first inverted, then passed through the pass transistor, and then inverted back to the original signal. This way, the primary path is used to pass the logic high signals (similar to the p-channel transistor in a complementary transmission gate switch) while the secondary path is used to pass the logic low signals (similar to the n-channel transistor in a complementary transmission gate switch).

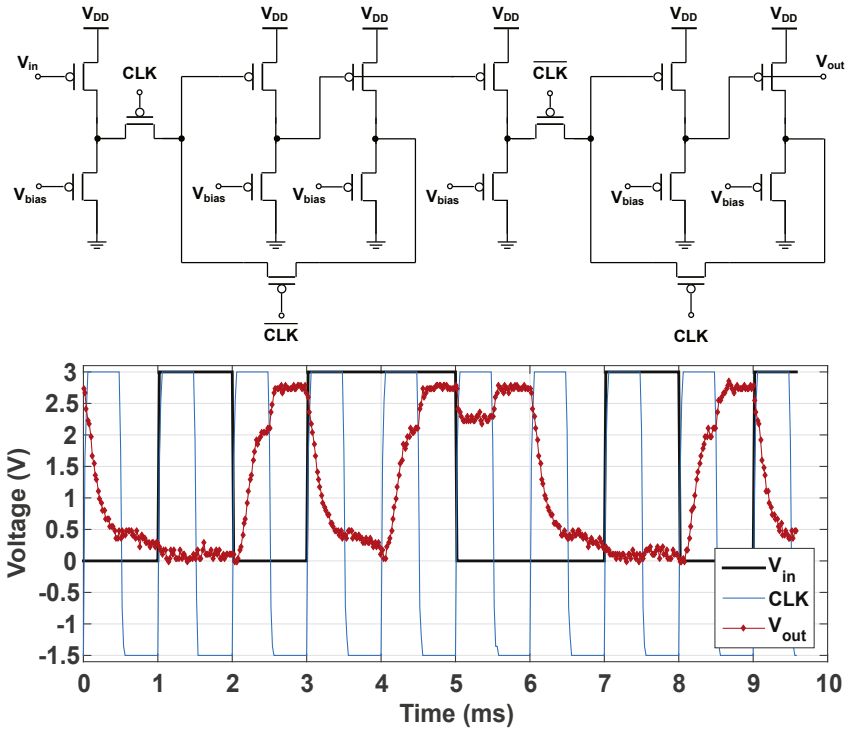

Fig. 6. Schematic and measurement results of a 1-stage shift register based on a static positive-edge-triggered master-slave flip-flop using the biased-load design. All TFTs have a channel length of 20 μm, gate-to-contact overlaps of 20 μm and the channel width ratio (K) is 5. The measurement was performed with a supply voltage of 3 V, a bias voltage of −1.5 V and a clock frequency of 1 kHz.

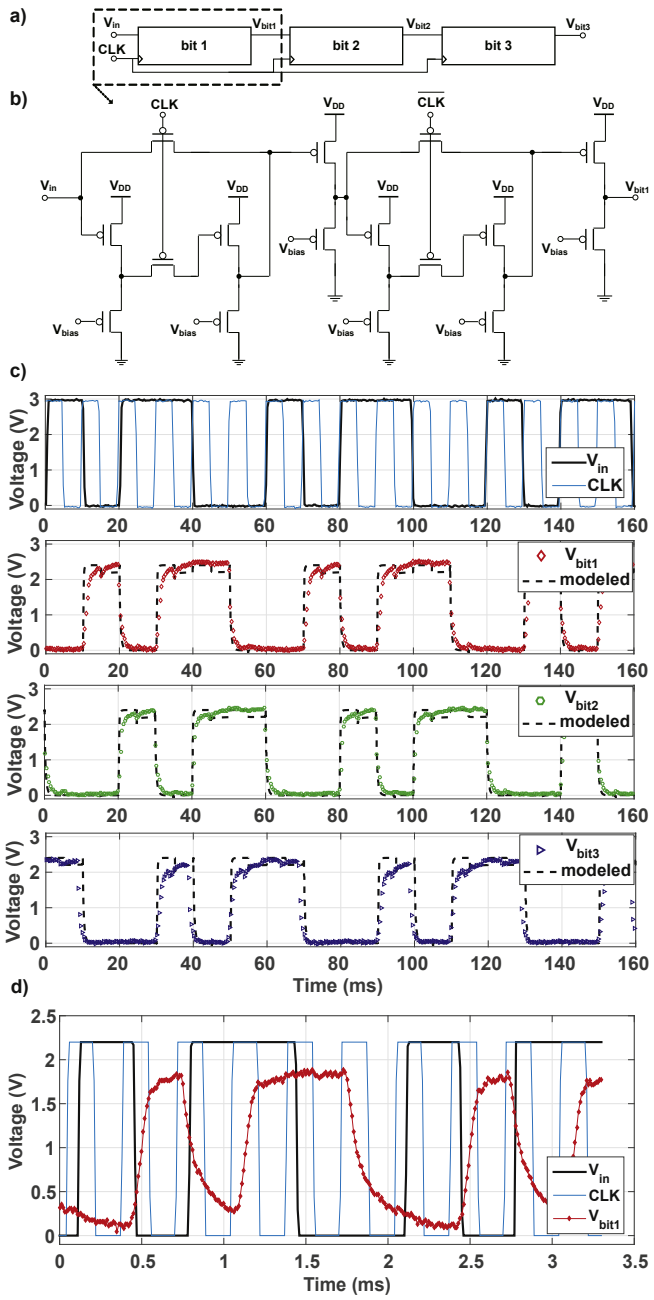

Fig. 7. (a) Conceptual schematic of the 3-stage shift register, where V_{bit1}, V_{bit2}, and V_{bit3} correspond to the output voltage of the first, second and third shifting stages, respectively. (b) Schematic of a 1-stage shift register based on a dynamic positive-edge-triggered master-slave flip-flop using the biased-load design. All TFTs have a channel length of 20 μm, gate-to-contact overlaps of 20 μm and the channel width ratio (K) is 5. (c) Measurement and modeling results of the 3-stage shift register performed with a supply voltage of 3 V, a bias voltage of −1 V and a clock frequency of 100 Hz. (d) Measurement results of the 1-stage shift register performed with a supply voltage of 2.2 V, a bias voltage of −1 V and a clock frequency of 3 kHz.

Thus, the dynamic positive-edge-triggered master-slave flip-flop shown in Fig. 7b consists of six biased-load inverters and four pass transistors, with a total transistor count of 16 per flip-flop, identical to the static approach shown in Fig. 6. The signal delay is slightly larger compared to the dynamic approach with a single signal path, but still significantly shorter compared with the static approach in Fig. 6. The proposed design is very effective in maintaining the logic voltage levels compared to the dynamic approach with a single signal path. Fig. 7c shows the transient measurement and modeling results of the 3-stage dynamic shift register (channel length of 20 μm, a bias voltage of −1 V, frequency of 100 Hz). The transient measurement results of a dynamic positive-edge-triggered master-slave flip-flop based on TFTs with a channel length of 20 μm are also shown in Fig. 7d. This flip-flop operates at a maximum frequency of about 3 kHz and has a power consumption of 233 μW. For this measurement, a bias voltage of −1 V was used; in principle, the flip-flop will also operate with a bias voltage of 0 V, albeit with larger signal delay and smaller noise margins. The intrinsic capacitance of the organic TFT used in this work can be modeled using Meyer's model [16]. This is a similarity between MOSFETs (BSIM model) and our organic TFT. The parasitic capacitance namely the overlap capacitance is calculated according to the corresponding device dimensions and is included in the BSIM model (cgso and cgdo parameters). Note that the transistor dynamic model includes the organic TFT intrinsic and parasitic capacitances. However, it does not include the interconnect parasitic capacitance which will degrade the modeling accuracy, especially at higher frequencies. This is the reason why the modeling results are not shown in Figs. 6 and 7.

Finally, Fig. 8 shows the schematic of a 1-stage shift register, the transient measurement and modeling results of a 2-stage shift register based on a dynamic positive-edge-triggered master-slave flip-flop using the pseudo-E design. The transistor count of the 2-stage shift register is 56 (28 per flip-flop). As explained in the previous section, the pseudo-E design provides a larger output voltage swing than the biased-load design (see Fig. 4), but also has a larger signal delay. The measurement shown in Fig. 8 was performed with a clock frequency of 100 Hz.

Table 3 summarizes the characteristics of recently reported organic-TFT-based shift registers. Fig. 9a shows a photograph of the flexible PI/BCB substrate with the organic circuits as it is being detached from the handling wafer. Fig. 9b show a photograph of a 1-stage dynamic shift register based on the biased-load design.

6. Conclusion

We have developed a digital library for low-voltage organic transistors that includes inverters, NAND gates, flip-flops and shift registers. The devices and circuits were fabricated on flexible plastic substrates using the small-molecule organic semiconductor DNTT, and owing to the use of a thin, high-capacitance gate dielectric, they operate with low voltages of about 3 V. The static and dynamic TFT circuit behavior was simulated using a compact model (BSIM3). The advantages, disadvantages and design trade-offs of circuits utilizing the zero-VGS, biased-load, pseudo-D and pseudo-E designs have been analyzed. 1-stage shift registers based on positive-edge-triggered master-slave flip-flops using the biased-load design operate with maximum clock frequencies of 1 kHz (static design) and 3 kHz (dynamic design). A 3-stage and 2-stage shift registers based on the biased-load and pseudo-E designs operate with a clock frequency of 100 Hz at a supply voltage of 3 V. For further improvements in terms of the maximum operating frequency, the parasitic capacitance effect should be minimized at the various design and testing levels. For TFTs, parasitic capacitances could be reduced by using smaller overlap areas. For circuit fabrication, a thicker dielectric material should be used at interconnect crossings. For circuit design, output buffers and I/O drivers should be used. For circuit layout, critical and fast switching signals should be routed with sufficient lateral and vertical distances. Finally, high-

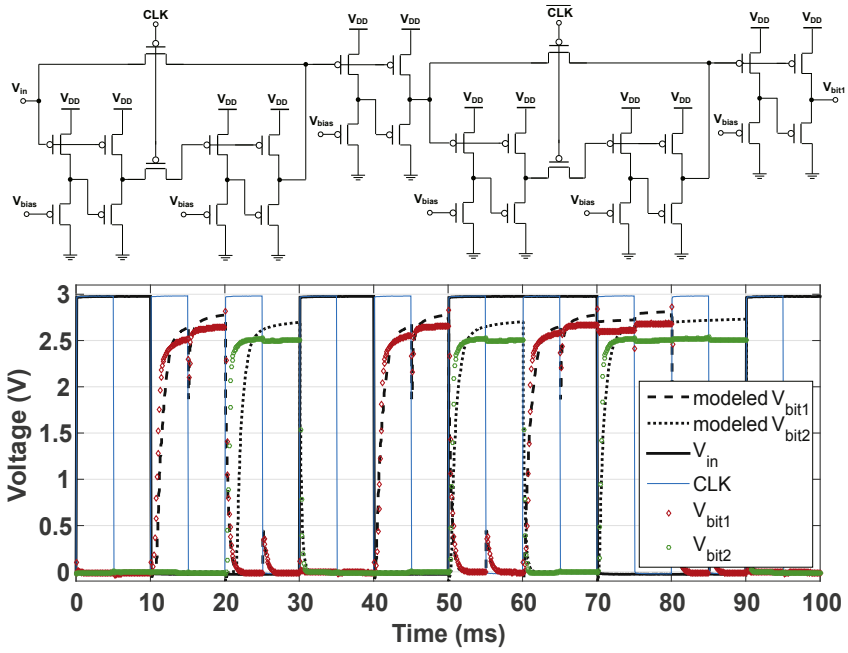

Fig. 8. Schematic of a 1-stage shift register and measurement and modeling results of a 2-stage shift register based on a dynamic positive-edge-triggered master-slave flip-flop using the pseudo-E design. V_{bit1} and V_{bit2} correspond to the output voltage of the first and second shifting stages, respectively. All TFTs have a channel length of 20 μm, and the channel width ratio (K) is 3. The measurement was performed with a supply voltage of 3 V, a bias voltage of −1 V and a clock frequency of 100 Hz.

Table 3
Summary of the characteristics of recently reported organic-TFT-based shift registers.

Parameter	this work (Fig. 6)	this work (Fig. 7)	this work (Fig. 8)	2017 [3]	2015 [17]	2014 [13]	2013 [18]	2004 [19]
Design type	Static master-slave	Dynamic master-slave	Dynamic master-slave	NOR D-FF	TG-based FF	NAND D-FF	Dynamic TSPC	–
TFTs per flip-flop	16	16	28	26	22	52	9	59[a]
Area per flip-flop (mm^2)	1.4 × 3.5	1.4 × 3.5	1.4 × 4.4	2.5 × 2.5	2.75[a]	0.65 × 4.3[a]	3 × 4.5	–
Shift register stages	1	1 (3)	2	3	32	240	3	32
Supply voltage (V)	3	2.2 (3)	3	20	3.3	20	20	35
Maximum clock frequency (kHz)	1	3 (0.1)	0.1	10	1	0.07	0.333	5

[a] Calculated.

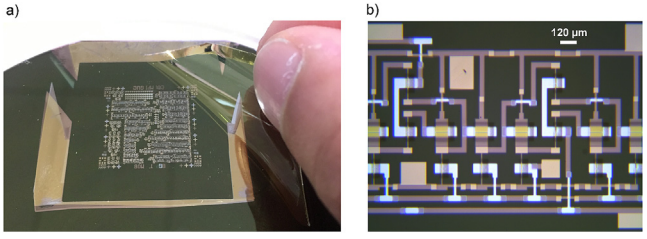

Fig. 9. (a) Photograph of the flexible PI/BCB substrate with the organic circuits as it is being detached from the handling wafer. (b) Photograph of 1-stage dynamic shift register based on the biased-load design.

impedance probes should be used for characterizing the dynamic circuit operation.

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