Parameter Uniformity of Submicron-Channel-Length Organic Thin-Film Transistors Fabricated by Stencil Lithography

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***Abstract*—Using high-resolution stencil lithography, we have fabricated bottom-gate, top-contact (inverted staggered) organic thin-film transistors that have a channel length of 0.5 μm and gate-to-source and gate-to-drain overlaps of 2 μm. Owing to the small channel length, the transistors have a large width-normalized transconductance of (0.50 $\pm$ 0.05) S/m, despite the relatively small charge-carrier mobility of (0.36 $\pm$ 0.04) cm^2/V $\cdot$ s. Across an array of 16 transistors, the uniformity of the transconductance is about 9% (1σ), the uniformity of the carrier mobility is about 7%, the uniformity of the threshold voltage is about 4%, the subthreshold slope varies between 95 and 150 mV/decade, and the on/off current ratio varies between 7 $\times$ 10^4 and 3 $\times$ 10^6. To our knowledge, this is the first time that the parameter distribution of submicron-channel-length organic TFTs is reported.**

***Index Terms*—Organic thin-film transistors, stencil lithography, submicron organic transistors.**

I. Introduction

ORGANIC thin-film transistors (TFTs) are field-effect transistors in which the semiconductor is a thin, usually polycrystalline layer of conjugated organic molecules [1]. Because they can be fabricated on a variety of substrates, organic TFTs are potentially useful for large-area electronics applications, such as active-matrix displays and sensor arrays [2]–[10]. In some of the more advanced applications envisioned for organic TFTs, such as the integrated row and column drivers of displays or sensor arrays, the TFTs have to be able to control electrical signals of a few volts at frequencies of several megahertz [11]. Since the charge-carrier field-effect mobility in organic TFTs is usually no greater than 5 to 10 cm^2/Vs [12], this implies that the critical dimensions of the TFTs, i.e., the channel length and the gate-to-source and gate-to-drain overlaps that determine the parasitic capacitances of the TFTs, must be in the range of about 1 μm or even below 1 μm [13].

A number of approaches have been implemented in order to fabricate organic TFTs with submicron dimensions. For example, direct-write electron-beam lithography has been used to investigate the characteristics of organic TFTs with channel lengths as short as 10 nm [14]–[20]. Using nanoimprint lithography, organic TFTs with channel lengths as small as 70 nm and parasitic gate-to-contact overlaps as small as 5 μm have been demonstrated [21]–[23]. By combining nanoimprint lithography (to pattern the gate electrodes) with self-aligned photolithography (to pattern the source and drain contacts using a self-aligned backside exposure), organic TFTs with channel lengths as small as about 0.7 μm and gate overlaps of 0.2 μm have been fabricated [24]. By employing a self-aligned inkjet-printing approach in combination with self-aligned photolithography, organic TFTs with a channel length of 0.2 μm and gate overlaps of 0.7 μm have been demonstrated [25]. Submicron-channel-length organic TFTs have also been fabricated using a vertical device architecture in which the channel length is defined by the thickness of a mesa [26], which eliminates the need for high-resolution lithography to define the channel length, although lithography is still required in order to minimize the parasitic overlap capacitances.

Here we demonstrate the use of high-resolution stencil lithography to fabricate organic TFTs with a channel length of 0.5 μm and a gate overlap of 2 μm. Unlike the above-mentioned patterning methods (photolithography, electron-beam lithography, nanoimprint lithography, inkjet-printing), stencil lithography allows the fabrication of organic TFTs without the need for resists, solvents, irradiation and mechanical pressure, all of which are potentially harmful to organic semiconductors [27]. Instead, the functional materials are deposited by thermal evaporation in vacuum through openings in the stencil masks. Stencil lithography is widely employed for the patterning of the organic emissive materials in commercially manufactured active-matrix organic light-emitting diode (AMOLED) displays; these masks are usually made of a nickel-iron alloy (invar fine metal masks; FMM), have a thickness of a few tens of microns, are patterned by chemical etching or laser cutting, and provide a resolution of about 20 μm [28]. Stencil masks (or shadow masks) for organic TFT fabrication are often made of laser-cut polyimide or stainless steel with a thickness of a few tens of microns and typically provide a minimum resolution of about 10 μm [29]–[32]. For

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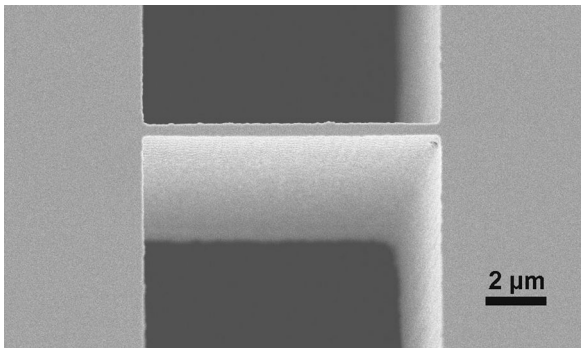

Fig. 1. Scanning electron microscopy image showing a detail of a high-resolution silicon stencil mask employed for the fabrication of submicron-channel-length organic TFTs.

the fabrication of organic TFTs with micron or submicron dimensions, high-resolution silicon-based stencil masks that were initially developed for ion-projection lithography [33] have recently been utilized. For example, using a 500 nm thick silicon nitride stencil mask supported by a silicon frame and patterned by photolithography and plasma etching, Sidler *et al*. and Fleischli *et al*. demonstrated organic TFTs with channel lengths as small as 2 μm [34], [35]. Using stencil masks based on 20 μm thick silicon membranes processed from silicon-on-insulator (SOI) wafers and patterned by electron-beam lithography and deep reactive ion etching [36]–[38], Kraft *et al*. demonstrated organic TFTs with a channel length of 0.5 μm and a gate overlap of 20 μm [39]. Here we extend this work by reducing the parasitic gate-to-source and gate-to-drain overlaps to 2 μm and by evaluating the parameter uniformity of these submicron-channel-length organic transistors.

II. Transistor Fabrication Process

A set of four stencil masks is required to fabricate the TFTs: one mask each to pattern the gate electrodes, the gate vias, the organic semiconductor layer, and the source/drain contacts. Fig. 1 shows a scanning electron microscopy (SEM) image of a detail on the source/drain mask.

In the first step of the TFT fabrication process, a 40-nm-thick layer of aluminum is deposited onto the surface of the substrate (a silicon wafer coated with a thick layer of silicon dioxide) by thermal evaporation in vacuum through the first stencil mask. To define the gate vias, a 30-nm-thick layer of gold is deposited through the second stencil mask in specific locations on the aluminum outside of the active transistor areas. In the third step, a hybrid gate dielectric composed of a 3.6-nm-thick layer of aluminum oxide (obtained by briefly exposing the surface of the aluminum gate electrodes to an oxygen plasma) and a 1.7-nm-thick self-assembled monolayer (SAM) of *n*-tetradecylphosphonic acid (obtained by immersing the substrate into a 2-propanol solution of the alkylphosphonic acid) is then produced; this hybrid AlO_x/SAM gate dielectric has a unit-area capacitance of 700 nF/cm^2 [40]. Next, a 25-nm-thick layer of the small-molecule organic semiconductor dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) [41] is deposited onto the hybrid AlO_x/SAM gate dielectric by sublimation in vacuum

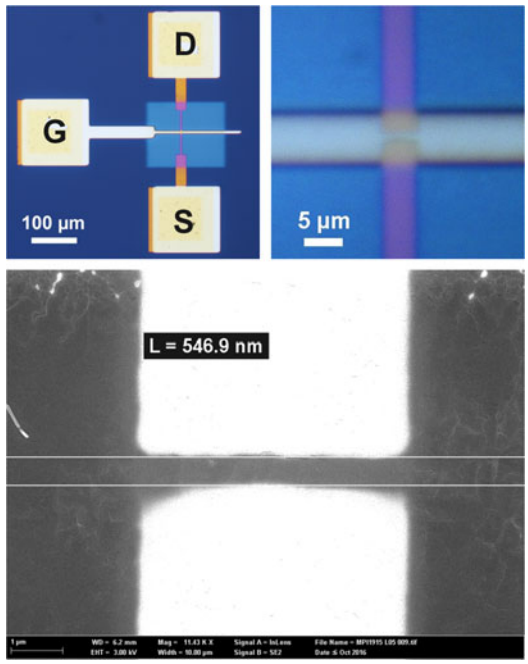

Fig. 2. Optical and scanning electron microscopy images of an organic TFT fabricated using a set of four high-resolution silicon stencil masks. The TFT has a channel length of 0.5 μm, a channel width of 5 μm, and gate-to-source and gate-to-drain overlaps of 2 μm.

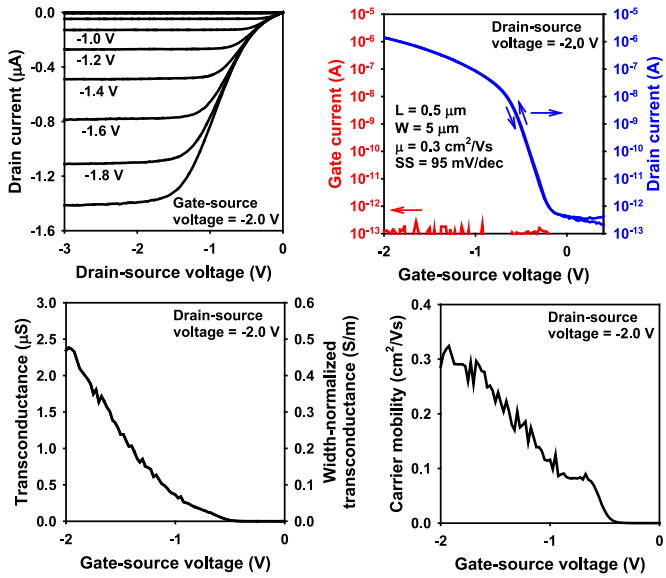

Fig. 3. Measured current-voltage characteristics of an organic TFT with a channel length of 0.5 μm, a channel width of 5 μm, and a gate-to-contact overlap of 2 μm. The TFT has a channel-width-normalized transconductance of 0.46 S/m, an effective carrier mobility in the saturation regime of 0.3 cm^2/Vs, a threshold voltage of -0.7 V, a subthreshold slope of 95 mV/decade, and an on/off current ratio of 3×10^6.

through the third stencil mask. During the DNTT deposition, the substrate is held at a temperature of 60 °C in order to promote the formation of a well-ordered semiconductor layer. Heating the substrate during the deposition of the semiconductor layer does not cause damage to the alkylphosphonic acid SAM, which has been shown to be stable at temperatures as high as 250 °C [42], [43]. In the last process step, a 30-nm-thick layer of gold

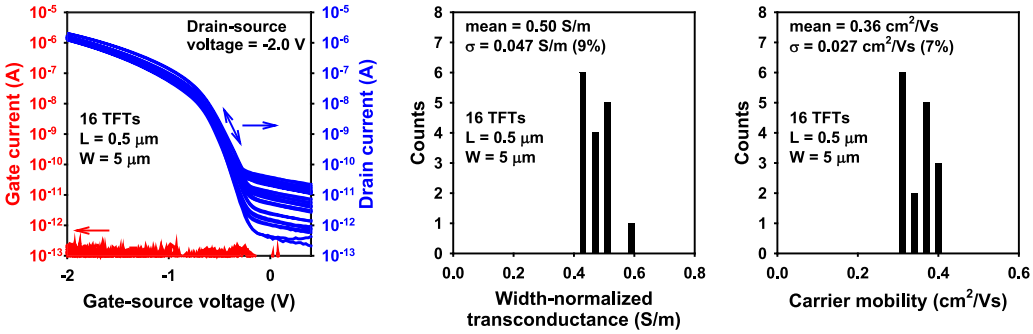

Fig. 4. Measured transfer characteristics of 16 TFTs fabricated on the same substrate, and distribution of the width-normalized transconductance and carrier mobility.

is deposited in vacuum through the fourth stencil mask in order to define the source and drain contacts. Mask alignment is performed manually using an optical microscope.

III. Transistor Characteristics

Fig. 2 shows optical microscopy images and an SEM image of a TFT with a channel length of 0.5 μm, a channel width of 5 μm, and a gate-to-contact overlap of 2 μm. Based on the lateral TFT dimensions and the unit-area gate-dielectric capacitance (700 nF/cm^2), the total capacitance of the transistors (sum of intrinsic and parasitic capacitances) is estimated to be about 160 fF.

The current-voltage characteristics of this TFT, measured on a manual probe station in ambient air using an Agilent 4156C Semiconductor Parameter Analyzer, are shown in Fig. 3. The transfer characteristics (drain current vs. gate-source voltage) indicate that the TFT has a transconductance of 2.3 μS (which corresponds to a channel-width-normalized transconductance of 0.46 S/m), an effective carrier mobility in the saturation regime of 0.3 cm^2/Vs, a threshold voltage of -0.7 V, a subthreshold slope of 95 mV/decade, and an on/off current ratio of 3×10^6. To our knowledge, this is the steepest subthreshold slope reported for a submicron-channel-length organic TFT. Long-channel organic TFTs (channel length greater than 10 μm) have shown subthreshold slopes as steep as 65 mV/decade [44], [45], and for polyelectrolyte-gated polymer TFTs with a channel length of 2.5 μm, a subthreshold slope of 70 mV/decade has been reported [46]. Also, to our knowledge, there are only two previous reports of organic TFTs with a channel length of 0.5 μm or less displaying an on/off current ratio greater than 3×10^6: Ante *et al*. used electron-beam lithography to fabricate organic TFTs with a channel length of 90 nm [47] and Min *et al*. employed nanowire lithography to fabricate organic TFTs with a channel length of 340 nm [48], both of which displayed on/off ratios of 10^7, but less steep subthreshold slopes of 160 mV/decade [47] and 1 V/decade [48].

The output characteristics (drain current vs. drain-source voltage) of the TFT in Fig. 3 indicate good saturation of the drain current for drain-source voltages between -2 and -3 V, providing a large differential output resistance (inverse of the slope of the drain current vs. drain-source voltage curves) of about 6.5 $\times 10^7$ Ω at a gate-source voltage of -2 V. Together with the transconductance of 2.3 μS measured at the same gate-source voltage (-2 V), this translates into an intrinsic gain (product of transconductance and output resistance) of 150 at this gate-source voltage. To our knowledge, this is the largest intrinsic gain reported for a submicron-channel-length organic TFT. Large intrinsic gain is important for integrated circuits, especially for amplifiers. Long-channel organic and inorganic TFTs, which often benefit from a larger differential output resistance, have shown intrinsic gain approaching 1000 [49]–[51], but at the cost of a significantly larger device capacitance.

For drain-source voltages between 0 V and about -1 V, a linear relation between the drain current and the drain-source voltage is expected for long-channel TFTs [51]. However, in submicron TFTs, the channel resistance (which is proportional to the channel length) is significantly smaller than the contact resistance (which is independent of the channel length) [52], so that a large portion of the applied drain-source voltage drops across the contacts, resulting in nonlinear current-voltage characteristics. Based on the channel length (0.5 μm), channel width (5 μm) and gate overlaps (2 μm), the channel resistance is estimated to be about 30 kΩ (15 Ωcm) [52] and the contact resistance is estimated to be about 4 MΩ (2 kΩcm) [53], which means that the contact resistance accounts for about 99% of the total device resistance. This explains both the severe nonlinearity of the output curves for small drain-source voltages and the fact that the effective carrier mobility (0.3 cm^2/Vs) is only about 10% of the carrier mobilities typically measured in long-channel DNTT TFTs [52].

IV. Parameter Uniformity

Fig. 4 shows the measured transfer characteristics of 16 nominally identical DNTT TFTs with a channel length of 0.5 μm, a channel width of 5 μm, and a gate-to-contact overlap of 2 μm fabricated on the same substrate and the distribution of the width-normalized transconductance and the carrier mobility extracted from these transfer curves. The width-normalized transconductance varies between 0.46 and 0.64 S/m, with a standard deviation of 9% (1σ), the carrier mobility varies between 0.32 and 0.41 cm^2/Vs, with a standard deviation of 7%, the threshold voltage varies between -0.6 and -0.7 V, with a standard deviation of 4%, the subthreshold slope varies between 95 and 150 mV/decade, the on/off current ratio varies between

7×10^4 and 3×10^6, and the off-state drain current is below 30 pA for all TFTs. To our knowledge, this is the first time that the parameter distribution of submicron-channel-length organic TFTs is reported. While the parameter variations observed here may be too large for certain analog-circuit applications with particularly demanding uniformity requirements, they will in principle be sufficient for digital circuits and pixel select transistors.

V. Summary and Outlook

We have developed a process for the fabrication of organic thin-film transistors with channel lengths as short as 0.5 μm and gate-to-contact overlaps as small as 2 μm using high-resolution silicon stencil masks fabricated from SOI wafers and patterned by electron-beam lithography and deep reactive ion etching. The TFTs have an average width-normalized transconductance of 0.5 S/m (with a standard deviation of 9%), an average effective carrier mobility of 0.36 cm^2/Vs (with a standard deviation of 7%), a subthreshold slope as steep as 95 mV/decade, an on/off current ratio as large as 3×10^6, and an intrinsic gain of 150.

At these channel and contact overlap lengths, the contact resistance accounts for about 99% of the total device resistance, resulting in a pronounced nonlinearity of the output characteristics at small drain-source voltages. Preliminary results suggest that with the current stencil-mask technology it will be possible to fabricate functional TFTs with a channel length as small as about 0.3 μm, which will further reduce the capacitance of the transistors, but will further aggravate the detrimental influence of the contact resistance on the linearity of the output curves. A promising strategy for reducing the contact resistance and improving the linearity of the current-voltage characteristics in short-channel organic TFT is the introduction of area-selective contact doping [47], [54], [55].

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