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Below-one-volt organic thin-film transistors with large on/off current ratios

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A B S T R A C T

In many of the applications envisioned for organic thin-film transistors (TFTs), the electrical power will be supplied by small batteries or energy harvesters, which implies that it will be beneficial if the TFTs can be operated with voltages of 1 V or even below 1 V. At the same time, the TFTs should have large on/off current ratios, especially for applications in digital circuits and active matrices. Here we demonstrate p-channel and n-channel organic TFTs fabricated on a flexible plastic substrate that have a turn-on voltage of exactly 0 V, a subthreshold slope of 100 mV/decade, and an on/off current ratio of 2×10^5 when operated with gate-source voltages between 0 and 0.7 V. Complementary inverters fabricated using these TFTs have a small-signal gain of 90 and a minimum noise margin of 79% at a supply voltage of 0.7 V. Complementary ring oscillators can be operated with supply voltages as small as 0.4 V.

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1. Introduction

Organic thin-film transistors (TFTs) can typically be fabricated at low process temperatures and thus on a variety of unconventional substrates, such as plastics [1—5], paper [6—11] and textiles [12]. This makes organic TFTs attractive for mobile and wearable electronics applications. For such applications, grid electricity is usually not available, so the TFTs and circuits must be powered by small batteries, near-field coupling [13] or solar cells, which imposes an upper limit on the operating voltage and power consumption of the devices and circuits. For example, the output voltage of single-junction solar cells at the maximum power point is usually in the range of 0.7—1 V [14—16]. This output voltage can obviously be boosted by connecting several cells in series, but in terms of process simplicity and system size, there are certain benefits if the TFTs and circuits can be operated with supply voltages in the range of 0.7—1 V and hence with a single solar cell. Significant progress in the development of organic TFTs operating with such low supply voltages has indeed been made [17—36]. Herlogsson et al. [21], Ke et al. [28] and Jinno et al. [34] have even demonstrated organic complementary circuits capable of operating with supply voltages well below 1 V.

However, the transistors in these reports have relatively small on/off current ratios: For the TFTs reported by Ke et al. [28], the ratio between the on-state drain current (measured at a gate-source voltage of 1 V) and the off-state drain current (at a gate-source voltage of 0 V) is less than 10^2, the TFTs reported by Jinno et al. [34] have on/off ratios of 2×10^4 for the p-channel TFTs and 2×10^2 for the n-channel TFTs (also measured for gate-source voltages from 0 to 1 V), and the electrolyte-gated TFTs reported by Herlogsson et al. [21] have on/off ratios of 10^4 at 0.7 V. For organic electrochemical transistors, Giovannitti et al. [31,32] have reported on/off ratios of 10^4 for voltages of 0.6 V [31,32]. To our knowledge, the largest on/off ratio of an organic transistor at a supply voltage of 1 V or less is 3×10^5, reported by Kim et al. [26] for an electrolyte-gated p-channel TFT at a supply voltage of −0.8 V. For organic n-channel TFTs, the largest on/off ratio for supply voltages of 1 V or less is 10^4 [21,31].

Since the realization of complementary circuits with large signal gain, large noise margins and small power consumption requires p-channel and n-channel transistors with large on/off current ratios, further improvements in the on/off current ratio, especially of organic n-channel transistors, are desirable. Here we report the fabrication of p-channel and n-channel organic TFTs that show on/off current ratios between 2×10^5 and 10^6 for supply voltages between 0.7 and 1 V, as well as low-voltage organic complementary inverters with large gain, large noise margins and small static power consumption.

2. Device and circuit fabrication

All transistors and circuits were fabricated on a 125-μm-thick flexible polyethylene naphthalate substrate (Teonex® Q65 PEN; kindly provided by William A. MacDonald, DuPont Teijin Films, Wilton, U.K.). The TFTs were fabricated in the bottom-gate, top-contact (inverted staggered) device structure. In the first step, a 30-nm-thick layer of aluminum was deposited by thermal evaporation in vacuum through a polyimide shadow mask (CADiLAC Laser, Hilpoltstein, Germany). To define the gate vias, a 30-nm-thick layer of gold was deposited through a second shadow mask in specific locations on the aluminum gate electrodes outside of the active transistor areas. The substrate was then briefly exposed to an oxygen plasma to increase the thickness of the native aluminum oxide (AlO_x) layer from ~1.5 nm to 3.6 nm and then immersed into a mixture of *n*-octadecylphosphonic acid (PCI Synthesis, Newburyport, MA, U.S.A.) and 12,12,13,13,14,14,15,15,16,16,17,17,18,18,18-pentadecafluoro-octadecylphosphonic acid (synthesized by Matthias Schlörholz, Heidelberg, Germany) in 2-propanol to allow a mixed monolayer to self-assemble on the plasma-oxidized aluminum surface [37]. The hybrid AlO_x/SAM gate dielectric has a thickness of 5.7 nm and a unit-area capacitance of 700 nF/cm^2 [37]. Next, a 12-nm-thick layer of N,N'-bis(2,2,3,3,4,4,4-heptafluorobutyl)-1,7-dicyano-perylene-(3,4:9,10)-tetracarboxylic diimide (PTCDI-(CN)$_2$-(CH$_2$C$_3$F$_7$)$_2$; ActivInk™ N1100; Polyera Corp., Skokie, IL, U.S.A. [38,39]) was deposited by sublimation in vacuum through the third shadow mask as the semiconductor for the n-channel TFTs, followed by the deposition of either a 15-nm-thick layer of 2,7-diphenyl[1]benzothieno[3,2-*b*]benzothiophene (DPh-BTBT; Sigma Aldrich [40,41]) or a 25-nm-thick layer of dinaphtho [2,3-b:2′,3'-f]thieno[3,2-*b*]thiophene (DNTT; Sigma Aldrich [8,10,34,39]) through the fourth shadow mask as the semiconductor for the p-channel TFTs. During the semiconductor depositions, the substrate was held at a temperature of 140 °C (N1100), 100 °C (DPh-BTBT) or 60 °C (DNTT). Finally, a 30-nm-thick layer of gold was deposited in vacuum through the fifth shadow mask to define the source and drain contacts. Mask alignment was performed manually using an optical microscope. All TFTs have a channel length of 40 μm and gate-to-source and gate-to-drain overlaps of 80 μm. All electrical measurements were performed in ambient air at room temperature. A schematic cross-section of the TFTs and the chemical structures of the organic semiconductors and the alkyl- and fluoroalkyl-phosphonic acids are shown in Fig. 1.

3. Transistor characteristics

To maximize the ratio between the drain currents measured at gate-source voltages of 1 V and 0 V, it is beneficial to fabricate TFTs that have a turn-on voltage of exactly 0 V. (We define the turn-on voltage, also called switch-on voltage [42], as the gate-source voltage at which the drain current has its minimum.) In general, this requires some form of deterministic, continuous and permanent control of the turn-on voltage. In organic TFTs, this can be accomplished by employing a gate dielectric in which two materials that induce different turn-on voltages are blended, so that the turn-on voltage is determined by the mixing ratio of these two materials. Examples are gate dielectrics based on polymer blends [43] or mixed self-assembled monolayers (SAMs) [37,44]. In TFTs with mixed-SAM gate dielectrics, the surface of the gate oxide is functionalized with a SAM composed of molecules with different functional groups, for example an alkyl- and a fluoroalkyl-phosphonic acid [37,39]. In the simplest case, the phosphonic acids are mixed in solution, and the substrate is dipped into this solution, leading to the spontaneous formation of a mixed SAM on the gate-oxide surface. When the organic semiconductor is deposited onto the SAM-functionalized gate oxide, the mixing-ratio-dependent contributions of the electric dipole moment of the SAM and of the electronic coupling between the SAM and the organic semiconductor produce a certain turn-on voltage [45]. This is illustrated in Fig. 2 for organic n-channel TFTs fabricated using alkyl-/fluoroalkyl-SAM gate dielectrics with four different mixing ratios and using the small-molecule organic semiconductor Polyera ActivInk™ N1100.

Fig. 2 indicates that the turn-on voltage of the N1100 TFTs is 0 V when the gate-dielectric SAM is prepared from a solution composed of 25% alkyl- and 75% fluoroalkyl-phosphonic acid molecules. Fig. 2c illustrates the good reproducibility of the process of setting the turn-on voltage to a particular value during TFT fabrication using mixed-SAM gate dielectrics. Conducting the same experiment with p-channel TFTs based on the popular organic semiconductor dinaphtho[2,3-b:2′,3'-f]thieno[3,2-b]thiophene (DNTT) [46] and its high-mobility decyl- and phenyl derivatives C$_{10}$-DNTT and DPh-DNTT [47–54], we found that a turn-on voltage of 0 V would require a SAM with a mixing ratio of approximately 80% alkyl- and 20% fluoroalkyl-phosphonic acid molecules. In other words, the fabrication of n-channel N1100 and p-channel DNTT, C$_{10}$-DNTT or DPh-DNTT TFTs with a turn-on voltage of 0 V would require two different SAMs for the n-channel and p-channel TFTs. Methods to prepare two different SAMs on the same substrate have been developed [55,56], but in terms of process simplicity, there are certain advantages if all TFTs on the substrate can be fabricated with the same SAM. Through the screening of various organic semiconductors we found that p-channel TFTs based on the recently reported benzothieno[3,2-b] benzothiophene derivative DPh-BTBT [40,41] happen to have a turn-on voltage of 0 V for a SAM mixing ratio of 25% alkyl- and 75% fluoroalkyl-phosphonic acids. In other words, using N1100 and DPh-BTBT as the semiconductors, n-channel and p-channel TFTs
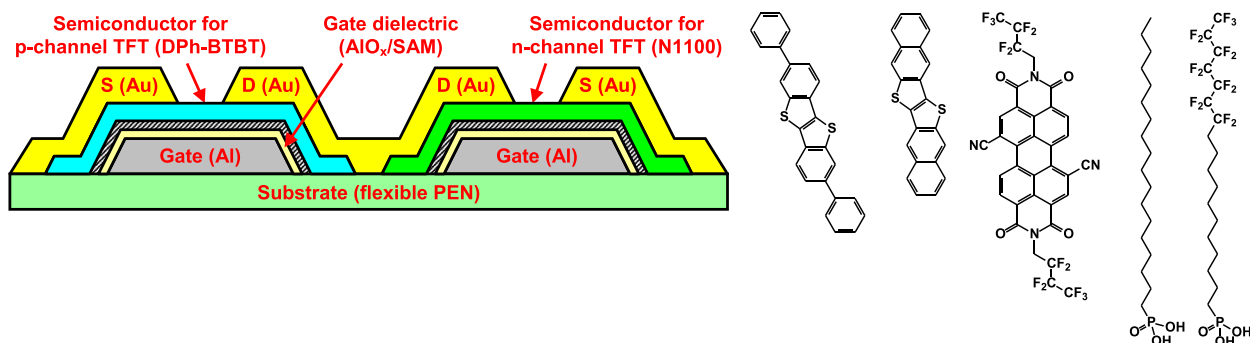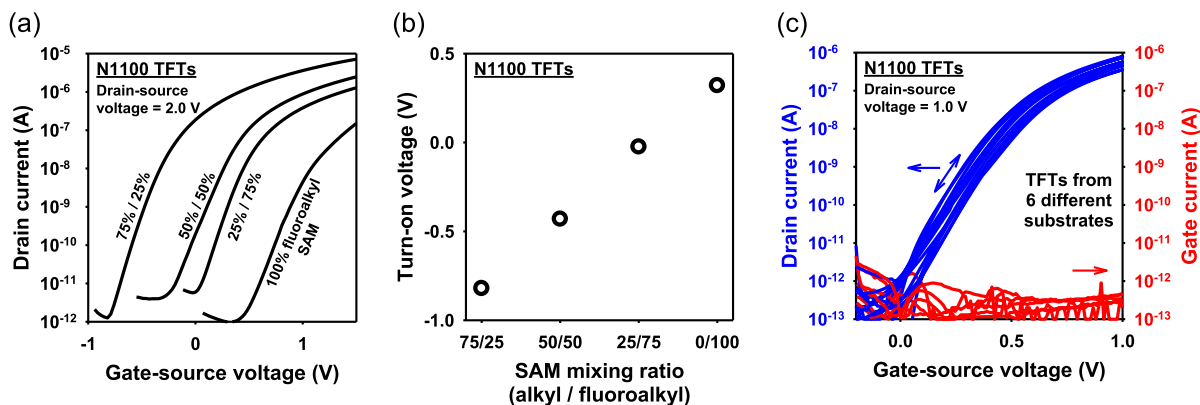

Fig. 1. Schematic cross-section of the thin-film transistors and chemical structures of the organic semiconductors DPh-BTBT, DNTT and Polyera ActivInk™ N1100 and of the alkyl- and fluoroalkyl-phosphonic acids employed for the gate dielectric.

Fig. 2. (a) Transfer characteristics of N1100 n-channel TFTs fabricated using gate dielectrics based on alkyl/fluoroalkyl-phosphonic acid SAMs with four different mixing ratios. The effect of the SAM mixing ratio on the turn-on voltage (defined as the gate-source voltage at which the drain current has its minimum) is clearly seen. The effective carrier mobility is very similar for all four TFTs. (b) Dependence of the turn-on voltage of the TFTs (defined as the gate-source voltage at which the drain current has its minimum) on the SAM mixing ratio. A turn-on voltage of 0 V is obtained for a mixing ratio of 25% alkyl/75% fluoroalkyl-phosphonic acids. (c) Transfer characteristics of N1100 TFTs with a SAM mixing ratio of 25% alkyl/75% fluoroalkyl-phosphonic acids fabricated on six different substrates over a period of two months, showing the good reproducibility of this method of setting the turn-on voltage by using a gate-dielectric SAM with a particular mixing ratio.
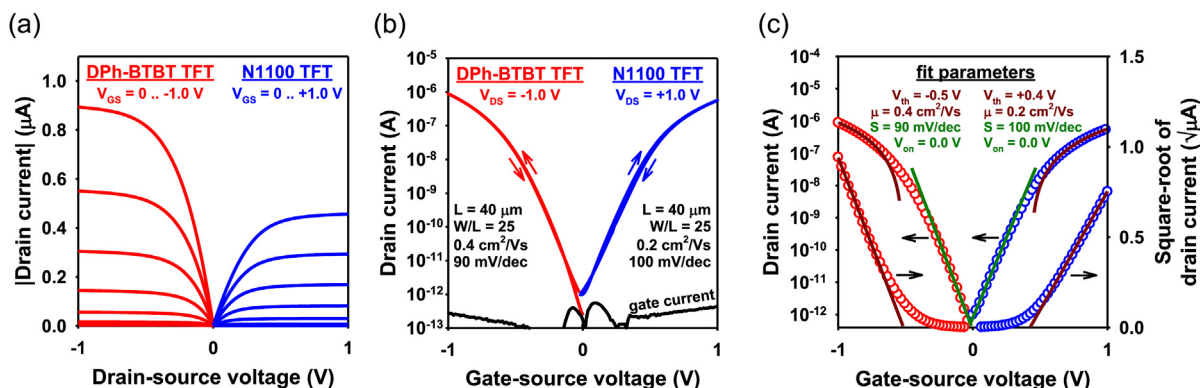
Fig. 3. (a) Output characteristics of DPh-BTBT p-channel TFTs (red lines) and N1100 n-channel TFTs (blue lines) fabricated on a PEN substrate using an alkyl/fluoroalkyl SAM with a mixing ratio of 25%/75% and measured with gate-source voltages (V_GS) in steps of 0.1 V. The TFTs have a channel length (L) of 40 μm and a channel width (W) of 1000 μm. (b) Transfer characteristics of the same TFTs, measured with drain-source voltages (V_DS) of −1 V and 1 V. The measured gate currents are shown as black lines. (c) Extraction of the threshold voltage (V_th), the effective carrier mobility (μ) and the subthreshold slope (S) by fitting Equations (1)–(5) to the measured transfer characteristics. Measurement data are shown as red and blue symbols, fits to the saturation regime as dark red lines, and fits to the subthreshold regime as green lines. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

with a turn-on voltage of 0 V can be fabricated using the same SAM. The carrier mobility of these DPh-BTBT TFTs is notably smaller than that of TFTs based on DNTT, C_{10}-DNTT or DPh-DNTT, but not smaller than those of the N1100 n-channel TFTs, which means that the performance of complementary circuits fabricated using DPh-BTBT p-channel and N1100 n-channel TFTs will not be limited by the carrier mobility of the DPh-BTBT TFTs.

Fig. 3a,b show the measured current-voltage characteristics of DPh-BTBT p-channel and N1100 n-channel TFTs fabricated on a flexible polyethylene naphthalate (PEN) substrate using an alkyl/fluoroalkyl-phosphonic acid gate-dielectric SAM with a mixing ratio of 25% alkyl/75% fluoroalkyl and measured with gate-source and drain-source voltages of −1 V and +1 V. The TFTs have a turn-on voltage of 0 V and on/off current ratios of 10^6 (DPh-BTBT) and 4×10^5 (N1100), measured for gate-source voltages between 0 and 1 V. To our knowledge, these are the largest on/off ratios reported for organic TFTs for this voltage range. To extract the threshold voltage (V_th), the effective carrier mobility (μ) and the subthreshold slope (SS) of the TFTs, the measured transfer characteristics were fitted to the following equations:

p-channel transistors:

$$I_D = - \frac{\mu \, C_{diel}}{2} \frac{W}{L} \left(V_{GS} - V_{th} \right)^2 \quad \text{for } V_{DS} \leq V_{GS} - V_{th} \leq 0 \text{(saturation regime)} \tag{1}$$

$$I_D = I_0 \exp\left(- \frac{q \left(V_{GS} - V_{on} \right)}{n \, k \, T} \right) \quad \text{for } V_{th} \leq V_{GS} \leq V_{on} \text{(subthreshold regime)} \tag{2}$$

n-channel transistors:

subthreshold current in inversion-mode transistors can be shown

$$I_D = \frac{\mu\, C_{diel}\, W}{2\, L}\, (V_{GS} - V_{th})^2 \quad \text{or } 0 \leq V_{GS} - V_{th} \leq V_{DS} \text{(saturation regime)} \tag{3}$$

$$I_D = I_0 \exp\left(\frac{q\,(V_{GS} - V_{on})}{n\,k\,T}\right) \quad \text{for } V_{on} \leq V_{GS} \leq V_{th}\text{(subthreshold regime)} \tag{4}$$

where I_D is the drain current, C_{diel} is the unit-area capacitance of the gate dielectric (700 nF/cm^2), W is the channel width (1000 μm), L is the channel length (40 μm), V_{GS} is the applied gate-source voltage, V_{on} is the turn-on voltage, I_0 is the drain current when the gate-source voltage is equal to the turn-on voltage, q is the electronic charge, k is Boltzmann's constant, and T is the temperature (300 K). The subthreshold slope S (i.e., the inverse slope of the log(I_D) versus V_{GS} curve in the subthreshold region) and the ideality factor n are related as follows:

$$S = \frac{\partial\, V_{GS}}{\partial\,(\log_{10} I_D)} = \frac{n\,k\,T}{q}\, \ln 10 \tag{5}$$

The result of the fitting procedure is illustrated in Fig. 3c. The measured drain current is in good agreement with the values calculated using Equations (1) and (3) (saturation regime) when the absolute value of the gate-source voltage is greater than approximately 0.7 V (DPh-BTBT) or 0.6 V (N1100) and with the values calculated using Equations (2) and (4) (subthreshold regime) when the absolute value of the gate-source voltage is smaller than approximately 0.3 V. The fitting procedure yields threshold voltages, carrier mobilities and subthreshold slopes of −0.5 V, 0.4 cm^2/Vs and 90 mV/decade for the DPh-BTBT TFTs and 0.4 V, 0.2 cm^2/Vs and 100 mV/decade for the N1100 TFTs.

Equations (1)–(5) were developed for field-effect transistors that operate in the inversion mode, such as silicon MOSFETs [57] and TFTs with intentionally doped carrier channels [58]. In inversion-mode transistors, the threshold voltage is conveniently defined as the gate-source voltage at which the density of the gate-induced minority carriers at the semiconductor-dielectric interface equals the density of the dopant-induced majority carriers in the semiconductor bulk (i.e., at the onset of strong inversion), and the

to have an exponential dependence on the applied gate-source voltage [57]. In contrast, organic TFTs with intrinsic semiconductor layers (like those discussed here) operate in the accumulation mode, and hence there is neither a physically meaningful definition of a threshold voltage nor any physically meaningful reason for an exponential relationship between the drain current and the gate-source voltage [59]. But since the threshold voltage is usually required for device modeling (except in surface-potential-based device models [60]) and since the drain current of organic TFTs in the subthreshold regime does in fact often show an exponential dependence on the gate-source voltage over several orders of magnitude (e.g., three orders of magnitude for the DPh-BTBT and N1100 TFTs in Fig. 3; five orders of magnitude for the C$_{10}$-DNTT TFTs in Ref. [61]), the fitting procedure illustrated in Fig. 3 appears nonetheless useful here, even if the values extracted for the threshold voltage and the subthreshold slope may just be fitting parameters.

As mentioned in the Introduction, for certain applications it may be beneficial if the TFTs can be operated at voltages below 1 V. For example, Colleaux et al. [20], Herlogsson et al. [21], Malti et al. [23], Schwabegger et al. [24], Giovannitti et al. [31,32] and Jinno et al. [34] have all demonstrated n-channel organic transistors capable of operating with gate-source voltages below 1 V, albeit with relatively small on/off current ratios ($\leq 10^4$). In contrast, the DPh-BTBT p-channel and N1100 n-channel TFTs which we have fabricated using an alkyl-/fluoroalkyl-phosphonic acid SAM with a mixing ratio of 25%/75% exhibit on/off current ratios of 2 × 10^5 for gate-source voltages between 0 and 0.7 V, as shown in Fig. 4a and b. Fig. 4c summarizes the on/off current ratios (measured from a gate-source voltage of 0 V) of low-voltage organic TFTs reported in literature, including electrolyte-gated and electrochemical organic transistors.
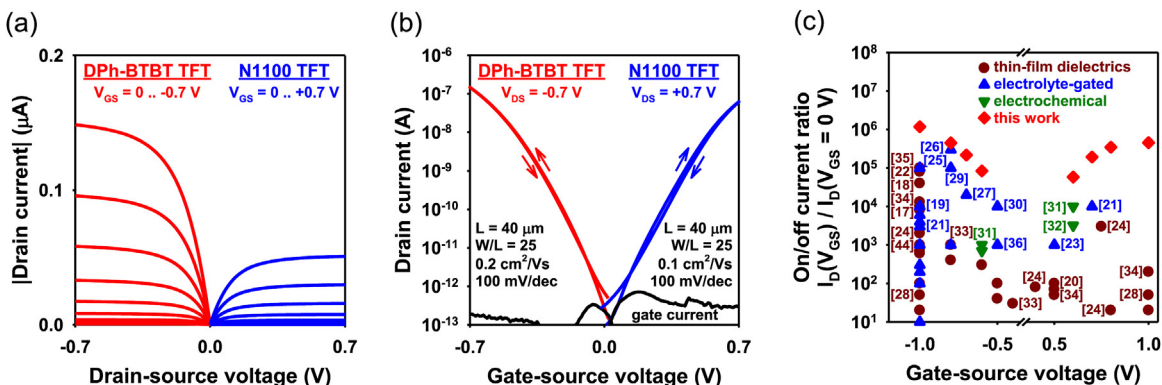
Fig. 4. (a) Output and (b) transfer characteristics of the same TFTs as in Fig. 3, but measured with maximum voltages of −0.7 V and 0.7 V (step size in the gate-source voltages in the output curves is 0.05 V). (c) Literature summary of the on/off current ratios reported for low-voltage organic TFTs, including electrolyte-gated and electrochemical organic transistors. The on/off current ratio is here defined as the ratio between the drain currents measured at a particular gate-source voltage (e.g., −1 V) and a gate-source voltage of 0 V. The numbers refer to the list of references.

4. Inverter and ring oscillator characteristics

Fig. 5 shows the static transfer characteristics of a complementary inverter and the signal propagation delay per stage of a 5-stage complementary ring oscillator, both fabricated on the same PEN substrate as the TFTs shown in Figs. 3 and 4, using a gate-dielectric SAM with a mixing ratio of 25%/75%. The small-signal gain and the minimum noise margin of the inverter (calculated using the method described in Ref. [37]) are 180 and 84% at a supply voltage of 1.0 V and 90 and 79% at a supply voltage of 0.7 V. For organic complementary inverters fabricated on glass substrates, Petritz et al. have reported small-signal gains up to 1600 and noise margins as large as 92.5% [62]. For complementary inverters fabricated on flexible plastic substrates, Jinno et al. reported small-signal gains between 30 and 60 for supply voltages between 0.5 and 0.9 V [34]. Owing to the small drain currents that flow through the TFTs when the gate-source voltage is zero, the static currents of the inverter (when the input voltage is equal to zero or equal to the supply voltage and hence the gate-source voltage at one or the other TFT is zero) are also very small, less than 10^{-12} A for a supply voltage of 1.0 V and less than 10^{-13} A for a supply voltage of 0.7 V. This corresponds to a static power consumption of less than 1 pW at a supply voltage of 1.0 V and less than 0.1 pW at a supply voltage of 0.7 V.

The signal propagation delay of a ring oscillator ($t_{d,RO}$) is usually given as the inverse of the measured oscillation frequency (f_{RO}) divided by twice the number of inverter stages (N) and is thus the average of the signal delays associated with each inverter switching once from the low to the high output state ($t_{d,LH}$) and once from the high to the low output state ($t_{d,HL}$) [63]:

$$t_{d,RO} = \frac{1}{2\,N\,f_{RO}} = \frac{t_{d,LH} + t_{d,HL}}{2} \tag{6}$$

When an inverter switches from the low (high) to the high (low) output state, its output node is charged (discharged) through the p-channel (n-channel) transistor of that inverter, so the signal delays associated with these switching events are determined by the conductance of the TFTs and the capacitive load connected to the inverter's output node, i.e., the input capacitance of the following inverter. Since the conductance of the TFTs and the input capacitance of the inverters are non-trivial functions of the voltages between the various inverter nodes and since these voltages change during the duration of each switching event, it is not possible to derive an accurate analytical equation for a ring oscillator's signal delay. (The reason for the voltage dependence of the inverters' input capacitance is the Miller effect, due to which the gate-drain capacitance of the TFTs acts as a feedback capacitance that makes the input capacitance a function of the transconductance of the TFTs and thus of the gate-source and drain-source voltages applied to them.) Under the condition that the supply voltage of the ring oscillator is sufficiently large so that the TFTs operate above the threshold voltage while charging and discharging the output node (and making a number of other simplifications, as well as ignoring the Miller effect), approximate equations for the signal delays $t_{d,LH}$ and $t_{d,HL}$ have been developed [63,64]. Fits 1 and 2 in Fig. 5c were calculated using equations (5) and (8) in Ref. [63] and equations (36) and (41) in Ref. [64], respectively, and using the values for the carrier mobilities and threshold voltages obtained from the fitting procedure illustrated in Fig. 3c. Fig. 5c shows that for supply voltages greater than the absolute value of the threshold voltages of the TFTs, these equations provide solutions that are within an order of magnitude of the measured signal delays.

When the supply voltage is smaller than the threshold voltage of the TFTs, the TFTs operate in the subthreshold regime while charging and discharging the output node. Analytical equations for the signal delays $t_{d,LH}$ and $t_{d,HL}$ under this condition are to our knowledge not available. As an alternative, the signal delays can be estimated numerically from the measured transfer and output characteristics, which conveniently cover both the subthreshold and the above-threshold regimes of TFT operation. One possibility is to estimate $t_{d,LH}$ and $t_{d,HL}$ from the commonly used equations for the transit frequency of the TFTs [65]:

$$t_{d,LH} = \frac{1}{2 f_{T,p}} = \frac{\pi\,C_{G,p}}{g_{m,p}}; \; t_{d,HL} = \frac{1}{2 f_{T,n}} = \frac{\pi\,C_{G,n}}{g_{m,n}} \tag{7}$$

where f_T is the transit frequency, C_G is the gate capacitance and g_m is the transconductance of the TFTs. The gate capacitance of the TFTs is estimated as follows:

$$C_G = C_{diel}\,W\,(L + L_{ov,GS} + L_{ov,GD}) \tag{8}$$

where C_{diel} is the unit-area capacitance of the gate dielectric (700 nF/cm^2), W is the channel width ($W_p = 200\ \mu m$; $W_n = 800\ \mu m$), L is the channel length (40 μm), $L_{ov,GS}$ is the gate-to-source overlap (80 μm) and $L_{ov,GD}$ is the gate-to-drain overlap (80 μm), so
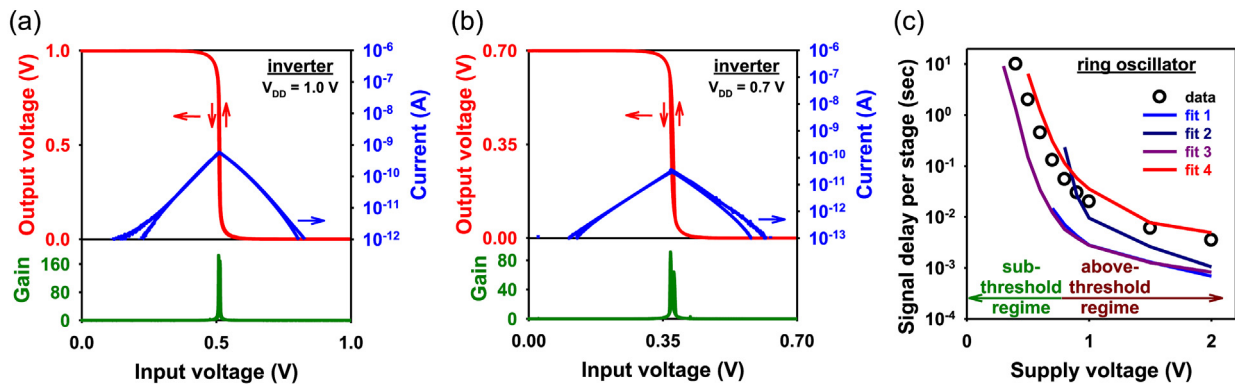
Fig. 5. (a) Transfer characteristics of a complementary inverter based on a DPh-BTBT p-channel and an N1100 n-channel TFT fabricated on a PEN substrate using an alkyl/fluoroalkyl SAM with a mixing ratio of 25%/75% and measured with a supply voltage (V_{DD}) of 1.0 V. (b) Transfer characteristics of the same inverter measured with a supply voltage of 0.7 V. (c) Signal propagation delay per stage of a 5-stage complementary ring oscillator based on DPh-BTBT and N1100 TFTs fabricated on the same substrate, plotted as a function of the supply voltage. The TFTs have a channel length of 40 μm and gate-to-contact overlaps of 80 μm. Also shown are four different fits, two of which were calculated using analytical equations (fit 1: equations (5) and (8) in Ref. [63]; fit 2: equations (36) and (41) in Ref. [64]) and two of which were calculated numerically from the measured transfer and output characteristics of the TFTs (fit 3: Equation (7) in the text; fit 4: Equation (10) in the text).
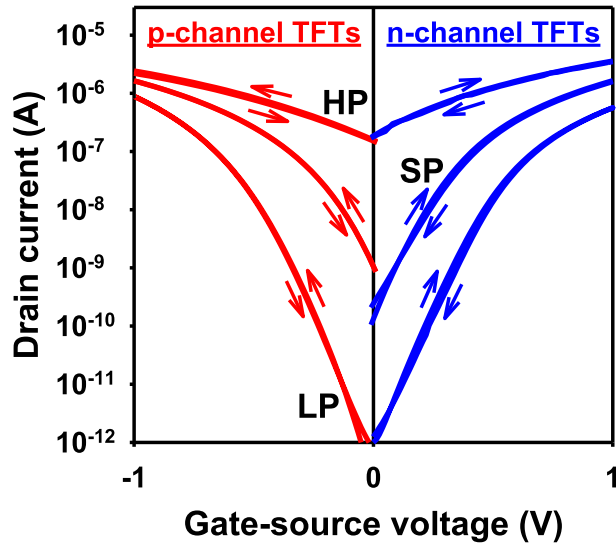
Fig. 6. Transfer characteristics of p-channel (red lines) and n-channel TFTs (blue lines) fabricated on different substrates using different organic semiconductors and SAM-based gate dielectrics with different SAM mixing ratios. The TFTs for the low-power (LP) option are the same as in Fig. 3 (SAM mixing ratio of 25%/75%; DPh-BTBT and N1100 as the semiconductors). The TFTs for the standard-performance (SP) option were fabricated using a SAM mixing ratio of 50%/50% and DNTT and N1100 as the semiconductors, and the TFTs for the high-performance (HP) option were fabricated using a purely fluoroalkyl SAM and DNTT for the p-channel TFT and a SAM mixing ratio of 75%/25% and N1100 for the n-channel TFT, with the goal of obtaining TFTs with more positive or negative threshold voltages and hence larger overdrive voltages and larger drain currents for a particular gate-source voltage. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

$C_{G,p} = 300$ pF and $C_{G,n} = 1.1$ nF. The transconductance is defined as the derivative of the drain current with respect to the gate-source voltage and is obtained numerically from the measured transfer characteristics of the TFTs:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \qquad (9)$$

The transconductance is a function of the gate-source and drain-source voltages applied to the TFTs, so for the purpose of fitting the results to the signal delays of the ring oscillator measured as a function of the supply voltage V_{DD}, the transconductance was calculated at the data points $V_{GS} = V_{DS} = V_{DD}$, although this condition is obviously not fulfilled during the entire duration of the switching events. Other weaknesses of this approach are that it treats the transconductance as a small-signal parameter, even though the voltages in the ring oscillators are obviously large-signal parameters, and that it ignores the load capacitance connected to the output nodes of the inverters.

An alternative approach is to estimate the signal delays $t_{d,LH}$ and $t_{d,HL}$ from the large-signal output resistances of the TFTs (R_{out}) and the inverter's load capacitance (C_L):

$$t_{d,LH} = R_{out,p} C_L; \quad t_{d,HL} = R_{out,n} C_L \qquad (10)$$

$$C_L = C_{G,p} + C_{G,n} = C_{diel}(W_p + W_n)(L + L_{ov,GS} + L_{ov,GD}) \qquad (11)$$

with $C_L = C_{G,p} + C_{G,n} = 1.4$ nF. The output resistance is obtained numerically from the measured output characteristics of the TFTs:

$$R_{out} = \frac{V_{DS}}{I_D} \qquad (12)$$

Unlike the small-signal transconductance in Equation (9), the output resistance in Equation (12) is a large-signal parameter, which better reflects the situation in the circuit. Like the transconductance, the output resistance is also a function of the gate-source and drain-source voltages and thus was also calculated at the data points $V_{DS} = V_{GS} = V_{DD}$. Other weaknesses of this approach are that it treats the output resistance of the TFTs as a linear parameter, which it obviously is not, and that it ignores the Miller effect.

Fits 3 and 4 in Fig. 5c were calculated using Equations (7) and (10), respectively. As can be seen, both are able to qualitatively reproduce the different slopes of the relation between the signal delay and the supply voltage in the subthreshold regime and the above-threshold regime, which arise from the different relations between the drain current and the applied voltages in these regimes (exponential in the subthreshold regime; quadratic in the above-threshold regime).

The signal delays of the ring oscillator in Fig. 5c are very large, e.g., 20 ms per stage at a supply voltage of 1 V and 130 ms per stage at a supply voltage of 0.7 V. One reason for the large signal delays is that the TFTs have very large channel lengths (40 μm) and gate-to-contact overlaps (80 μm); this problem can be alleviated by designing TFTs with micron-scale lateral dimensions [28,39,65]. The other reason is that the difference between the gate-source voltage and the threshold voltage (i.e., the overdrive voltage) and hence the drain current available to charge and discharge the output node is very small at these supply voltages. For example, at a supply voltage of 0.7 V, the overdrive voltage is only about 0.2 V. This problem can be alleviated by shifting the threshold voltage closer to zero or even beyond 0 V, i.e. to positive values for the p-channel TFTs and negative values for the n-channel TFTs. However, this will necessarily lead to larger drain currents at a gate-source voltage of 0 V and thus to larger static currents and larger static power consumption of the circuits. This is the well-known trade-off between power consumption and dynamic performance: All else being equal (carrier mobility, subthreshold slope, lateral device dimensions, etc.), better dynamic performance can be traded for only at the expense of larger power consumption. In silicon microelectronics, this trade-off is addressed by implementing transistors with several different threshold voltages on the same chip, so within the same circuit, the circuit designers can choose between various transistor options, e.g., a low-power (LP) option, a standard-performance (SP) option and a high-performance (HP)

Table 1
Summary of the turn-on voltages and threshold voltages of the TFTs in Fig. 6.

Option	p-channel TFTs				n-channel TFTs			
	SAM mixing ratio	semiconductor	turn-on voltage (V)	threshold voltage (V)	SAM mixing ratio	semiconductor	turn-on voltage (V)	threshold voltage (V)
LP	25%/75%	DPh-BTBT	0.0	−0.5	25%/75%	N1100	0.0	0.4
SP	50%/50%	DNTT	0.2	−0.2	50%/50%	N1100	−0.2	0.2
HP	0%/100%	DNTT	1.2	0.2	75%/25%	N1100	−0.8	−0.2

option [66]. In silicon microelectronics, the different threshold voltages are realized by implanting different dopant densities into the channel region of the transistors. Fig. 6 illustrates that a similar strategy is possible in organic-TFT technology as well, except that the different threshold voltages are implemented here by using different combinations of the semiconductor and the mixing ratio of the gate-dielectric SAM. For example, the TFTs for the SP option in Fig. 6 were fabricated using a SAM mixing ratio of 50% alkyl- and 50% fluoroalkyl-phosphonic acids and using DNTT and N1100 as the semiconductors for the p-channel and n-channel TFTs, so the DNTT TFTs have a turn-on voltage of 0.2 V and a threshold voltage of −0.2 V, and the N1100 TFTs have a turn-on voltage of −0.2 V and a threshold voltage of 0.2 V. The TFTs for the HP option were fabricated using a fluoroalkyl SAM and DNTT for the p-channel TFTs and a SAM mixing ratio of 75%/25% and N1100 for the n-channel TFTs, so the DNTT TFTs have a turn-on voltage of 1.2 V and a threshold voltage of 0.2 V, and the N1100 TFTs have a turn-on voltage of −0.8 V and a threshold voltage of −0.2 V (see also Table 1). As a result of the shifted turn-on voltages, a certain supply voltage will give TFT overdrive voltages that are larger by 0.2−0.3 V for the SP option and by 0.6−0.7 V for the HP option, compared to the LP option (for which the TFTs are the same as in Fig. 3), which would result in significantly smaller signal delays, especially at supply voltages below 1 V. However, the shifted turn-on voltages also mean that the drain currents at a gate-source voltage of 0 V and hence the static power consumption of complementary circuits fabricated using these TFTs are two orders of magnitude larger for the SP option and five orders of magnitude larger for the HP option, compared to the LP option.

5. Outlook

For the TFTs reported here, the subthreshold region extends over approximately three orders of magnitude in drain current, with a slope of about 100 mV/decade. If the subthreshold region extended over five orders of magnitude and had a slope closer to the room-temperature limit of 60 mV/decade, the TFTs would have on/off current ratios of 10^7 or 10^8 over a gate-source-voltage range of 0.5 or 1 V, similar to silicon transistors [66]. For p-channel organic TFTs, this goal is within reach [10,26,61]. For n-channel organic TFTs, further improvements are still required.

Acknowledgements

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