

Control of threshold voltage in low-voltage organic complementary inverter circuits with floating gate structures

Tomoyuki Yokota,¹ Takashi Nakagawa,¹ Tsuyoshi Sekitani,¹ Yoshiaki Noguchi,¹ Kenjiro Fukuda,¹ Ute Zschieschang,² Hagen Klauk,² Ken Takeuchi,¹ Makoto Takamiya,³ Takayasu Sakurai,³ and Takao Someya^{1,a)}

¹Department of Electrical and Electronic Engineering, Department of Applied Physics, The University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan

²Max Planck Institute for Solid State Research, Heisenbergstrasse 1, 70569 Stuttgart, Germany

³Institute of Industrial Science, The University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, Japan

(Received 21 January 2011; accepted 16 April 2011; published online 11 May 2011)

We have demonstrated threshold-voltage control of p- and n-channel organic transistors with a floating-gate structure and self-assembled monolayer-based gate dielectrics and applied this technique to tune the switching voltage of organic complementary inverters. The threshold voltages of the p- and n-channel transistors are changed independently and systematically across a wide range from +2.4 to -1 V and from -0.3 to +1.5 V, respectively, when the program voltages of -6 V and +6 V are applied to the p- and n-channel transistors, respectively. Furthermore, we fabricated tunable organic complementary inverters, and ring oscillators whose oscillations are controlled by varying floating-gate charges. © 2011 American Institute of Physics. [doi:10.1063/1.3589967]

Organic thin-film transistors (TFTs) have recently attracted considerable attention for realizing large-area flexible electronics, such as robotic sensory arrays,¹ e-papers,^{2,3} and radio-frequency identification tags.^{4,5} In order to reduce the power consumption of organic electronics systems, it is important to realize p- and n-channel organic TFTs and complementary circuits⁶ with low operating voltages,⁷ and to be able to control the threshold voltages of the TFTs in a systematic manner. There are several approaches to control the threshold voltage of organic TFTs, such as surface modification of the gate dielectric with a self-assembled monolayer (SAM) having electron-donating or electron-withdrawing substituents⁸⁻¹⁰ and surface modification of the contact metals.¹¹ In these approaches, the threshold voltage of the transistors can be set to a specific value during manufacturing. On the other hand, it is often desirable to control the threshold voltage after manufacturing, since the threshold voltage of organic transistors is known to change inadvertently during operation due to the dc bias-stress effect and air exposure.¹² Previously, the double-gate structure^{13,14} has been used to control the threshold voltage of organic TFTs after manufacturing. However, this structure was impossible in low operational TFTs because the operational voltage was very large.

In this letter, we demonstrate the threshold-voltage control of low-voltage organic TFTs with a floating-gate structure after manufacturing, which allows us to control the behavior of low-voltage organic complementary inverters and ring oscillators during operation. Control of the threshold voltage is achieved by charging the floating gates of the TFTs by applying a program voltage to the control gate.

A floating-gate transistor is a field-effect transistor with two gate electrodes; in addition to the control gate, it has a floating gate embedded in the gate dielectric. When the dielectric is sufficiently thin, electronic charge can be

brought onto the floating gate by quantum tunneling or thermal emission, simply by applying a sufficiently large program voltage between the control gate and the source contact. Charging the floating gate changes the transistor's threshold voltage (V_{th}), because the charge on the floating gate partially screens the electric field between control gate and semiconductor. This V_{th} shift can be detected by measuring the drain current at a certain gate source voltage. Because the floating gate is completely isolated, charge stored on the floating gate remains there without the need for any applied voltage.

In the fabrication process, a 25-nm-thick aluminum (Al) layer was thermally evaporated as the control gate onto a silicon substrate using a shadow mask. As the bottom dielectric, a 4-nm-thick aluminum oxide (AlO_x) layer was formed by oxygen-plasma treatment (300 W for 30 min at 8.45×10^{-3} Pa m^3/s oxygen) and covered with a 2-nm-thick SAM by immersion into a 2-propanol solution containing 5-mM of n-octadecylphosphonic acid for 16 h at room temperature.^{7,14} Subsequently, the floating gate (Al) and the top dielectric (4-nm-thick AlO_x + 2-nm-thick SAM) were created in a similar manner, as described in Ref. 15. Purified pentacene and F_{16}CuPc (Ref. 16) were deposited in vacuum through shadow masks onto the top dielectric to form the 50-nm-thick organic semiconductor layers for the p- and n-channel TFTs, respectively. Finally, a 50-nm-thick Au layer was evaporated through a shadow mask to form the source and drain contacts (Fig. 1(b)).

Figures 2(a)–2(d) show the current–voltage characteristics of pentacene and F_{16}CuPc floating-gate transistors. Each transfer characteristic was measured after a program voltage had been applied to the control gate; note that this program voltage was not present during the measurement.

In Fig. 3, the threshold voltages of the p- and n-channel TFTs are plotted as a function of the program voltage that had been applied to the control gate before the measurement. As can be seen, for program voltages between 0 and -6 V for the p-channel TFTs and between 0 and +6 V for the

^{a)}Author to whom correspondence should be addressed. Electronic mail: someya@ee.t.u-tokyo.ac.jp.

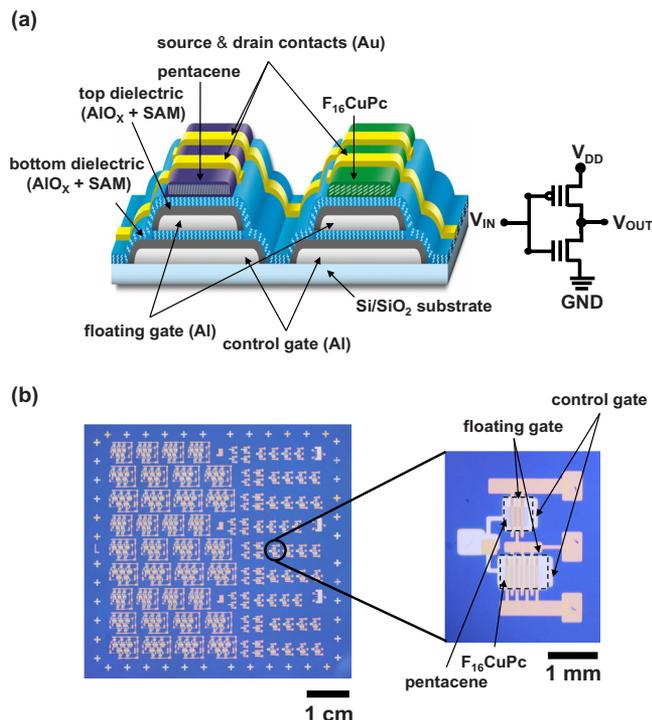


FIG. 1. (Color online) (a) Schematic cross-section and circuit diagram of the floating-gate complementary inverters. The substrate is silicon covered by thermally grown silicon dioxide. (b) Optical microscope images of floating-gate complementary inverters.

n-channel TFTs, the threshold voltages were controlled systematically over a wide range, from +2.4 to -1 V for the p-channel TFTs and from -0.3 to +1.5 V for the n-channel TFTs.

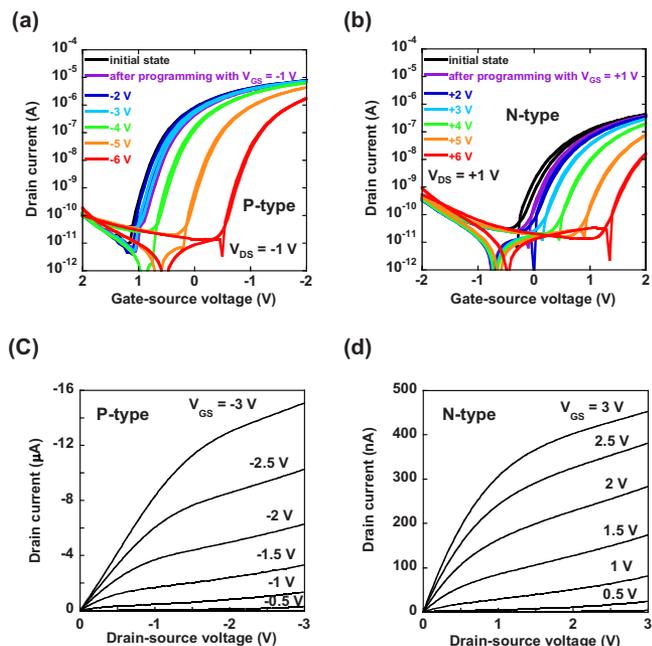


FIG. 2. (Color online) Electrical characteristics of p-channel pentacene and n-channel $F_{16}CuPc$ TFTs with channel length and width of $50 \mu m$ and $3500 \mu m$, respectively. (a) Transfer characteristics of pentacene TFTs recorded after program operations performed with program voltages ranging from -1 to -6 V. The duration of each program pulse was 1 s. (b) Transfer characteristics of $F_{16}CuPc$ TFTs recorded after program operations performed with program voltages ranging from 1 to 6 V. The duration of each program pulse was 1 s. [(c) and (d)] Output characteristics of pentacene and $F_{16}CuPc$ TFTs prior to applying any program voltages.

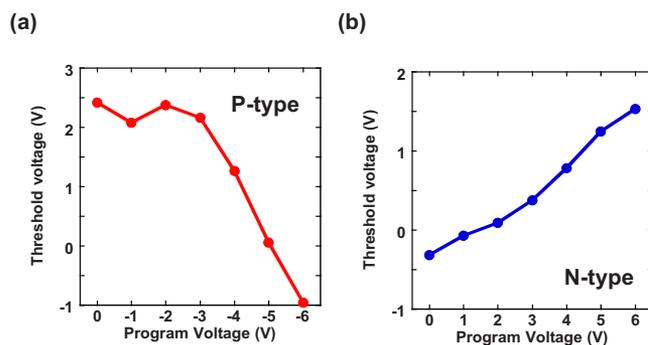


FIG. 3. (Color online) Threshold voltage of the (a) p-channel TFTs and (b) n-channel TFTs as a function of the program voltage applied prior to the measurement for a duration of 1 s.

Figure 4(a) shows the transfer characteristics of a complementary inverter for supply voltages of 1.5, 2.0, 2.5, and 3.0 V. These characteristics were measured before any program voltages that exceed the inverter-input voltage had been applied. The inverter is composed of a pentacene TFT with a channel width of $1000 \mu m$ and a $F_{16}CuPc$ TFT with a channel width of $3000 \mu m$; both TFTs have a channel length of $50 \mu m$. The inverter exhibits a small-signal gain larger than 10 at a supply voltage of 1.5 V.

Figure 4(b) shows the transfer characteristics of the same inverter at a supply voltage of 1.5 V measured after a program voltage had been applied to the input node (i.e., to the control gates of the TFTs). As can be seen, the application of a positive (negative) program voltage causes the threshold voltages of the p- and n-channel TFTs and hence the switching voltage of the inverter to shift systematically toward more positive (negative) voltages. In this way, the switching voltage of the inverter can be shifted across the entire range of input voltages (from 0 to 1.5 V) in a deterministic manner. The small-signal gain is almost constant for program voltages

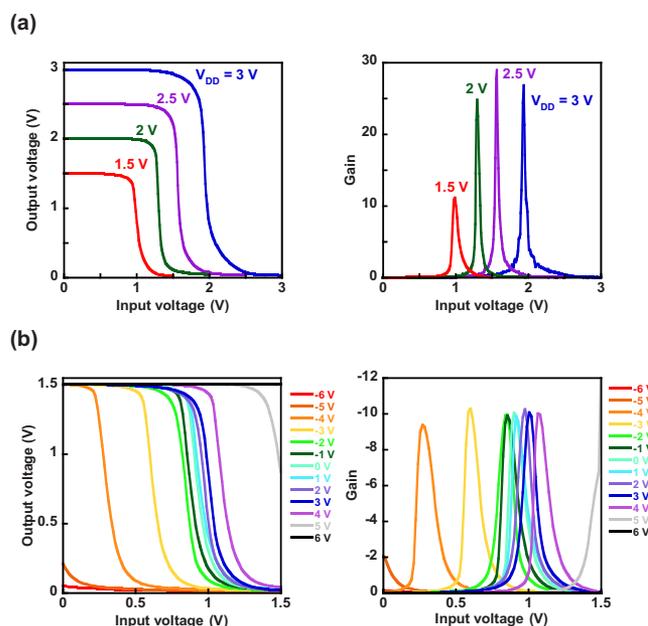


FIG. 4. (Color online) (a) Transfer characteristics of a complementary inverter for supply voltages between 1.5 and 3 V, measured prior to applying any program voltages. (b) Transfer characteristics of the inverter at a supply voltage of 1.5 V measured after program voltages between -6 and +6 V had been applied to the input node for a duration of 1 s. The switching voltage is systematically controlled by the program pulses.

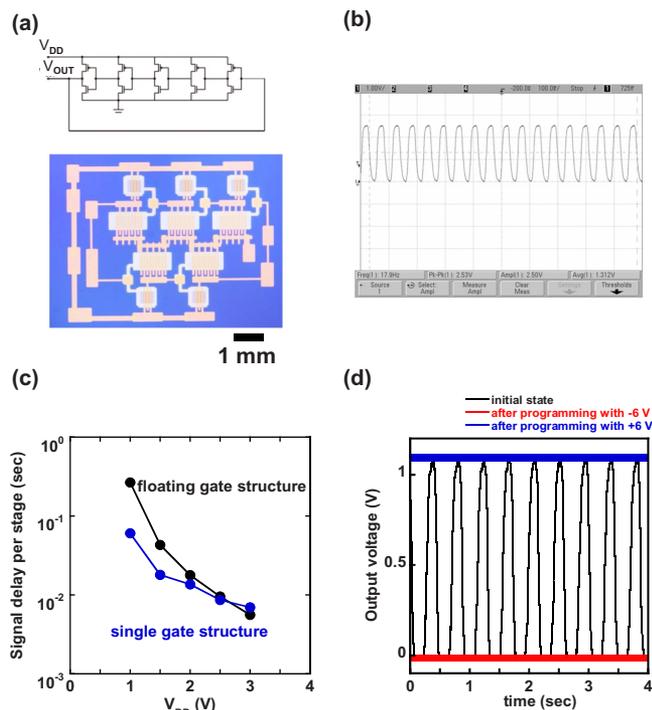


FIG. 5. (Color online) (a) Circuit diagram and optical microscope image of a five-stage complementary ring oscillator. (b) Output signal of the ring oscillator at $V_{DD} = 3$ V. (c) Signal propagation delay as a function of supply voltage. (d) Output signals recorded at V_{DD} of 1.5 V after the application of program voltages of -6 , 0 , and 6 V to the control gates of all TFTs in the ring oscillator for a duration of 1 s.

ages between -4 and $+4$ V. In the extreme cases, i.e., for program voltages of -6 and $+6$ V, the switching voltage is moved outside of the input voltage range, so that the output voltage of the inverter is almost constant at 0 V and 1.5 V, respectively.

We have also fabricated five-stage complementary ring oscillators [Fig. 5(a)]. Figure 5(b) shows the oscillation of the fabricated ring oscillator; the oscillation frequency is 17.9 Hz at a supply voltage V_{DD} of 3 V. Even at a supply voltage as low as 1 V the ring oscillator is still functional, with a frequency of 0.38 Hz. Figure 5(c) shows the signal propagation delay as a function of V_{DD} . Figure 5(d) shows the output signal of the ring oscillator at a supply voltage of 1.5 V measured after we had applied a program voltage to the control gates of all TFTs in the ring oscillator. The oscillator frequency is 2.3 Hz for a program voltage of 0 V. On the other hand, when program voltages of $+6$ V and -6 V are applied, the ring oscillator no longer oscillates, but exhibits constant output voltages of 1.1 V and 0 V, respectively. In this manner, the oscillation frequency is systematically controlled by the program voltage.

In conventional silicon-based floating gate transistors, carrier charging and discharging into floating-gate have been understood as tunneling in which high-energy carriers (hot-carriers) pass through gate dielectric layers, when very high voltages as program voltages are applied to gate and source electrodes. However, carrier densities in organic semiconductors are two or three orders of magnitude smaller than that in silicon semiconductors¹⁷ so that hot-carriers could not be generated in organic semiconductors. On the other hand, we have clearly demonstrated in our previous report a floating-gate embedded in SAM gate dielectric layers are charged and discharged by nonlinear tunneling currents that

was observed when very high voltages (program voltages) are applied. Moreover, our previous work used only p-type organic semiconductors, pentacene, and their charging and discharging into floating-gate rely entirely on hole-tunneling from channel layers.¹⁵ In this work, we clearly demonstrate that tunneling passing through SAM layers is observed not only in p-type, but also in n-type organic semiconductors.

The relationship between the program voltage and the threshold voltage documented in Figs. 2(a) and 2(b) provides some insight into the mechanism by which the threshold voltages responds to the program pulse. Applying a negative program voltage to the control gate [as in Fig. 2(a) for the p-channel TFT] creates a potential gradient across the transistor that reduces the amount of negative charge on the floating gate and thereby makes the threshold voltage more negative. This is consistent with the results of our previous report.¹⁵ In contrast, when a positive program voltage is applied [as in Fig. 2(b) for the n-channel TFT], the amount of negative charge on the floating gate increases, shifting the threshold voltage toward more positive values.

By systematically controlling the threshold voltage of the transistors, the noise margin of the integrated circuits can be increased significantly.^{10,18} In addition to improving the noise immunity of the circuits this also makes them more useful in applications in which the circuits are utilized to re-shape the waveforms of digital signals that have become degraded during signal processing.

This work is partially supported by JST/CREST, Special Coordination Funds for Promoting, and NEDO. One of the authors (T.Y.) is grateful to the research fellowships for young scientists of JSPS.

- ¹Y. Kato, T. Sekitani, Y. Noguchi, T. Yokota, M. Takamiya, T. Sakurai, and T. Someya, *IEEE Trans. Electron Devices* **57**, 995 (2010).
- ²J. A. Rogers, Z. Bao, K. Baldwin, A. Dodabalapur, B. Crone, V. R. Raju, V. Kuck, H. Katz, K. Amundson, J. Ewing, and P. Drzaic, *Proc. Natl. Acad. Sci. U.S.A.* **98**, 4835 (2001).
- ³K. Fujimoto, T. Hiroi, K. Kudo, and M. Nakamura, *Adv. Mater. (Weinheim, Ger.)* **19**, 525 (2007).
- ⁴P. F. Baude, D. A. Ender, M. A. Haase, T. W. Kelley, D. V. Muires, and S. D. Theiss, *Appl. Phys. Lett.* **82**, 3964 (2003).
- ⁵S. Steudel, K. Myny, V. Arkhipov, C. Deibel, and P. Heremans, *Nature Mater.* **4**, 597 (2005).
- ⁶B. Crone, A. Dodabalapur, Y.-Y. Lin, R. W. Filas, Z. Bao, A. LaDuca, R. Sarpeshkar, H. E. Katz, and W. Li, *Nature (London)* **403**, 521 (2000).
- ⁷H. Klauk, U. Zschieschang, J. Pflaum, and M. Halik, *Nature (London)* **445**, 745 (2007).
- ⁸S. Kobayashi, T. Nishikawa, T. Takenobu, S. Mori, T. Shimoda, T. Mitani, H. Shimotani, N. Yoshimoto, S. Ogawa, and Y. Iwasa, *Nature Mater.* **3**, 317 (2004).
- ⁹K. P. Pernstich, S. Haas, D. Oberhoff, C. Goldmann, D. J. Gundlach, B. Batlogg, A. N. Rashid, and G. Schitter, *J. Appl. Phys.* **96**, 6431 (2004).
- ¹⁰U. Zschieschang, F. Ante, M. Schlörholz, M. Schmidt, K. Kern, and H. Klauk, *Adv. Mater. (Weinheim, Ger.)* **22**, 4489 (2010).
- ¹¹M. Kitamura, Y. Kuzumoto, S. Aomori, M. Kamura, J. H. Na, and Y. Arakawa, *Appl. Phys. Lett.* **94**, 083310 (2009).
- ¹²H. Sirringhaus, *Adv. Mater. (Weinheim, Ger.)* **21**, 3859 (2009).
- ¹³K. Hizu, T. Sekitani, T. Someya, and J. Otsuki, *Appl. Phys. Lett.* **90**, 093504 (2007).
- ¹⁴K. Fukuda, T. Yokota, K. Kuribara, T. Sekitani, U. Zschieschang, H. Klauk, and T. Someya, *Appl. Phys. Lett.* **96**, 053302 (2010).
- ¹⁵T. Sekitani, T. Yokota, U. Zschieschang, H. Klauk, S. Bauer, K. Takeuchi, M. Takamiya, T. Sakurai, and T. Someya, *Science* **326**, 1516 (2009).
- ¹⁶Z. Bao, A. J. Lovinger, and J. Brown, *J. Am. Chem. Soc.* **120**, 207 (1998).
- ¹⁷T. Sekitani, Y. Takamatsu, S. Nakano, T. Sakurai, and T. Someya, *Appl. Phys. Lett.* **88**, 253508 (2006).
- ¹⁸S. De Vusser, S. Steudel, K. Myny, J. Genoe, and P. Heremans, *Appl. Phys. Lett.* **88**, 162116 (2006).