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Stencil lithography for organic thin-film transistors with a channel length of 300 nm

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ABSTRACT

For some of the more demanding applications envisioned for organic transistors, lateral device dimensions of less than 1 μm may be necessary or should at least be explored in order to evaluate the scalability of organic transistors. Using stencil lithography based on high-resolution silicon stencil masks and employing two small-molecule organic semiconductors with good long-term air stability, we have fabricated organic p-channel and n-channel transistors with a channel length of 0.3 μm. Owing to the small channel length, the transistors have large channel-width-normalized transconductances (1.5 S/m for the p-channel and 0.2 S/m for the n-channel transistors). In addition, the transistors have steep subthreshold slopes (80 and 200 mV/decade) and large on/off current ratios (10^6).

1. Introduction

Organic thin-film transistors (TFTs) are potentially useful for flexible, large-area electronics applications, such as active-matrix displays [1,2], sensor arrays [3,4] and certain types of signal-processing or communication circuits [5,6]. Some of these systems will benefit from TFTs that are able to switch or amplify electrical signals with frequencies of several tens to a few hundred megahertz at supply voltages of a few volts [7]. Given the general limitations of organic TFTs in terms of charge-carrier mobility, this implies that these TFTs will need to have channel lengths around or below 1 μm [7–9].

Methods for the fabrication of submicron-channel-length TFTs include high-resolution photolithography [7,8,10], electron-beam lithography [11–13], self-aligned inkjet printing [14–16], nanoimprint lithography [17–19], femtosecond laser ablation [20], reverse offset printing [21] and stencil lithography [22]. In stencil lithography, the functional materials are deposited by vacuum evaporation or sublimation through apertures in a set of reusable masks, without the need for resists, solvents, irradiation, mechanical pressure, etching, lift-off or other forms of subtractive patterning [23]. Stencil lithography is one of the preferred methods for the patterning of the organic light-emitting diodes in commercially manufactured active-matrix organic light-emitting diode (AMOLED) displays [24]. Stencil masks for AMOLED manufacturing are typically made of a nickel-iron alloy, and the apertures are usually produced by laser cutting [25]. For the fabrication of organic TFTs with micron or submicron channel lengths, high-resolution silicon-based stencil masks, similar to those developed in the 1990s for ion-projection lithography [26], have been adopted [27–29]. These masks are fabricated by a combination of electron-beam lithography and deep reactive ion etching in thin silicon or silicon nitride membranes [23,30]. Depending on the lateral dimensions and the thickness of the membranes, apertures as small as about 20 nm can be accurately defined [31]. By bringing the stencil mask into sufficiently close contact with the substrate during the material deposition, the extent of lateral blurring on the substrate surface can be reduced to about 0.2 μm [32]. This suggests that the channel length of TFTs fabricated using stencil lithography can be made as small as about 0.2 μm. The smallest organic-TFT channel length demonstrated so far using stencil lithography is 0.5 μm [22,33].

Here we demonstrate the use of stencil lithography based on high-resolution silicon stencil masks with a membrane thickness of 20 μm for the fabrication of p-channel and n-channel organic TFTs with a channel length of 0.3 μm. Despite the small channel length, the TFTs have a small off-state drain current (10 pA), a steep subthreshold slope (80 mV/decade for the p-channel TFTs, 200 mV/decade for the n-channel TFTs), a large on/off current ratio (10^6), and drain-current saturation in the output characteristics. Owing to the small channel length, the TFTs also have a large width-normalized transconductance of 1.5 S/m for the p-channel TFTs and 0.2 S/m for the n-channel TFTs.

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2. Experimental

The TFTs were fabricated in the bottom-gate, top-contact (inverted staggered) device architecture with patterned aluminum gate electrodes. The submicron-channel-length TFTs were fabricated on silicon substrates coated with a thick layer of silicon dioxide. For comparison, we also fabricated long-channel TFTs on 125-μm-thick flexible polyethylene naphthalate substrates (Teonex® Q65 PEN; kindly provided by William A. MacDonald, DuPont Teijin Films, Wilton, U.K.). In the first process step, the aluminum gate electrodes were deposited by thermal evaporation in vacuum through the first stencil mask. The aluminum has a thickness of 30 nm and a root-mean-square surface roughness of 1 nm, measured by atomic force microscopy. The gate dielectric is a combination of a thin layer of aluminum oxide (AlO_x) and a self-assembled monolayer (SAM) of either an alkylphosphonic acid (for the p-channel TFTs) or a fluoroalkylphosphonic acid (for the n-channel TFTs) [33]. The AlO_x layer was produced by briefly exposing the substrate to an oxygen plasma. To allow a high-quality SAM to form on the AlO_x layer, the substrate was then immersed into a solution of *n*-tetradecylphosphonic acid (PCI Synthesis, Newburyport, MA, U.S.A.) or 12,12,13,13,14,14,15,15, 16,16,17,17,18,18,18-pentadecafluoro-octadecylphosphonic acid (synthesized by Matthias Schlörholz, Heidelberg, Germany) in 2-propanol [33]. Depending on the SAM, the AlO_x/SAM gate dielectric has a thickness of 5.3 nm (tetradecylphosphonic acid) or 5.7 nm (pentadecafluoro-octadecylphosphonic acid) and a unit-area capacitance of 700 nF/cm^2 or 600 nF/cm^2, respectively [33]. As the semiconductor, we deposited a 25-nm-thick layer of dinaphtho[2,3-b:2′,3′-f]thieno [3,2-b]thiophene (DNTT; Sigma Aldrich) for the p-channel TFTs and a 12-nm-thick layer of N,N′-bis(2,2,3,3,4,4,4-heptafluorobutyl)-1,7-dicyano-perylene-(3,4:9,10)-tetracarboxylic diimide ($PTCDI\text{-}(CN)_2\text{-}(CH_2C_3F_7)_2$; ActivInk™ N1100; Polyera Corp., Skokie, IL, U.S.A.) for the n-channel TFTs by sublimation in vacuum through two other stencil masks. During the semiconductor depositions, the substrate was held at a temperature of 60 °C (DNTT) or 140 °C (N1100) [33]. Finally, a 30-nm-thick layer of gold was deposited through another mask to define the source and drain contacts. The vacuum depositions were performed at a background pressure of 10^{-6} mbar with a rate of 2 nm/s for aluminum and 0.03 nm/s for the semiconductors and for gold. During the metal depositions, the substrate was at room temperature. The masks were aligned manually under an optical microscope and fixed onto the substrate holder using metal clamps. All electrical measurements were performed in ambient air at room temperature using a manual probe station and an Agilent 4156C Semiconductor Parameter Analyzer. The effective charge-carrier mobility was calculated at each point along the measured transfer curve using Equation 2 in Ref. [34]. A schematic cross-section of the TFTs and the chemical structures of the organic semiconductors and of the alkyl- and fluoroalkyl-phosphonic acids are shown in Fig. 1.

3. Long-channel TFTs

Fig. 2 shows the measured output and transfer characteristics of long-channel DNTT p-channel and N1100 n-channel TFTs fabricated on a flexible PEN substrate. These TFTs have a channel length of 30 or 40 μm. The DNTT TFT has an effective charge-carrier mobility of 2.4 cm^2/Vs, a threshold voltage of −0.8 V, an on/off current ratio of 10^8, a subthreshold slope of 75 mV/decade, and a channel-width-normalized transconductance of 0.06 S/m. The N1100 TFT has an effective mobility of 0.3 cm^2/Vs, a threshold voltage of 0.6 V, an on/off current ratio of 10^8, a subthreshold slope of 100 mV/decade, and a channel-width-normalized transconductance of 0.008 S/m.

One advantage of DNTT and N1100 over many other organic semiconductors is their excellent air stability [35–37]. This is demonstrated in Fig. 3 where the transfer curves of the TFTs from Fig. 2 that were measured immediately after device fabrication are compared to the transfer curves of the same TFTs measured a little more than a year later, during which time the TFTs had been continuously exposed to ambient air with a relative humidity of 30–60%. As can be seen, the threshold voltage and the subthreshold slope of the DNTT TFT and the subthreshold slope of the N1100 TFT are unchanged. The threshold voltage of the N1100 TFT has shifted by 200 mV towards more positive values. The reason for this threshold-voltage shift is unknown, although previous work suggests that it is not related to the air exposure, as a similar shift was found to also occur during storage in dry nitrogen [38]. The carrier mobility of both TFTs is still more than 50% of the initial mobility, which is notably better compared to many other organic semiconductors (see, for example, Fig. 5 in Ref. [39]).

4. Submicron-channel-length TFTs

As mentioned in the Introduction, for some applications of organic TFTs it may be beneficial if the TFTs have a channel length of less than 1 μm. Fig. 4 shows a photograph and a scanning electron microscopy (SEM) image of a TFT fabricated by stencil lithography that has a channel length of 0.3 μm, gate-to-source and gate-to-drain overlaps of 20 μm and a channel width of 5 μm, along with the measured output and transfer characteristics of DNTT and N1100 TFTs with these dimensions. Owing to the small thickness of the gate dielectric compared to the channel length [40], the desirable saturation of the drain current at large drain-source voltages is observed in the output characteristics (Fig. 4c). The DNTT TFT has an effective carrier mobility of 0.3 cm^2/Vs, a threshold voltage of −1.4 V, an on/off current ratio of 10^6, a subthreshold slope of 80 mV/decade, and a channel-width-normalized transconductance of 1.5 S/m. The N1100 TFT has an effective mobility of 0.06 cm^2/Vs, a threshold voltage of 1.3 V, an on/off current ratio of 10^6, a subthreshold slope of 200 mV/decade, and a channel-width-normalized transconductance of 0.2 S/m. These parameters are summarized in Table 1.

The subthreshold slopes of 80 and 200 mV/decade are to our knowledge the steepest subthreshold slopes reported to date for

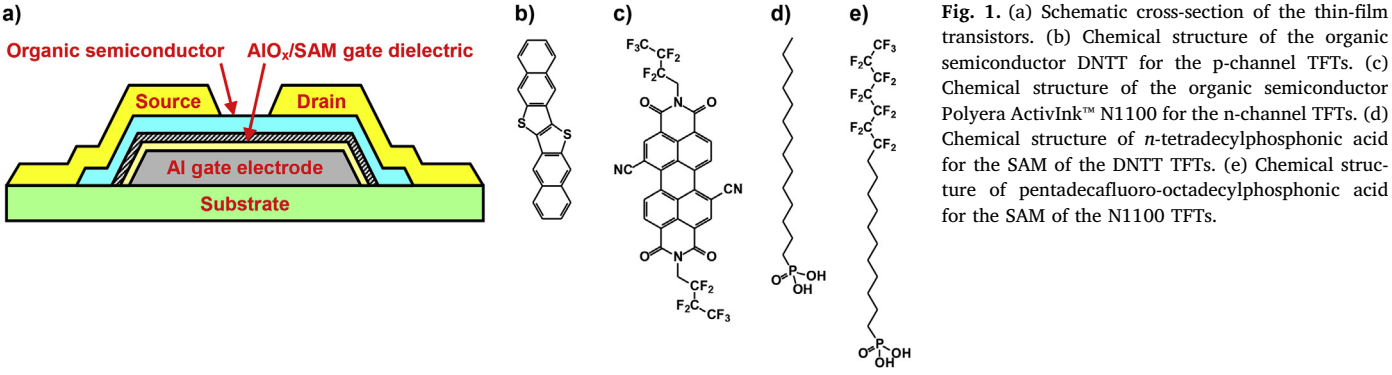

Fig. 1. (a) Schematic cross-section of the thin-film transistors. (b) Chemical structure of the organic semiconductor DNTT for the p-channel TFTs. (c) Chemical structure of the organic semiconductor Polyera ActivInk™ N1100 for the n-channel TFTs. (d) Chemical structure of *n*-tetradecylphosphonic acid for the SAM of the DNTT TFTs. (e) Chemical structure of pentadecafluoro-octadecylphosphonic acid for the SAM of the N1100 TFTs.

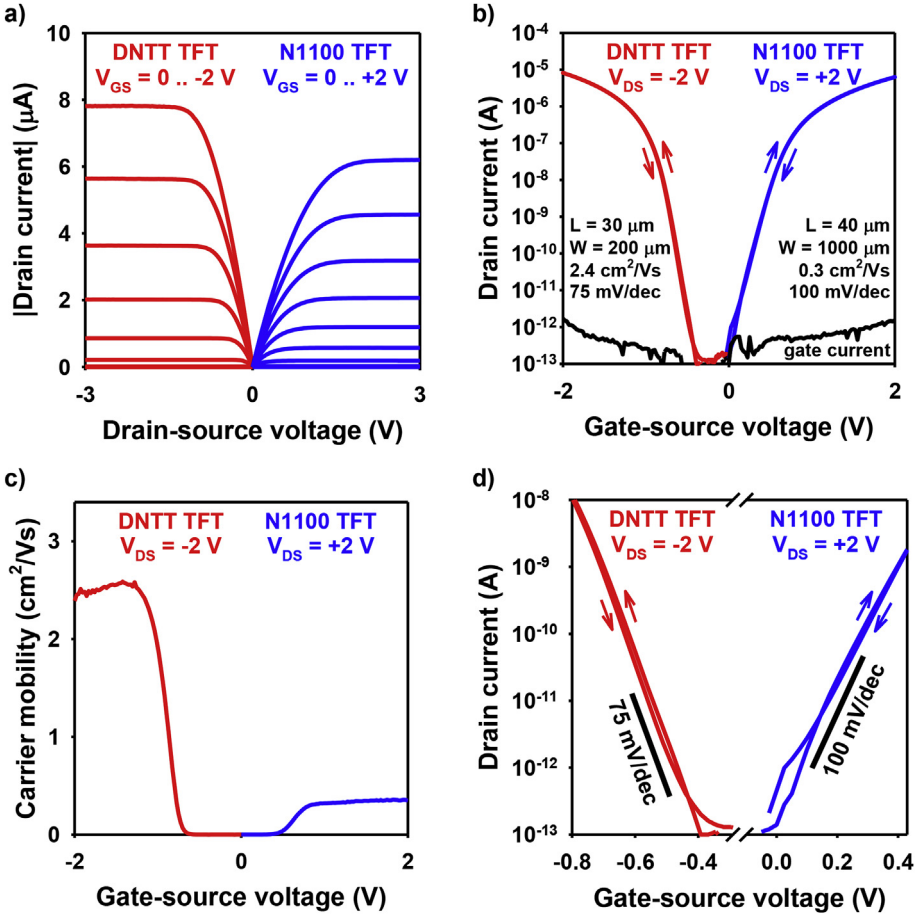

Fig. 2. (a) Output characteristics (b) and transfer characteristics of long-channel DNTT p-channel and N1100 n-channel TFTs fabricated on a flexible PEN substrate. (c) Charge-carrier mobility plotted as a function of the gate-source voltage. (d) Subthreshold region.

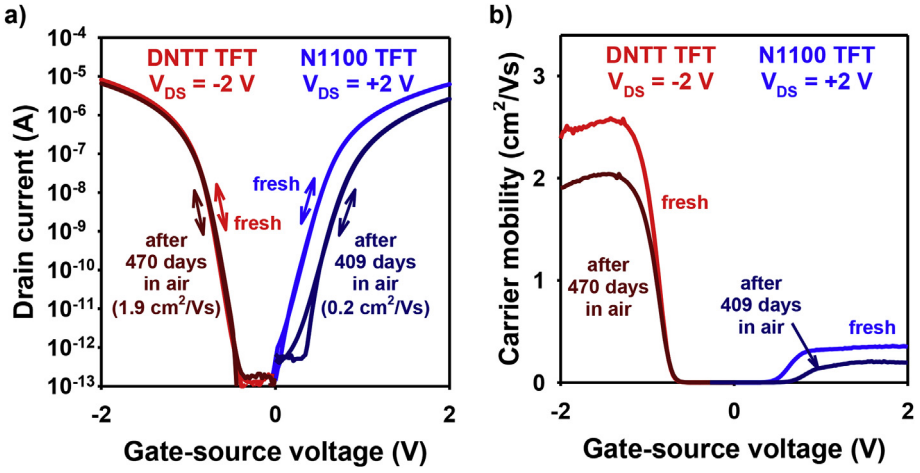

Fig. 3. Shelf-life stability of long-channel DNTT p-channel and N1100 n-channel TFTs. (a) Transfer characteristics measured after device fabrication and a little more than a year later. (b) Charge-carrier mobility plotted as a function of the gate-source voltage.

submicron p-channel and n-channel organic TFTs, respectively. The channel-width-normalized transconductances of 1.5 S/m and 0.2 S/m are to our knowledge the largest width-normalized transconductances reported to date for p-channel and n-channel organic field-effect transistors, respectively. For comparison, a transconductance of 25 S/m has been reported for inorganic metal-oxide TFTs [8], a transconductance of 400 S/m has been reported for organic electrochemical transistors [41], and state-of-the-art silicon MOSFETs have a transconductance of 6000 S/m [42]. The transconductance is important, as it is one of only two parameters that determine the transit frequency of a field-effect transistor, the other being the gate capacitance [7,8]. The gate capacitance depends on the gate-to-source and gate-to-drain overlaps, which are 20 μm for the TFTs in Fig. 4, but which can be made as small as 2 μm using stencil lithography [22]. A TFT with a channel length of 0.3 μm, gate-to-source and gate-to-drain overlaps of 2 μm and a unit-area gate-dielectric capacitance of 700 nF/cm^2 would have a width-normalized gate capacitance of 30 fF/μm. The theoretical transit frequency of a TFT with this gate capacitance and a transconductance of 1.5 S/m (which is

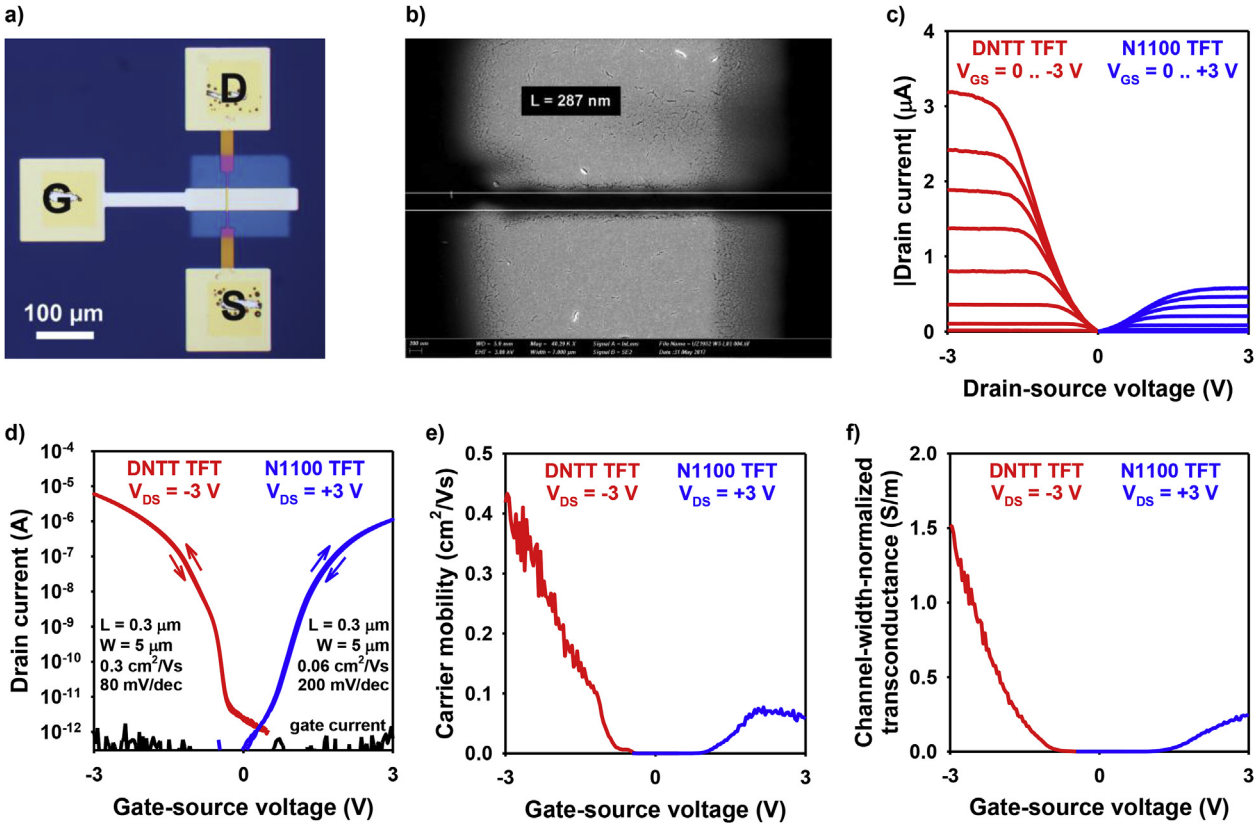

Fig. 4. (a) Photograph and (b) SEM image of a TFT with a channel length of 0.3 µm, gate-to-source and gate-to-drain overlaps of 20 µm and a channel width of 5 µm fabricated by stencil lithography. (c) Output and (d) transfer characteristics of DNTT p-channel and N1100 n-channel TFTs with these dimensions. (e) Charge-carrier mobility and (f) channel-width-normalized transconductance plotted as a function of the gate-source voltage.

Table 1
Summary of the electrical parameters of the TFTs with a channel length of 0.3 µm and a channel width of 5 µm.

	DNTT p-channel TFTs	N1100 n-channel TFTs
effective carrier mobility (cm^2/Vs)	0.3	0.06
threshold voltage (V)	−1.4	1.3
on/off current ratio	10^6	10^6
subthreshold slope (mV/decade)	80	200
width-normalized transconductance (S/m)	1.5	0.2

the transconductance of the DNTT TFT in Fig. 4) is 7 MHz, which would be a factor of two larger than the highest transit frequency reported to date for organic TFTs operated with the same voltage (3 V) [43], but 20 times smaller than the transit frequency of flexible metal-oxide TFTs with similar dimensions operated with a similar voltage [7,8]. This large difference in transit frequency is mainly due the large difference in the contact resistance, which is about three orders of magnitude larger in the organic TFTs [33] than in the metal-oxide TFTs in Refs. [7] and [8]. This clearly shows that the focus of future work needs to be on a better understanding and on a further reduction of the contact resistance of organic TFTs [44].

5. Conclusions

We have used stencil lithography based on high-resolution silicon stencil masks to fabricate p-channel and n-channel organic TFTs with a channel length of 0.3 µm. The TFTs have a small off-state drain current (10 pA), a steep subthreshold slope (80 mV/decade for the p-channel TFTs, 200 mV/decade for the n-channel TFTs), a large on/off current ratio (10^6) and a large width-normalized transconductance (1.5 S/m for the p-channel TFTs, 0.2 S/m for the n-channel TFTs). These results demonstrate the potential of stencil lithography for the fabrication of organic TFTs with submicron dimensions.

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References

[1] M. Mizukami, S.-I. Cho, K. Watanabe, M. Abiko, Y. Suzuri, S. Tokito, J. Kido, Flexible organic light-emitting diode displays driven by inkjet-printed high-mobility organic thin-film transistors, IEEE Electron. Device Lett. 39 (2018) 39.
[2] J.S. Kim, C.K. Song, AMOLED panel driven by OTFTs on polyethylene fabric substrate, Org. Electron. 30 (2016) 45.
[3] T. Yokota, T. Sekitani, T. Tokuhara, N. Take, U. Zschieschang, H. Klauk, K. Takimiya, T.C. Huang, M. Takamiya, T. Sakurai, T. Someya, Sheet-type flexible organic active matrix amplifier system using pseudo-CMOS circuits with floating-gate structure, IEEE Trans. Electron. Dev. 59 (2012) 3434.
[4] X. Ren, K. Pei, B. Peng, Z. Zhang, Z. Wang, X. Wang, P.K.L. Chan, A low-operating-power and flexible active-matrix organic-transistor temperature-sensor array, Adv. Mater. 28 (2016) 4832.
[5] D. Raiteri, P. van Lieshout, A. van Roermund, E. Cantatore, Positive-feedback level shifter logic for large-area electronics, IEEE J. Solid State Circ. 49 (2014) 524.
[6] K. Myny, M. Rockele, A. Chasin, D.V. Pham, J. Steiger, S. Botnaras, D. Weber, B. Herold, J. Ficker, B. van der Putten, G.H. Gelinck, J. Genoe, W. Dehaene, P. Heremans, Bidirectional communication in an HF hybrid organic/solution-processed metal-oxide RFID tag, IEEE Trans. Electron. Dev. 61 (2014) 2387.
[7] N. Münzenrieder, L. Petti, C. Zysset, T. Kinkeldei, G.A. Salvatore, G. Tröster, Flexible self-aligned amorphous InGaZnO thin-film transistors with submicrometer channel length and a transit frequency of 135 MHz, IEEE Trans. Electron. Dev. 60 (2013) 2815.
[8] N. Münzenrieder, G.A. Salvatore, L. Petti, C. Zysset, L. Büthe, C. Vogt, G. Cantarella, G. Tröster, Contact resistance and overlapping capacitance in flexible sub-micron

long oxide thin-film transistors for above 100MHz operation, Appl. Phys. Lett. 105 (2014) 263504.
[9] A. Risteska, K. Myny, S. Steudel, M. Nakamura, D. Knipp, Scaling limits of organic digital circuits, Org. Electron. 15 (2014) 461.
[10] M.-H. Wu, H.-C. Lin, H.-C. Lin, H.-W. Zan, H.-F. Meng, T.-Y. Huang, Submicron organic thin-film transistors fabricated by film profile engineering method, Appl. Phys. Lett. 105 (2014) 043304.
[11] K. Tsukagoshi, K. Shigeto, I. Yagi, Y. Aoyagi, Interface modification of a pentacene field-effect transistor with a submicron channel, Appl. Phys. Lett. 89 (2006) 113507.
[12] F. Ante, D. Kälblein, U. Zschieschang, T.W. Canzler, A. Werner, K. Takimiya, M. Ikeda, T. Sekitani, T. Someya, H. Klauk, Contact doping and ultrathin gate dielectrics for nanoscale organic thin-film transistors, Small 7 (2011) 1186.
[13] T.V.A.G. de Oliveira, A. Eleta, L.E. Hueso, A.M. Bittner, Mixed self-assembled monolayer gate dielectrics for low-voltage solution-processed polymer field-effect transistors, J. Mater. Chem. C 3 (2015) 1181.
[14] C.W. Sele, T. von Werne, R.H. Friend, H. Sirringhaus, Lithography-free, self-aligned inkjet printing with sub-hundred-nanometer resolution, Adv. Mater. 17 (2005) 997.
[15] Y.Y. Noh, N. Zhao, M. Caironi, H. Sirringhaus, Downscaling of self-aligned, all-printed polymer thin-film transistors, Nat. Nanotechnol. 2 (2007) 784.
[16] E. Gili, M. Caironi, H. Sirringhaus, Organic integrated complementary inverters with ink-jet printed source/drain electrodes and sub-micron channels, Appl. Phys. Lett. 100 (2012) 123303.
[17] C. Auner, U. Palfinger, H. Gold, J. Kraxner, A. Haase, T. Haber, M. Sezen, W. Grogger, G. Jakopic, J.R. Krenn, G. Leising, B. Stadlober, Residue-free room temperature UV-nanoimprinting of submicron organic thin film transistors, Org. Electron. 10 (2009) 1466.
[18] F. Zanella, N. Marjanovic, R. Ferrini, H. Gold, A. Haase, A. Fian, B. Stadlober, R. Müller, J. Genoe, H. Hirshy, A. Drost, M. König, K.D. Lee, J. Ring, R. Pretot, C.C. Enz, J.M. Sallese, Design and modeling of self-aligned nano-imprinted sub-micrometer pentacene-based organic thin-film transistors, Org. Electron. 14 (2013) 2756.
[19] S.G. Higgins, B.V.O. Muir, G. Dell'Erba, A. Perinot, M. Caironi, A.J. Campbell, Self-aligned organic field-effect transistors on plastic with picofarad overlap capacitances and megahertz operating frequencies, Appl. Phys. Lett. 108 (2016) 023302.
[20] S.G. Bucella, G. Nava, K.C. Vishunubhatla, M. Caironi, High-resolution direct-writing of metallic electrodes on flexible substrates for high performance organic field effect transistors, Org. Electron. 14 (2013) 2249.
[21] K. Fukuda, Y. Yoshimura, T. Okamoto, Y. Takeda, D. Kumaki, Y. Katayama, S. Tokito, Reverse-offset printing optimized for scalable organic thin-film transistors with submicrometer channel lengths, Adv. Electron. Mater 1 (2015) 1500145.
[22] U. Zschieschang, F. Letzkus, J.N. Burghartz, H. Klauk, Parameter uniformity of submicron-channel-Length organic thin-film transistors fabricated by stencil lithography, IEEE Trans. Nanotechnol. 16 (2017) 837.
[23] J. Brugger, J.W. Berenschot, S. Kuiper, W. Nijdam, B. Otter, M. Elwenspoek, Resistless patterning of sub-micron structures by evaporation through nanostencils, Microelectron. Eng. 53 (2000) 403.
[24] S.-K. Hong, J.-H. Sim, I.-G. Seo, K.-C. Kim, S.-I. Bae, H.-Y. Lee, N.-Y. Lee, J. Jang, New pixel design on emitting area for high resolution active-matrix organic light-emitting diode displays, J. Disp. Technol. 6 (2010) 601.
[25] T.A. Mai, B. Richerzhagen, Manufacturing of 4th generation OLED masks with the laser MicroJet technology, Society for Information Display Int'l Symp. Digest Techn. Papers, 2007, p. 1596.
[26] J. Melngailis, A.A. Mondelli, I.L. Berry III, R. Mohondroa, A review of ion projection lithography, J. Vac. Sci. Technol. B 16 (1998) 927.
[27] F.D. Fleischli, K. Sidler, M. Schaer, V. Savu, J. Brugger, L. Zuppiroli, The effects of channel length and film microstructure on the performance of pentacene transistors, Org. Electron. 12 (2011) 336.
[28] T. Zaki, F. Ante, U. Zschieschang, J. Butschke, F. Letzkus, H. Richter, H. Klauk, J.N. Burghartz, A 3.3 V 6-bit 100 kS/s current-steering digital-to-analog converter using organic p-type thin-film transistors on glass, IEEE J. Solid State Circ. 47 (2012) 292.
[29] U. Zschieschang, R. Hofmockel, R. Rödel, U. Kraft, M.J. Kang, K. Takimiya, T. Zaki, F. Letzkus, J. Butschke, H. Richter, J.N. Burghartz, H. Klauk, Megahertz operation of flexible low-voltage organic thin-film transistors, Org. Electron. 14 (2013) 1516.
[30] F. Letzkus, J. Butschke, B. Höfflinger, M. Irmscher, C. Reuter, R. Springer, A. Ehrmann, J. Mathuni, Dry etch improvements in the SOI wafer flow process for IPL stencil mask fabrication, Microelectron. Eng. 53 (2000) 609.
[31] V. Flauraud, T.S. van Zanten, M. Mivelle, C. Manzo, M.F.G. Parajo, J. Brugger, Large-Scale arrays of bowtie nanoaperture antennas for nanoscale dynamics in living cell membranes, Nano Lett. 15 (2015) 4176.
[32] O. Vazquez-Mena, L.G. Villanueva, V. Savu, K. Sidler, P. Langlet, J. Brugger, Analysis of the blurring in stencil lithography, Nanotechnology 20 (2009) 415303.
[33] U. Kraft, M. Sejfic, M.J. Kang, K. Takimiya, T. Zaki, F. Letzkus, J.N. Burghartz, E. Weber, H. Klauk, Flexible low-voltage organic complementary circuits: finding the optimum combination of semiconductors and monolayer gate dielectrics, Adv. Mater. 27 (2015) 207.
[34] H.H. Choi, K. Cho, C.D. Frisbie, H. Sirringhaus, V. Podzorov, Critical assessment of charge mobility extraction in FETs, Nat. Mater. 17 (2018) 2.
[35] B.A. Jones, A. Facchetti, M.R. Wasielewski, T.J. Marks, Tuning orbital energetics in arylene diimide semiconductors. Materials design for ambient stability of n-type charge transport, J. Am. Chem. Soc. 129 (2007) 15259.
[36] T. Yamamoto, K. Takimiya, Facile synthesis of highly π-extended heteroarenes, dinaphtho[2,3-b:2',3'-f]chalcogenopheno[3,2-b]chalcogenophenes, and their application to field-effect transistors, J. Am. Chem. Soc. 129 (2007) 2224.
[37] U. Zschieschang, H. Klauk, Low-voltage organic transistors with steep subthreshold slope fabricated on commercially available paper, Org. Electron. 25 (2015) 340.
[38] U. Zschieschang, K. Amsharov, M. Jansen, K. Kern, H. Klauk, R.T. Weitz, Separating the impact of oxygen and water on the long-term stability of n-channel perylene diimide thin-film transistors, Org. Electron. 26 (2015) 340.
[39] E.D. Glowacki, M. Irimia-Vladu, M. Kaltenbrunner, J. Gasiorowski, M.S. White, U. Monkowius, G. Romanazzi, G.P. Suranna, P. Mastrorilli, T. Sekitani, S. Bauer, T. Someya, L. Torsi, N.S. Sariciftci, Hydrogen-bonded semiconducting pigments for air-stable field-effect transistors, Adv. Mater. 25 (2013) 1563.
[40] J.N. Haddock, X. Zhang, S. Zheng, Q. Zhang, S.R. Marder, B. Kippelen, A comprehensive study of short channel effects in organic field-effect transistors, Org. Electron. 7 (2006) 45.
[41] D. Khodagholy, J. Rivnay, M. Sessolo, M. Gurfinkel, P. Leleux, L.H. Jimison, E. Stavrinidou, T. Herve, S. Sanaur, R.M. Owens, G.G. Malliaras, High transconductance organic electrochemical transistors, Nat. Commun. 4 (2013) 2133.
[42] C. Auth, et al., A 10nm High Performance and Low-power CMOS Technology Featuring 3rd Generation FinFET Transistors, Self-aligned Quad Patterning, Contact over Active Gate and Cobalt Local Interconnects, International Electron Device Meeting (IEDM), San Francisco, 2017 December 2017.
[43] T. Zaki, R. Rödel, F. Letzkus, H. Richter, U. Zschieschang, H. Klauk, J.N. Burghartz, S-parameter characterization of submicrometer low-voltage organic thin-film transistors, IEEE Electron. Device Lett. 34 (2013) 520.
[44] A. Yamamura, S. Watanabe, M. Uno, M. Mitani, C. Mitsui, J. Tsurumi, N. Isahaya, Y. Kanaoka, T. Okamoto, J. Takeya, Wafer-scale, layer-controlled organic single crystals for high-speed circuit operation, Sci. Adv 4 (2018) eaao5758.