Organic Electronics 14 (2013) 1318–1322

Contents lists available at SciVerse ScienceDirect

Organic Electronics

journal homepage: www.elsevier.com/locate/orgel

Letter

AC characterization of organic thin-film transistors with asymmetric gate-to-source and gate-to-drain overlaps

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ARTICLE INFO

Article history:
Received 14 December 2012
Received in revised form 15 February 2013
Accepted 16 February 2013
Available online 4 March 2013

Keywords:
Organic thin-film transistors
Scattering parameters
Small-signal model

ABSTRACT

This paper presents S-parameter characterization and a corresponding physics-based small-signal equivalent circuit for organic thin-film transistors (OTFTs). Furthermore, the impact of misalignment between the source/drain contacts and the patterned gate on the dynamic TFT performance is explored and a simple method to estimate the misalignment from the measured S-parameters is proposed. An excellent fit between theoretical and experimental S-parameters is demonstrated. For this study, OTFTs based on the air-stable organic semiconductor dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) having a channel length of 1 μm and a gate-to-contact overlap of 5 or 20 μm and being operated at a supply voltage of 3 V are utilized. The intentional asymmetry between gate-to-source and gate-to-drain overlaps is precisely controlled by the use of high-resolution silicon stencil masks.

1. Introduction

Owing to the low-temperature and large-area manufacturability of organic thin-film transistors (OTFTs), they offer promising virtues in thin, light-weight and mechanically-flexible applications. Recent reports have indicated the possibility to realize OTFT-based complex analog front-end and digital back-end circuits, e.g. signal amplifiers [1], analog-to-digital converters [2], digital-to-analog converters [3] and digital processors [4]. Regardless of the device structure (staggered or coplanar) and the fabrication process (printing or vacuum evaporation), the usual lack of a self-alignment process typically necessitates the design of non-negligible overlaps between the source/drain contacts and the gate electrode [5]. Since these overlaps affect the static and/or dynamic TFT characteristics, we present here a physics-based small-signal model that includes these contact effects. The model is verified with scattering (S) parameter characteristics of an OTFT having a channel length of 1 μm and a gate overlap of 20 μm [6], and excellent agreement between theoretical and experimental results is achieved. Unlike other user-configured methods that directly measure gate and drain modulation currents [7,8], the use of a self-contained method in this work by measuring S-parameters is superior, since it only requires a vector network analyzer (VNA) to characterize the entire ac electrical properties of the OTFTs. This simple and accurate approach is well suited for wafer probing systems since it is very fast and is performed at relatively low frequencies (100 kHz–5 MHz) [9]. Furthermore, the limited alignment capabilities of most OTFT technologies make it very difficult to avoid mismatch between the gate-to-source and gate-to-drain overlaps, which has a direct influence on the device performance and is particularly detrimental for OTFTs with small feature sizes. Therefore,

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http://dx.doi.org/10.1016/j.orgel.2013.02.014

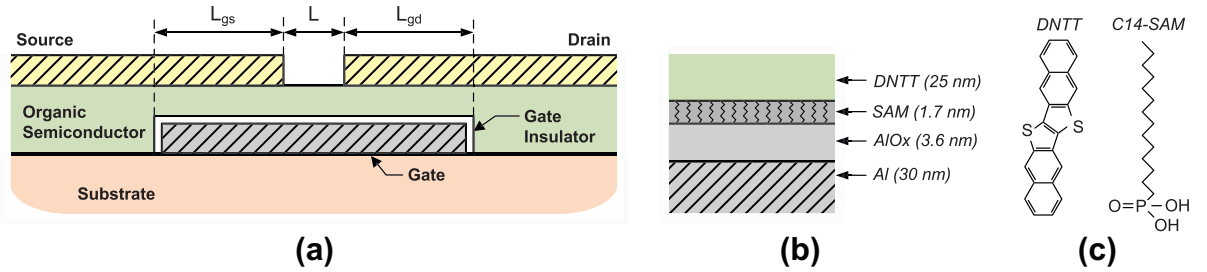

Fig. 1. (a) Cross-sectional view of a staggered (bottom-gate, top-contact) OTFT with a channel length (L), gate-to-source overlap (L_{gs}) and gate-to-drain overlap (L_{gd}). Note that for symmetrical transistors: $L_{gs} = L_{gd} = L_{ov}$. (b) Magnification of the hybrid gate insulator between the bottom-gate (Al) and the semiconductor (DNTT) layers. The insulator is comprised of a 3.6-nm-thick AlO_x layer and a 1.7-nm-thick tetradecylphosphonic acid self-assembled monolayer (SAM). (c) Molecular structures of DNTT and tetradecylphosphonic acid.

a detailed frequency analysis of aggressively scaled asymmetric OTFTs that have a channel length of 1 μm and a gate-to-source overlap of 1,2,...,7 μm (while maintaining a total gate-to-contact overlap of 10 μm) are presented. This study is useful for process corner simulations and we propose a very simple method to estimate the actual misalignment from the measured S-parameters. Such small features and precise determination of the misalignment are enabled by using an OTFT process that is based on high-resolution silicon stencil masks to fabricate low-voltage (3 V), inverted-staggered (bottom-gate, top-contact) OTFTs [10,11].

2. OTFT fabrication

A set of four high-resolution silicon stencil masks are used to fabricate fully patterned OTFTs on a glass substrate. Referring to Fig. 1, 30-nm-thick gold interconnects (required for electrical probing; not shown in the figure), 30-nm-thick aluminum gate electrodes, a 20-nm-thick organic semiconductor layer (air-stable dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene; DNTT), and 25-nm-thick gold source/drain contacts are all deposited in vacuum through the stencil masks. The gate dielectric is a combination of a 3.6-nm-thick oxygen-plasma-grown AlO_x layer and a 1.7-nm-thick solution-processed tetradecylphosphonic acid self-assembled monolayer (SAM) [10,11]. The capacitance of the hybrid gate dielectric per unit area (C_i) is about 900 nF cm^{-2}, allowing the OTFTs to operate at low supply voltages ($\leqslant$3 V). Photographs of the complete OTFT substrate and of the stencil mask used to pattern the source/drain contacts are shown in Fig. 2. The OTFTs have a channel width (W) of 100 μm, a channel length (L) of 1 μm, and a gate-to-contact overlap (L_{ov}) of 5 or 20 μm. To study the effect of asymmetry between the gate-to-source (L_{gs}) and gate-to-drain (L_{gd}) overlaps, where $L_{gs} + L_{gd} = 2\ L_{ov}$, the OTFT with L_{ov} = 5 μm is duplicated and intentionally misaligned on the mask level in order to realize OTFTs with well-defined L_{gs} = 1,2,...,7 μm, while keeping $L_{gs} + L_{gd}$ = 10 μm. Vernier structures are employed to measure the particular degree of misalignment.

3. OTFT modeling and characterization

Fig. 3 shows a physics-based OTFT small-signal equivalent circuit depicting both intrinsic and extrinsic

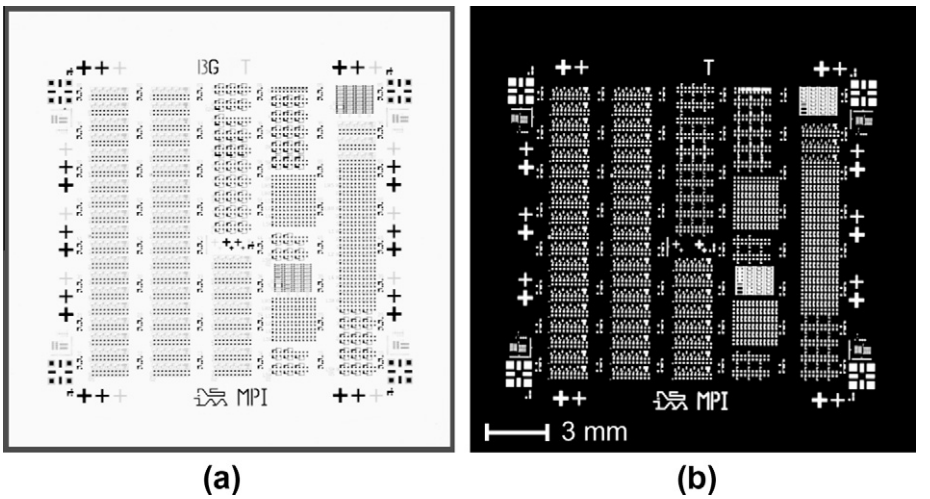

Fig. 2. Photographs of: (a) an OTFT chip fabricated on a glass substrate, (b) the stencil mask employed to pattern the gold source/drain contacts.

components (adopted from [8]). For simplicity the gate leakage current and the very small ohmic resistances resulting from the three conductive terminals are neglected in the model. The intrinsic part is composed of gate-to-source and gate-to-drain overlap capacitances (C_{gs},C_{gd}), output resistance (r_o) and transconductance (g_m). Although the use of fully patterned OTFTs minimizes the overlap capacitances, the usual lack of a self-alignment process for OTFTs makes these overlap capacitances inevitable. According to the experimental measurements presented in [12], the OTFT overlap capacitances at each terminal are found at the bias of interest (saturation regime) to be:

$$C_{gs} = WL_{gs}C_I + \frac{2}{3}WLC_I, \quad (1)$$

$$C_{gd} = WL_{gd}C_I. \quad (2)$$

Furthermore, the dynamic performance of the OTFTs is strongly limited by the contact interface between the metallic source/drain and the semiconductor layers [13]. Detailed analysis of the capacitance–voltage (C–V) characteristics and frequency responses of metal–insulator–semiconductor (MIS) structures have been presented in literature to describe the current injection mechanism through the contact interfaces of OTFTs [13,14]. Accordingly, the extrinsic part consists of junction capacitances (C_j), junction resistances (r_j) and series resistances (r_s). The origin of the junction capacitance is most likely the formation of a small depletion region near the metal–semiconductor interface, while the junction resistance governs the injection current to the channel [14]. Unlike MIS structures, the series resistance of an OTFT has to account not only for the vertical but also for the much larger lateral components of the total contact resistance [15].

Full 2-port S-parameters of OTFTs were measured and compared to simulation results of the equivalent circuit. Measurements were performed on-chip, in ambient air and at room temperature using an HP 3577A VNA at frequencies up to 5 MHz. A de-embedding procedure that uses a 12-term error correction model is employed to remove the effects of measurement equipment and test fixture and to conduct accurate measurements at the terminals of the device-under-test (DUT) [16].

Fig. 4a depicts measured and simulated S-parameters for an OTFT with W = 100 μm, L = 1 μm and L_{ov} = 20 μm. The measurements were carried out under various bias conditions [6], but only the saturation regime is illustrated here (gate-source voltage V_{GS} = −3 V, drain-source voltage V_{DS} = −2 V), as it is the bias of interest for most analog circuits. A relatively large gate-to-contact overlap of 20 μm is utilized in this experiment in order to minimize the effect of unintentional misalignment. Fig. 4b shows extracted and simulated current gains (β). The current gain decays with increasing frequency, following the $1/f$ slope (−20 dB/decade) expected for a field-effect transistor. The current-gain cutoff frequency (f_T), defined as the frequency at which the current gain is unity ($|\beta|$ = 1), is found to be about 0.4 MHz. As depicted in both figures, the equivalent circuit model results agree well with measurements over the entire frequency range, and the relative mean square errors (rMSEs) are found to be <0.03%, 10.4%, 6.9% and <0.03% for S_{11}, S_{12}, S_{21} and S_{22}, respectively. The corresponding model parameter set is summarized in Table 1. Owing to the parts of the organic semiconductor that extend beyond the periphery of the intrinsic transistor and cause additional fringe currents, the model has to account for an induced parasitic capacitance by adding $C_I A_{fringe}$ to Eq. (1), where $A_{fringe} \simeq 480\ \mu m^2$ (about 12% of the total overlap area).

Table 1
Summary of small-signal model parameters.

Parameter	Symbol	Value	Unit
Intrinsic mobility	μ_o	~2.5	cm^2/Vs
Threshold voltage	V_{TH}	−1.2	V
Insulator capacitance	C_I	900	nF/cm^2
Junction capacitance	C_j	2000	nF/cm^2
Junction resistance	r_j	60	Ω cm
Series resistance	r_s	9.0	Ω cm
Output resistance	r_o	1.1	kΩ cm

Given the large value of C_j, the model can be further simplified as follows. The intrinsic current gain is given by:

$$\beta = \frac{g_m - jwC_{gd}}{jw(C_{gs} + C_{gd})} \quad (3)$$

The contact resistances can be considered by computing g_m with the effective charge-carrier mobility (μ_{eff}), which is represented in the saturation region for symmetrical OTFTs as [6]:

$$\mu_{eff} = \frac{2\mu_o L}{2L + \mu_o WC_I R_C(V_{GS} - V_{TH})} \quad (4)$$

With R_C = 200 Ω cm, an excellent agreement is achieved, as demonstrated by the dotted line in Fig. 4b. The small difference between the measured and simulated data near 100 kHz, which is the frequency limit of the network analyzer used, is owed to the accuracy of both the measurements and the calibration procedure.

Fig. 5a shows the current gain of asymmetric OTFTs with W = 100 μm, L = 1 μm, L_{gs} = 1, 4 and 7 μm and L_{gs} + L_{gd} = 10 μm. The −20 dB/decade slopes level off at lower frequencies for smaller L_{gs}. This occurs due to a current flow through the relatively large C_{gd}. In other words, as C_{gd} decreases for smaller L_{gd}, the decay in the current gain levels off at a higher frequency, which implies that the device behaves more like a conventional silicon MOSFET, where $C_{ds} \simeq 0$ and $C_{ds} \ll C_{gs}$ in the saturation region. The extracted frequency at which the current gain is unity ($|\beta|$ = 1) for each asymmetric OTFT is shown in Fig. 5b. As a reference, the dotted line designates the cutoff frequency (f_T) that is commonly calculated by $f_T = g_m/(2\pi(C_{gs} + C_{gd}))$. On the other hand, $f(|\beta| = 1)$ can be derived from Eq. (3) and written as:

$$f(|\beta| = 1) = \frac{g_m}{2\pi C_{gs}} \cdot \frac{1}{\sqrt{1 + 2C_{gd}/C_{gs}}} \quad (5)$$

which is represented by a solid line in Fig. 5b with g_m = 120 μA/V. Even though the impact of misalignment is not considered in g_m, a reasonable agreement is obtained. This indicates that in this frequency range the

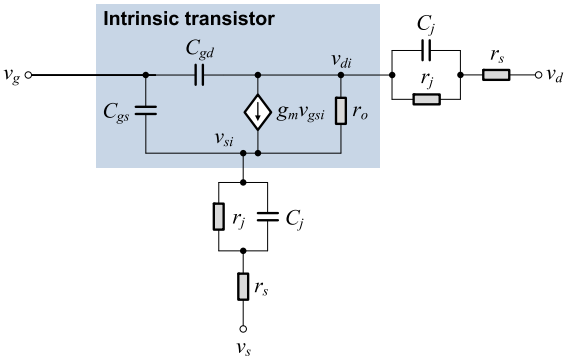

Fig. 3. Schematic diagram of the OTFT small-signal model, including both intrinsic (highlighted) and extrinsic (not highlighted) components.

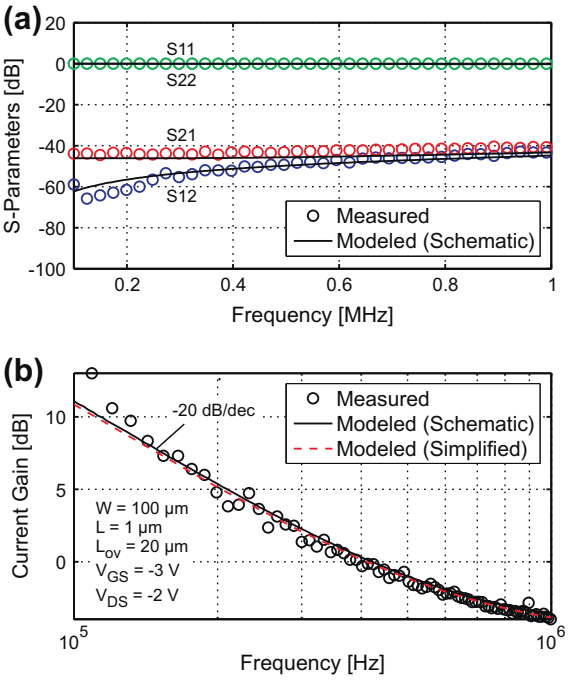

Fig. 4. (a) Full 2-port measured and simulated S-parameters of an OTFT with $W = 100$ µm, $L = 1$ µm and $L_{ov} = 20$ µm operated in the saturation region. (b) Extracted short-circuit current gain of the OTFT [6], where the solid line represents the result of the small-signal equivalent circuit, the schematic of which is shown in Fig. 3, and the dotted line represents the output of the simplified model using Eqs. (3) and (4). The figure depicts the excellent agreement between the measured and simulated TFT characteristics.

impact of misalignment on the overlap capacitances is more detrimental. Moreover, it can be deduced from Eq. (3) that the current gain levels off at $|\beta| = L_{gd}/(L_{gs} + L_{gd})$. Given the sum $L_{gs} + L_{gd} = 10$ µm, one can easily estimate the values of L_{gs} and L_{gd} separately from the measured results. For example, the upper curve in Fig. 5b levels off at $|\beta| \simeq -1$ dB, which matches properly with the designed dimensions $L_{gs} = 1$ µm and $L_{gd} = 9$ µm.

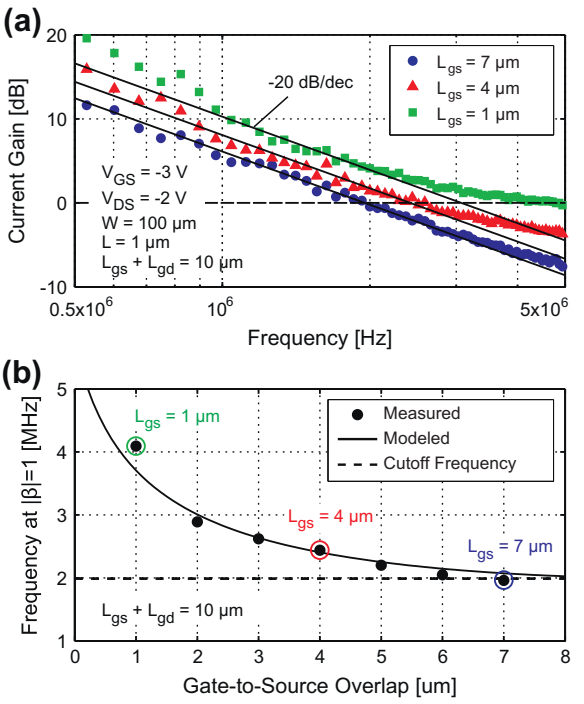

Fig. 5. (a) Measured S-parameters for asymmetrical OTFTs with $W = 100$ µm, $L = 1$ µm and $L_{gs} + L_{gd} = 10$ µm. The -20 dB/decade slopes level off at lower frequencies for OTFTs with smaller L_{gs}. (b) Extracted unity-gain cutoff frequency for all OTFTs with $L_{gs} = 1, 2, \ldots, 7$ µm and $L_{gs} + L_{gd} = 10$ µm. The dotted line represents as a reference the simulated prevalent FET-based cutoff frequency $f_T = g_m/(2\pi(C_{gs} + C_{gd}))$, while the solid line represents the simulated $f(|\beta| = 1)$ given in Eq. (5).

4. Conclusion

By developing a physics-based OTFT small-signal model, we have illustrated the correspondence of S-parameters characterization to prevalent methods like LCR-meter measurements for relatively large MIS structures. A reliable fit between measured and simulated S-parameters has been demonstrated. Furthermore, we have investigated the impact of contact misalignment on the dynamic TFT performance. Due to the limited alignment capabilities of many OTFT technologies, this effect has to be considered in process corner simulations. In this study, misalignment was precisely controlled by an OTFT process that is based on high-resolution silicon stencil masks. Although OTFTs are similar in many aspects to conventional silicon MOSFETs, our results obtained on intentionally asymmetrical transistors has shown that incorporating assumptions like $C_{gd} \ll C_{gs}$ into the calculation of the cutoff frequency might produce underestimated results.

Acknowledgments

The authors thank Johannes Digel of the Institute of Electrical and Optical Communications Engineering (Prof. Dr.-Ing. Manfred Berroth), University of Stuttgart, for assistance in high-frequency characterization, and Prof. Kazuo Takimiya at Hiroshima University for providing the organic

semiconductor DNTT. We gratefully acknowledge financial support provided by the German Research Foundation (DFG) under Grant BU 1962/4–1.

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