# User Customizable Logic Paper (UCLP) With Sea-Of Transmission-Gates (SOTG) of 2-V Organic CMOS and Ink-Jet Printed Interconnects

Koichi Ishida, *Member, IEEE*, Naoki Masunaga, Ryo Takahashi, Tsuyoshi Sekitani, Shigeki Shino, Ute Zschieschang, Hagen Klauk, Makoto Takamiya, *Member, IEEE*, Takao Someya, *Member, IEEE*, and Takayasu Sakurai, *Fellow, IEEE*

***Abstract*—In this paper we present User Customizable Logic Paper (UCLP) with a Sea-of Transmission-Gates (SOTG) of 2-V organic CMOS transistors. This can enable users to fabricate custom integrated circuits, by printing 200 $\mu$m wide interconnects with at-home ink-jet printers for the prototyping of large-area electronics and educational purposes. The SOTG reduces the area of the circuits in UCLP by between 11% and 85% compared with a conventional gate array architecture.**

***Index Terms*—Customizability, education, gate array, ink-jet printer, large-area electronics, printed interconnects, prototyping, room-temperature sintering, transmission gate logic, 2-V organic CMOS.**

## I. Introduction

THE recent and rapid progression of printable electronics means that it is now becoming feasible for ordinary people to fabricate macroscopic printed custom integrated circuits operating at visible speeds, using at-home ink-jet printers [1], [2]. Organic transistors can realize large-area electronics such as smart flexible displays, power transmission sheets, and electronic skin for robots. As the system integration scale with organic transistors increases, prototyping of the organic circuits becomes more important. A second benefit of prototyping with organic transistors is that their slow operating speeds make it easier for learners to intuitively understand and experience the operations of integrated circuits. This is in contrast to silicon integrated circuits, where nanometer-scale transistors operate at the lightning speed of a GHz clock, well beyond the scope of the human sense of vision and time.

Therefore, this paper proposes the use of User Customizable Logic Paper (UCLP) for both prototyping of larger-area electronics and educational applications. In particular, learners can study and experience the operation of integrated circuits by fabricating custom integrated circuits, using at-home ink-jet printers to print conducting interconnects on paper that contains prefabricated arrays of organic transistors. The feasibility of UCLP is demonstrated with the newly proposed Sea-of Transmission-Gates (SOTG) of organic CMOS transistors, providing field customizability through the use of the printable electronics technology for the first time. UCLP is applicable to a wide range of products of printable electronics including flexible displays and electronic paper, as well as for educational purposes. This technology provides a new means to add programmability for integrated circuits used in large-area electronics.

In this paper we describe UCLP and some key technologies including ink-jet printed interconnects and organic SOTG architecture. In Section II, UCLP and ink-jet printed interconnects are introduced, while in Section III, the SOTG architecture is introduced. In Section IV, experimental results are described and discussed. And finally the conclusions are given in Section V.

## II. UCLP and Ink-Jet Printed Interconnects

### A. User Customizable Logic Paper

Fig. 1 shows a prototype of UCLP, which was proposed in [3]. In UCLP, paper that contains an array of vias and an organic SOTG film are stacked. Although it would be ideal to fabricate the whole UCLP including the organic transistors using ink-jet printers, this proves to be very difficult since both high temperature (130–150 °C) and an organic solvent are required to fabricate the organic transistors. Since high temperatures and organic solvents cannot be handled by ink-jet printers, in UCLP the organic transistors are prefabricated and the field customizability is provided by the printed interconnects. Conventional printed interconnects, however, also require high temperatures (130–150 °C), which damages the organic transistors. The technology that enables us to solve the problem is the newly developed room-temperature sintering, conductive Ag nanoparticle ink, which is introduced in Section II-B.

Fig. 2(a) shows the cross section of the SOTG film which is described in detail in Section III. The 2 V organic CMOS transistors are fabricated on polyimide film [4], [5]. Organic

Manuscript received April 20, 2010; revised July 05, 2010; accepted July 16, 2010. Date of publication October 14, 2010; date of current version December 27, 2010. This paper was approved by Guest Editor Alison Burdett. This study was supported in part by CREST/JST and the Grant-in-Aid for Scientific Research (KAKENHI; WAKATE S), NEDO, the Special Coordination Funds for Promoting and Technology.

K. Ishida, R. Takahashi, and T. Sakurai are with the Institute of Industrial Science, University of Tokyo, Tokyo 153-8505, Japan (e-mail: ishida@iis.u-tokyo.ac.jp).

N. Masunaga was with the Institute of Industrial Science, University of Tokyo, Tokyo 153-8505, Japan. He is now with Terumo Corporation, Tokyo 100-0005, Japan.

T. Sekitani and T. Someya are with the Department of Electrical and Electronic Engineering, University of Tokyo, Tokyo 113-8654, Japan.

S. Shino is with Mitsubishi Paper Mills Ltd., Nagaokakyo 617-8666, Japan.

U. Zschieschang and H. Klauk are with the Max Planck Institute for Solid State Research, Stuttgart 70569, Germany.

M. Takamiya is with the VLSI Design and Education Center, University of Tokyo, Tokyo 113-8654, Japan.

Digital Object Identifier 10.1109/JSSC.2010.2074330

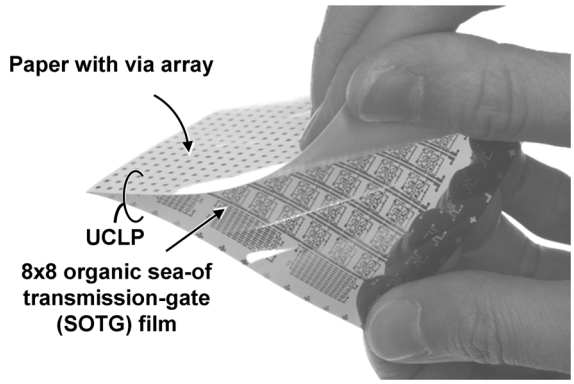



Fig. 1. Photograph of User Customizable Logic Paper (UCLP).

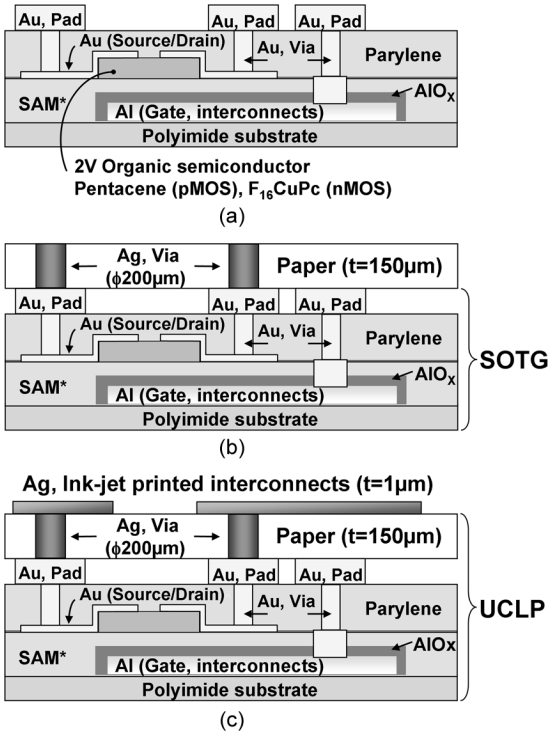



Fig. 2. Device structure of UCLP. (a) Cross section of SOTG. (b) Cross section of UCLP. (c) UCLP with ink-jet printed interconnects.

semiconductors for nMOS and pMOS are $F_{16}$CuPc (hexa-deca-fluoro-copper-phthalo-cyanine) and pentacene, respectively [4]. Self-assembled mono-layers (SAM) realize 2-V organic transistors [5], which are covered with a protective layer of parylene. Connection pads to the paper are formed with gold on top of this protective layer. An organic-metallic hybrid passivation layer, not indicated in Fig. 2(a), protects the organic CMOS and lengthens its lifetime to six months or more in air. Fig. 2(b) shows the cross section of UCLP. Organic CMOS SOTG and a rewiring layer on paper are stacked. Electrical connections are provided by Ag conductive adhesive. Then the interconnects are ink-jet printed onto the paper by users as shown in Fig. 2(c).

### *B. Ink-Jet Printed Interconnects*

A number of ink-jet printed interconnects technologies have been developed to date. However, either a high temperature

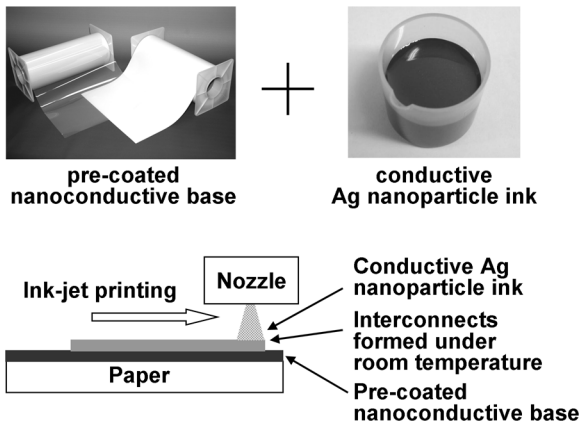



Fig. 3. Materials of ink-jet printed interconnects.

(130–150 °C) sintering or chemical process with organic solvent is required after the printing process, which causes damage to organic transistors. In contrast, our proposed ink-jet printing technology does not require such processes. The technology consists of pre-coated nanoconductive base and silver nanoparticle ink as shown in Fig. 3. The pre-coated nanoconductive base is a type of micro-porous layer made of Polyethylene, Polyvinyl alcohol, boracic acid, and other materials to absorb the solvent in the silver nanoparticle ink. Its thickness is around 40 um. The ink includes 15% silver particles, alcohol, surface active agent, and dispersant. The diameter of silver nanoparticles in the ink is typically 20 nm.

The ink chemically reacts with the pre-coated nanoconductive base on the paper at room temperature, that is, a sintering-free process, and does not cause damage to organic transistors. When the printed interconnect is stored in a laminated bag, the life time is five months or longer. In air, resistance of the interconnects increases by 10% after one month.

Fig. 4(a) shows a photograph of the printing process of the interconnects on UCLP using an off-the-shelf ink-jet (piezo-jet) printer. Fig. 4(b) shows photographs of printed interconnects and a via hole. The thickness of the Ag interconnect is 1 $\mu$m (typ.) and the measured sheet resistance is 0.2 $\Omega$/square (typ.). The via holes of 200 $\mu$m in diameter are prefabricated in UCLP by punching, in order to form a connection to the SOTG. The measured via resistance is 2.7 $\Omega$/via.

In this study, a 3 mm pad and via pitch rule is adopted. The reasons are as follows. Firstly, we have to consider misalignment in feeding the paper in the printer. To adopt an off-the-shelf, family-use printer, a large misalignment should be accepted. A 300 $\mu$m misalignment error is assumed in this study, and therefore, each via extension is 300 $\mu$m as shown in Fig. 5. Secondly, the Line/Space design rule ($\mathrm{L/S} = 200\ \mu\mathrm{m}$) of the printed interconnect is determined by both printing resolution and sheet resistance. Typical printers realize 100 $\mu$m resolution with the silver nanoparticle ink. However, the minimum line width should be determined by the sheet resistance of the ink. The sheet resistance depends on the room temperature and relative humidity during printing. A sheet resistance of 0.14 $\Omega$/square can be achieved by family-use printers at a high room temperature of 30 °C and relative humidity of 80%Rh.

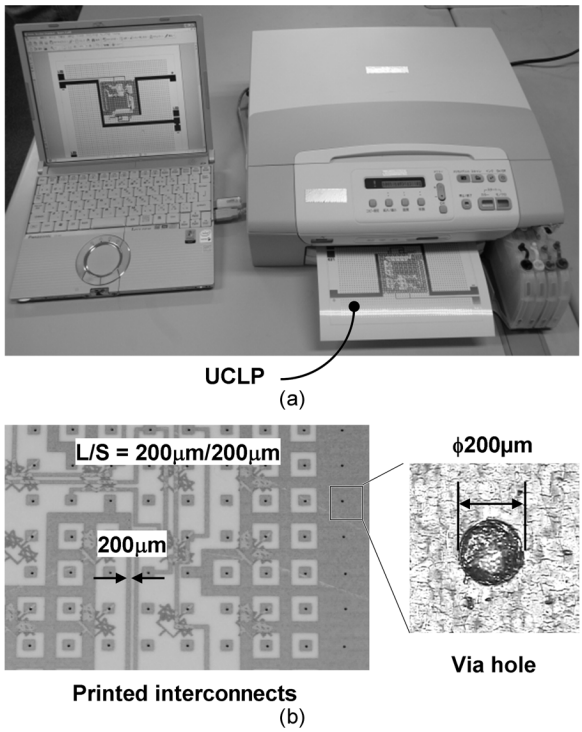



Fig. 4. (a) Photograph of the printing process of the interconnects on UCLP using an off-the-shelf ink-jet printer. (b) Photographs of printed interconnects and a via hole.

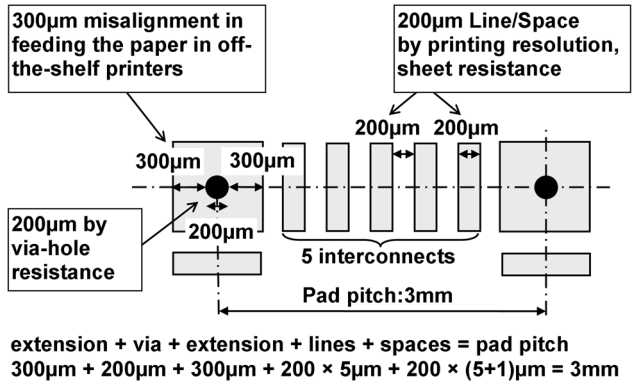



Fig. 5. Pad/via layout rule on paper.

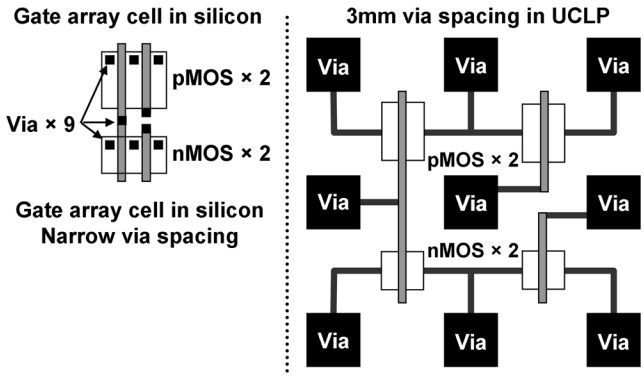



Fig. 6. Area issue on gate array architecture in UCLP.

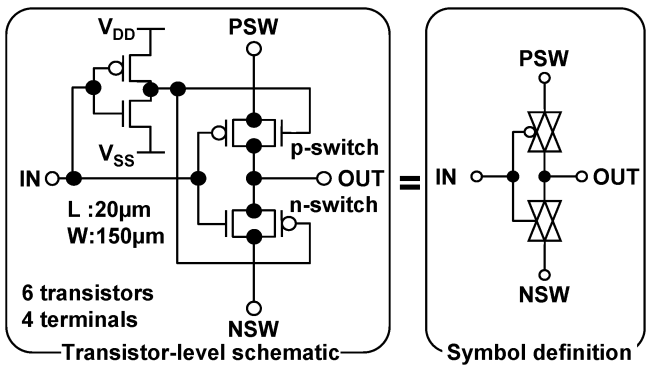



Fig. 7. Schematic and symbol definition of SOTG unit cell.

However, we assume a sheet resistance of $0.2\,\Omega/\text{square}$ by considering a practical room temperature of 17 °C and relative humidity of 35%Rh. We adopt 200-$\mu$m wide interconnects in this study, and thus resistance between two pads can be estimated around 2.2 Ω. The line space of 200 $\mu$m is determined by crosstalk. The crosstalk of the proposed printed interconnects is caused by resistive coupling rather than capacitive coupling. The sheet resistance of the pre-coated nanoconductive base is typically $9\times10^9\,\Omega/\text{square}$, but satellite ink drops by family-use printers lower the actual sheet resistance to around 10% of this value. Thus, the isolation of 20-mm long interconnects with a space of 200 $\mu$m can be estimated at around 9 MΩ. Thirdly, the minimum via-hole diameter should be larger than 200 $\mu$m to achieve an acceptable via resistance of $2.\tilde{7}\,\Omega$. Finally, in order to implement practical circuits, the number of interconnects between the pads should be around five. As the result, a 3-mm pad and via pitch rule is determined.

## III. Sea-Of Transmission-Gate Architecture

### A. Architecture

The large pad and via pitch of 3 mm mentioned in the previous section presents a design challenge for UCLP to increase integration density. Gate array (G/A) architectures have been widely used in silicon technologies. The G/A architecture includes two pMOS transistors, two nMOS transistors, and nine via holes in a logic cell. In silicon technologies, a narrow via spacing rule is available, and therefore the number of vias is not critical for the cell area as shown in Fig. 6. On the other hand, since we adopt a 3-mm pad and via pitch in UCLP, pads and vias now dominate the cell area as shown in Fig. 6. The number of vias becomes a critical issue in UCLP, and in order to solve the problem, an area-efficient SOTG is proposed instead of the conventional G/A approach.

Fig. 7 shows the schematic of the SOTG unit cell. SOTG uses a type of pass transistor logic and a single SOTG cell has six transistors. Each unit cell has a pair of complementary transmission gates, n-switch (NSW) and p-switch (PSW), and four terminals for ink-jet printed interconnects. $V_{DD}$ and $V_{SS}$ are common to every SOTG cell. In SOTG, the output (OUT) is connected to either PSW or NSW depending on the input (IN).

Fig. 8 shows several examples of logic gate implementation with the proposed SOTG cells. Binary decision diagrams (BBD) [6] are also shown in Fig. 8. An inverter requires one logic cell that consists of six transistors, as shown in Fig. 8(a). At first glance, the SOTG architecture seems to require a large number

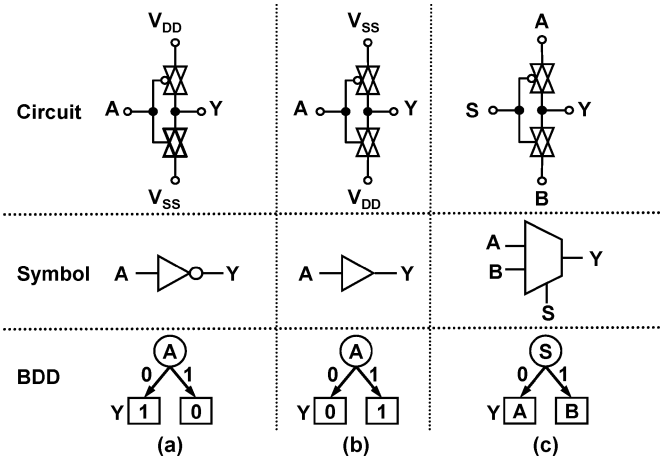



Fig. 8. Examples of logic gate implementation with SOTG cells. (a) Inverter. (b) Buffer. (c) Two-input multiplexer.

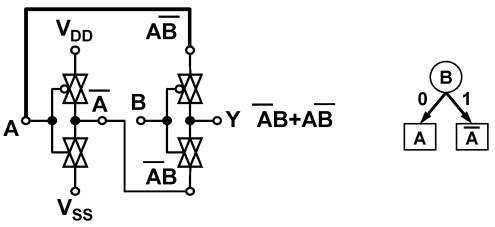


Fig. 9. Two-input XOR gate implementation with SOTG cells.

| A | B | $f_0$ | $f_1$ | $f_2$ | $f_3$ | $f_4$ | $f_5$ | $f_6$ | $f_7$ | $f_8$ | $f_9$ | $f_{10}$ | $f_{11}$ | $f_{12}$ | $f_{13}$ | $f_{14}$ | $f_{15}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| Type | | i | iii | ii | ii | iii | ii | iv | iii | iii | iv | ii | iii | ii | iii | iii | i |

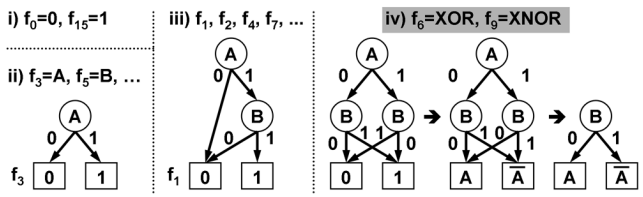



Fig. 10. Truth table of two-input logic functions and their binary decision diagram.

of transistors, however as will be shown this is not critical for the proposed UCLP. In terms of saving on rewiring cost or area, the SOTG architecture makes it easy to customize the UCLP. In fact, either a buffer or a two-input multiplexer can be implemented with one logic cell, as shown in Figs. 8(b) and 8(c).

An XOR gate consists of the 2-input multiplexer, the inverter, and two additional interconnects, shown in Fig. 9. Thanks to the complementary transmission gates, not only the XOR, but also any two-input logical operation can be realized with two logic cells as shown in Fig. 10. Furthermore, a D-flip flop can be implemented with only four logic cells and six interconnects, in addition to the power supply connection to both $V_{DD}$ and $V_{SS}$, as shown in Fig. 11.

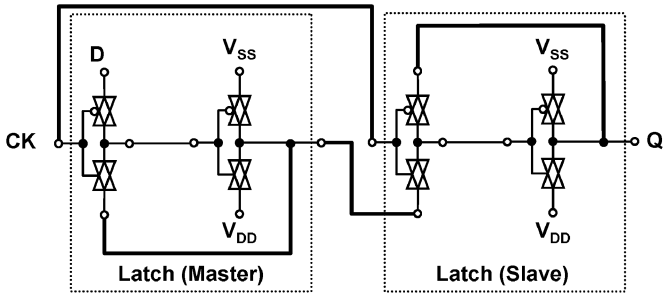
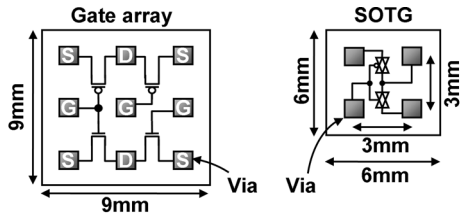



Fig. 11. D-flip flop (positive edge triggered) implementation with SOTG cells.




| | Gate array (Conventional) | SOTG (This work) |
|---|---|---|
| Number of transistors | 4 | 6 |
| Transistor area | 4.6mm$^2$ | 6.9mm$^2$ |
| Number of vias | 9 | 4 |
| Cell area* | 81mm$^2$ | 36mm$^2$ |

*Calculated on a fixed via spacing of 3mm.

Fig. 12. Comparison of unit logic cell between G/A and SOTG.

### *B. Area Comparison With G/A Architecture*

Fig. 12 shows logic cells of the conventional G/A architecture and the proposed SOTG architecture. Numbers of transistors in a typical G/A logic cell and a SOTG cell are four and six, respectively. Transistor W/L are chosen to be 150 $\mu$m wide and 20 $\mu$m long, determined by the driving capability and process yield. Under the condition of a fixed via spacing rule of 3 mm, a typical G/A logic cell occupies a layout area of 81 mm$^2$ because there are nine vias in each logic cell, as shown in Fig. 12. On the other hand, the area of logic cell of SOTG is only 36 mm$^2$ although the SOTG cell contains more transistors than in G/A. In UCLP, the logic cell area is determined by the number of vias; in fact, the transistor area for a conventional G/A cell occupies only 6% of the total cell area. Fig. 13(a) indicates the number of transistors in various logic functions. The number of transistors in the SOTG tends to be more than that in the G/A except in a few functions such as a multiplexer and a latch. In contrast, the area required for logic functions in SOTG are less than those in G/A in each function shown in Fig. 13(b). The results indicate that SOTG can reduce the area of logic cells by 11% (for INV and NAND) and up to 85% (MUX) for the UCLP, compared with a typical G/A architecture.

Fig. 14 shows an area comparison for the ISCAS89 s27 benchmark circuit [7]. If no misalignment by an off-the-shelf printer is accepted, (i.e., the via extensions in pads are 0 mm), a 1.8-mm via and pad pitch can be achieved, and as a result the areas of G/A and SOTG are comparable. The area of SOTG tends towards a constant with the pad pitch below 2.4 mm as shown in Fig. 14. However, as shown in Fig. 14 the SOTG has

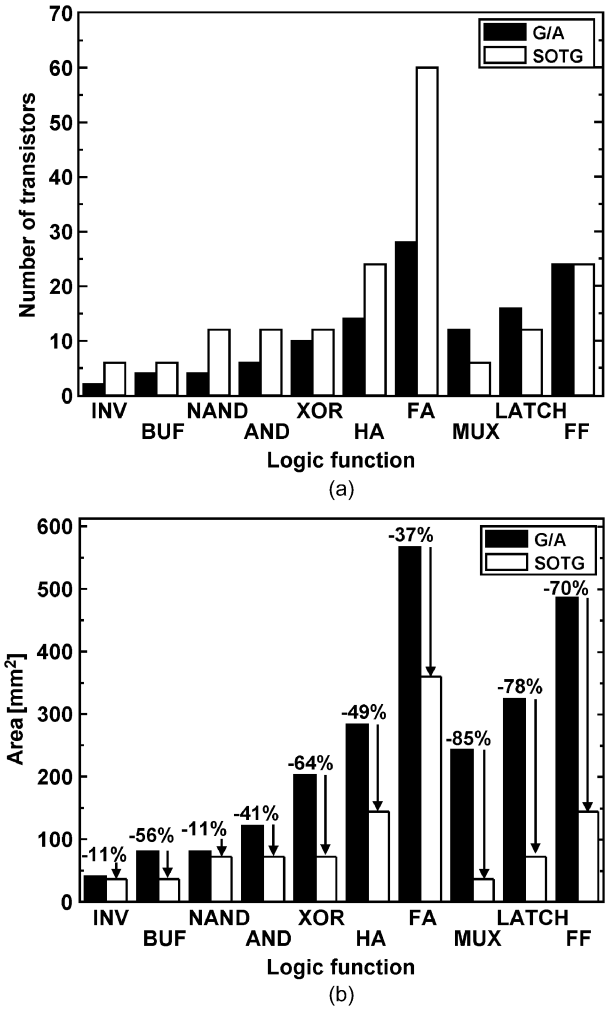



Fig. 13. Comparison on various logic functions. (a) Number of transistors. (b) Area.

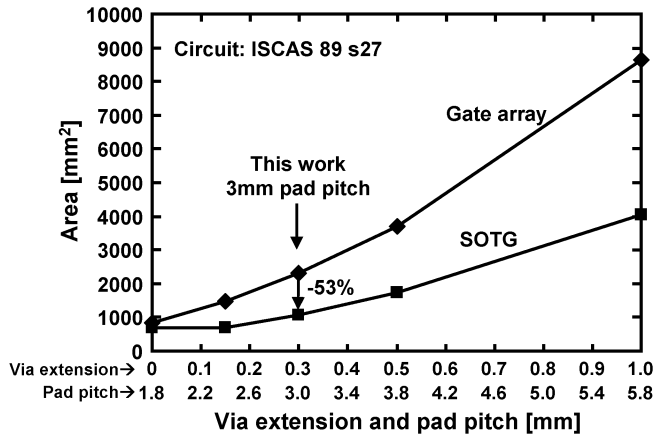



Fig. 14. Area comparison of ISCAS89 s27 benchmark circuit implementation.

an advantage when the UCLP is constrained to accept larger misalignments, since the area efficiency of SOTG improves compared with G/A. In this work, the area of s27 can be reduced by 53% for a 3-mm pad/via pitch.

The ESD requirements for organic transistors are not addressed in this paper because this type of logic circuit was not available. In practical use ESD protection must be considered. However we make the observation that the SOTG requires only one ESD protection device in each logic cell while the conventional G/A architecture requires three devices for their inputs.

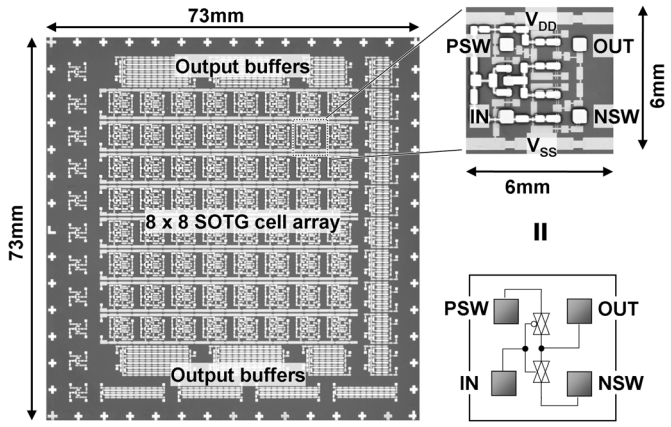



Fig. 15. Photograph of the 8 × 8 SOTG cell array.

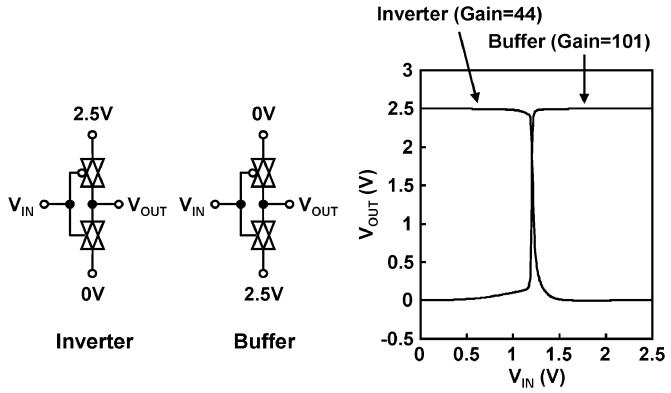



Fig. 16. Measured static characteristics of the SOTG unit cell.

## IV. Experimental Results

Fig. 15 shows a photograph of the 8 × 8 SOTG cell array and details of a single SOTG cell. The sizes of the 8 × 8 SOTG cell array and the single SOTG cell are 73 mm square and 6 mm square, respectively. The minimum design rule of the SOTG is 20 $\mu$m.

Fig. 16 shows the measured SOTG cell static characteristics at 2.5-V $V_{DD}$, which is a typical value of the supply voltage for the organic CMOS. The single SOTG cell can operate as both an inverter and a buffer. The inverter gain is 44 while the amplifier/buffer gain is 101. These results show sufficient gains to be used for logic circuit implementation.

In order to evaluate signal attenuation due to the printed interconnects on the paper, the open drain pMOS LED driver with three printed interconnects shown in Fig. 17(a) is measured at 2.5-V $V_{DD}$. Fig. 17(b) shows the measured waveform in the case with conventional metallic interconnects for reference; in this case the output swing is around 2.0 V with 2.5-V $V_{DD}$. Fig. 17(c) shows the output waveform from the proposed printed interconnects on the paper. Although the output swing is slightly

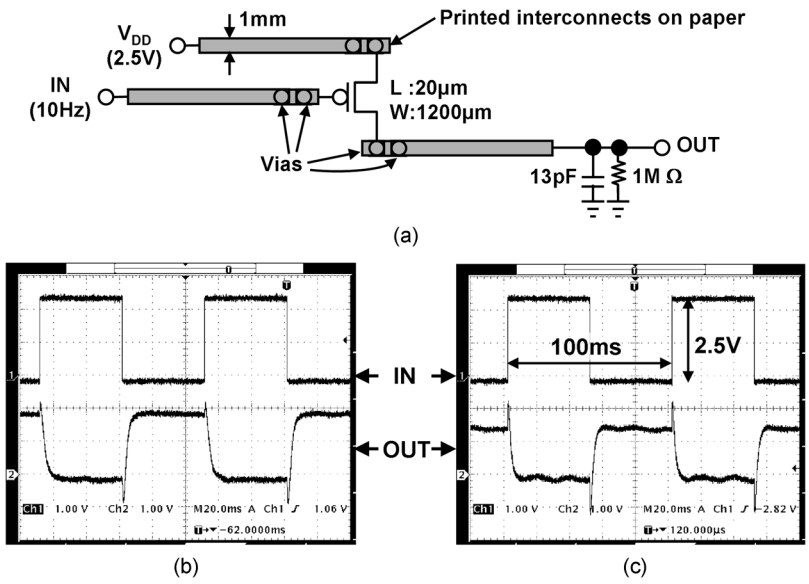



Fig. 17. Measured waveform of organic transistor through the printed interconnects. (a) Measurement circuit. (b) Output waveform with metallic interconnects. (c) Output waveform with printed interconnects.

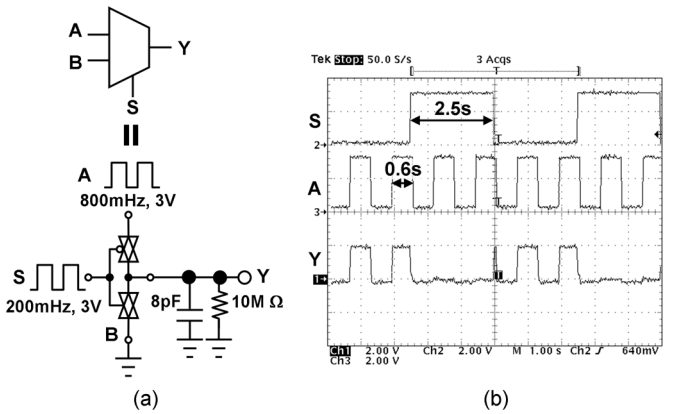



Fig. 18. Measurement waveform of SOTG-based two-input multiplexer. (a) Measurement circuit. (b) Measured waveforms.

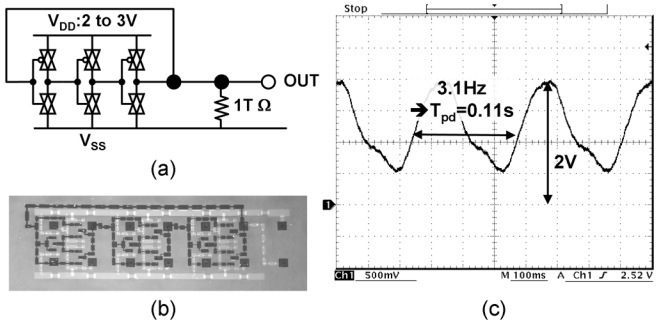



Fig. 19. Measurement result of SOTG-based ring oscillator. (a) Measurement circuit. (b) Photograph of the ring oscillator. (c) Measured waveform.

degraded due to the printed interconnects, it is acceptable because the driver can drive low-power LEDs and logic gates of the SOTG.

In order to demonstrate the functionality of the proposed SOTG cell, Fig. 18(a) shows the measured schematic of a two-input multiplexer using the SOTG logic cell. 3-V $V_{DD}$ is applied in the measurement. Square waves of 200 mHz are applied to the select signal, S, and square waves of 800 mHz are applied to input terminal A. Input terminal B is connected to $V_{SS}$. Fig. 18(b) shows measured waveforms. The result confirm that the organic CMOS transmission gates successfully conduct both high and low signals, and therefore, the feasibility of the SOTG architecture is verified by measurement.

In order to measure the propagation delay of the SOTG logic cell, a ring oscillator using three organic SOTG logic cells was fabricated on a polyimide substrate. Fig. 19(a) shows the schematic and Fig. 19(b) shows the chip photograph. Since the operating speed of organic circuits is slow, a three-stage ring oscillator gives a very low-frequency oscillation. Although the oscillator can operate from 2.0 to 3.0 V $V_{DD}$, the measurement is carried out at $V_{DD}$ of 2 V to measure the maximum propagation delay. The measured frequency is 3.1 Hz at $V_{DD}$ of 2 V, that is, the propagation delay of each logic cell is 0.11 s as shown in Fig. 19(c). The speed is limited by the mobility and parasitic gate capacitance of the nMOS devices. With wider transistors, the output driving capability will increase; however, the speed will not. The slow transistor speed is appropriate for educational purposes, because the LED driven by the output pulse flashes at visible (observable) speed.

From the measurements, the output swings of SOTG cells are slightly degraded either because of the relatively high resistance of printed interconnects as shown in Fig. 17, or the limited driving capability of the transmission gate as shown in Fig. 18. This degradation limits the number of gate stages in practical circuits. In this study, the transistor area occupies only 19% of

TABLE I
KEY FEATURES OF THE INK-JET PRINTED INTERCONNECTS, 2 V ORGANIC CMOS, AND SOTG

| Ink-jet printed interconnects | |
|---|---|
| Materials | Nanoconductive base/Ag nanoparticle ink |
| Sheet resistance | 0.2Ω/square(typ.) |
| Via resistance | 2.7 Ω/via |
| **Organic CMOS** | |
| Materials (pMOS, nMOS) | Pentacene, $F_{16}CuPc$ |
| Mobility (pMOS, nMOS) | 0.53 $cm^2$/Vs, 0.02 $cm^2$/Vs |
| Gate oxide thickness | 6nm |
| Gate width, length | 150μm, 20μm |
| Supply voltage | 2 to 3V |
| **SOTG** | |
| Ring oscillator frequency | 3.1Hz@2V |
| Number of transistors/pads | 6/4 |
| Array size | 73x73$mm^2$ (8 x8 array) |
| Area reduction by | 11%(INV) to 85%(MUX) |

the total SOTG cell area; this transistor area was chosen by considering the process yield. However to enhance the driving capability and increase the number of possible stages, wider transistors are recommended for use in a practical UCLP.

The total power consumption of an $8 \times 8$ SOTG cell array can be estimated as follows. Each transistor in the unit cell has a parasitic capacitance of 21 pF. The total parasitic capacitance in the unit cell is given by $2 \times 16 = 126$ pF. When the 64 cells operate at 10 Hz with 3 V $V_{DD}$, the total power consumption of an $8 \times 8$ SOTG is given by

$$CV^2F = 64 \times 126 \times 3^2 \times 10 = 726\,\mathrm{nW}.$$

The key features of the ink-jet printed interconnects, 2-V organic CMOS, and SOTG are summarized in Table I.

## V. CONCLUSION

This paper has presented a UCLP with a SOTG of 2-V organic CMOS transistors, to enable users to fabricate custom integrated circuits by printing 200-$\mu$m wide interconnects with ink-jet printers. Applications include prototyping of large-area electronics and educational purposes.

The proposed SOTG architecture reduces the area of the circuits in UCLP by between 11% and 85% compared to a conventional G/A architecture. This type of technology will provide ways to add programmability for integrated circuits used in large-area electronics, and is a step toward manufacturing ICs at home with an off-the-shelf printer.

## REFERENCES


[1] M. Böhm, A. Ullmann, D. Zipperer, A. Knobloch, W. H. Glauert, and W. Fix, "Printable electronics for polymer RFID applications," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2006, pp. 270–271.

[2] L. Liu, M. Takamiya, T. Sekitani, Y. Noguchi, S. Nakano, K. Zaitsu, T. Kuroda, T. Someya, and T. Sakurai, "A 107 pJ/b 100 kb/s 0.18 $\mu$m capacitive-coupling transceiver for printable communication sheet," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 292–293.

[3] K. Ishida, N. Masunaga, R. Takahashi, T. Sekitani, S. Shino, U. Zschieschang, H. Klauk, M. Takamiya, T. Someya, and T. Sakurai, "User Customizable Logic Paper (UCLP) with organic Sea-of Transmission-Gates (SOTG) architecture and ink-jet printed interconnects," in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, Feb. 2010, pp. 138–139.

[4] H. Klauk, U. Zschieschang, J. Pflaum, and M. Halik, "Ultralow-power organic complementary circuits," *Nature*, vol. 445, pp. 745–748, Feb. 2007.

[5] K. Ishida, N. Masunaga, Z. Zhou, T. Yasufuku, T. Sekitani, U. Zschieschang, H. Klauk, M. Takamiya, T. Someya, and T. Sakurai, "Stretchable EMI measurement sheet with $8 \times 8$ coil array, 2 V organic CMOS decoder, and 0.18 $\mu$m silicon CMOS LSIs for electric and magnetic field detection," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 249–259, Jan. 2010.

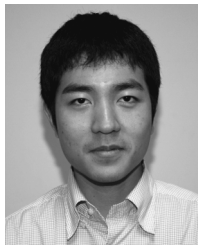
[6] S. Akers, "Binary decision diagrams," *IEEE Trans. Computers*, vol. C-27, no. 6, pp. 509–516, Jun. 1978.

[7] F. Brglez, D. Bryan, and K. Kozminski, "Combinational profiles of sequential benchmark circuits," in *Proc. ISCAS*, May 1989, pp. 1929–1934.


**Koichi Ishida** (S'00–M'06) received the B.S. degree in electronics engineering from the University of Electro-Communications, Tokyo, Japan, in 1998, and received the M.S. and Ph.D. degrees in electronics engineering from the University of Tokyo, Tokyo, Japan, in 2002 and 2005, respectively.

He joined Nippon Avionics Co., Ltd. Yokohama, Japan, in 1989, where he developed high-reliability hybrid microcircuits applied to aerospace programs. Since July 2007, he has been working at the Institute of Industrial Science, University of Tokyo, as a research associate. His research interests include low-voltage low-power CMOS analog circuits, RF wireless communication circuits, and on-chip power supplies.

Dr. Ishida is a member of IEICE.



**Naoki Masunaga** received the B.S. and M.S. degrees in electronic engineering from Sophia University, Tokyo, Japan, and the University of Tokyo, Tokyo, Japan, in 2008 and 2010, respectively.

He is now with Terumo Corporation. His research interests are in the field of integrated circuit design.

**Ryo Takahashi** received the B.S. degree in electrical and electronic engineering from Tokyo Institute of Technology, Tokyo, Japan, in 2009. He is currently studying in the graduate school of Electrical Engineering at the University of Tokyo.

His research interests are in the field of integrated circuit design.

**Tsuyoshi Sekitani** was born in Yamaguchi, Japan, in 1977. He received the B.S. degree from Osaka University, Japan, and the Ph.D. degree in applied physics from the University of Tokyo, Japan, in 1999 and 2003, respectively.

From 1999 to 2003, he was with the Institute for Solid State Physics (ISSP), University of Tokyo. From 2003 to 2009, he was a Research Associate of the Quantum-Phase Electronics Center, University of Tokyo. Since 2010, he has been an Assistant Professor in the Department of Electrical and Electronic Engineering, University of Tokyo.

**Shigeki Shino** received the B.S. and M.S. degrees in functional polymer science from Shinshu University, Japan, in 1989 and 1991, respectively.

In 1991, he joined Mitsubishi Paper Mills Ltd. where he is currently working on the development of silver nanoparticle inks and micro-porous layers. He is a deputy general manager of the imaging and development company.

**Ute Zschieschang** received the Dipl.-Ing. from Oberflächentechnik, Fachhochschule Mittweida in 2000, and the Dr. rer. nat. from Technische Universität Bergakademie Freiberg, Germany, in 2006.

In 2005, she joined the Max Planck Institute for Solid State Research, Stuttgart, Germany.

**Hagen Klauk** received the Diplom-Ingenieur degree in electrical engineering from Chemnitz University of Technology, Germany, in 1995, and the Ph.D. degree in electrical engineering from the Pennsylvania State University, University Park, in 1999.

From 2000 to 2005 he was with the Polymer Electronics group at Infineon Technologies, Erlangen, Germany. In 2005 he joined the Max Planck Institute for Solid State Research, Stuttgart, Germany, to lead an Independent Junior Research Group in organic electronics.

**Makoto Takamiya** (S'98–M'00) received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Japan, in 1995, 1997, and 2000, respectively.

In 2000, he joined NEC Corporation, Japan, where he was engaged in the circuit design of high-speed digital LSIs. In 2005, he joined the University of Tokyo, Japan, where he is an Associate Professor of VLSI Design and Education Center. His research interests include the circuit design of the low-power RF circuits, the ultra low-voltage digital circuits, and the large area electronics with organic transistors.

Dr. Takamiya is a member of the technical program committee for IEEE Symposium on VLSI Circuits and IEEE Custom Integrated Circuits Conference (CICC).

**Takao Someya** (M'03) received the Ph.D. degree in electrical engineering from the University of Tokyo, Tokyo, Japan, in 1997.

In 1997, he joined the Institute of Industrial Science (IIS), University of Tokyo, as a Research Associate and was appointed to be a Lecturer of the Research Center for Advanced Science and Technology (RCAST), University of Tokyo, in 1998, and an Associate Professor of RCAST in 2002. From 2001 to 2003, he worked for the Nanocenter (NSEC) of Columbia University and Bell Labs, Lucent Technologies, as a Visiting Scholar. From 2003 to 2009, he was an Associate Professor in the Department of Applied Physics and Quantum-Phase Electronics Center, University of Tokyo. Since 2009, he has been a Professor of Electrical and Electronic Engineering, University of Tokyo. His current research interests include organic transistors, flexible electronics, plastic integrated circuits, large-area sensors, and plastic actuators.

Prof. Someya is a member of the IEEE Electron Devices Society, the Materials Research Society (MRS), and the Japanese Society of Applied Physics. He serves as a subcommittee member for IEEE/IEDM and a program co-chair for the 3rd Organic Microelectronics Workshop.

**Takayasu Sakurai** (S'77–M'78–SM'01–F'03) received the Ph.D. degree in electrical engineering from the University of Tokyo, Tokyo, Japan, in 1981.

In 1981 he joined Toshiba Corporation, where he designed CMOS DRAM, SRAM, RISC processors, DSPs, and SoC Solutions. He has worked extensively on interconnect delay and capacitance modeling known as Sakurai model and alpha power-law MOS model. From 1988 through 1990, he was a Visiting Researcher at the University of California Berkeley, where he conducted research in the field of VLSI CAD. From 1996, he has been a professor at the University of Tokyo, working on low-power high-speed VLSI, memory design, interconnects, ubiquitous electronics, organic IC's and large-area electronics. He has published more than 400 technical publications including 100 invited presentations and several books and filed more than 200 patents.

Dr. Sakurai will be an executive committee chair for VLSI Symposia and a steering committee chair for IEEE A-SSCC from 2010. He served as a conference chair for the Symposium on VLSI Circuits, and ICICDT, a vice chair for ASPDAC, a TPC chair for the A-SSCC, and VLSI symp., an executive committee member for ISLPED and a program committee member for ISSCC, CICC, A-SSCC, DAC, ESSCIRC, ICCAD, ISLPED, and other international conferences. He is a recipient of 2010 IEEE Donald O. Pederson Award in Solid-State Circuits, 2010 IEEE Paul Rappaport award, 2010 IEICE Electronics Society Award, 2009 Achievement Award of IEICE, 2005 IEEE ICICDT award, 2004 IEEE Takuo Sugano Award and 2005 P&I patent of the year award and four product awards. He gave keynote speech at more than 50 conferences including ISSCC, ESSCIRC and ISLPED. He was an elected AdCom member for the IEEE Solid-State Circuits Society and an IEEE CAS and SSCS distinguished lecturer. He is a STARC Fellow and an IEICE Fellow.