Thermal stability of organic thin-film transistors with self-assembled monolayer dielectrics

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We have investigated the annealing effects on 2 V-operation pentacene organic thin-film transistors (TFTs) with self-assembled monolayer-based gate dielectrics. When pentacene TFTs without passivation layers are annealed at 100 °C, the pentacene crystal structure changes to the bulk phase, resulting in an irreversible degradation of electronic performances. This degradation is suppressed by a 2.5-μm-thick passivation layer. The mobility of the encapsulated TFTs decreases by only 12% upon annealing at 140 °C. We have also investigated the bias-stress effect and found the drain current of low-voltage pentacene TFTs annealed at 70 °C decreases by 1% during continuous bias stress for 1 h. © *2010 American Institute of Physics*. [doi:10.1063/1.3299017]

Organic thin-film transistors (TFTs) have attracted considerable attention since they are among the key elements for realizing large-area, printable, flexible and/or stretchable electronics,[1–3] large-area sensors,[4,5] and actuators.[6] High operating voltage and electric instability of organic TFTs have been major concerns for many years. Thanks to recent efforts, the operating voltages of organic TFTs have been reduced significantly by utilizing high-capacitance gate dielectrics, such as thin insulating polymers,[7,8] metal oxides with large permittivity,[9–11] or self-assembled nanodielectrics.[12,13] Furthermore, low-voltage organic TFTs using gate dielectrics comprising an oxygen-plasma-grown AlO_x layer (with a thickness of a few nanometers) and an alkyl-phosphonic acid self-assembled monolayer (SAM) have been reported.[14–16] Pentacene TFTs with SAM-based gate dielectrics show excellent electrical characteristics, including mobility as large as 0.7 $cm^2/V\,s$ and on/off ratio as large as 10^7. However, the effect of exposure to high temperatures on the current-voltage characteristics of these TFTs with SAMs has not been reported. It is known that the pentacene thin-film structure and the electrical characteristics of pentacene TFTs are affected by the environmental temperature.[17,18] Therefore, it is important to investigate the thermal stability of pentacene TFTs with SAM-based gate dielectrics and to study the effect of encapsulation layers.

In this letter, we fabricated pentacene TFTs using SAMs of *n*-tetradecylphosphonic acid as part of the gate dielectric.[19,20] Some TFTs were encapsulated with a polychloro-para-xylylene passivation layer and were compared with TFTs without encapsulation layer. When TFTs without passivation layer were annealed at 100 °C, the field-effect mobility decreased from 0.55 to 0.24 $cm^2/V\,s$. In contrast, the mobility of TFTs with passivation layer decreased by only 12% upon annealing at 140 °C. The drain current of TFTs annealed at 70 °C changed by only 1% when a dc bias stress of −2 V was applied continuously for 1 h. X-ray diffraction (XRD) measurements revealed that the pentacene thin-film phase did not change to the bulk phase even after annealing at 160 °C when the pentacene was encapsulated with a 2.5-μm-thick polychloro-para-xylylene passivation layer.

The cross-sectional structure of the top-contact pentacene TFTs is schematically shown in Fig. 1(a). First, a 25-nm-thick Al gate electrode was thermally evaporated through a shadow mask onto a heavily doped silicon wafer. The gate dielectric consists of a thin layer of aluminum oxide (thickness: 5 nm) and a SAM of *n*-tetradecylphosphonic acid, the chemical structure of which is shown in Fig. 1(b). The aluminum oxide film was prepared by an oxygen-plasma treatment of the Al gate electrode and provides a large density of hydroxyl groups for molecular adsorption. The plasma power was 300 W, and the duration of the plasma treatment was 30 min. The SAM of n-tetradecylphosphonic acid was prepared by submersing the substrate in a 2-propanol solution of the

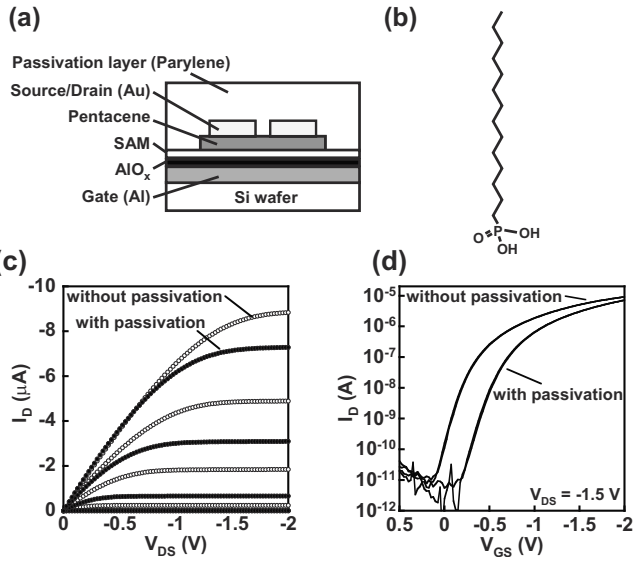

FIG. 1. (a) Cross section of pentacene TFTs with a gate dielectric based on a SAM. (b) Chemical structure of n-tetradecylphosphonic acid. (c) Drain current (I_D) of TFTs with and without parylene encapsulation layer as a function of the drain-source voltage (V_{DS}). The gate-source voltage V_{GS} is varied from 0 to −2 V in steps of −0.5 V. (d) The corresponding transfer curves: V_{GS} is swept from +0.5 to −2 V at V_{DS}=−1.5 V.

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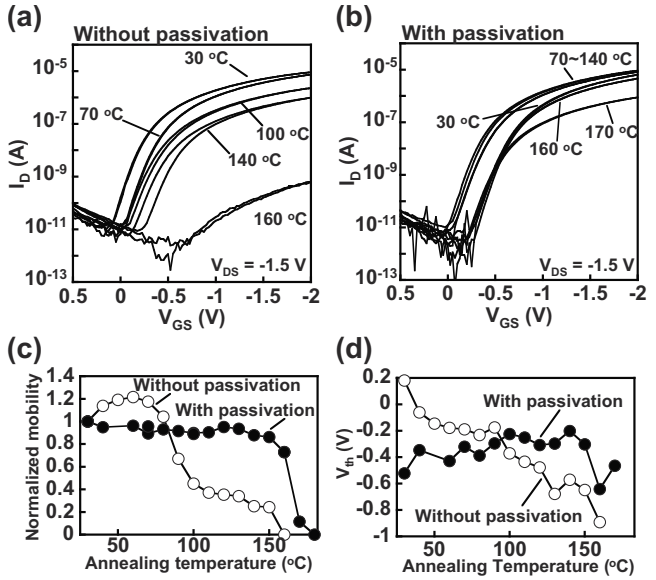

FIG. 2. Transfer characteristics of the transistors before and after the annealing process: (a) without passivation layer, (b) with passivation layer. All measurements were performed at 30 °C in a nitrogen-filled glovebox. (c) Normalized mobility and (d) threshold voltage of the TFTs with and without passivation layer after annealing at temperatures up to 180 °C.

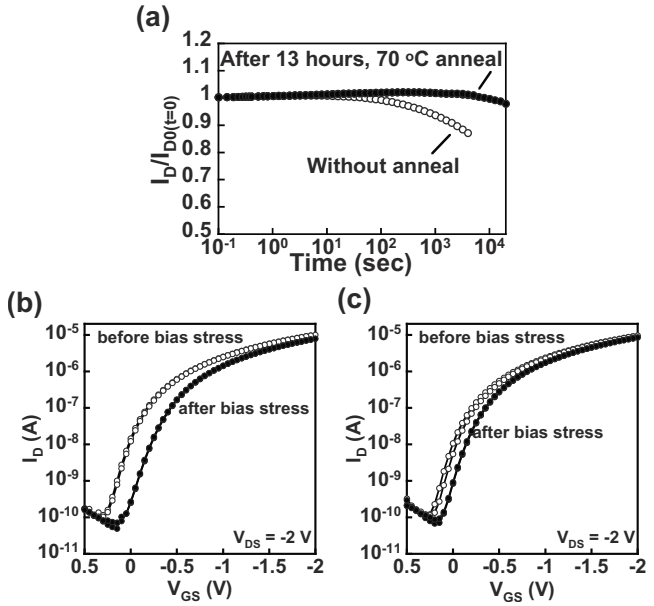

FIG. 3. (a) Normalized drain current (I_D) as a function of time during continuous DC bias stress ($V_{GS}=V_{DS}=-2$ V) of a pentacene TFTs. The measurements were performed on the annealed FETs at 70 °C for 13 h and nonannealed FETs on SAM insulators. [(b) and (c)] The corresponding transfer characteristics of FETs on SAM insulators without (b) and with (c) the annealing process taken before and after the application of dc bias voltages for 4000 s: V_{GS} is swept from +0.5 to −2 V with the application of $V_{DS}=-2$ V.

phosphonic acid molecules at room temperature.[16,21] Purified pentacene was deposited in vacuum through a shadow mask to form a 30-nm-thick patterned semiconductor layer on the gate dielectric. During the pentacene deposition, the substrate was at room temperature. A 50-nm-thick Au layer was evaporated through a shadow mask to form the source and drain electrodes. The nominal length and width of the channel were 50 and 500 μm, respectively, for all TFTs. Finally, some of the substrates were uniformly encapsulated with a 2.5-μm-thick polychloro-para-xylylene (diX-SR, parylene, Daisankasei Co., Ltd.) passivation layer. The fabrication of the SAM gate dielectric does not require the control of the thickness and high process temperatures, so this process is compatible to almost all plastic substrates. Furthermore, this technique can form dielectrics with excellent uniform thickness, thus leading to small device-to-device variations in electrical characteristics.[14]

The current-voltage characteristics of the TFTs were measured with a semiconductor parameter analyzer (4155C, Agilent Technologies) in a nitrogen-filled glovebox with concentrations of oxygen and moisture below 1 ppm. Figure 1(c) exhibits the output characteristics of TFTs with and without parylene passivation. The drain current (I_D) was measured as a function of the drain-source voltage (V_{DS}) for gate-source voltages (V_{GS}) between 0 to −2 V in steps of 0.5 V. Figure 1(d) shows the transfer characteristics of the same transistors for $V_{DS}=-1.5$ V.

In order to investigate the thermal stability of the TFTs, the devices were annealed at a certain temperature for 30 min in a nitrogen-filled glovebox. After allowing the TFTs to cool to 30 °C, the electrical characteristics were measured again at 30 °C in nitrogen. Figures 2(a) and 2(b) show the temperature-induced changes in the transfer characteristics of pentacene TFTs with and without parylene passivation. The electrical characteristics of the TFTs without parylene passivation changed significantly during annealing: The on-state drain current decreased from 9.1 to 1.0 μA upon annealing at 140 °C. In contrast, the encapsulated TFTs does not degrade for temperatures as high as 140 °C; the on-state current increased from 7.1 to 9.2 μA during annealing at 140 °C. Figure 2(c) shows the change in mobility as a function of annealing temperature, normalized to the mobility prior to annealing. The mobility of the TFTs without passivation layer increased slightly from 0.55 to 0.64 $cm^2/V\,s$ upon annealing at 70 °C, but it decreased substantially to 0.24 $cm^2/V\,s$ upon annealing at 100 °C. In contrast, the change in mobility of the encapsulated TFTs during annealing for temperatures up to 140 °C is very small; annealing at 140 °C reduced the mobility by only 12% (from 0.93 to 0.81 $cm^2/V\,s$). Encapsulation also improves the stability of the threshold voltage (V_{th}), as shown in Fig. 2(d). The threshold voltage of the TFTs without encapsulation changes from 0.18 to –0.57 V upon annealing at 140 °C. In contrast, the threshold voltage of the encapsulated TFTs changes from −0.52 to −0.20 V upon annealing at 140 °C.

We also investigated how the dc bias stress stability of pentacene TFTs without parylene passivation is affected by annealing at a temperature of 70 °C.[22–25] The drain current (I_D) of the TFTs was monitored over time while continuously applying a dc bias of $V_{GS}=V_{DS}=-2$ V. Figure 3(a) shows the drain current normalized to the initial value at the start of the measurement as a function of time. For TFTs that were not annealed prior to the bias-stress experiment the drain current decreased by more than 10% during 1 h of bias stress. In contrast, TFTs annealed at 70 °C for 13 h in nitrogen show much better bias-stress stability; the drain current of these TFTs decreases by only 1% during the 1 h bias stress. Figures 3(b) and 3(c) show the transfer characteristics of the TFTs before and after bias stress. The mobility of the TFTs annealed at 70 °C decreases only slightly during bias stress, from 0.58 to 0.57 $cm^2/V\,s$, and the bias stress-

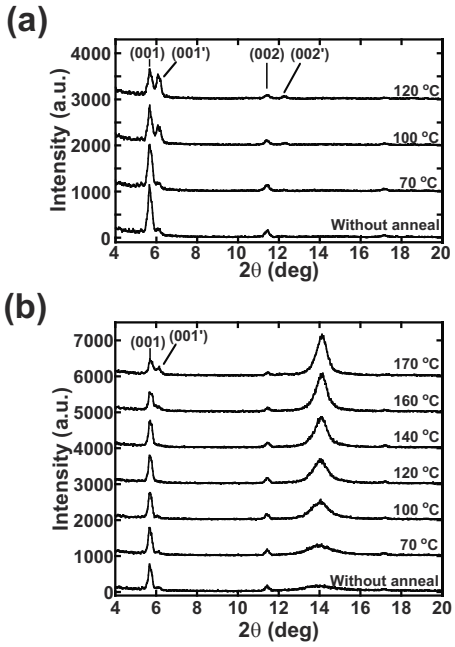

FIG. 4. (a) XRD spectra of a pentacene film (thickness: 30 nm) deposited on a SAM-based gate dielectric without parylene passivation layer after annealing at 70, 100, and 120 °C for 30 min. (b) XRD spectra of a pentacene film deposited on a SAM-based gate dielectric, covered with a parylene passivation layer, and annealed at temperatures of 70, 100, 120, 140, 160, and 170 °C for 30 min.

induced threshold voltage shift in these TFTs is less than 0.07 V.

In order to investigate how the pentacene crystal structure is affected by exposure to high temperatures we performed XRD measurements on pentacene films with a thickness of 30 nm deposited on AlO_x/SAM gate dielectrics with and without parylene passivation. Figure 4(a) shows the XRD spectra of a pentacene film without parylene passivation, and Fig. 4(b) shows those with parylene passivation. The diffraction peaks in the spectra of the as-deposited pentacene films indexed as (001) indicate that the as-deposited pentacene consists mainly of the thin-film phase, and it is highly oriented in the out-of-plane direction with a lattice spacing d(001) of 15.4 Å.[18,26] For pentacene without parylene passivation, diffraction peaks (001′) corresponding to a lattice spacing of 14.4 Å were observed after annealing at 100 °C. In contrast, for pentacene with the parylene passivation, the (001′) diffraction peaks did not appear as long as the annealing temperature was below 160 °C.

Pentacene crystallizes in four different polymorphs that are classified according to their d(001) spacing as follows: 14.1, 14.4, 15, and 15.4 Å.[26,27] The two polymorphs with d(001) spacings of 14.4 and 15.4 Å have been found in pentacene films deposited onto silicon dioxide; these are referred to as the "bulk phase" and the "thin film phase," respectively.[28] It has been reported that exposure to high temperatures induces a change from the thin-film phase to the bulk phase, and that the appearance of the bulk phase causes the electrical characteristics of pentacene TFTs to degrade.[17,18] We have already reported that pentacene TFTs with polymer gate dielectric are stable upon annealing at 140 °C,[17] and that the bias-stress effect in these devices is significantly suppressed by postdeposition annealing.[23]

The appearance of the bulk phase upon annealing in the TFTs without parylene passivation is consistent with the significant reduction in the mobility of the TFTs, as seen in Fig. 2(c). These results indicate that the parylene passivation layer greatly suppresses the change of the pentacene crystal structure from the thin-film phase to the bulk phase, causing the encapsulated TFTs to be far more stable at high temperatures than the TFTs without parylene passivation.

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