Modeling of Drain Current Mismatch in Organic Thin-Film Transistors

Deyu Tu, Kazuo Takimiya, Ute Zschieschang, Hagen Klauk, and Robert Forchheimer

***Abstract*—In this paper, we present a consistent model to analyze the drain current mismatch of organic thin-film transistors. The model takes charge fluctuations and edge effects into account, to predict the fluctuations of drain currents. A Poisson distribution for the number of charge carriers is assumed to represent the random distribution of charge carriers in the channel. The edge effects due to geometric variations in fabrication processes are interpreted in terms of the fluctuations of channel length and width. The simulation results are corroborated by experimental results taken from over 80 organic transistors on a flexible plastic substrate.**

***Index Terms*—Current fluctuation, mismatch, modeling, organic thin-film transistors (OTFTs).**

I. Introduction

ORGANIC thin-film transistors (OTFTs) are well recognized as a very promising solution to implement integrated circuits on flexible plastic substrates, especially for flexible displays [1], [2]. A few advanced examples have already been demonstrated, such as radio-frequency identification (RFID) tags [3], [4], digital–analog converters (DAC) [5], [6], and analog–digital converters (ADC) [7]. The complexity of integrated circuits at large-scale requires accurate models to describe transistor behaviors. A lot of effort has been devoted to develop various models for OTFTs [8]–[13]. However, most of those works are focused on dc current modeling, to our knowledge none of them deals with the current mismatch in OTFTs.

Mismatch is the time-independent variation of the drain current between two or more nominally identical devices in a circuit. The performance of most analog and even digital circuits can be affected by the device mismatch. There are a few works discussing the current mismatch in conventional silicon metal-oxide-semiconductor field effect transistors (MOSFETs) [11]–[13]. However, the differences between MOSFETs and OTFTs are so significant that we cannot simply inherit those models for OTFTs. For example, OTFTs only work in the accumulation regime, while MOSFETs work in the inversion regime. As known, the diversity of OTFTs is extremely large, such as different substrates, semiconductors, dielectrics, conductors, device structures, fabrication processes, and so on. Unlike with MOSFETs, there is no "standard" OTFT device. In addition, a lot of factors (oxygen, moisture, etc.) cause scattering of individual characteristics even for the same type of OTFT. The deviation of the OTFT characteristics makes it challenging to model the current mismatch. Recently, a new organic semiconductor, DNTT, has been developed that exhibits excellent air stability and parameter uniformity [14]–[16], which reduces the difficulties for mismatch modeling.

Here, we report a consistent model to describe the drain current mismatch of nominally identical OTFTs. The model is based on charge fluctuations and edge effects, including two main features of OTFTs: bias-dependent mobility and charge accumulation. A Poisson distribution is proposed to represent the distribution of accumulated charge in the transistor channel. The charge fluctuation leads to a deviation in the drain current. The variation of many factors in OTFTs, such as layer thickness, contact resistance, etc., can be explained through the charge fluctuation. The variation of individual device geometries is considered as the edge effects, represented by the fluctuations in channel length and width. OTFTs with DNTT as the semiconductor have been characterized and the statistical experimental results are shown to be consistent with our simulation.

II. Model Derivation

In this model, we use local current fluctuations in the transistor channel to derive the deviation of drain currents, which is given by the charge fluctuations. In addition, the random fluctuations caused by the edge effects are included as well. Taking these two factors into account, the total current mismatch is then derived from the dc model [8], [9] for OTFTs.

A. Local Current Fluctuations

As shown in Fig. 1(a), considering the nonlinear charge distribution, the transistor channel is split into a number of series elements in longitude, to calculate the local fluctuations. At the position x along the channel, a small channel element of length Δx contributes a local current fluctuation i_Δ, which is a zero-mean stationary random process on x. An equivalent circuit of the split transistor channel, composed of resistors connected in series, is presented in Fig. 1(b). The current fluctuation i_Δ causes a resistance variation r_Δ. The resistance of the element Δx becomes $\Delta R + r_\Delta$, while the resistance of the entire channel is $R + r_\Delta$. The drain current of the entire channel, including the current fluctuation, is $I_D + \Delta i_d$.

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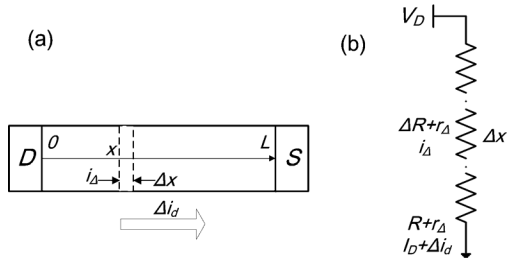

Fig. 1. (a) Schematics of split transistor channel, a local current fluctuation i_Δ is contributed by the element Δx. (b) The equivalent circuit of the split channel. "D" and "S" denote drain and source, respectively.

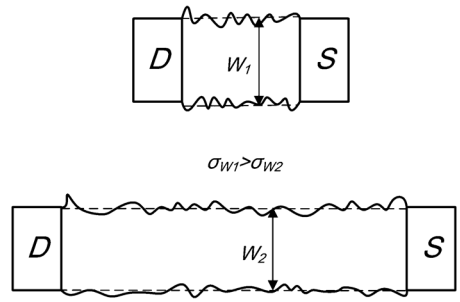

Fig. 2. Exaggerated illustration of the variation of the channel width, inversely proportional to the channel length. "D" and "S" denote drain and source, respectively.

Small-signal approximation gives us the relationship between i_Δ and r_Δ as

$$\frac{r_\Delta}{\Delta R} = -\frac{i_\Delta}{I_D}. \tag{1}$$

As well, the relationship between i_Δ and r_Δ is written as

$$\frac{r_\Delta}{R} = -\frac{\Delta i_d}{I_D}. \tag{2}$$

Then, we have the drain current fluctuation from (1) and (2), as

$$\Delta i_d = \frac{\Delta R}{R} i_\Delta = \frac{\Delta x}{L} i_\Delta. \tag{3}$$

Considering the stochastic local current fluctuations, the mean square of the drain current fluctuation is [8]

$$\begin{aligned}\overline{\Delta I_D^2} &= \sum_L \overline{(\Delta i_d)^2} = \sum_{\Delta x->0} \overline{\left(\frac{\Delta x}{L} i_\Delta\right)^2} \\ &= \frac{1}{L^2}\int_0^L \left(\Delta x \cdot \overline{i_\Delta^2}\right) dx.\end{aligned} \tag{4}$$

The local current fluctuation i_Δ can be expressed with the fluctuation of the accumulated local charge $\Delta Q(x)$ as

$$i_\Delta = \frac{\Delta Q(x)}{Q(x)} I_D \tag{5}$$

where $Q(x)$ is the local charge accumulated at position x in the channel.

The local charge fluctuation is proportional to threshold voltage fluctuations as follows:

$$\Delta Q(x) = -C_0 \Delta V_T \tag{6}$$

where C_0 is the dielectric capacitance per unit area, ΔV_T is the local fluctuation of the threshold voltage V_T. From the standard deviation [6], the mean square of ΔV_T is expressed as

$$\overline{\Delta V_T^2} = \sigma_{VT}^2 = \frac{A_{VT}^2}{W \Delta x} \tag{7}$$

where W is the channel width and A_{VT} is a constant reflecting the uncertainty in the number of charge carriers in the accumulation layer. We assume a Poisson distribution [13], [17]for the fluctuation of charge carriers, then

$$A_{VT}^2 = \frac{q^2 N_c}{C_0^2} \tag{8}$$

where q is the electron charge and N_c is the density of traps where charge carriers may be accumulated.

B. Edge Effects

The random fluctuations due to the edge effects are another very important factor for current mismatch, which is necessarily included in this mismatch model. The edge effects are geometric variations introduced during fabrication, reflecting the fluctuation of the device active area. Both the variations of the effective channel length L and width W are considered as edge effects. Generally, the variations of L and W decrease as the channel size increases, since the parameters "average" over a greater distance [12], schematically shown in Fig. 2. The deviation of L is proportional to $1/W$ and likewise for W proportional to $1/L$. Here, we use a mismatch factor to represent the edge effects in this model, as

$$S_{WL}^2 = \sigma^2\left(\frac{\Delta L}{L}\right) + \sigma^2\left(\frac{\Delta W}{W}\right). \tag{9}$$

C. Static Drain Current Model

As reported in the previous work [8], a charge drift model is used to describe the static drain current for OTFTs. The channel current per unit width at point x is [8]

$$\frac{I_D}{W} = \mu(x) Q(x) \frac{dV(x)}{dx} \tag{10}$$

where $\mu(x) = \mu_0 (V_{GT} - V(x))^\gamma (\gamma > 0)$ is the voltage-dependent charge mobility, μ_0 is the charge mobility at low field, $V(x)$ is the longitude potential along the channel and γ is the mobility enhancement factor, reflecting the density of states mobility model which includes temperature-dependence and is widely accepted in OTFTs [9]. Then, the partial along the channel dx is written as

$$dx = W \frac{\mu(x) Q(x)}{I_D} dV(x). \tag{11}$$

In terms of terminal bias, the static drain current in linear region is in this form [4], [5]

$$I_D = \frac{W}{L} \mu_0 C_0 \frac{V_{GT}^{\gamma+2} - (V_{GT} - V_D)^{\gamma+2}}{\gamma + 2}. \tag{12}$$

In order to make the model compact, we only keep the most important part in [8]but neglect the bias-dependent capacitance, the contact effect, and the threshold voltage shift [8]. However,

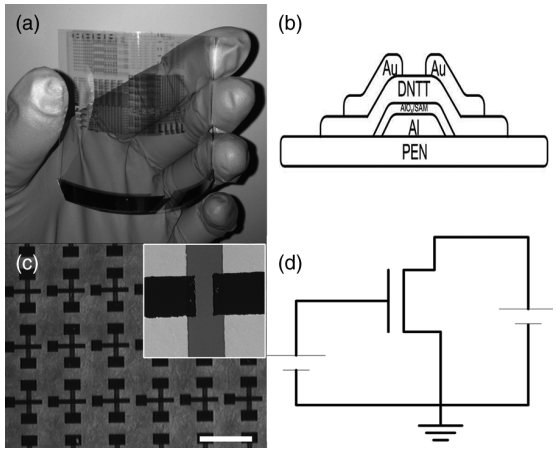

Fig. 3. (a) Flexible PEN substrate with OTFTs. (b) Schematic cross-section of the DNTT OTFTs. (c) The array of DNTT OTFTs with nominally identical channel length (30 μm) and channel width (100 μm). Scale bar=1 mm. Zoom-in: a typical channel edge profile. (d) The transistor test configuration, where the drain current is measured by applying bias to the gate and the drain and grounding the source.

this equation is upgradable for these features. For the current in saturation region, we have $V_{GT} - V_D = 0$ in (12).

D. Drain Current Mismatch

Substituting (5)–(8) and (11) into (4), the deviation of drain currents is calculated as

$$\overline{\Delta I_D^2} = \frac{\mu_0 q^2 I_D N_c}{C_0 L^2} \int_0^{V_D} (V_{GT} - V(x))^{\gamma-1}\, dV(x). \qquad (13)$$

Completing the integral in (13) and including the edge effects in (9), the drain current mismatch including edge effects is finally expressed as

$$\frac{\sigma_{I_D}^2}{I_D^2} = \frac{\mu_0 q^2 N_c \left(V_{GT}^{\gamma} - (V_{GT} - V_D)^{\gamma}\right)}{\gamma C_0 L^2 I_D} + S_{WL}^2$$
(linear region)
$$= \frac{\mu_0 q^2 N_c V_{GT}^{\gamma}}{\gamma C_0 L^2 I_D} + S_{WL}^2.$$
(saturation region) (14)

III. Results and Discussion

We measured over 80 organic TFTs to evaluate their drain current fluctuations. All the devices with identical design were fabricated on a flexible polyethylene naphthalate (PEN) substrate [Fig. 3(a)], by vacuum-evaporation through 50-μm-thick polyimide shadow masks [15]. The transistors, with bottom-gate, top-contact configuration, have Al gate electrodes, a 5.3-nm-thick thin AlO_x/SAM gate dielectric, 25-nm-thick DNTT as the semiconductor, and Au drain/source contacts, shown in Fig. 3(b). A part of a 10×10 transistor array is presented in Fig. 3(c), while the designed channel length and width are 30 and 100 μm, respectively. The measurements were conducted on a Micromanipulator 6200 probe station with an Agilent 4156C Semiconductor Parameter Analyzer in ambient air at room temperature, after the TFTs had been exposed to the air for six months. With a test configuration shown in Fig. 3(d),

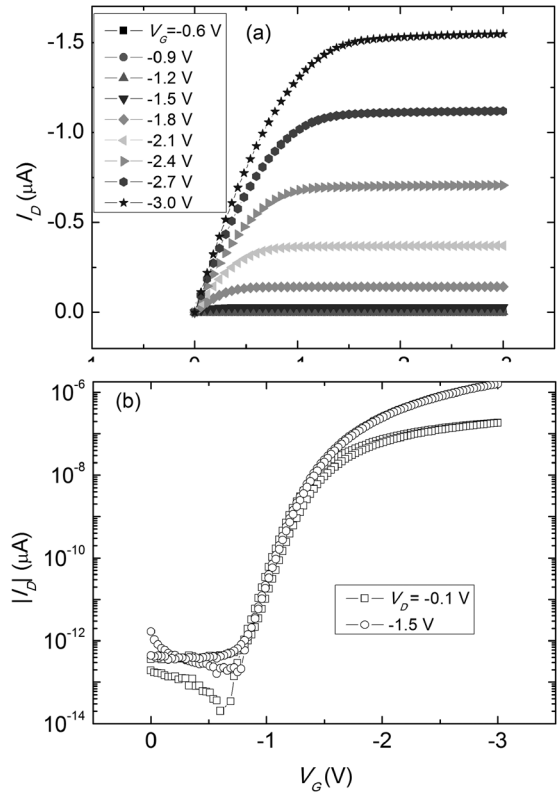

Fig. 4. (a) Typical output and (b) transfer characteristics of DNTT OTFTs.

the output and transfer characteristics (Fig. 4) were recorded via a homemade LabView program. The drain current standard deviations obtained from those characteristics indicate the current variation of the identical OTFTs on the same substrate.

A. Current Mismatch Versus Drain Voltage

Using the drain current model [8], some model parameters are extracted, such as $\mu_0 = 0.6$ cm^2/V·s, $C_0 = 0.5$ μF/cm^2, and $\gamma = 1.3$. With these basic parameters, the mismatch power normalized to the dc power (σ_{ID}^2/I_D^2) for drain–source voltages from 0 to -3 V is presented in Fig. 5. The scatters represent experimental data and the curves are simulation results determined by (14). The density of traps N_c is estimated as 6.8×10^{17} cm^{-2}, corresponding to $A_{VT} = 2.2$ V·μm. In the saturation region, the mismatch reaches a constant similar to the drain current, as expected from (14). As the gate voltage is increased, the mismatch approaches a minimum, becomes smaller and less dependent on the drain voltage. This is due to the smaller deviation of the drain currents over larger currents and the edge effects become predominated. Then, we can extract $S_{WL} = 0.41$ from the experimental data in the inset of Fig. 5. The results of current mismatch show some similarities to the noise analysis of transistors, however, the former is due to spatial fluctuations in fixed charges, while the latter is related to temporal fluctuations in localized states along the channel [13].

B. Current Mismatch Versus Gate Voltage

Fig. 6 presents the normalized current mismatch versus V_G above the threshold voltage. At smaller V_G, the mismatch is dominated by accumulated charge fluctuations and it is very large in this region. But the mismatch converges to a smaller

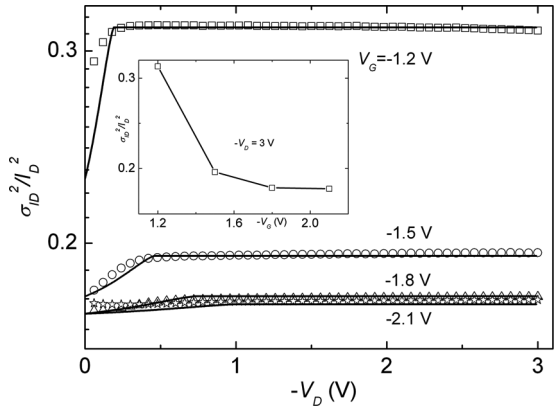

Fig. 5. Normalized drain current mismatch versus drain-source voltage at different gate-source voltages. The symbolic scatters are experimental data, while the curves are simulation results. Inset: the experimental data at $V_D = -3$ V, while $V_G = -1.2, -1.5, -1.8, -2.1$ V, respectively.

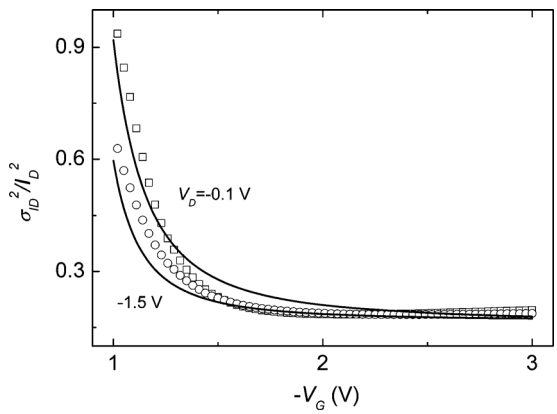

Fig. 6. Normalized drain current mismatch versus gate voltage at different drain voltages. The symbolic scatters are experimental data, while the curves are simulation results.

level at larger V_G. The simulated curves match the experimental data better in the linear and saturation regions, where OTFTs are mostly operated, than the subthreshold region, due to that (14) originates from the dc drain current expression for linear regions. The simulated curves follow an inverse proportional power law, which shows a trend similar to that in conventional silicon transistors. However, the mismatch of these organic transistors is still two orders of magnitude larger than in silicon transistors. This implies that there is plenty of room to improve the mismatch in organic transistors, by developing new materials (less fluctuation in charge carriers) and more precise manufacturing (smaller edge effects [7]).

IV. Conclusion

In summary, we have analyzed the drain current mismatch in organic thin-film transistors with a consistent model. The model is based on the fluctuations of trapped charge and the edge effects. The local current fluctuations are used to derive the drain current deviation. The variations of the channel length and width due to fabrication errors are taken into account as the edge effects. Experimental data obtained from organic transistors with DNTT as the semiconductor are consistent with our simulation. This work may assist the design of analog circuits or even digital circuits with organic thin-film transistors.

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References

[1] H. Klauk, "Organic thin-film transistors," *Chemical Soc. Rev.*, vol. 39, no. 7, pp. 2643–2666, Jun. 2010.
[2] H. Sirringhaus, N. Tessler, and R. H. Friend, "Integrated optoelectronic devices based on conjugated polymers," *Science*, vol. 280, no. 5370, pp. 1741–1744, Jun. 1998.
[3] E. Cantatore, T. C. T. Geuns, G. H. Gelinck, E. van Veenendaal, A. F. A. Gruijthuijsen, L. Schrijnemakers, S. Drews, and D. M. de Leeuw, "A 13.56-MHz RFID system based on organic transponders," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 84–92, Jan. 2007.
[4] K. Myny, S. Steudel, S. Smout, P. Vicca, F. Furthner, B. van der Putten, A. K. Tripathi, G. H. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, "Organic RFID transponder chip with data rate compatible with electronic product coding," *Org. Electron.*, vol. 11, pp. 1176–1179, 2010.
[5] W. Xiong, Y. Guo, U. Zschieschang, H. Klauk, and B. Murmann, "A 3-V, 6-Bit C-2C digital-to-analog converter using complementary organic thin-film transistors on glass," *IEEE J. Solid-State Circuits*, vol. 45, no. 7, pp. 1380–1388, Jul. 2010.
[6] T. Zaki, F. Ante, U. Zschieschang, J. Butschke, F. Letzkus, H. Richter, H. Klauk, and J. N. Burghartz, "A 3.3 V 6-bit 100 kS/s current-steering digital-to-analog converter using organic p-type thin-film transistors on glass," *IEEE J. Solid-State Circuits*, vol. 47, pp. 292–300, 2012.
[7] W. Xiong, U. Zschieschang, H. Klauk, and B. Murmann, "A 3 V, 6 b successive approximation ADC using complementary organic thin-film transistors on glass," in *2010 IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, USA, Feb. 2010, pp. 134–135.
[8] D. Tu, L. Herlogsson, L. Kergoat, X. Crispin, M. Berggren, and R. Forchheimer, "A static model for electrolyte-gated organic field-effect transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3574–3582, Oct. 2011.
[9] O. Marinov, M. J. Deen, U. Zschieschang, and H. Klauk, "Organic thin-film transistors: Part I—compact DC modeling," *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 2952–2961, Dec. 2009.
[10] S. Locci, M. Morana, E. Orgiu, A. Bonfiglio, and P. Lugli, "Modeling of short-channel effects in organic thin-film transistors," *IEEE Trans. Electron Devices*, vol. 55, no. 10, pp. 2561–2567, Oct. 2008.
[11] M. C. J. M. Vissenberg and M. Matters, "Theory of the field-effect mobility in amorphous organic transistors," *Phys. Rev. B*, vol. 57, p. 12964, May 1998.
[12] L. Li, H. Marien, J. Genoe, M. Steyaert, and P. Heremans, "Compact model for organic thin-film transistor," *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 210–212, Mar. 2010.
[13] L. Li, K.-S. Chung, and J. Jang, "Field effect mobility model in organic thin film transistor," *Appl. Phys. Lett.*, vol. 98, p. 023305, 2011.
[14] P. G. Drennan and C. C. McAndrew, "Understanding MOSFET Mismatch for analog design," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 450–456, Mar. 2003.
[15] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1440, Oct. 1989.
[16] C. Galup-Montoro, M. C. Schneider, H. Klimach, and A. Arnaud, "A compact model of MOSFET mismatch for circuit design," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1649–1657, Aug. 2005.
[17] T. Yamamoto and K. Takimiya, "Facile synthesis of highly extended heteroarenes, dinaphtho[2,3-b:2′, 3′-f]chalcogenopheno[3,2-b]chalcogenophenes, their application to field-effect transistors," *J. Amer. Chem. Soc.*, vol. 129, pp. 2224–2225, 2007.
[18] U. Zschieschang, F. Ante, D. Kälblein, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Someya, J. Blochwitz-Nimoth, and H. Klauk, "Dinaphtho[2,3-b:2′,3 ′-f]thieno[3,2-b]thiophene (DNTT) thin-film transistors with improved performance and stability," *Organic Electron.*, vol. 12, no. 8, pp. 1370–1375, Jun. 2011.
[19] F. Ante, D. Kälblein, T. Zaki, U. Zschieschang, K. Takimiya, M. Ikeda, T. Sekitani, T. Someya, J. N. Burghartz, K. Kern, and H. Klauk, "Contact resistance and megahertz operation of aggressively scaled organic transistors," *Small*, vol. 8, pp. 73–79, 2012.

[20] R. Difrenza, P. Llinares, and G. Ghibaudo, "A new model for the current factor mismatch in the MOS transistors," *Solid-State Electron.*, vol. 47, no. 7, pp. 1167–1171, Jul. 2003.

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