Low-Temperature Solution-Processed Memory Transistors Based on Zinc Oxide Nanoparticles

By *Hendrik Faber, Martin Burkhardt, Abdesselam Jedaa, Daniel Kälblein, Hagen Klauk,* and *Marcus Halik**

On the way towards wide-spread flexible large-area electronics, several features are of particular interest. With focus on low-cost applications, the manufacturing requires high throughput, preferably realized by simple methods on large-area flexible substrates, for example spin coating,[1,2] inkjet-printing[3–5] or roll-to-roll techniques.[6] In view of mobile applications with low power consumption, complementary logic circuit designs are beneficial; these require p-channel and n-channel field-effect transistors with large, balanced mobilities and good air stability. For low-temperature-processed p-channel transistors with mobility greater than 1 $cm^2V^{-1}s^{-1}$ and excellent air stability, a variety of conjugated organic semiconductors are available.[7,8] Performance and stability of organic semiconductors for air-stable n-channel transistors have improved as well,[9,10] although the largest mobilities are still below 1 $cm^2V^{-1}s^{-1}$.

Beyond field-effect transistors, additional functionalities, such as non-volatile memory properties, are of interest, for example to individualize radio-frequency identification tags[11,12] or to store user-relevant information on smart cards.[13] Ideally, these additional features are realized with the same electronic devices that are used for the logic circuits.

Inorganic semiconductors typically have large electron mobilities, but they are not usually compatible with low-temperature solution processing. Precursor solutions of the desired inorganic material can sometimes be processed with solution techniques and then converted through thermal treatment.[2,14–16] However, the required temperatures are often too high to be compatible with plastic substrates.[16] Another approach utilizes nano-sized inorganic components, such as nanoparticles, nanorods or nanowires.[17–21] These can be dispersed in suitable solvents and thereby processed with solution-based methods. Therefore, efforts to combine the possibility of solution processing with the superior electronic properties of inorganic semiconductors have been undertaken in recent years, using various approaches.

Here, we report on air-stable n-channel thin-film transistors (TFTs) based on solution-processed zinc oxide nanoparticles (ZnO-NPs). The transistors exhibit large drain currents in combination with a tunable non-volatile hysteresis, which makes them attractive candidates for non-volatile memory transistors. Due to the low processing temperatures of 100 °C, the transistors are compatible with flexible plastic substrates.

Zinc oxide was chosen as a non-toxic semiconductor with a large band gap of 3.4 eV and large electron mobility. It can be synthesized by solution-based or vapor-based methods into various types of nano-structures, ranging from nanoparticles[17,22] over nanorods,[19,23] nanorings,[24] tetrapods,[25] to nanowires.[23,26]

We have used a mono-disperse core-shell system with a spherical ZnO core with a diameter of about 5 nm coated with an organic ligand shell of about 1 nm thickness. The particles were provided by SusTech Darmstadt (Germany) as a stable dispersion in methyl tert-butyl ether (MTBE) (14.5 wt % of ZnO-NP).

Crack-free films with uniform thickness of about 30 nm, determined by scanning electron microscopy SEM, and reproducibly small agglomerate size were obtained by spin-coating from a dilute formulation of 0.5 wt % ZnO-NPs in MTBE. The atomic force microscopy (AFM) image in Figure 1a shows a uniform film composed of individual spheres with a diameter of about 15 to 25 nm. These spheres are agglomerates of about 10 to 15 primary ZnO nanoparticles, as can be seen from the scanning tunneling microscopy (STM) image shown in Figure 1b. Films prepared from formulations with higher concentration produce significantly larger agglomerates, 300 to 400 nm in diameter, and thus films with inhomogeneous thickness. In addition, these films exhibit large cracks up to 1 μm in width after drying. Formulations with a concentration of less than 0.5 wt % ZnO nanoparticles tend to dewet and leave parts of the surface uncovered, regardless of the type of substrate.

Thin-film transistors were fabricated in bottom-gate (Fig. 1c) or top-gate configuration (Fig. 1d), both on glass and thermally oxidized silicon substrates. Gate electrodes and source/drain contacts were prepared by thermal evaporation of aluminum through a shadow mask. (On some substrates, gold was used for the gates.) As the gate dielectric, a 140 nm thick layer of poly(4-vinylphenol) (PVP) was deposited by spin-coating. On most substrates, the PVP was mixed with a cross-linking agent; these films were thermally cross-linked at a temperature of 200 °C. This temperature is above the glass transition temperature of polyethylene terephthalate (PET) and polyethylene naphthalate (PEN). Although this does not eliminate the possibility of realizing functional devices on such substrates,[27,28] lower process temperatures are of interest. Therefore, in some top-gate devices, PVP films were also prepared without cross-linking agent and dried at 100 °C. For all devices, the semiconductor layer was deposited by spin-coating a 0.5 wt %

[*] Prof. M. Halik, H. Faber, M. Burkhardt, A. Jedaa
Organic Materials & Devices
Institute of Polymer Materials
University Erlangen-Nürnberg
Martensstraße 07, D-91058 Erlangen (Germany)
E-mail: marcus.halik@ww.uni-erlangen.de
Dr. H. Klauk, D. Kälblein
Max Planck Institute for Solid State Research
Heisenbergstraße 1, D-70569 Stuttgart (Germany)

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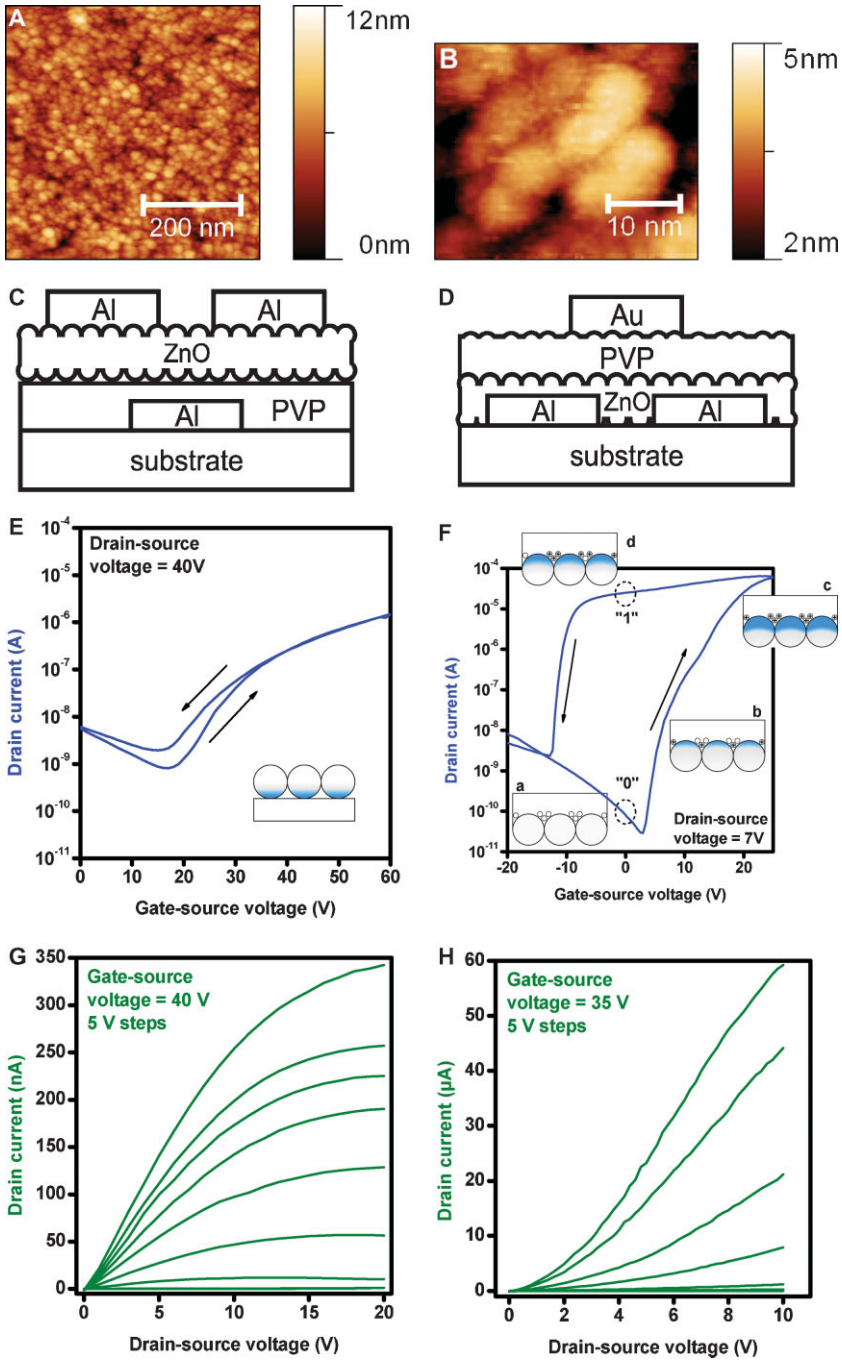

Figure 1. (A) Atomic force microscopy (AFM) image of a ZnO film showing a homogenous distribution of ZnO agglomerates. (B) Scanning tunneling microscopy (STM) image of a single ZnO agglomerate consisting of several core/shell nanoparticles. (C) Schematic cross-section of a bottom-gate TFT. (D) Schematic cross-section of a top-gate TFT. (E) Transfer characteristics of a bottom-gate TFT. The inset depicts the formation of a gate-induced carrier channel in the ZnO film. (F) Transfer characteristics of a top-gate TFT. The inset depicts the formation of a gate-induced carrier channel as well as the trapping and release of positive charges along the PVP/ZnO interface and the associated carrier accumulation in the ZnO. (G) Output characteristics of a bottom-gate TFT. (H) Output characteristics of a top-gate TFT.

suspension of ZnO nanoparticles in MTBE. All TFTs have a channel length (L) of 20 μm and a channel width (W) of 300 μm.

The electrical characteristics of ZnO TFTs in bottom-gate (Fig. 1e,g) and top-gate configuration (Fig. 1f,h) were measured in ambient light and ambient atmosphere. In both configurations, the TFTs show typical n-channel transistor behavior. However, the electron mobility extracted from the transfer characteristics is significantly larger in the top-gate devices ($2.5\,cm^2V^{-1}s^{-1}$) than in the bottom-gate devices ($0.008\,cm^2V^{-1}s^{-1}$).

The bottom-gate TFTs (Fig. 1c,e,g) require relatively large gate-source voltages (up to 60 V) to achieve useful drain current (I_D) modulation. The on/off current ratio is 10^3 and the threshold voltage (V_T) is 27 V. The electron mobility of $0.008\,cm^2V^{-1}s^{-1}$, calculated using equation 1, is comparable to or slightly smaller than the mobility previously reported for ZnO-NP transistors, even though the films in these previous reports were processed at higher temperatures (between 230 and 600 °C).[17,19,29] Due to the large gate-source voltages, the gate current through the PVP gate dielectric is quite large, so that the ratio between drain current and gate current is no greater than 10.

$$I_D = \frac{W}{2L}\mu C_i(V_{GS} - V_T)^2 \quad (1)$$

A completely different behavior is seen for the top-gate devices (Fig. 1d,f,h), even though the materials, process conditions, film thicknesses and transistor dimensions are the same as for the bottom-gate TFTs. The gate-source voltage required to achieve good drain current modulation is much smaller (about 25 V), the drain currents are larger (up to 60 μA), the threshold voltage is smaller (12 V) and the on/off ratio is much larger (10^6) than for the bottom-gate TFTs. Most importantly, the electron mobility calculated from equation 1 is larger by more than two orders of magnitude ($2.5\,cm^2V^{-1}s^{-1}$). Because the maximum gate-source voltage is smaller, the gate currents are smaller and the drain-to-gate-current ratio is usefully large (10^3). Note that the characteristics shown in Figure 1f were obtained from a TFT that was processed with a maximum temperature of 100 °C and after the device had been stored in ambient air for more than six months without significant degradation of the electrical characteristics.

Comparing the output characteristics of the bottom-gate and top-gate TFTs we note that the drain current of the top-gate transistors does not saturate at large drain-source voltages, and that the top-gate TFTs appear to have larger contact resistance than the bottom-gate TFTs, which may be related to a thin layer of native oxide forming on the surface of the Al source and drain contacts. Also, unlike the bottom-gate TFTs, the top-gate devices have a large hysteresis in the transfer characteristics (about 20 V at a drain current of 10^{-8} A). This hysteresis was observed regardless of the thickness of the PVP dielectric, regardless of whether a cross-linking agent was used or not and regardless of the process temperature (100 or 200 °C).

We believe that the observed differences in the electrical characteristics between top-gate and bottom-gate TFTs are due to the significant differences in the morphology of the semiconductor-dielectric interface as a consequence of the different process flows.

First we want to discuss the bottom-gate devices which show the current-voltage characteristics of a regular field-effect transistor, with negligible hysteresis and good current saturation, but also with relatively small electron mobility (0.008 $cm^2V^{-1}s^{-1}$). For the bottom-gate transistors the ZnO nanoparticles are deposited on the smooth surface of the cross-linked PVP dielectric, which is insensitive to the organic solvents of the ZnO-NP suspension.[30] After spin-coating and drying the ZnO-NP suspension, the nanoparticles form a homogeneous film of 30 nm ± 10 nm thickness. The film is composed of agglomerates with a diameter of about 15–25 nm, as shown in Figure 1a and 1b. The film structure is clearly dominated by agglomerates. The interface between the PVP dielectric and the ZnO-NP film appears as an assembly of densely packed ZnO-NP agglomerates on the smooth PVP surface, as shown schematically in Figure 1c. Due to the spherical shape of the agglomerates this implies the existence of small air gaps between adjacent agglomerates at the interface. When a positive potential is applied to the gate, charge carriers will accumulate inside the agglomerates only in close vicinity (within a few Angstroms) of the ZnO/PVP interface, i.e. only near the "bottom" of the agglomerates, but not in those parts of the agglomerates that make contact with adjacent agglomerates. Carriers traveling from source to drain therefore pass through regions of low carrier density (see Fig. 1e, inset), which causes the apparent mobility calculated using Equation 1 to be small. (Charge transfer between individual ZnO nanoparticles within the agglomerates is expected to be more efficient, due to the gate-induced deformation of the organic ligand shells, as reported for functionalized Au nanoparticle clusters.)[31]

For the top-gate transistors, the PVP dielectric is deposited on top of the dried ZnO-NP film. In this case, the PVP dielectric images the surface roughness of the underlying ZnO film and fills the gaps between the agglomerates along the interface. Consequently, a homogeneous (albeit rough) semiconductor/dielectric interface is formed. For positive gate-source voltages, charge carriers will accumulate along the entire semiconductor/dielectric interface, including those parts of the agglomerates where contact between adjacent agglomerates occurs, so that source and drain are connected by a channel with high carrier density. This explains why the mobility calculated using equation 1 is substantially larger for the top-gate TFTs compared with the bottom-gate TFTs, regardless of whether the PVP was cross-linked or not. For transistors with a semiconductor layer composed of nanoparticle-based agglomerates, the top-gate configuration provides higher performance, due to the more homogeneous semiconductor/dielectric interface.

Equation 1 assumes a planar path for carriers traveling from source to drain. Considering that in our top-gate TFTs the rough semiconductor/dielectric interface forces the carriers to travel along highly non-planar paths, equation 1 possibly underestimates the field-effect mobility by about 50%.

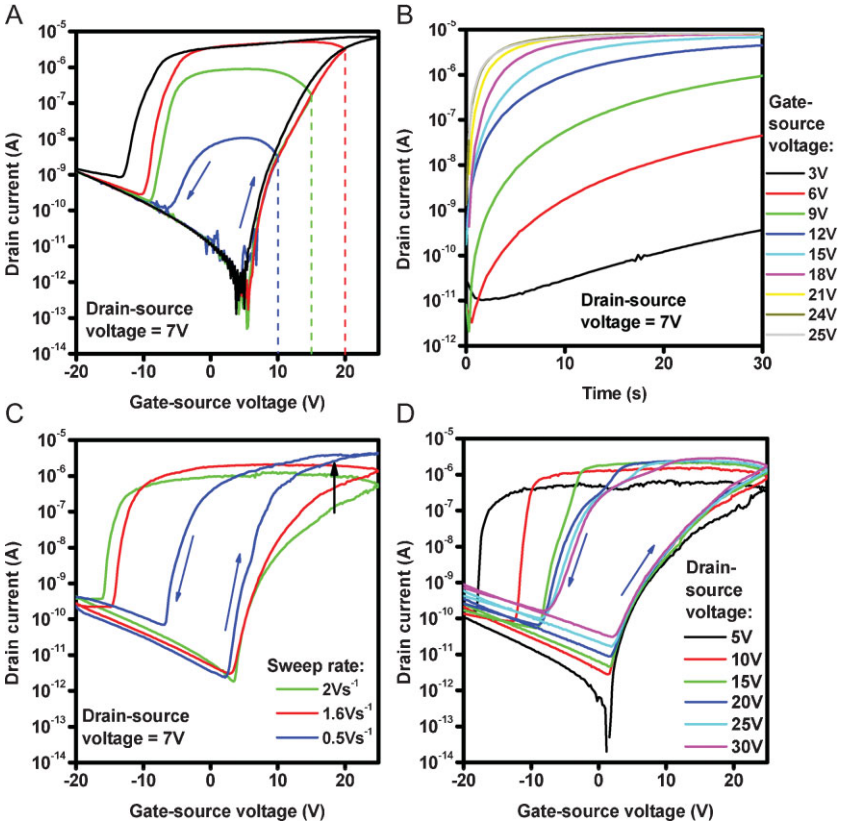

Figure 2. Electrical characteristics of top-gate memory transistors. (A) Transfer characteristics as a function of the maximum gate-source voltage (10, 15, 20, 25 V), showing that the negative gate-source voltage required to return the TFT to the off-state increases. (B) Time-dependent response of the drain current to the application of a positive gate-source voltage, showing that the response is more rapid for larger gate-source voltages. (C) Transfer characteristics for different sweep rates, indicating that the time constant of the trapping/detrapping dynamics is on the order of a few hundred milliseconds. (D) Transfer characteristics for different drain-source voltages, showing that the release of trapped charges is assisted by the lateral electric field.

The transfer characteristics of the top-gate TFTs show a very large hysteresis of about 20 V (defined here as the difference in the gate-source voltages at which the drain current is 10^{-8} A during forward and reverse sweeps; see Fig. 1f). At a gate-source voltage $V_{GS} = 0$ V, two logic states of high conductance (''1'') and low conductance (''0'') can be distinguished, depending on the sweep direction. These two states are relatively stable over time, even in the absence of a supply voltage, so that the device can be employed as a non-volatile memory transistor. The conductance ratio between the two states (at $V_{GS} = 0$ V) is 3×10^5, which is sufficient for practical applications.

Since the hysteresis of about 20 V is observed regardless of the composition and processing conditions of the PVP dielectric, we believe the hysteresis is due to an interface effect, rather than a bulk effect.[32] When the gate-source voltage is swept from negative to positive values, the semiconductor is initially free of carriers (Fig. 1f, inset a), i.e. the threshold voltage is positive, and a gate-source voltage more positive than 5 V is required to induce a carrier channel. For large positive gate-source voltages, however, positive charges from the PVP (perhaps mobile ions) are trapped along the rough PVP/ZnO interface (Fig. 1f, inset b,c). When the gate-source voltage is now swept back to zero, these charges remain trapped at the PVP/ZnO interface and continue to accumulate a carrier channel in the ZnO (Fig. 1f, inset d), so that a large drain current is measured even at zero gate-source voltage (i.e., the threshold voltage is now negative). The application of a negative gate-source voltage (about −7 V) is required to release and remove the trapped charges from the interface, so that the condition for charge accumulation in the ZnO is eliminated, the carrier channel disappears, and the transistor returns to the off-state.

Figure 2a shows that when the forward sweep is extended to larger positive gate-source voltages (10, 15, 20, 25 V), the negative gate-source voltage required to return the TFT to the off-state also increases (−7, −9, −11, −13 V). This suggests that a larger positive gate-source voltage increases the energy required to release the charges trapped at the interface.

Figure 2b shows that the time-dependent response of the drain current to the sudden application of a positive gate-source voltage is more rapid for larger gate-source voltages. In other words, the drain current approaches the steady state more rapidly when the gate-source voltage is larger. This indicates that the time between the application of the positive gate-source voltage and the trapping of the charges at the PVP/ZnO interface is shorter when the transverse electric field is larger, suggesting a field-dependent drift velocity of the trapped charges in the PVP dielectric.

To estimate the time constants of the trapping/detrapping behavior, the gate-source voltage was swept from negative to positive and back to negative values with three different sweep rates, as shown in Figure 2c. As can be seen, the trapping and detrapping behavior is in fact time-dependent, although the time constants appear to be quite large (several hundred milliseconds).

Figure 2d shows that the detrapping dynamics also depend on the drain-source voltage, i.e. on the lateral electric field. When the lateral field is larger, the negative gate-source voltage required to release the charges trapped at the PVP/ZnO interface during the forward sweep is notably reduced (from −18 to −8 V). This behavior is reminiscent of the Poole-Frenkel effect by which the release of trapped charges is accelerated by a lateral electrical field.[33]

In addition to a large conductance ratio between the two memory states, the time-dependent stability of the conductance in each of the states (retention time) is also important. Figure 3a shows that the conductance of the OFF state is very stable, while the conductance of the ON state decreases quite rapidly over time, due to the field-assisted release of the trapped charges in the presence of a drain-source voltage ($V_{DS} = 7$ V). As a result, the conductance ratio decreases from above 10^5 to less than 10^2 within 20 min. The loss of ON-state conductance is expected to be smaller if a smaller or no drain-source voltage is applied during the retention measurement (absence of field-assisted detrapping). For realistic applications, retention times of several years will be required; this will require further optimization of the charge trapping characteristics of the PVP/ZnO interface.

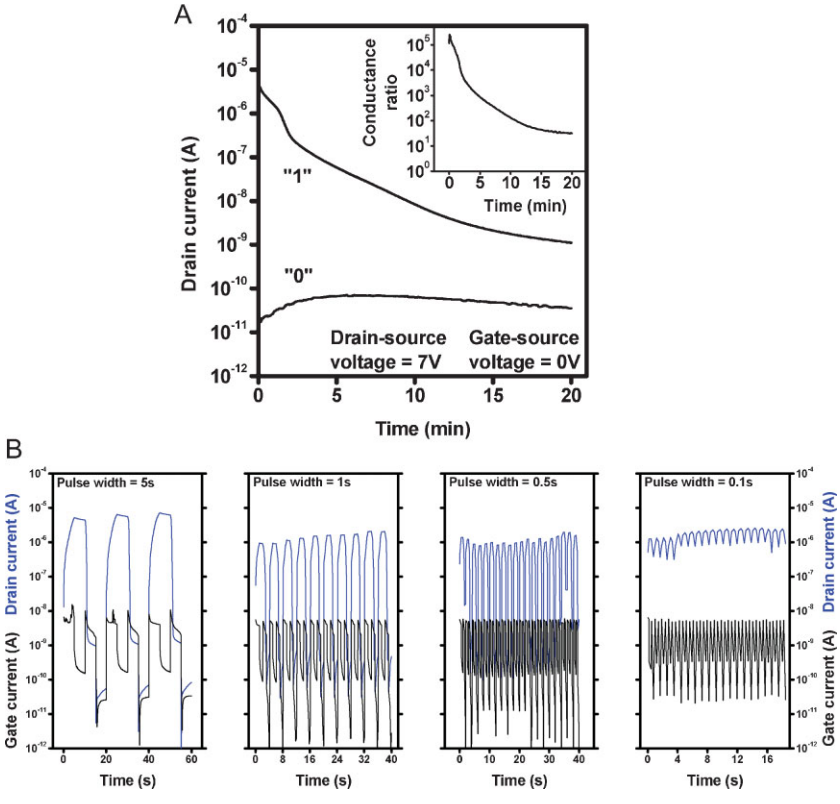

Figure 3. (A) Time-dependent stability of the conductance in the two memory states. The OFF-state (''0'') was obtained with a gate-source voltage of −20 V, the ON-state (''1'') with a gate-source voltage of 25 V, each applied for 5 s. The inset shows the conductance ratio. (B) Switching dynamics for different pulse widths of the program and erase pulses. The drain-source voltage is 7 V.

In order to probe the time required to switch the transistor between the two memory states, the gate-source voltage was cycled between the OFF state (erase pulse, $V_{GS} = -20$ V) and the ON state (program pulse, $V_{GS} = 25$ V) with pulse widths ranging from 5 s to 0.1 s, and the drain and gate currents were recorded continuously for a drain-source voltage of 7 V. After each erase and program pulse, a read pulse was applied ($V_{GS} = 0$ V). Figure 3b shows that the conductance ratio decreases with decreasing pulse width, from 10^5 for a pulse width of 5 s, to 10^4 for a pulse width of 0.5 s, to about 10^1 for a pulse width of 0.1 s. This is consistent with the data shown in Figure 2c, from which the time constant associated with the trapping/detrapping behavior was estimated to be in the range of a few hundred milliseconds. For a pulse width of 0.1 s, the conduction ratio is limited by incomplete detrapping of the charges, which suggests that for these particular program and erase voltages (−20 and 25 V), the detrapping takes somewhat longer than the trapping. Using a pulse width of 1 s we have applied more than 100 erase/read/program/read cycles without degradation of the conductance ratio, suggesting good endurance characteristics.

In summary, we have demonstrated thin-film transistors based on ZnO nanoparticles for the semiconductor and polyvinylphenol as the gate dielectric, both processed from solution and with a maximum temperature of 100 °C to ensure compatibility to flexible polymeric substrates. Field-effect mobilities of $0.008\ cm^2V^{-1}s^{-1}$ for bottom-gate TFTs and $2.5\ cm^2V^{-1}s^{-1}$ for top-gate TFTs were obtained. The top-gate TFTs show non-volatile memory properties with a large, stable hysteresis and a conductance ratio of more than 10^5. We believe the memory effect is due to the voltage-controlled trapping and release of positive charges at the rough semiconductor/dielectric interface. The memory transistors operate in ambient air, have good shelf-life (more than six months), and useful endurance properties.

Experimental

Device fabrication: All bottom-gate and top-gate transistors were fabricated on glass substrates. For the top-gate TFTs, 30 nm thick aluminum source and drain contacts were deposited by thermal evaporation through a shadow mask (channel length 20 μm, channel width 300 μm). ZnO films were prepared by spin-coating (2000 rpm, 20 s) a solution of zinc oxide nanoparticles in methyl tert-butyl ether (0.5 wt% ZnO), followed by drying for 6 min at a temperature of 50 °C in air. For the dielectric layer, a solution of poly(4-vinylphenol) (PVP, 8 g, $M_W = 20\,000$) and the cross-linking agent poly(melamine-co-formaldehyde) methylated (1.6 g) in propylene glycol monomethyl ether acetate (PGMEA, 86.4 g) was deposited by spin-coating, followed by drying for 1 min at a temperature of 100 °C and cross-linking for 6 min at a temperature of 200 °C. The film thickness is about 140 nm, and the dielectric capacitance is 23 $nFcm^{-2}$. On some substrates the PVP was prepared without cross-linking agent; these films were dried for 20 h in a reduced pressure (10 mbar) at a temperature of 100 °C, but not cross-linked, so these TFTs are fully compatible with flexible polymeric substrates (maximum process temperature 100 °C). The top-gate TFTs were completed by thermal evaporation of 40 nm thick gold gate electrodes through a shadow mask. For the bottom-gate TFTs, aluminum gate electrodes were deposited first, followed by PVP gate dielectric, ZnO nanoparticles semiconductor layer, and aluminum source and drain contacts, using essentially the same process parameters as for the top-gate TFTs.

Characterization: Film thickness and morphology were characterized by scanning electron microscopy (Zeiss Ultra 55) and atomic force microscopy (Veeco di 300, nanoscope IIIa). Scanning tunneling microscopy was performed using a nanosurf easy scan 2. Electrical characterization was carried out in ambient air using an Agilent 4156C Semiconductor Parameter Analyzer.

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