



Dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNNT) thin-film transistors with improved performance and stability

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ARTICLE INFO

Article history:

Received 9 February 2011

Received in revised form 27 April 2011

Accepted 28 April 2011

Available online 19 May 2011

Keywords:

Organic thin-film transistors

Air stability

Bias-stress stability

ABSTRACT

Organic thin-film transistors based on the vacuum-deposited small-molecule conjugated semiconductor dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNNT) have been fabricated and characterized. The transistors have field-effect mobilities as large as $2 \text{ cm}^2/\text{V s}$ and an on/off ratio of 10^8 . Owing to the large ionization potential of DNNT, the TFTs show excellent stability for periods of several months of storage in ambient air. Unipolar ring oscillators based on DNNT TFTs with a channel length of $10 \mu\text{m}$ oscillate with a signal propagation delay as short as $7 \mu\text{sec}$ per stage at a supply voltage of 5 V . We also show that DNNT TFTs with usefully small channel width/length ratio are able to drive blue organic LEDs to a brightness well above that required for active-matrix displays.

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Organic thin-film transistors (TFTs) are of interest for rollable or foldable active-matrix displays [1–4], conformable sensor or actuator arrays [5–8], and flexible identification tags [9,10]. One of the challenges in the development of organic TFTs is to find a conjugated semiconductor that provides both a large field-effect mobility and a good stability during operation in ambient air. For many years, the small-molecule hydrocarbon pentacene has enjoyed immense popularity, because pentacene TFTs can be operated in air and initially provide relatively large mobilities, usually around $1 \text{ cm}^2/\text{V s}$ or above [1–10]. The main problem with pentacene is that the molecules easily oxidize in air [11], so that the field-effect mobility decreases over time when the devices are exposed to air. The air-induced mobility degradation can be avoided by encapsulation [12–

15], but from the standpoint of manageable process complexity, a conjugated semiconductor with a strong intrinsic resistance against oxidation is very desirable. With this in mind, a fused heteroarene, dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNNT) has recently been synthesized that is characterized by a larger ionization potential (and hence better air stability) than pentacene, and by a crystal structure and thin-film morphology that promotes high-mobility charge transport, similar to pentacene [16–19].

Here we report on the performance and stability of inverted staggered (bottom-gate, top-contact) DNNT TFTs that utilize a high-capacitance gate dielectric which allows the transistors to operate with voltages of about 3 V [20–23]. The initial field-effect mobility extracted from the transfer characteristics of the TFTs is $2.1 \text{ cm}^2/\text{V s}$ when the channel length is sufficiently long ($50 \mu\text{m}$) so that the influence of the contact resistance on the device resistance is negligible, and $1.2 \text{ cm}^2/\text{V s}$ for shorter channel length ($10 \mu\text{m}$). These mobilities are slightly larger compared

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with the mobilities previously reported for low-voltage DNNT TFTs [23]. Compared with the previous report [23] the thickness of the DNNT layer has been reduced from 30 to 25 nm, which is expected to reduce the parasitic potential drop associated with the vertical current path between the source/drain contacts (located on top of the semiconductor) and the carrier channel (located at the bottom of the semiconductor) and hence is expected to increase the transconductance and effective mobility of the TFTs [24].

The TFTs and circuits were fabricated on glass (Corning Eagle 2000) or flexible polyethylene naphthalate (Teonex[®] Q65 PEN; kindly provided by William A. MacDonald, DuPont Teijin Films, Wilton, UK). Aluminum with a thickness of 20 nm was evaporated directly onto the substrate through a polyimide shadow mask (CADiLAC Laser, Hilpoltstein, Germany) to define the gate electrodes. The aluminum was briefly exposed to an oxygen plasma to create a 3.6 nm thick AlO_x film, followed by immersion of the substrate in a 2-propanol solution of *n*-tetradecylphosphonic acid to form a 1.7 nm thick self-assembled monolayer (SAM) on the surface of the oxidized gates. This results in an AlO_x/SAM gate dielectric with a thickness of 5.3 nm and a capacitance of 800 nF/cm² [25–27]. A 25 nm thick DNNT layer was vacuum-deposited through a shadow mask, followed by the deposition of 30 nm thick gold through another shadow mask to define the source/drain contacts. The channel length is between 10 and 50 μm and the channel width is 100 μm or 200 μm. The maximum process temperature is 60 °C (the substrate temperature during the DNNT deposition). Fig. 1. shows the chemical structure of the semiconductor DNNT, a schematic cross-section of the TFTs, and photographs of a TFT with a channel length of 10 μm. All electrical measurements, including the shelf-life and bias-stress measurements, were performed in ambient air at room temperature.

The static performance of the flexible DNNT TFTs measured shortly after fabrication is summarized in Fig. 2. The TFTs have an on/off ratio of 10⁸ and a subthreshold swing of 100 mV/decade. For the shortest channel length ($L = 10 \mu\text{m}$), the transconductance (normalized to the

channel width) reaches 0.12 S/m. This is a factor of three larger than the transconductance of pentacene TFTs based on the same fabrication process and the same channel length fabricated on glass substrates [20] and similar to the transconductance of photolithographically patterned bottom-contact pentacene TFTs with a channel length of 5 μm on flexible polymeric substrates recently reported by the IMEC group [10]. The field-effect mobility extracted from the transfer characteristics of our DNNT TFTs in the saturation regime ranges from 1.2 cm²/V s ($L = 10 \mu\text{m}$) to 2.1 cm²/V s ($L = 50 \mu\text{m}$). The observation that the mobility extracted from the transfer characteristics decreases with decreasing channel length indicates that the relative contribution of the contact resistance to the total device resistance increases with decreasing channel length. This effect has been analyzed in detail for pentacene TFTs [28] and is expected to be even more pronounced for DNNT TFTs, since the larger ionization potential of DNNT (5.4 eV) compared with pentacene (5.0 eV) [18] is expected to produce a larger energy barrier at the interface between the semiconductor and the Au source and drain contacts (Fermi energy about 5 eV), and hence a larger contact resistance.

Fig. 3a. shows how the saturation mobility of a flexible DNNT TFT with a channel length of 50 μm evolves over time when the substrate is kept in ambient air with a humidity of 40–70% under weak yellow light (laboratory conditions). The mobility decreases from initially 2.1 to 2.0 cm²/V s after three months and then to 1.5 cm²/V s after a total of eight months in air. For comparison, Fig. 3a. also shows that the DNNT TFTs have substantially better air stability than pentacene TFTs fabricated with the same technology (i.e., same type of substrate, same gate dielectric, same contacts).

Although the air stability of the DNNT transistors is better than that of the pentacene devices, there is a slight drop in the mobility of the DNNT TFTs, from initially 2.1 to 1.5 cm²/V s after eight months in air. The mechanism for this slow degradation is unknown. Although oxidation of the DNNT molecules cannot be completely ruled out, it is unlikely given the molecular structure of DNNT. An alternative explanation for the observed mobility degradation is that air-borne molecules (e.g., H₂O, O₂, O₃) penetrate into the grain boundaries of the polycrystalline DNNT film and then interact with the mobile charge carriers or with the DNNT molecules at or near the grain boundaries in a way that is detrimental for the field-effect mobility [29,30].

In addition to the shelf-life stability we have also investigated the bias-stress stability. Fig. 3b illustrates the time-dependent decrease in drain current and the associated shift in threshold voltage of DNNT TFTs fabricated on a glass substrate during prolonged gate-bias stress. As in the case of TFTs based on hydrogenated amorphous silicon [31,32] and pentacene [33] the drain current decays faster when the applied gate-source voltage is larger. The reason is that a larger gate-source voltage results in a larger carrier density in the channel and hence in a larger trapping rate. The carrier density accumulated in the transistor channel at a certain gate-source voltage can be estimated as follows:

$$n = \frac{1}{q} C_{\text{diel}} |V_{\text{GS}} - V_{\text{th}}| \quad (1)$$

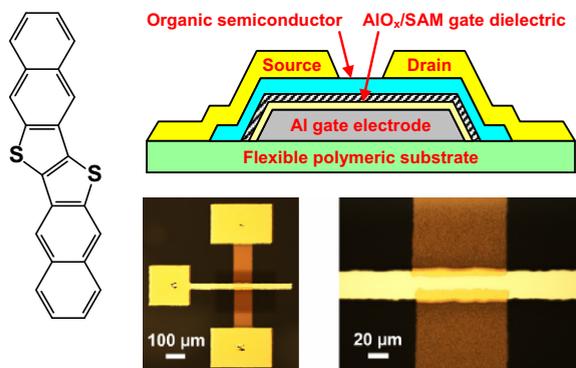


Fig. 1. Chemical structure of the conjugated organic semiconductor dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNNT), schematic TFT cross-section, and photographs of a DNNT TFT with a channel length of 10 μm and a channel width of 100 μm patterned using polyimide shadow masks.

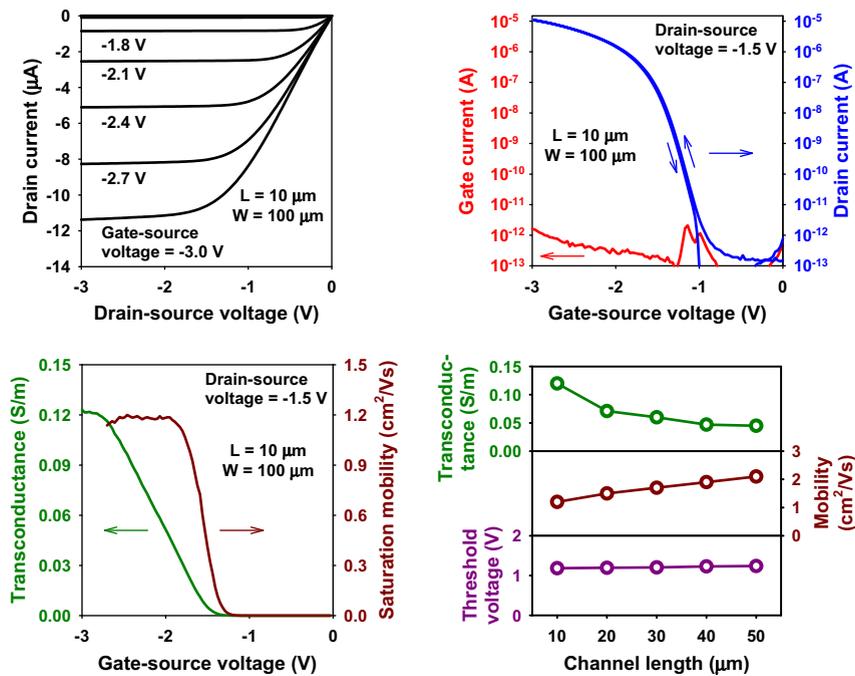


Fig. 2. Electrical characteristics of a DNTT TFT with a channel length of 10 μm . The transconductance has been normalized to the channel width ($W = 100 \mu\text{m}$). The influence of the channel length on the transconductance, the saturation mobility extracted from transfer characteristics and the threshold voltage is also shown.

where q is the elementary charge (1.6×10^{-19} C), C_{diel} is the capacitance of the gate dielectric per unit area, and V_{th} is the threshold voltage. According to Eq. (1), the carrier density in our DNTT TFTs ($C_{\text{diel}} = 800 \text{ nF/cm}^2$, $V_{\text{th}} = -1.4 \text{ V}$) is about $8 \times 10^{12} \text{ cm}^{-2}$ at a gate-source voltage of -3 V and $3 \times 10^{12} \text{ cm}^{-2}$ at a gate-source voltage of -2 V . In addition to the carrier density it is also useful to estimate the sheet resistance of the transistor channel, as suggested by the Princeton group [32]:

$$R_{\text{sheet}} = \frac{V_{\text{DS}}}{I_{\text{D}}} \frac{W}{L} \quad (2)$$

where V_{DS} is the drain-source voltage, I_{D} is the drain current, W is the channel width, and L is the channel length. According to Eq. (2), the sheet resistance of the DNTT TFT in Fig. 3b. ($W = 100 \mu\text{m}$, $L = 30 \mu\text{m}$) in the linear regime ($V_{\text{DS}} = -0.1 \text{ V}$) is about $1 \text{ M}\Omega/\text{sq}$ at a gate-source voltage of -3 V and $2.5 \text{ M}\Omega/\text{sq}$ at a gate-source voltage of -2 V . When the DNTT TFTs are stressed with a gate-source voltage of -3 V it takes 10^4 s for the drain current to decay by 10%, whereas at a gate-source voltage of -2 V the lifetime for a 10% decay is 10^5 s . These lifetimes are similar to those reported by the Princeton group for a-Si:H TFTs fabricated at a temperature of $285 \text{ }^\circ\text{C}$ [31,32] despite the fact that the DNTT TFTs were fabricated at a more flexible-substrate-friendly temperature of $60 \text{ }^\circ\text{C}$.

A direct comparison between the bias stress-induced drain-current decay of DNTT and pentacene TFTs is more difficult, since the drain current of pentacene TFTs decays in part simply due to the rapid oxidation of the pentacene molecules. In order to decouple the bias stress-induced threshold-voltage shift from the oxidation-induced degra-

dation, the MIT group has performed bias-stress measurements on the pentacene TFTs in nitrogen [33]. However, since their pentacene TFTs utilized a different gate dielectric (parlylene-N), a direct comparison with our DNTT TFTs is not possible.

To assess the dynamic performance of the TFTs we have fabricated unipolar ring oscillators based on inverters with saturated load [20,23]. The drive TFTs have a channel length of $10 \mu\text{m}$ and a gate overlap of $15 \mu\text{m}$, from which a gate capacitance of $0.3 \text{ pF}/\mu\text{m}$ (normalized to the channel width) can be estimated. Fig. 4 shows the signal delay per stage of a 5-stage ring oscillator on a glass substrate measured as a function of supply voltage. At a supply voltage of -5 V , the stage delay is $7 \mu\text{s}$. This is the shortest signal delay reported for an organic ring oscillator at this supply voltage (5 V), and it is within a factor of 20 of the fastest organic ring oscillators reported to date [10], despite the smaller supply voltage (5 V instead of 10 V) and the more relaxed channel length ($10 \mu\text{m}$ instead of $2 \mu\text{m}$).

Although functional active-matrix displays based on organic light-emitting diodes (LEDs) and organic TFTs have been demonstrated [1,3,4], there is some uncertainty about whether organic TFTs are capable of driving organic LEDs to the brightness required for practical display applications [34]. Fig. 5 shows photographs of a blue organic LED controlled by a DNTT TFT for five different gate-source voltages. The TFT has a channel width (W) of $200 \mu\text{m}$ and a channel length (L) of $10 \mu\text{m}$ ($W/L = 20$). The LED is a bottom-emitting fluorescent low-voltage device manufactured by Novaled [35,36] and has an active area of 0.067 cm^2 . This area is about 1000 times larger than the pixel area in a notebook computer display (e.g., the area

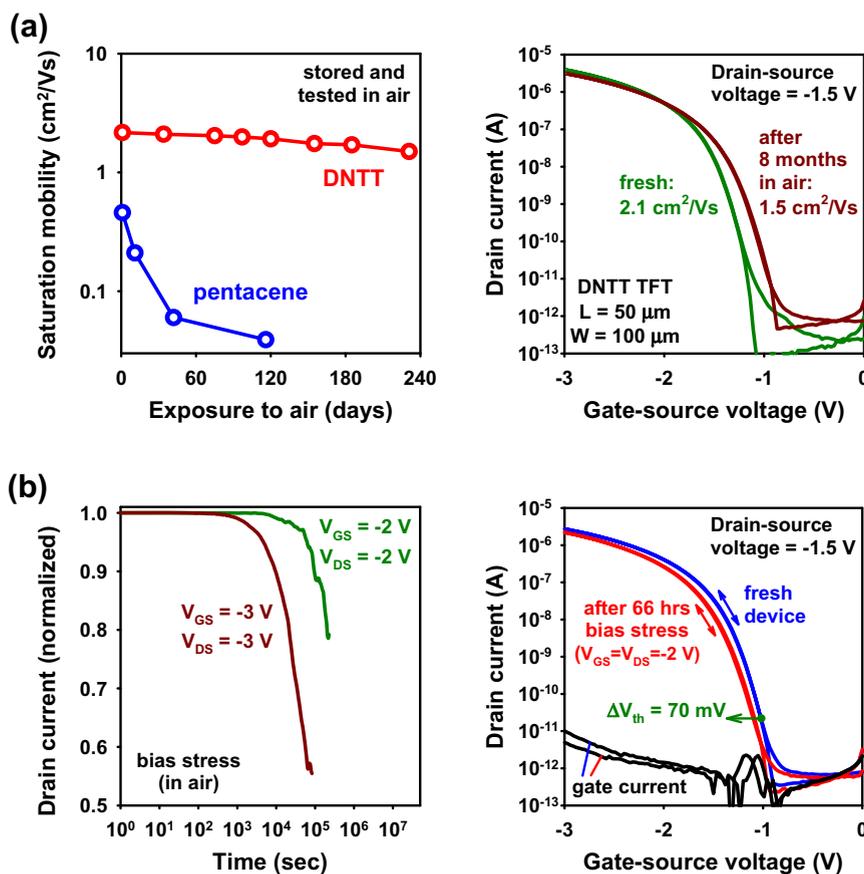


Fig. 3. (a) Shelf-life stability of a DNTT TFT (channel length 50 μm) in comparison to that of a pentacene TFT based on the same technology. (b) Bias-stress stability of DNTT TFTs (channel length 30 μm).

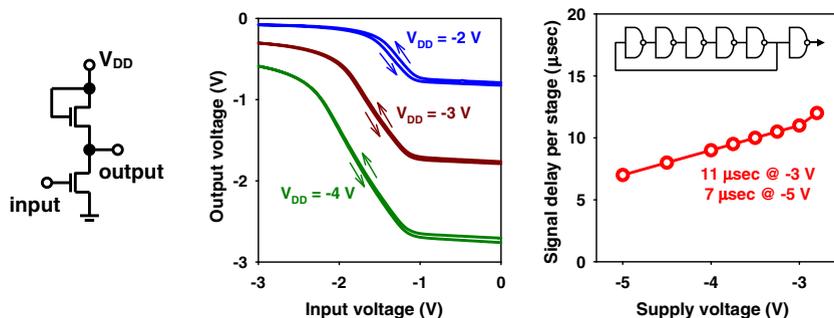


Fig. 4. Circuit schematic and transfer characteristics of a unipolar inverter with saturated load, and signal delay per stage as a function of supply voltage for a unipolar five-stage ring oscillator based on DNTT TFTs (channel length 10 μm, gate overlap 15 μm).

of an RGB subpixel in a display with a 17-inch diagonal and SXGA resolution is about $7 \times 10^{-5} \text{ cm}^2$). The LED has a luminous efficiency of 7 cd/A and CIE color coordinates of 0.14/0.25. The LED and the TFT were connected using a BNC cable. When a gate-source voltage of -3.5 V is applied to the TFT and a potential of -5 V to the cathode of the LED, the TFT drives a current of 67 μA through the LED. At this current, the potential difference between source and drain of the TFT is 2.2 V and the potential difference between anode and cathode of the LED is 2.8 V. The current

of 67 μA produces a luminance of 70 cd/m², which is within an order of magnitude of the maximum brightness of most commercially available computer monitors (typical display brightness: ~500 cd/m²; typical subpixel brightness: 600–1500 cd/m²). Assuming the luminance is approximately proportional to the current density, a TFT with $W/L = 1$ would be able to drive an LED with the same efficiency (7 cd/A), but with a typical display subpixel area of 10^{-4} cm^2 to a brightness of 2500 cd/m², which is well above the maximum brightness required for most display

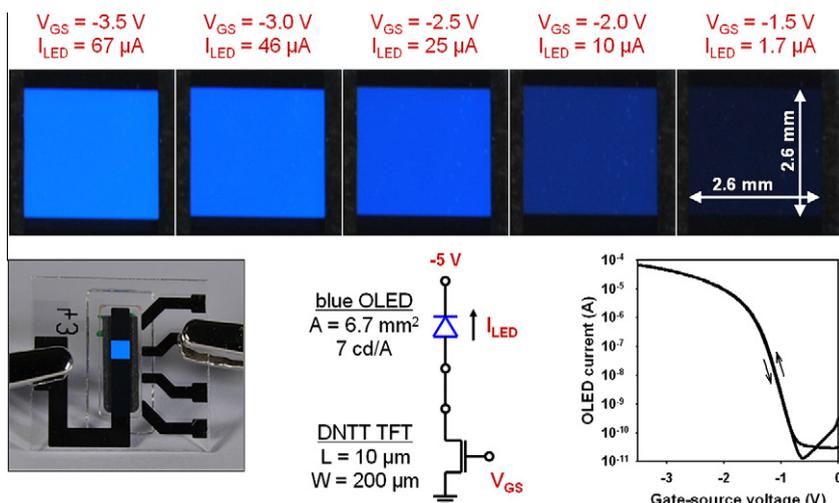


Fig. 5. Photographs of a blue organic light-emitting diode (LED) with an area of 6.7 mm² controlled by a DNTT TFT with a channel width of 200 μm and a channel length of 10 μm. At the maximum gate-source voltage (−3.5 V), the luminance of the organic LED reaches 70 cd/m². (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

applications. Organic LEDs based on phosphorescent emitter materials, which typically have luminous efficiencies between 30 and 70 cd/A, depending on color [35–37], would reach a brightness of 10,000–20,000 cd/m² when controlled by a DNTT TFT with $W/L = 1$. This clearly shows that organic TFTs even with the smallest possible footprint ($W/L = 1$) are fully capable of providing the electrical current required to drive organic LEDs in active-matrix displays.

In summary we have evaluated the current–voltage characteristics, the air stability, the bias–stress stability, the dynamic performance, and the OLED-drive capability of low-voltage TFTs based on the organic semiconductor dinaphtho-thieno-thiophene (DNTT), a fused heteroarene with large ionization potential. We have found that DNTT TFTs have larger mobility, better air stability, better bias–stress stability, and better dynamic performance than pentacene TFTs fabricated with the same technology, suggesting that DNTT has great potential for organic electronics, including flexible active-matrix OLED displays.

Acknowledgements

The authors thank Richard Rook at CADiLAC Laser for providing high-quality shadow masks and Carmen Müller at the Max Planck Institute for Solid State Research for professional photography. We gratefully acknowledge financial support provided by the New Energy and Industrial Technology Development Organization (NEDO) of Japan.

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