LETTERS

Ultralow-power organic complementary circuits

Hagen Klauk[1], Ute Zschieschang[1], Jens Pflaum[2] & Marcus Halik[3]

The prospect of using low-temperature processable organic semiconductors to implement transistors, circuits, displays and sensors on arbitrary substrates, such as glass or plastics, offers enormous potential for a wide range of electronic products[1]. Of particular interest are portable devices that can be powered by small batteries or by near-field radio-frequency coupling. The main problem with existing approaches is the large power consumption of conventional organic circuits, which makes battery-powered applications problematic, if not impossible. Here we demonstrate an organic circuit with very low power consumption that uses a self-assembled monolayer gate dielectric and two different air-stable molecular semiconductors (pentacene and hexadecafluorocopperphthalocyanine, F_{16}CuPc). The monolayer dielectric is grown on patterned metal gates at room temperature and is optimized to provide a large gate capacitance and low gate leakage currents. By combining low-voltage p-channel and n-channel organic thin-film transistors in a complementary circuit design, the static currents are reduced to below 100 pA per logic gate. We have fabricated complementary inverters, NAND gates, and ring oscillators that operate with supply voltages between 1.5 and 3 V and have a static power consumption of less than 1 nW per logic gate. These organic circuits are thus well suited for battery-powered systems such as portable display devices[2] and large-surface sensor networks[3] as well as for radio-frequency identification tags with extended operating range[4].

The gate–source voltage V_{GS} required to induce a charge density Q in the channel of a field-effect transistor is determined by the gate dielectric capacitance C: $V_{GS} = Q/C = Qt/\varepsilon\varepsilon_0$, where t and ε are the thickness and permittivity of the dielectric, respectively. Thus the operating voltage of a transistor scales with the dielectric thickness. A promising path to high-mobility, low-voltage organic transistors is the use of gate dielectrics based on molecular self-assembled monolayers (SAMs) that provide a capacitance approaching 1 μF cm^{-2} and thus allow organic transistors to operate with voltages of a few volts. So far, SAM-dielectric organic transistors have been demonstrated only on silicon[5–8] and on substrates coated with indium tin oxide[7]. The implementation of high-performance integrated circuits, however, requires a gate material with large electrical conductivity that can be deposited at low temperatures on an insulating substrate to define individual gate electrodes for each transistor. Here we describe how to grow high-quality SAM dielectrics with very small leakage currents on evaporated, patterned aluminium gates. We found that the charge leakage through SAMs on aluminium is no larger than the leakage through high-quality SAMs on silicon[5–7], suggesting that SAMs on aluminium can be densely packed, as in the case of SAMs on silicon.

Whereas the formation of SAMs on natively oxidized silicon is best facilitated with silane anchor groups[9], we have chosen phosphonic acid anchor groups for self-assembly on aluminium[10–12]. Figure 1a shows the chemical structure of n-octadecylphosphonic acid, which we selected for this work. SAMs were prepared in a solution of 2-propanol at room temperature[12]. Substrates were glass or flexible polyethylene naphthalate (for transistors, circuits and leakage-current test structures) or silicon (for X-ray measurements). Aluminium 20 nm thick was deposited by thermal evaporation. Before self-assembly the aluminium surface was briefly exposed to an oxygen plasma (150 W, 15 s). The plasma treatment increases the thickness of the (native) aluminium oxide layer and creates a density of hydroxyl groups sufficient for molecular adsorption. Small-angle

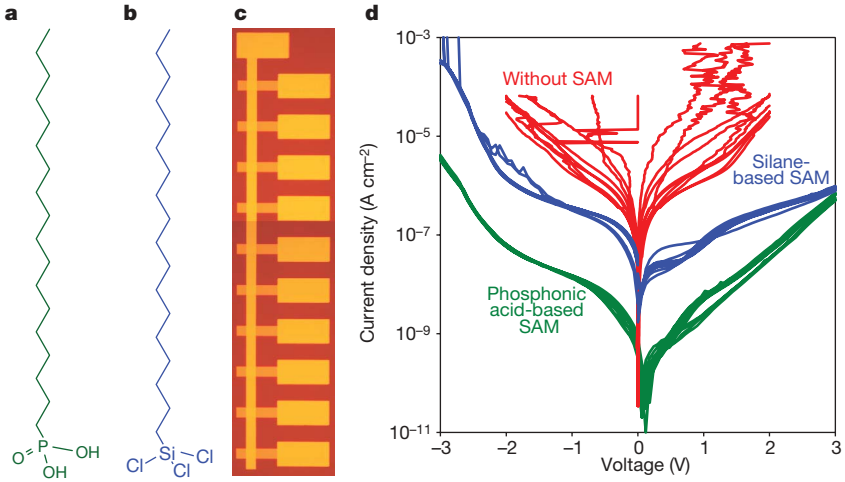

Figure 1 | Self-assembled monolayer dielectrics on metal gates. **a**, Chemical structure of n-octadecylphosphonic acid. **b**, Chemical structure of n-octadecyltrichlorosilane. **c**, Photograph of the leakage current test structure with shadow-mask-patterned aluminium bottom and gold top electrodes. **d**, Leakage current density as a function of applied voltage. Each measurement was repeated on ten junctions to evaluate the uniformity.

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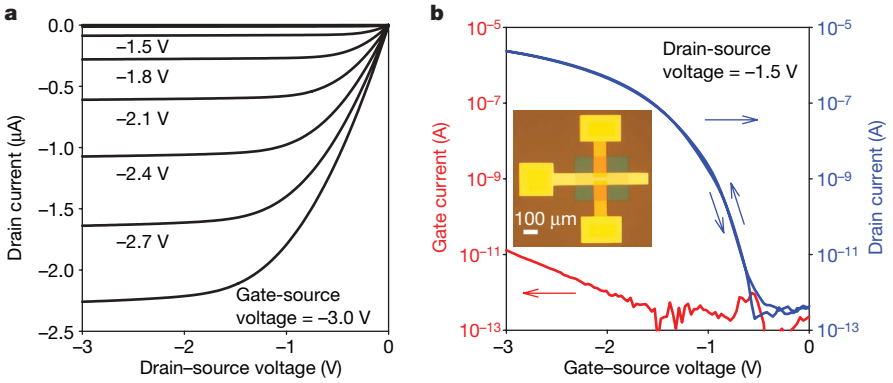

Figure 2 | p-channel pentacene TFT with SAM gate dielectric. The TFT has a channel length of 30 μm and a channel width of 100 μm. **a**, Drain current as a function of drain–source voltage. **b**, Drain current and gate current as a function of gate–source voltage (the inset is a photograph of the transistor). Owing to the small thickness and the good insulating properties of the dielectric the TFT can be operated with low voltages and has a maximum gate current of only 15 pA. The carrier mobility is 0.6 $cm^2 V^{-1} s^{-1}$.

X-ray reflectivity measurements indicate that the thickness of the aluminium oxide increases from 1.8 to 3.8 nm during the plasma treatment (see Supplementary Fig. 1). Static contact angles are 10° before and 105° after SAM preparation, confirming the formation of a hydrophobic monolayer[10]. From the reflectivity measurements we conclude that the SAM has a thickness of 2.1 nm. Assuming the molecules are 2.3 nm long (as calculated using CambridgeSoft Chem3D Pro; www.cambridgesoft.com), this suggests that the molecules stand approximately upright with a tilt angle of about 24° with respect to the surface normal.

Although the SAM adds only 2.1 nm to the total dielectric thickness, it reduces the leakage current density between the plasma-treated aluminium bottom electrodes and thermally evaporated gold top electrodes by three orders of magnitude, from about 5×10^{-5} A cm^{-2} to $(5 \pm 1) \times 10^{-8}$ A cm^{-2} at an applied voltage of 2 V. Figure 1d shows that in comparison with the phosphonic acid-based dielectric, the plasma-grown oxide alone is a poor insulator with substantial leakage currents, small breakdown voltage, and significant device-to-device variation. (Low-voltage organic transistors employing a 5-nm-thick plasma-grown Al_2O_3 dielectric without SAM have been reported[13], but the gate leakage in these devices was $\sim 10^{-5}$ A cm^{-2} at 2 V.) Alkane-silanes also form SAMs on aluminium with large contact angles (100°), but the leakage currents are an order of magnitude larger compared with phosphonic acid SAMs (see Fig. 1d). For comparison, state-of-the-art low-power silicon transistors at the 90 nm technology node with an equivalent oxide thickness of 2.2 nm and a dielectric capacitance of 1.5 μF cm^{-2} have gate current densities around 10^{-3} A cm^{-2} (ref. 14).

The capacitance of our SAM-based dielectric was measured by impedance spectroscopy for frequencies between 1 Hz and 10 kHz for capacitors with contact areas between 0.28 and 1.13 cm^2. The measured capacitance is 0.7 ± 0.05 μF cm^{-2} (see Supplementary Fig. 2). This is approximately the value we calculate if we assume a permittivity of 2.5 for the SAM[15] and of 9 for the aluminium oxide[16], and a thickness of 2.1 nm for the SAM and of 3.6 nm for the aluminium oxide (as indicated by reflectivity measurements on Al/AlO_x/SAM samples, see Supplementary Information; $C_{total} = 1/[1/C_{SAM} + 1/C_{AlOx}]$).

X-ray photoelectron spectroscopy (XPS) was used to evaluate the surface composition. Spectra taken of an aluminium-coated silicon wafer before and after plasma treatment show Al (2*p*) and O (1*s*) signals that can be correlated with Al and AlO_x, but do not show a Si (2*p*) signal, suggesting that the aluminium covers the wafer completely. A spectrum taken after the preparation of a phosphonic acid-based SAM shows a P (2*p*) signal at a binding energy of 133.3 eV. This is the same binding energy observed in a powder sample of n-octadecylphosphonic acid, suggesting that the phosphonic acid group is not significantly altered by the adsorption on the surface. From the XPS data we have calculated the surface coverage of the SAMs and found that the packing density of n-octadecylphosphonic acid SAMs on plasma-treated aluminium is greater by a factor of 2.5 than the packing density of n-octadecyltrichlorosilane on the same surface (4.6 versus 1.9 molecules per nm^2). This may explain the difference in leakage currents and the fact that n-alkylphosphonic acid SAMs provide excellent insulation even in the absence of an aromatic endgroup[6].

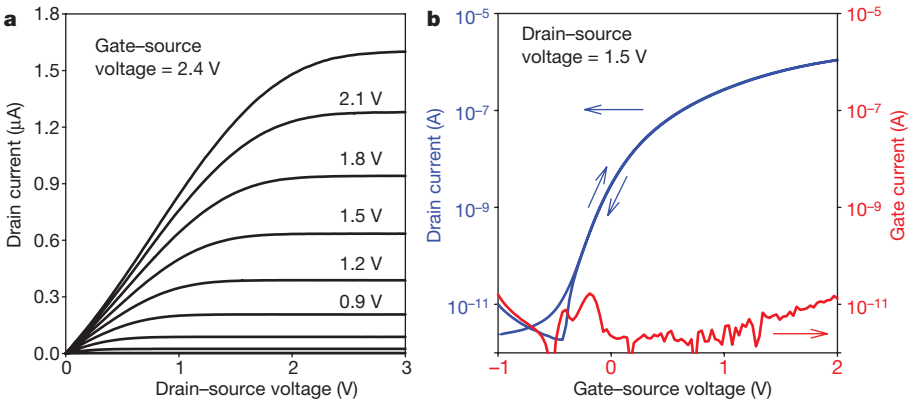

Figure 3 | n-channel F_{16}CuPc TFT with SAM gate dielectric. The TFT has a channel length of 30 μm and a channel width of 1,000 μm. **a**, Drain current as a function of drain–source voltage. **b**, Drain current and gate current as a function of gate–source voltage. The maximum gate current is 15 pA and the carrier mobility is 0.02 $cm^2 V^{-1} s^{-1}$.

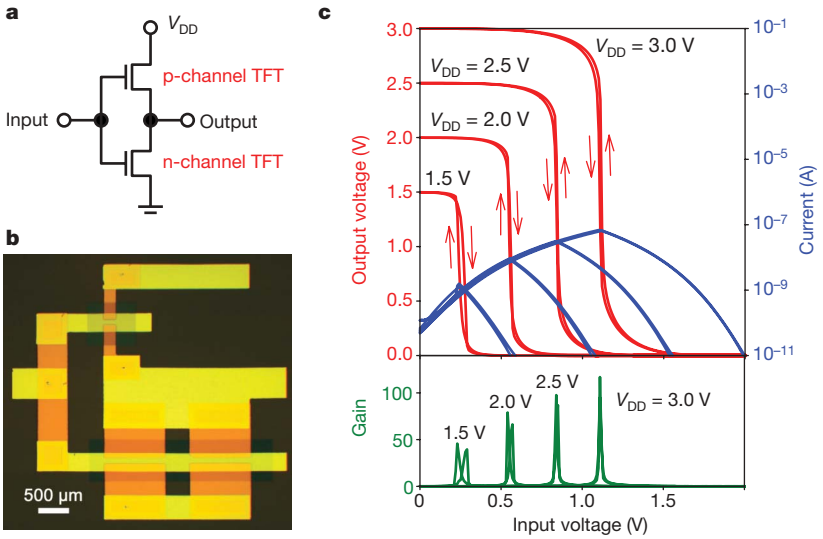

Figure 4 | Complementary inverter with SAM gate dielectric. **a**, Circuit schematic of the inverter. **b**, Photograph of the inverter. **c**, Output voltage, current, and small-signal gain as a function of input voltage for supply voltages between 1.5 and 3.0 V. The inverter shows rail-to-rail output switching, a maximum static current of 100 pA, and a small-signal gain as large as 100.

To prepare organic thin-film transistors (TFTs) and complementary circuits with SAM-based dielectric we have used a five-level shadow-mask process that is outlined in the Supplementary Information. The maximum process temperature is 90 °C. With the exception of the SAM growth, this is an all-dry manufacturing process that avoids the use of toxic or environmentally harmful solvents. We developed an integrated, one-step via process that exploits the specific surface selectivity of the self-assembling molecules during the adsorption process. All electrical measurements were carried out in ambient air at room temperature.

Figure 2 shows the electrical characteristics of a p-channel pentacene TFT with a channel length of 30 μm and a channel width of 100 μm. It has a carrier mobility of 0.6 $cm^2 V^{-1} s^{-1}$, a transconductance of 2.2 μS, a subthreshold swing of 100 mV per decade (see Supplementary Fig. 3), an on/off current ratio of 10^7, and a maximum gate current of 15 pA (see Supplementary Fig. 4 for statistics on 100 devices). These parameters are all similar to those reported previously for SAM gate dielectric TFTs on silicon substrates[6], but here this performance is demonstrated for TFTs with patterned metal gates on glass substrates. The gate current is smaller than the drain current by more than five orders of magnitude, confirming the high quality of the molecular gate dielectric. The mobility of the SAM-dielectric pentacene TFTs is similar to that of hydrogenated amorphous silicon TFTs widely used in commercial flat panel displays. We attribute this large mobility at least in part to the low surface energy[17] and low permittivity[18] of the molecular dielectric. Our organic TFTs can be operated with lower voltages than amorphous silicon TFTs and allow the realization of high-performance complementary devices and circuits.

The electrical characteristics of an n-channel $F_{16}CuPc$ TFT having a channel length of 30 μm, a channel width of 1,000 μm, a mobility of 0.02 $cm^2 V^{-1} s^{-1}$, a subthreshold swing of 160 mV per decade, an on/off ratio of 10^5, and a maximum gate current of 15 pA are shown in Fig. 3 (see also Supplementary Fig. 5). The mobility is similar to the best reported for $F_{16}CuPc$ TFTs on inorganic and on SAM-functionalized dielectrics[19–21].

Using p-channel pentacene and n-channel $F_{16}CuPc$ TFTs we have realized the first low-voltage organic complementary circuits with patterned gates on glass substrates. (Low-voltage organic complementary inverters have been demonstrated using a silicon gate and a 10- to 20-nm-thick polymer dielectric or a 100-nm-thick thermally grown SiO_2 dielectric; see refs 22, 23.) Our inverters with SAM-based gate dielectric show sharp switching with rail-to-rail output swings, large signal gain (~100), and negligible hysteresis for supply voltages as low as 1.5 V (see Fig. 4). Complementary two-input NAND gates also show the correct logic function (see Supplementary Fig. 6). Compared with circuits based on a single carrier type[2–4], complementary circuits consume far less static power, because all transistors of one carrier type are always in the non-conducting off-state, except during switching[24]. Indeed, the static currents (when $V_{in} = 0$ or $V_{in} = V_{DD}$) in our complementary gates are very small: always below 100 pA. Thus, the static power dissipation is less than 1 nW per logic gate, making these truly low-power organic circuits.

Complementary five-stage ring oscillators show stable oscillations for supply voltages as low as 1.5 V, the lowest operating voltage reported for an organic circuit. The circuits oscillate with rail-to-rail output voltage and signal delays as low as 1.4 ms per stage (see Supplementary Fig. 7). Improvements in circuit speed are expected by employing air-stable n-channel organic semiconductors with mobilities similar to pentacene[25] and TFTs with smaller critical dimensions (see Supplementary Fig. 8). All measurements were performed in air without protecting the circuits from ambient oxygen and humidity (see Supplementary Fig. 10 for results of operational stability tests and Supplementary Fig. 11 for shelf-life data).

Finally, we have taken advantage of the simplicity, robustness and low thermal budget of our process and prepared SAM-dielectric devices on flexible, transparent polyethylene naphthalate (PEN). Gate leakage is somewhat larger and carrier mobility is slightly smaller than on glass (see Supplementary Fig. 12), but this is expected when advancing from rigid to flexible substrates[26] and does not preclude the realization of low-power organic circuits on flexible substrates.

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Supplementary Information is linked to the online version of the paper at www.nature.com/nature.

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Metal films were deposited by thermal evaporation in a turbo-pumped vacuum evaporator from a resistively heated tungsten filament. Film thickness was monitored with a quartz crystal. Nominal thickness of the deposited films was 20 nm for aluminum and 30 nm for gold. Atomic force microscopy indicates that the evaporated aluminum films have a root-mean-square (rms) surface roughness of 0.8 nm.

Oxygen plasma treatment of the aluminum surface was performed in a turbo-pumped 13.56 MHz parallel-plate reactive ion etcher evacuated to a base pressure of 10^{-6} mbar and back-filled with oxygen (0.1 mbar, 150 W, 15 sec, substrates at room temperature).

Phosphonic acid self-assembled monolayers were prepared immediately following oxygen plasma treatment by immersing substrates in a 2-propanol solution containing 5 mM of n-octadecylphosphonic acid, $CH_3(CH_2)_{17}PO(OH)_2$ (PolyCarbon Industries, PCI Synthesis, Devens, U.S.A.; see Figure 1a). The solution was kept at room temperature and substrates remained in solution for about 16 hours. Substrates were then rinsed in pure 2-propanol, blown dry with nitrogen, and briefly baked on a hotplate at 60 °C (see ref. 12).

Small-angle X-ray reflectivity measurements were performed on three types of samples. Sample 1 was a natively oxidized silicon wafer with a nominally 20 nm thick layer of aluminum. Sample 2 was a natively oxidized silicon wafer with nominally 20 nm thick aluminum which was exposed to an oxygen plasma (150 W, 15 sec). Sample 3 was a natively oxidized silicon wafer with nominally 20 nm thick aluminum, exposed to an oxygen plasma, and with a self-assembled monolayer of n-octadecylphosphonic acid. Small-angle X-ray reflectivity measurements were performed with Cu-Kα radiation (λ = 1.542 Å) at room temperature. The experimental reflectivity curves were analyzed according to the Parratt algorithm (ref. 27) which allows an estimation of the thickness, roughness, and electron density of each individual layer. The reliability of the estimated quantities is better than 95 %. Measured reflectivity curves along with the curve fits are shown in Figure S1. The values obtained for the thickness and roughness of each layer in each sample are summarized in the following table:

Layer	Sample 1	Sample 2	Sample 3
SAM	-	-	2.1 nm ± 1.4 nm
AlO_x	1.8 nm ± 1.8 nm	3.8 nm ± 0.9 nm	3.6 nm ± 0.2 nm
Al	16.0 nm ± 1.3 nm	16.3 nm ± 1.0 nm	15.8 nm ± 1.5 nm

The leakage current density through the SAM-based dielectric was measured on test structures (see Figure 1c) consisting of shadow-mask-patterned, plasma-treated aluminum bottom electrodes (100 µm wide), phosphonic acid-based SAM, and orthogonal gold top electrodes (100 µm wide) that were implemented along with the TFTs and circuits on the same substrates using the shadow-mask process outlined below, except that in the test structures no organic semiconductor was deposited between the SAM and the gold top electrodes. The area of each test structure was 1×10^{-4} cm^2. Test structures with a silane-based SAM (n-octadecyltrichlorosilane, $CH_3(CH_2)_{17}SiCl_3$; ABCR, Karlsruhe, Germany; see Figure 1b) and without any SAM (in which the insulation between the aluminum bottom electrodes and the gold top electrodes is provided solely by the

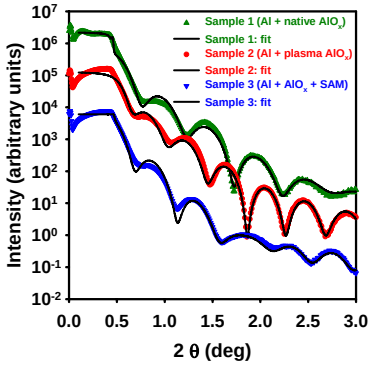

Figure S1 | Small-angle X-ray reflectivity. Measurement data and curve fits (obtained according to the Parratt algorithm) for three samples are shown: Sample 1: nominally 20 nm aluminum, natively oxidized; Sample 2: nominally 20 nm aluminum, exposed to an oxygen plasma; Sample 3: nominally 20 nm aluminum, exposed to an oxygen plasma and covered with a self-assembled monolayer of n-octadecylphosphonic acid.

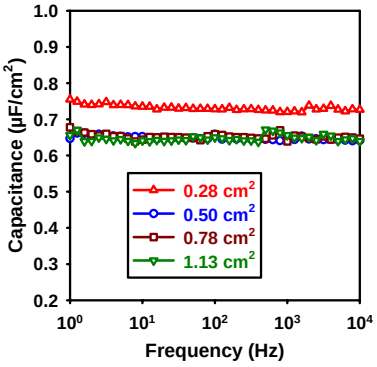

Figure S2 | Capacitance of the phosphonic acid-based SAM dielectric. The capacitance was measured by impedance spectroscopy on four capacitors with oxygen-plasma-treated aluminum bottom electrodes, self-assembled monolayer, and gold top electrodes. Contact area ranges from 0.28 to 1.13 cm^2, and the capacitance is shown as a function of frequency.

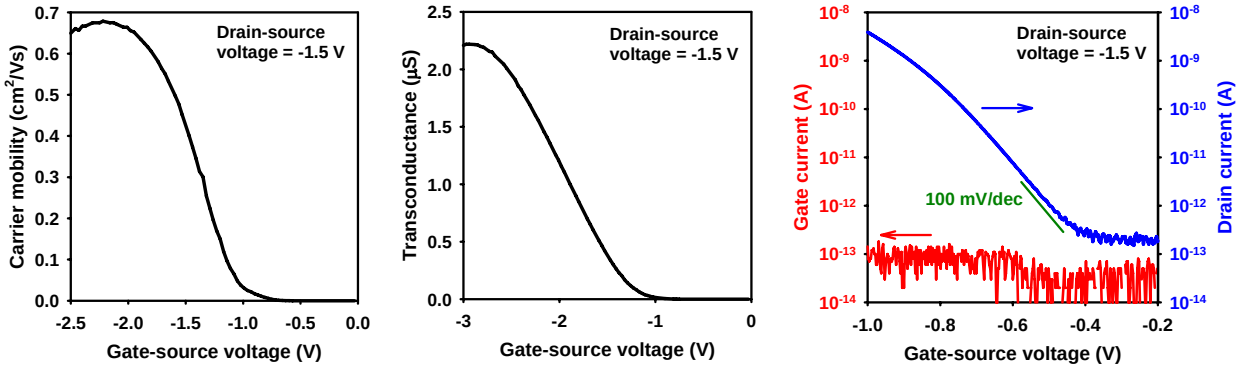

Figure S3 | Carrier mobility, transconductance and subthreshold swing of a p-channel pentacene TFT. The TFT has a channel length of 30 μm and a channel width of 100 μm. Mobility, transconductance and subthreshold drain current are shown as a function of gate-source voltage for a drain-source voltage of -1.5 V.

oxygen-plasma-grown aluminum oxide layer) were prepared for comparison. Results of the leakage current measurements are summarized in Figure 1d.

To prepare low-voltage organic thin-film transistors (TFTs) and low-power organic complementary circuits we have developed a 5-level shadow-mask process. The shadow masks were made by patterning polyimide foils with a thickness of 50 μm using a laser (CADiLAC Laser, Hilpoltstein, Germany; special thanks to Richard Rook). Patterned metal gates and the first level of interconnects were prepared by evaporating 20 nm thick aluminum through a first shadow mask. In order to allow access to the gate electrodes for electrical probing and to define vertical

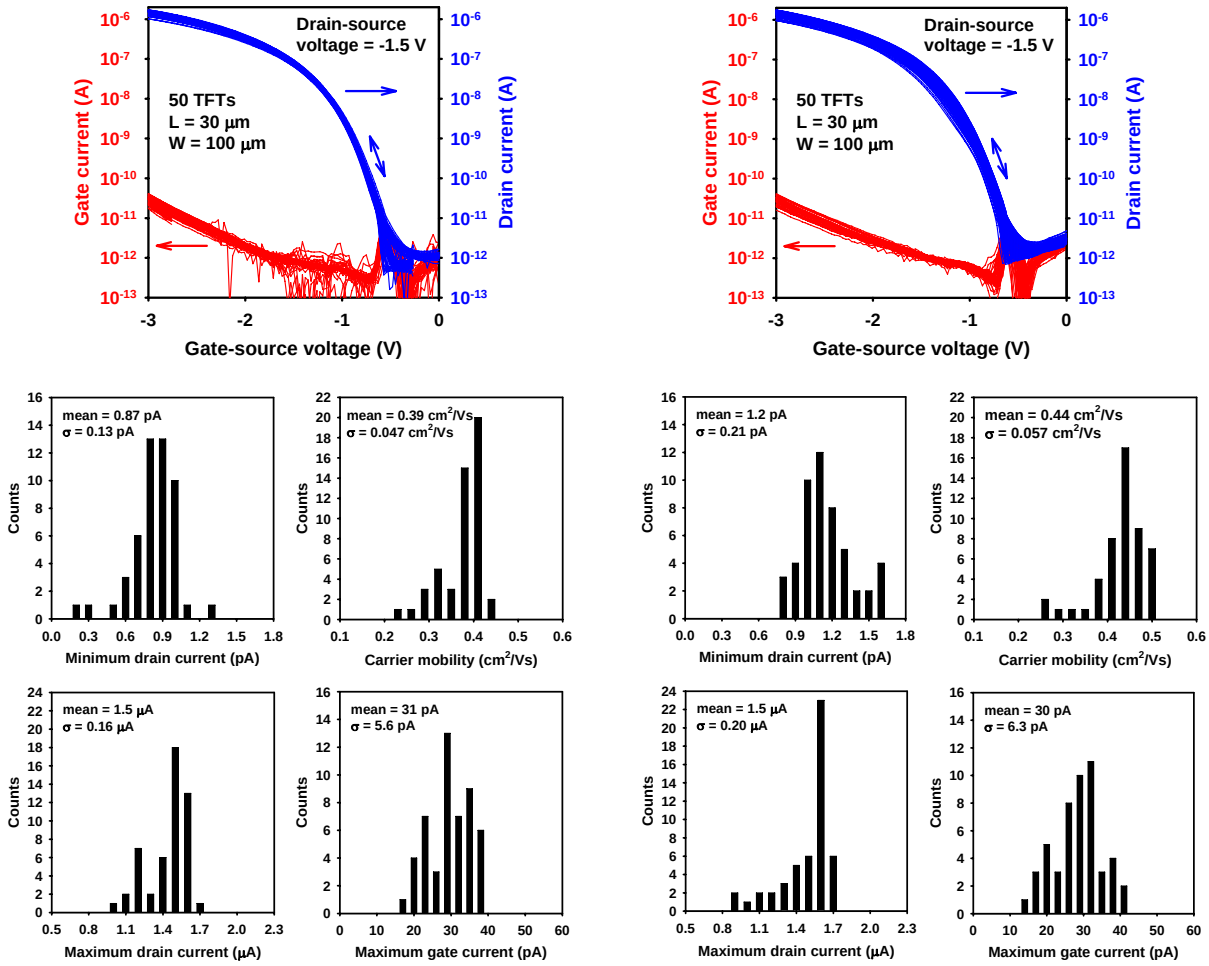

Figure S4 | Statistical analysis of the electrical characteristics of 100 pentacene TFTs obtained on two substrates manufactured within a one-week period. 50 TFTs on each substrate were tested. The TFTs have a channel length of 30 μm and a channel width of 100 μm. The measured drain current and gate current *vs*. gate-source voltage curves were overlaid to illustrate the statistical variation in the TFT characteristics.

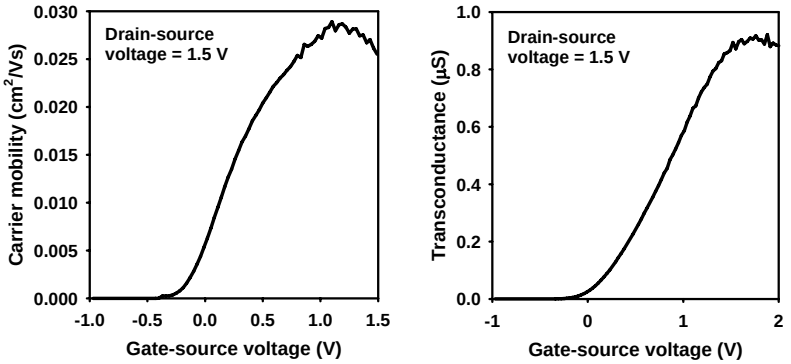

Figure S5 | Carrier mobility and transconductance of an n-channel F_{16}CuPc TFT. The TFT has a channel length of 30 μm and a channel width of 1000 μm. Mobility and transconductance are shown as a function of gate-source voltage for a drain-source voltage of 1.5 V.

interconnects for integrated circuits, small pads of 20 nm thick gold were then evaporated through a second shadow mask in specific areas on the aluminum. After the gold deposition, substrates were exposed to an oxygen plasma (150 W, 15 sec). A molecular monolayer was then allowed to self-assemble by immersing the substrates in a 2-propanol solution of n-octadecylphosphonic acid. While the plasma-treated aluminum surface presents a large density of functional groups for adsorption of a self-assembled monolayer, no monolayer is formed on the gold pads, thus leaving electrically conducting vias where needed for probing and for interconnects. Substrates remained in solution for about 16 hours, were then rinsed in pure 2-propanol, blown dry, and briefly baked on a hotplate at 60 °C. Next, a 30 nm thick layer of hexadecafluorocopperphthalocyanine (F_{16}CuPc; Aldrich, Germany) was thermally evaporated through a third shadow mask to define the active semiconductor layer for the n-channel transistors, and a 30 nm thick layer of pentacene ($C_{22}H_{14}$; Fluka, Germany) was thermally evaporated through a fourth shadow mask for the p-channel TFTs. Both organic semiconductors were purified twice by temperature-gradient sublimation in a quartz tube and deposited by thermal evaporation from resistively heated molybdenum boats in a vacuum of about 10^{-6} mbar. During the semiconductor depositions the substrate was held at a temperature of 90 °C for F_{16}CuPc and 60 °C for pentacene, since this was found to give the best performance for the respective transistors. Organic TFTs and circuits were completed by evaporating a 30 nm thick layer of gold through a fifth shadow mask to define the source and drain contacts and the second level of interconnects. The channel widths of the transistors were chosen to obtain similar drive currents for the p-channel pentacene TFTs and the n-channel F_{16}CuPc TFTs despite the significant difference in mobility between the two materials.

The shadow masks were aligned manually under an optical microscope. This allows us to align each mask to within 5 μm with respect to a given set of registration marks. The maximum area over which a certain alignment accuracy can be guaranteed is limited mainly by the mechanical properties of the polyimide mask, and we are usually able to achieve an alignment accuracy of 10 μm or better over the active area of our substrates (25×25 mm^2).

Employing a shadow-mask process affords a clean, simple, fast, reliable, versatile, and highly scalable manufacturing process (see refs. 3 and 4). In particular, it allows us to pattern the organic semiconductors without exposing them to potentially harmful process chemicals, such as photoresists, organic solvents, or even water. In addition, the shadow-mask process permits us to implement a top-contact TFT structure which provides a significantly lower contact resistance compared with the bottom-contact TFT structure. (Top-contact TFTs based on evaporated small-molecule semiconductors cannot be easily manufactured by photolithography, since the process chemicals would irreversibly damage the organic semiconductor films. Photolithography with aqueous resists has been considered, but even water exposure has been shown to degrade the performance of pentacene TFTs.)

All the transistors employ gold as the source/drain contact metal. Our TFT characteristics show that gold works very well for both the pentacene (p-channel) and the F_{16}CuPc (n-channel) TFTs (see Figures 2, 3, S3, S4 and S5). Assuming that gold has a workfunction of about 5 eV (depending on surface texture and contaminations), the lowest unoccupied molecular orbital (LUMO) of the F_{16}CuPc is roughly aligned with the gold Fermi level (ref. 28), thus favoring the injection of electrons from a gold contact into the F_{16}CuPc. On the other hand, the highest occupied molecular orbital (HOMO) of the pentacene is located about 0.9 eV below the gold Fermi level, favoring the injection of holes from the gold into the pentacene, leading to the observed p-type behavior of the pentacene TFTs (ref. 29).

The reason F_{16}CuPc was chosen as the semiconductor for the n-channel TFTs in this work is that to our knowledge it is the only commercially available organic material that gives n-channel mobilities in thin films greater than 10^{-2} cm^2/Vs when measured

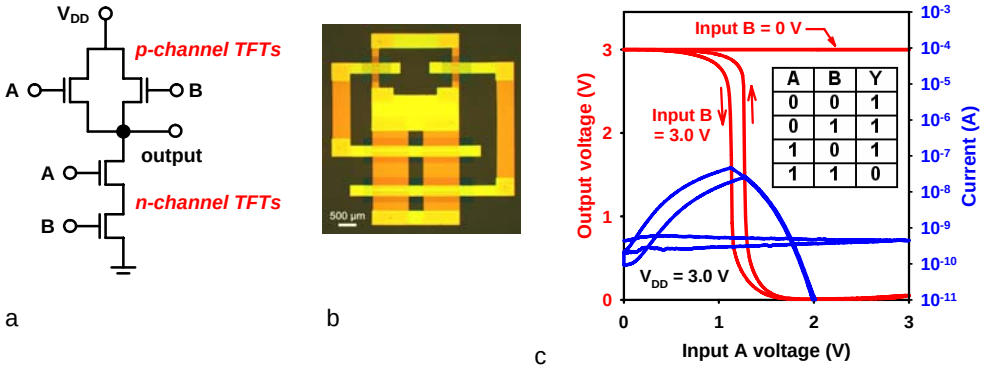

Figure S6 | Complementary 2-input NAND gate. a, Circuit schematic. **b.** Photograph of the circuit. **c,** Transfer characteristics (inset: truth table of the 2-input NAND gate).

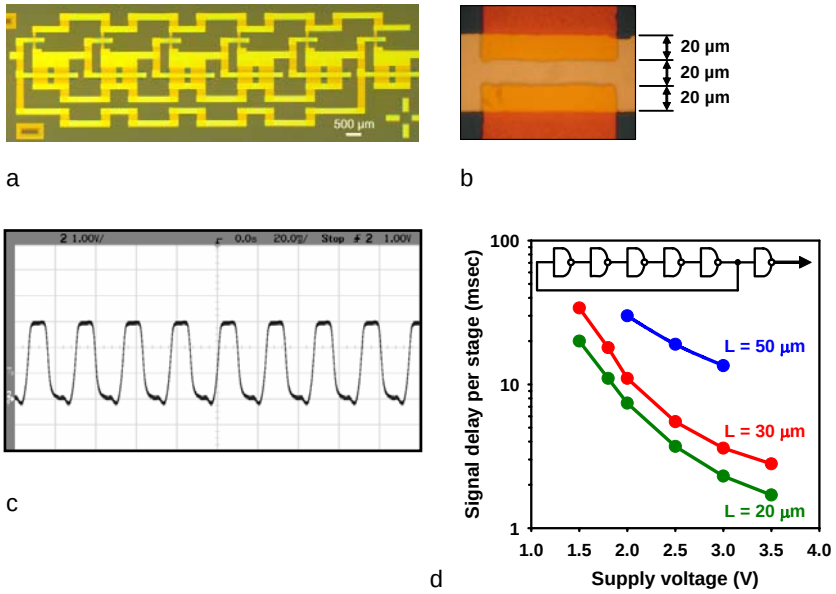

Figure S7 | Complementary 5-stage ring oscillators. **a**, Photograph of the circuit. The TFTs have channel widths of 100 µm (p-channel) and 1000 µm (n-channel). **b**, Close-up photograph of a pentacene TFT with channel length and contact-to-gate overlap of 20 µm. **c**, Output voltage signal of a ring oscillator with critical dimensions of 20 µm for a supply voltage of 3 V, showing an amplitude of 3 V and a period of 23 msec (corresponding to a signal delay of 2.3 msec per stage). **d**, Signal propagation delay as a function of channel length and supply voltage (inset: circuit schematic).

under ambient conditions without encapsulation.

The transistor parameters carrier mobility (µ) and transconductance (g_m) were calculated in the saturation regime using the standard formalism for field-effect transistors: $\mu = 2 \cdot L / (W \cdot C) \cdot (\delta \sqrt{I_D} / \delta V_{GS})^2$, $g_m = \delta I_D / \delta V_{GS}$ where L is the channel length, W is the channel width, C is the dielectric capacitance (0.7 µF/cm^2), I_D is the drain current, and V_{GS} is the gate-source voltage (see, for example, ref. 30).

To evaluate yield and uniformity of the transistors, arrays of 50 pentacene TFTs with a channel length of 30 µm and a channel width of 100 µm were characterized. Figure S4 shows the results of measurements carried out on two substrates that were processed within a one-week period. All 100 TFTs are functional, with maximum gate currents (measured at a gate-source voltage of -3 V) between 16 and 42 pA for all 100 devices and an average carrier mobility of 0.42 cm^2/Vs. This confirms the high yield and good uniformity of the self-assembled monolayer gate dielectric process.

The p-channel pentacene TFTs have a negative switch-on voltage, i.e. the transistors are not conducting at $V_{GS} = 0$ V. This is

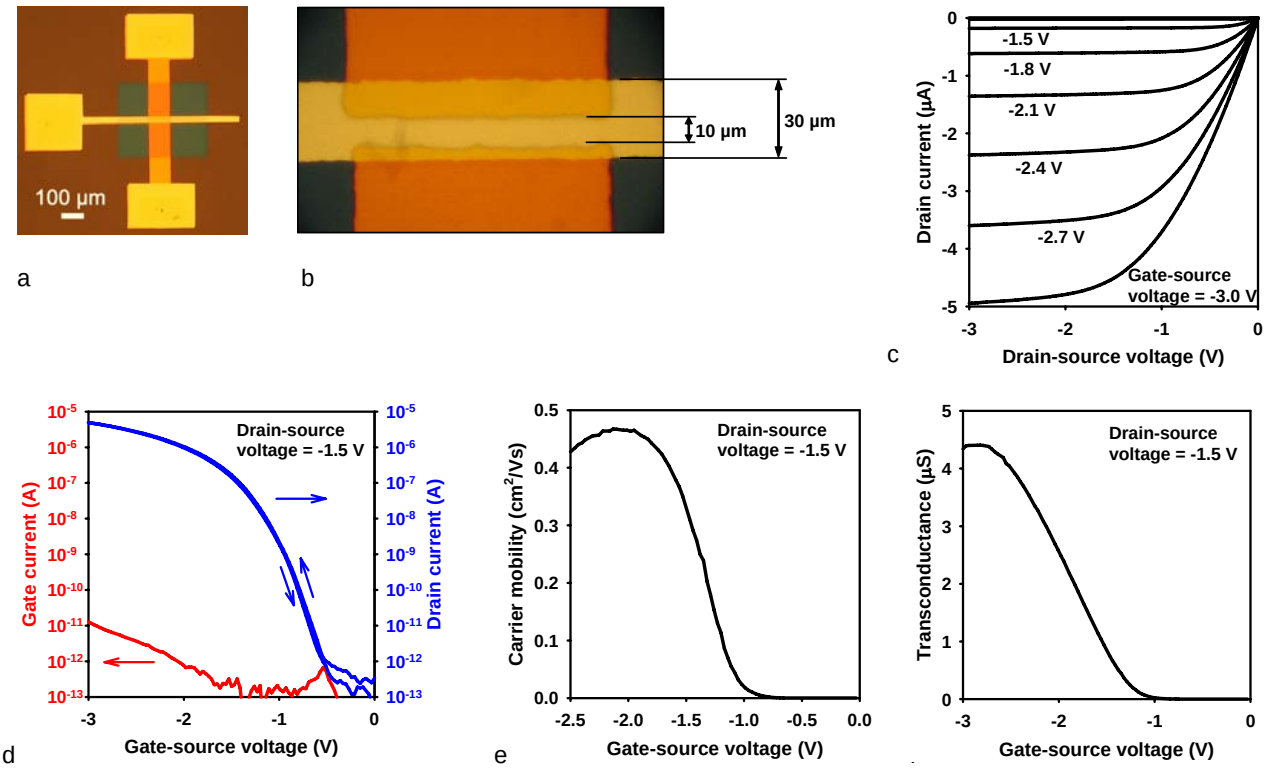

Figure S8 | Pentacene TFT with a channel length and contact overlap of 10 µm. **a&b**, Photographs of the transistor. **c**, Output characteristics. **d**, Transfer characteristics. **e**, Carrier mobility. **f**, Transconductance. The channel width is 100 µm.

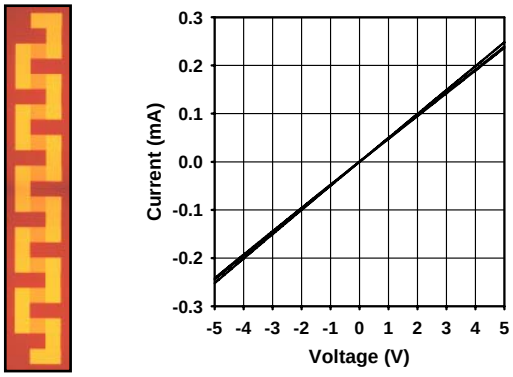

Figure S9 | Via chain. Left: Photograph of the via chain test structure consisting of 20 vias connected in series. Right: Current as a function of voltage through a chain of 20 vias, confirming the small electrical resistance and excellent uniformity of the vias defined by exploiting the surface selectivity of the molecular self-assembly process. The measurement was repeated on three chains with 20 vias each and the measured curves were overlaid to illustrate the insignificant variation in performance.

in contrast to many literature reports of pentacene TFTs with thicker gate dielectrics which often have a significant channel conductance at V_{GS} = 0 V (see, for example, refs. 1, 2, 23, 26), but is in line with other reports of pentacene TFTs with thin dielectrics where near-zero or negative switch-on voltages have been observed (see refs. 6, 22). For most applications, a switch-on voltage that is equal to zero or slightly negative is desirable.

The integrated circuits implemented in this work were designed without interconnect crossovers, i.e. there are no crossovers between signal lines, supply voltage lines or ground lines (see Figures 4, S6 and S7). This was done to reduce the detrimental effects of capacitive coupling through the thin SAM-based dielectric. For more complex circuits where interconnect crossovers cannot be easily avoided, low-capacitance crossovers can be realized with an additional process step using a thicker dielectric, such as vapor-deposited parylene (ref. 3) or vacuum-deposited metal oxides (ref. 4).

The dynamic performance of the complementary circuits is limited by the carrier mobility of the n-channel F_{16}CuPc TFTs (0.02 cm^2/Vs), by the channel length of the transistors (20 µm), and by the parasitic capacitances due to the overlap between the source/drain contacts and the gate (20 µm). Brooks A. Jones and coworkers have recently reported the synthesis of an air-stable perylene-based semiconductor that has shown an n-channel mobility of 0.6 cm^2/Vs (ref. 25). Assuming that the signal delay is inversely proportional to the carrier mobility, signal delays of about 80 µsec per stage at 3 V would be expected for complementary circuits with balanced carrier mobilities of 0.6 cm^2/Vs, channel lengths of 20 µm, and a gate-to-contact overlap of 20 µm. A further reduction to about 20 µsec per stage at 3 V can be expected by reducing the critical dimensions to 10 µm. As Figure S8 shows, functional, well-behaved TFTs with a channel length of 10 µm and a contact overlap of 10 µm can indeed be prepared using shadow masks. The transistor has a carrier mobility of 0.4 cm^2/Vs, an on/off current ratio greater than 10^7, and a transconductance of 4.5 µS (45 µS/mm).

One concern with any integrated circuit process is the conductivity and uniformity of the interconnect vias. In our process, vias are defined by exploiting the surface-selective

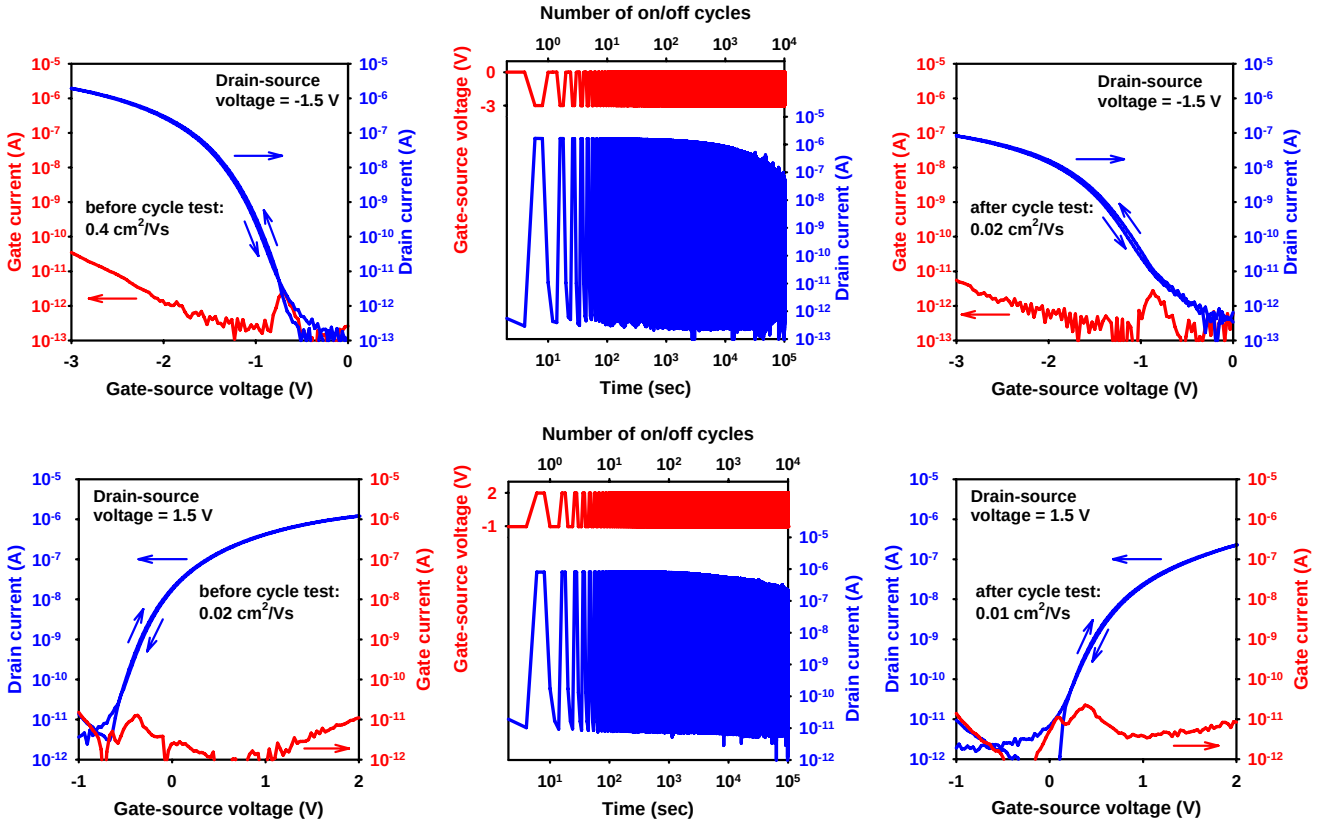

Figure S10 | Operational stability of SAM-dielectric TFTs. Top: Cycle test on a pentacene TFT. **Bottom:** Cycle test on a F_{16}CuPc TFT.

adsorption of phosphonic acids which form high-quality monolayers on plasma-treated aluminum, but not on gold. To confirm the formation of low-resistance vias by this process, test structures consisting of 20 series-connected vias (so-called via chains) were fabricated along with the TFTs and circuits. Figure S9 shows the electrical currents measured through three identical via chains, each consisting of 20 vias, as a function of applied voltage. As can be seen, the current through the vias is perfectly ohmic. The resistance extracted from the current-voltage characteristics is 20 kΩ which corresponds to a resistance per via of 1 kΩ. The variation in resistance between the three chains is negligible.

To evaluate the operational stability of our TFTs we have performed cycle tests in which a continuous square-wave voltage signal with an amplitude of 3 V and a period of 10 sec is applied to the gate of an individual transistor. The results of cycle tests on a pentacene TFT and a F_{16}CuPc TFT with 10,000 cycles over 100,000 sec (27.8 hours) performed in air at room temperature are shown in Figure S10. During the cycle test the mobility of the pentacene TFT decreased from 0.4 cm^2/Vs to 0.02 cm^2/Vs and the mobility of the F_{16}CuPc TFT degraded from 0.02 cm^2/Vs to 0.01 cm^2/Vs. The observed rate of mobility reduction suggests that the degradation of the organic semiconductors is enhanced by self-heating, possibly a result of the large current densities in the channel (~ 10^3 A/cm^2). The gate current does not increase during the cycle tests, suggesting that the SAM-based gate dielectric is stable during transistor operation.

During shelf-life tests when the devices are not operated the carrier mobility degrades less rapidly. For our pentacene TFTs we have seen a reduction in mobility by 80% after 100 days which is similar to the degradation of unprotected pentacene TFTs with thicker inorganic or polymer gate dielectrics reported in the literature (see Figure S11). No increase in gate current was observed during the shelf-life tests.

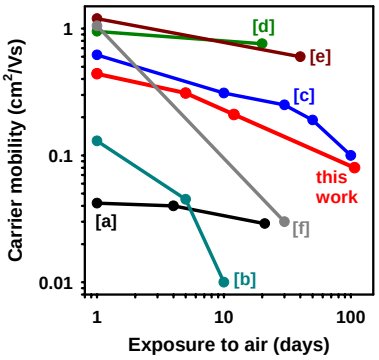

Figure S11 | Shelf life of pentacene TFTs. The graph compares the degradation of the carrier mobility of our SAM-dielectric pentacene TFTs during exposure to ambient air with that of pentacene TFTs reported in the literature.
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Pentacene and F_{16}CuPc TFTs were also prepared on flexible, transparent polyethylene naphthalate film (Teonex® Q65 PEN; DuPont Teijin Films, Wilton, U.K.; special thanks to William A. MacDonald). To facilitate a laboratory-scale shadow-mask process, the PEN film was cut into pieces about 80 × 80 mm^2 in size and mounted to a solid support using thermally conductive adhesive GEL-film (Gel-Pak, Hayward, U.S.A.). The same

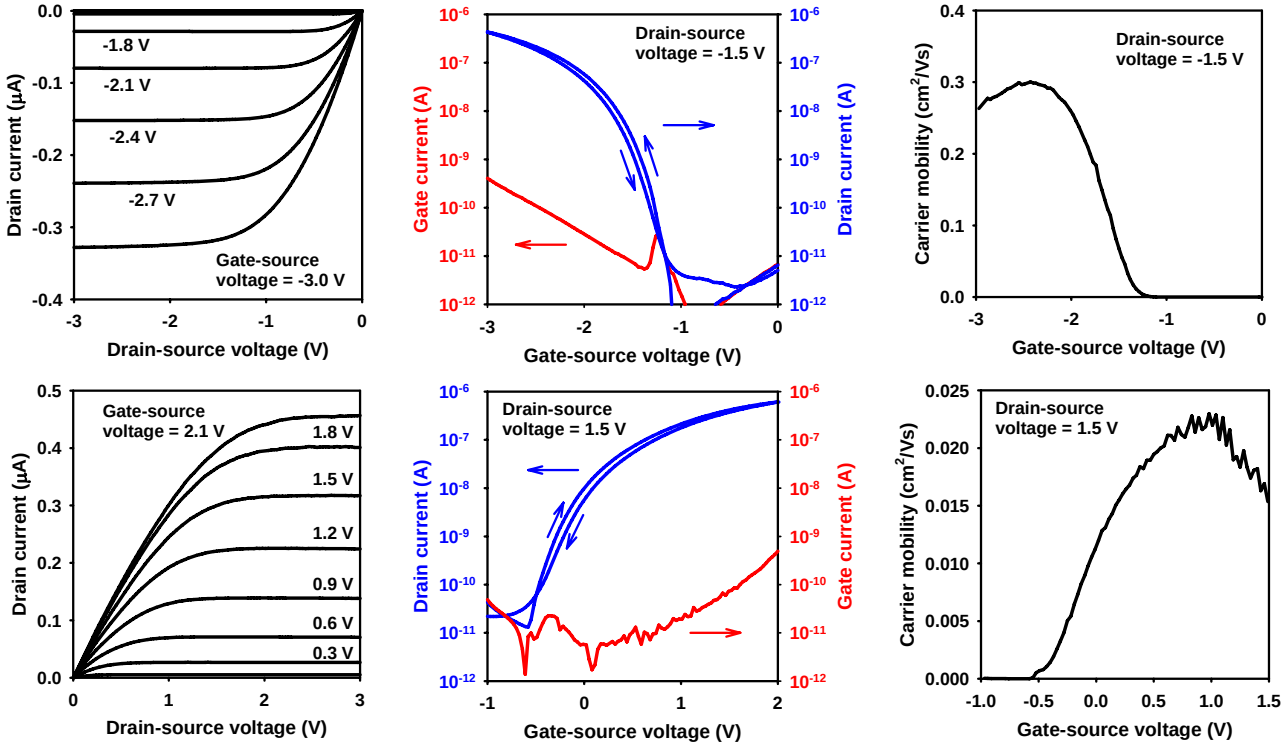

Figure S12 | Pentacene and F_{16}CuPc TFTs with SAM dielectric on a flexible polymeric substrate. **Top**: Flexible p-channel pentacene TFT with a channel length of 50 μm and a channel width of 100 μm. **Bottom:** Flexible n-channel F_{16}CuPc TFT with a channel length of 50 μm and a channel width of 1000 μm.

shadow-mask process described above for glass substrates was employed for the flexible PEN substrates. Figure S12 shows the electrical characteristics of a p-channel pentacene TFT and an n-channel F_{16}CuPc TFT on flexible PEN film. The pentacene TFT has a carrier mobility of 0.3 cm^2/Vs, a subthreshold swing of 140 mV/dec, a maximum gate current of 400 pA, an on/off current ratio of 10^5, and a transconductance of 0.5 µS. The F_{16}CuPc TFT has a carrier mobility of 0.02 cm^2/Vs, a subthreshold swing of 130 mV/dec, a maximum gate current of 500 pA, an on/off current ratio of 10^5, and a transconductance of 0.4 µS. As expected, some of the electrical characteristics are slightly lower compared with the TFTs on glass, most likely due to the somewhat rougher surface of the PEN, but the TFT performance is sufficient to permit the fabrication of functional integrated circuits, and we have found that the yield of functional TFTs on PEN is as high as it is on glass.

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