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Achieving Ultralow Turn-On Voltages in Organic Thin-Film Transistors: Investigating Fluoroalkylphosphonic Acid Self-Assembled Monolayer Hybrid Dielectrics

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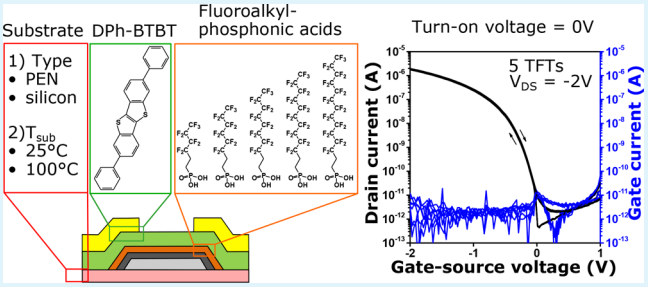
Supporting Information

ABSTRACT: The properties of organic thin-film transistors (TFTs) and thus their ability to address specific circuit design requirements depend greatly on the choice of the materials, particularly the organic semiconductor and the gate dielectric. For a particular organic semiconductor, the TFT performance must be reviewed for different combinations of substrates, fabrication conditions, and the choice of the gate dielectric in order to achieve the optimum TFT and circuit characteristics. We have fabricated and characterized organic TFTs based on the small-molecule organic semiconductor 2,7-diphenyl[1]-benzothieno[3,2-*b*][1]benzothiophene in combination with an ultrathin hybrid gate dielectric consisting of aluminum oxide and a self-assembled monolayer. Fluoroalkylphosphonic acids with chain lengths ranging from 6 to 14 carbon atoms have been used to form the self-assembled monolayer in the gate dielectric, and their influence on the TFT characteristics has been studied. By optimizing the fabrication conditions, a turn-on voltage of 0 V with an on/off current ratio above 10^6 has been achieved, in combination with charge-carrier mobilities up to 0.4 $cm^2/V\,s$ on flexible plastic substrates and 1 $cm^2/V\,s$ on silicon substrates.



KEYWORDS: *organic thin-film transistors, hybrid dielectrics, self-assembled monolayers, DPh-BTBT, substrate temperature, turn-on voltage*

1. INTRODUCTION

The development of organic thin-film transistors (TFTs) is important for potential portable and wearable electronic applications.[1,2] In order to ensure portability and safe handling of the systems, it is necessary that their power consumption is sufficiently low so they can be powered by solar cells or small batteries. This requires that the TFTs employed in such devices have low operating voltages. Moreover, for the realization of low-power complementary circuits, it is beneficial to have TFTs with turn-on voltages as close to 0 V as possible in order to minimize the off-state drain current while maximizing the on/off current ratio obtained with a certain maximum gate−source voltage. Low-voltage operation of organic TFTs can be achieved by employing ultrathin hybrid gate dielectrics composed of a thin metal oxide layer and an organic self-assembled monolayer (SAM), which provide a large dielectric capacitance while minimizing gate leakage and improving the overall TFT performance.[3−6] A suitable choice of molecule for the SAM is essential in achieving the desired semiconductor morphology and the optimum TFT characteristics. Previously, silane-based SAMs that bind to silicon dioxide (SiO_2) as the gate oxide have been chemically and electrically engineered by using molecules with different functional groups to achieve an optimum crystalline microstructure of the organic semiconductor and thus obtain high-performance TIPS-pentacene TFTs in terms of stability and charge-carrier mobility.[7] Alkyl silanes and fluoroalkyl silanes have also been studied in pentacene TFTs to evaluate their impact on turn-on voltages and transport mechanisms in the organic semiconductor.[8] Another attractive combination of materials for the hybrid gate dielectric is aluminum oxide (AlO_x) together with a SAM based on phosphonic acids, especially those with a saturated aliphatic chain of carbon and hydrogen atoms attached to the phosphonic acid head group, which align by mutual cohesive forces to form self-assembled monolayers.[9] The turn-on voltage of organic TFTs can be controlled by employing gate dielectrics based on mixed SAMs with different combinations of alkylphosphonic acids and fluoroalkylphosphonic acids.[10−14] Kraft et al. used fluoroalkyl-phosphonic acids to shift the threshold voltage of both p-channel and n-channel organic TFTs by about 1 V due to their strong electron-withdrawing character as compared to the

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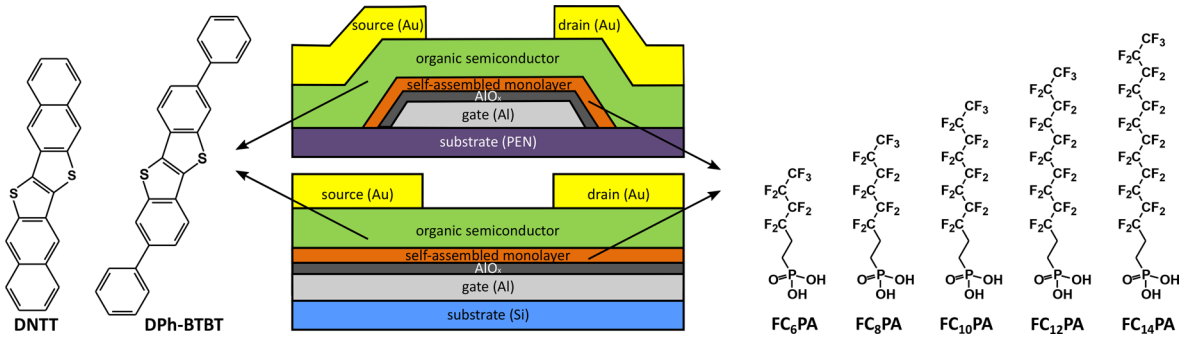

Figure 1. Chemical structures of organic semiconductors DNTT and DPh-BTBT, schematic cross sections of the TFTs fabricated on flexible polyethylene naphthalate (PEN) substrates with patterned gate electrodes and of the TFTs fabricated on doped silicon substrates with a common gate electrode, and chemical structures of fluoroalkylphosphonic acids with five different chain lengths used to form the self-assembled monolayer in the hybrid dielectric.

alkylphosphonic acid-based monolayers.[15] Another approach is to vary the chain length of the phosphonic acid molecules in order to tune the threshold voltage and other electrical properties of the TFTs.[16−18] In this work, we explore the use of hybrid AlO_x/SAM gate dielectrics in combination with a relatively new organic semiconductor, 2,7-diphenyl[1]-benzothieno[3,2-*b*][1]benzothiophene (DPh-BTBT)[19−21] and different fabrication conditions to study their influence on the performance of p-channel organic TFTs. In addition, we investigate the use of fluoroalkylphosphonic acids with a wide range of chain lengths in combination with DPh-BTBT to explore the effect of the thickness of the SAM on the morphology of the organic semiconductor layer and the TFT performance. This combination of materials and fabrication conditions could be instrumental in designing improved low-voltage organic complementary circuits.

2. EXPERIMENTAL SECTION

All TFTs were fabricated in the inverted staggered (bottom-gate, top-contact) configuration with either DPh-BTBT or, for comparison, dinaphtho[2,3-*b*:2′,3′-*f*]thieno[3,2-*b*]thiophene (DNTT)[22−24] (both purchased from Sigma Aldrich; Figure 1) as the organic semiconductor and fluoroalkylphosphonic acids (Specific Polymers) of various chain lengths (Figure 1 and Table 1), which form the SAM in the hybrid gate dielectric.

Table 1. Chemical Names and Formulas of the Fluoroalkylphosphonic Acids Employed for the Self-Assembled Monolayers as Part of the Hybrid Gate Dielectric

chemical name	chemical formula
1*H*,1*H*,2*H*,2*H*-perfluorohexylphosphonic acid	FC_6PA
1*H*,1*H*,2*H*,2*H*-perfluorooctylphosphonic acid	FC_8PA
1*H*,1*H*,2*H*,2*H*-perfluorodecylphosphonic acid	$FC_{10}PA$
1*H*,1*H*,2*H*,2*H*-perfluorododecylphosphonic acid	$FC_{12}PA$
1*H*,1*H*,2*H*,2*H*-perfluorotetradecylphosphonic acid	$FC_{14}PA$

TFTs were fabricated on heavily doped silicon substrates and on flexible, 125 μm-thick polyethylene naphthalate (PEN) substrates (Teonex Q65; kindly provided by William A. MacDonald, DuPont Teijin Films, Wilton, U.K.). For the gate electrodes, a 30 nm-thick layer of aluminum was deposited by thermal evaporation in vacuum with a rate of about 2 nm/s. For the TFTs on the silicon substrates, the aluminum was deposited without patterning and served as a common gate electrode for all TFTs on the substrate, whereas on the PEN substrates, the aluminum was deposited through a polyimide shadow mask (CADiLAC Laser, Hilpoltstein, Germany) to define a patterned gate electrode for each transistor. The substrates were then exposed to an RF oxygen plasma (oxygen flow rate: 30 sccm; oxygen partial pressure: 10 mTorr; RF power: 200 W; duration: 30 s) to increase the thickness of the native aluminum oxide to about 3.6 nm. The substrates were then immersed into a 1 mM solution of a particular fluoroalkylphosphonic acid in 2-propanol to allow a monolayer to self-assemble on the aluminum oxide surface. Each substrate was kept immersed in the solution for a minimum of 12 h, after which it was rinsed with 2-propanol to remove any physisorbed molecules, dried with nitrogen, and subsequently heated to a temperature of 80 °C for 10 min to stabilize the monolayer. After formation of the SAM, a nominally 25 nm-thick layer of the organic semiconductor (DPh-BTBT or DNTT) was deposited onto the hybrid AlO_x/SAM gate dielectric by sublimation in vacuum with a rate of about 2 nm/min. During the DPh-BTBT semiconductor deposition, the substrate was held either at room temperature (25 °C) or at an elevated temperature (100 °C). For the DNTT TFTs, the substrate was heated to 60 °C during the semiconductor deposition. On the PEN substrates, the semiconductor was deposited through a shadow mask, whereas on the silicon substrates, the semiconductor was deposited without a mask and patterned later by scratching under a microscope. In the last step, 30 nm-thick gold was deposited by thermal evaporation in vacuum with a rate of 1.2 nm/s and patterned using a shadow mask to define the source and drain contacts. The static electrical characteristics of the TFTs were measured using a Micromanipulator probe station and an Agilent 4156C Semiconductor Parameter Analyzer. All substrates were stored and measured in ambient air at room temperature in a yellow light cleanroom environment. The transfer characteristics were measured by applying a drain−source voltage (V_{DS}) of −2 V (on silicon substrates) or −3 V (on PEN substrates) and sweeping the gate−source voltage (V_{GS}) from 1 to −2 V (in steps of −30 mV) or from 1 to −3 V (in steps of −40 mV) and back to 1 V. The effective charge-carrier mobility (hereafter referred to as the carrier mobility) was extracted from the following equation: $\mu_{eff} = \frac{2L}{WC_{diel}}\left(\frac{\partial\sqrt{I_D}}{\partial V_{GS}}\right)^2$, where L and W are the channel length and channel width, respectively. The TFTs on the silicon substrates have a channel length of 100 μm and a channel width of 200 μm, while the TFTs on PEN have a channel length of 20 μm and a channel width of 100 μm. C_{diel} is the capacitance of the gate dielectric per unit area, which was determined using a sine wave generator, a transimpedance amplifier (to convert the displacement current into a voltage), and an oscilloscope. Apart from the carrier mobility, other TFT characteristics were also extracted from the transfer curves for comparison. The turn-on voltage was considered as the gate−source voltage (V_{GS}) at which the drain current (I_D) is at its minimum,[25] signifying the transition between the off-state and the on-state. The threshold voltage (V_{th}) was obtained by fitting the measured transfer curve to the following equation: $I_D = \frac{\mu C_{diel} W}{2L}(V_{GS} - V_{th})^2$. As one indicator of the quality of

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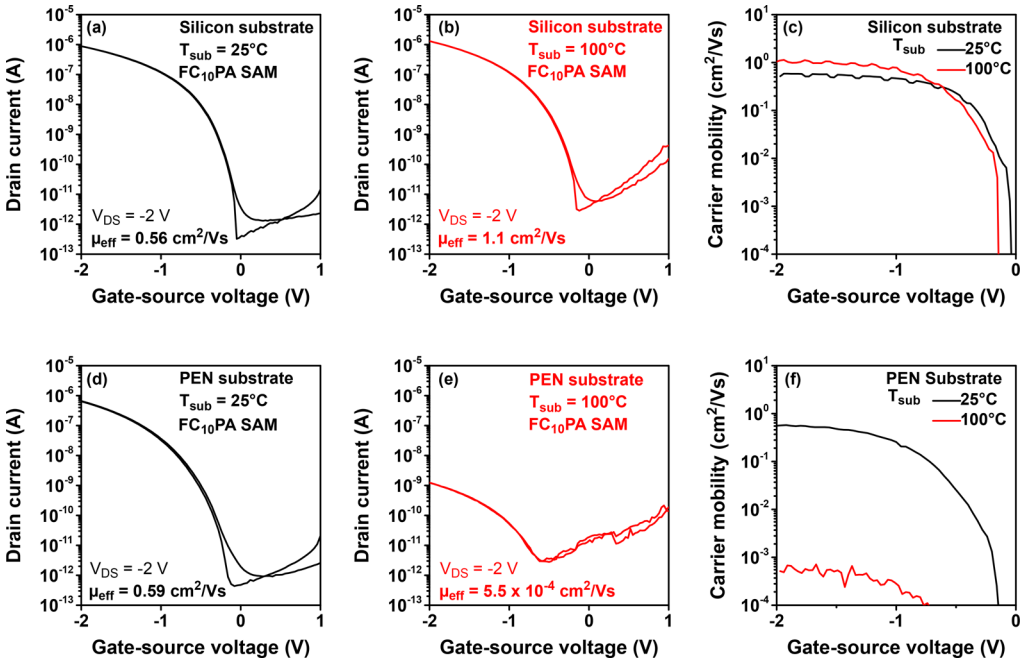

Figure 2. Transfer curves of DPh-BTBT TFTs fabricated on silicon substrates with the substrate held at temperatures of (a) 25 °C and (b) 100 °C during the semiconductor deposition and (c) carrier mobilities extracted from the transfer curves. Transfer curves of DPh-BTBT TFTs fabricated on flexible PEN substrates with the substrate held at temperatures (d) 25 °C and (e) 100 °C during the semiconductor deposition and (f) carrier mobilities extracted from the transfer curves.

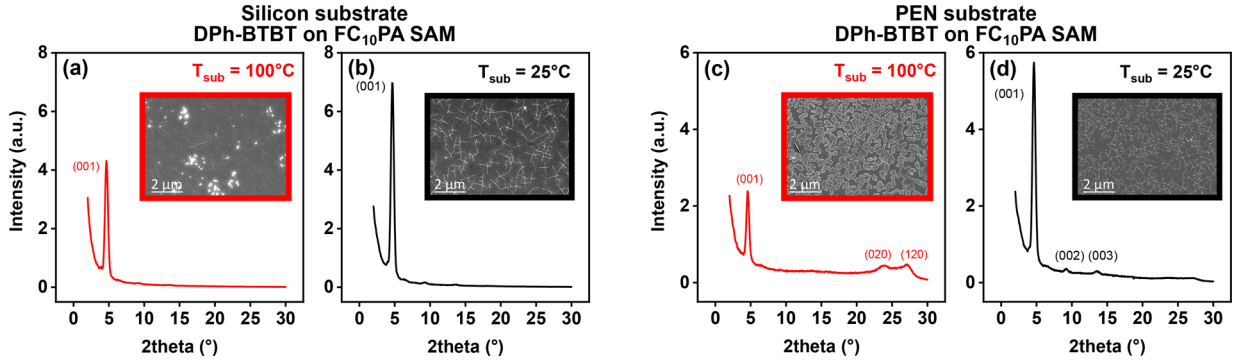

Figure 3. Out-of-plane XRD spectra and corresponding scanning electron microscopy images of DPh-BTBT thin films deposited onto hybrid $AlO_x/FC_{10}PA$ SAM dielectrics on silicon substrates held at temperatures of (a) 100 °C (red line) and (b) 25 °C (black line) and on PEN substrates held at temperatures of (c) 100 °C (red line) and (d) 25 °C (black line) during the semiconductor deposition.

the gate dielectric in reducing leakage currents, the gate current (I_G) was measured as a function of the gate−source voltage, and its values at V_{GS} = −2 V (on silicon substrates) and V_{GS} = −3 V (on PEN substrates) were considered for comparison. The on/off current ratio (I_{ON}/I_{OFF}) was calculated as the ratio between the drain current (I_D) measured at the most negative applied gate−source voltage (either V_{GS} = −2 V or V_{GS} = −3 V) and the drain current (I_D) measured at a gate−source voltage of zero (V_{GS} = 0 V). The thin-film morphology of the semiconductor surface was imaged by a Zeiss Merlin scanning electron microscope with an acceleration voltage of 3 kV. Grazing incidence X-ray diffraction (XRD) was performed using a Rigaku SmartLab system equipped with a 9 kW copper X-ray source (λ = 1.5406 Å). The X-ray incident angle was constant at 0.2°, and the diffraction signals were captured with a 0D detector in the out-of-plane direction. The horizontal width of the incident X-ray beam was 5 mm, which is smaller than the width of the investigated substrates.

3. RESULTS AND DISCUSSION

The organic semiconductor DPh-BTBT was deposited by thermal sublimation in vacuum with the provision of heating the substrate during the semiconductor deposition process. Conventionally, substrates are heated to an optimum temperature to facilitate the diffusion of semiconductor molecules on the surface and form polycrystalline thin films for maximum carrier mobility and overall TFT performance.[26,27] However, increasing the substrate temperature beyond the optimum may result in island-mode growth or desorption of semiconductor molecules from the surface.[28] In Section 3.1, we investigate

Table 2. Measured Unit-Area Capacitance of Hybrid AlO_x/SAM Gate Dielectrics Employing Fluoroalkylphosphonic Acids with Five Different Chain Lengths To Form the SAM

fluoroalkylphosphonic acid	gate dielectric capacitance C_{diel} (μF/cm^2)
FC_6PA	1.1
FC_8PA	0.88
$FC_{10}PA$	0.75
$FC_{12}PA$	0.58
$FC_{14}PA$	0.61

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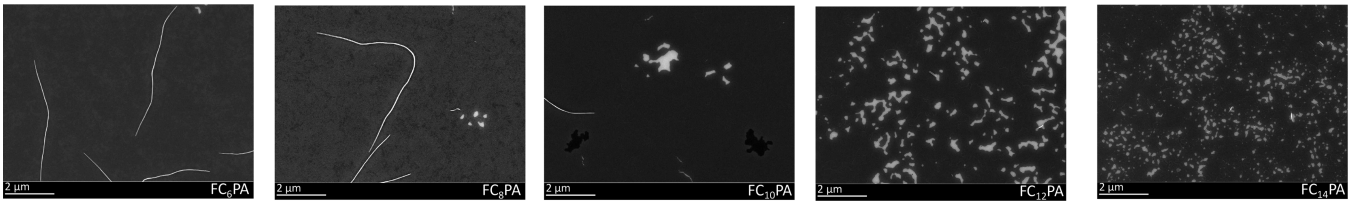

Figure 4. Scanning electron microscopy (SEM) images showing the thin-film morphology of DPh-BTBT films deposited onto hybrid AlO_x/SAM gate dielectrics based on fluoroalkylphosphonic acids with chain lengths of 6, 8, 10, 12, and 14 carbon atoms (from left to right) on silicon substrates, with the substrate held at a temperature of 100 °C during the semiconductor deposition.

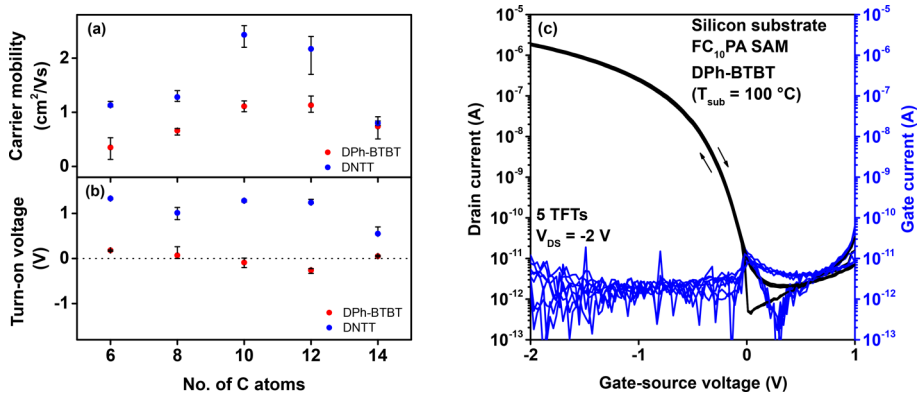

Figure 5. (a) Carrier mobilities and (b) turn-on voltages of DPh-BTBT and DNTT TFTs with hybrid AlO_x/SAM gate dielectrics based on fluoroalkylphosphonic acids with chain lengths of 6, 8, 10, 12, and 14 carbon atoms fabricated on silicon substrates. (c) Transfer curves of five DPh-BTBT TFTs with a hybrid AlO_x/$FC_{10}PA$-SAM gate dielectric fabricated on a silicon substrate, showing a turn-on voltage of exactly 0 V. The substrate was held at a temperature of 100 °C during the DPh-BTBT deposition and at a temperature of 60 °C for the DNTT deposition.

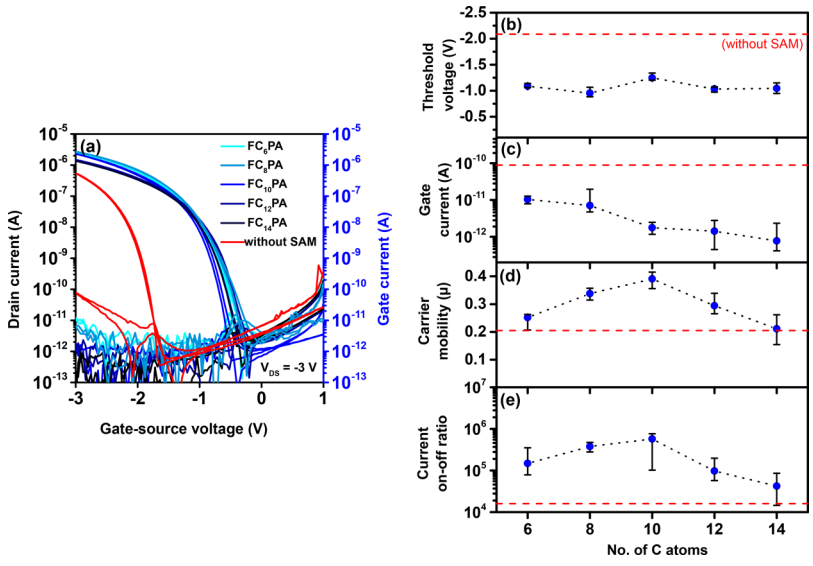

Figure 6. (a) Transfer curves of DPh-BTBT TFTs with hybrid AlO_x/SAM gate dielectrics based on fluoroalkylphosphonic acids with five different chain lengths fabricated on flexible PEN substrates. The transfer curve of a DPh-BTBT TFT with an AlO_x gate dielectric without SAM is shown for comparison. (b) Threshold voltage, (c) gate leakage current, (d) carrier mobility, and (e) on/off current ratios of the TFTs from panel (a) plotted as a function of the chain length of the fluoroalkylphosphonic acid. The red dashed lines indicate the parameter values of the TFT with an AlO_x gate dielectric without SAM.

how the substrate temperature during the DPh-BTBT deposition affects the DPh-BTBT film growth and the characteristics of TFTs fabricated on silicon and on flexible PEN substrates, and based on this information, DPh-BTBT TFTs were fabricated on the respective substrates with different fluoroalkylphosphonic acids forming the gate dielectric SAM. Section 3.2 examines the influence of the chain length of the fluoroalkylphosphonic acid on the semiconductor morphology and the TFT performance.

3.1. Optimum Substrate Temperature during Semiconductor Deposition. A striking difference is observed between TFTs fabricated on silicon and on PEN in the way the morphology of the DPh-BTBT layer and the TFT performance are affected by the substrate temperature during the semiconductor deposition. As seen in Figure 2a–c, the TFTs

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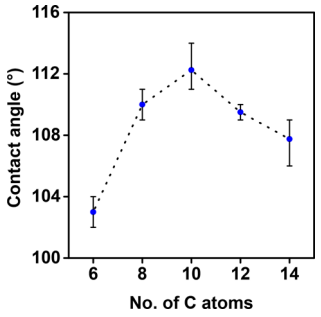

Figure 7. Water contact angles measured on the surfaces of fluoroalkylphosphonic acid SAMs with different chain lengths on PEN substrates.

fabricated on silicon have carrier mobilities of 0.56 cm^2/V s when the substrate is held at a temperature of 25 °C during the DPh-BTBT deposition and 1.1 cm^2/V s when the DPh-BTBT is deposited at a substrate temperature of 100 °C. This is the expected behavior for organic semiconductors deposited by thermal sublimation where a higher substrate temperature promotes larger grain size and enhanced crystallinity in the thin film.[29] In contrast, for DPh-BTBT TFTs fabricated on PEN, Figure 2d–f shows that heating the substrate during the DPh-BTBT deposition to a temperature of 100 °C yields a carrier mobility that is 3 orders of magnitude lower than that obtained without substrate heating.

The thin-film morphologies as seen in the scanning electron microscopy (SEM) images show that when the PEN substrate is heated during the semiconductor deposition, the DPh-BTBT molecules form isolated islands (Figure 3c, inset) instead of a continuous film formed when the PEN substrate is held at 25 °C (Figure 3d, inset). Since a percolation path for the molecules is harder to form through isolated islands, the carrier mobility is significantly lower. For silicon substrates held at 100 °C (Figure 3a, inset) and 25 °C (Figure 3b, inset), the thin-film morphologies indicate thin films with almost complete coverage in both cases, thereby establishing that the substrate temperature has little influence on the thin-film morphology of DPh-BTBT films on silicon substrates.

Out-of-plane XRD measurements (Figure 3) performed on the DPh-BTBT films on PEN and silicon substrates indicate the possible orientation of the DPh-BTBT molecules, establishing the influence of the substrate temperature on the thin-film morphology for the two different substrates. On the PEN substrate for the films deposited at a substrate temperature of 25 °C , the DPh-BTBT molecules are mostly in an upright-standing orientation, with a dominant diffraction peak at 2θ = 4.65° that corresponds to a (001) interlayer spacing of 19 Å. The appearance of the peaks corresponding to (002) and (003) further indicates a good layer-by-layer structure of the film. On the other hand, the DPh-BTBT films deposited on PEN at a substrate temperature of 100 °C are characterized by a mix of upright-standing and lying-down orientation of the molecules, with peaks appearing at 2θ = 4.65°, 23.8°, and 27.1° that correspond to the (001), (020), and (120) orientations, respectively. The intensity of the (001) signal is much smaller than that measured on the film deposited at a substrate temperature of 100 °C. Only the semiconductor molecules that are standing upright contribute to the lateral carrier transport, which explains why the carrier mobility is significantly larger when the semiconductor deposition is carried out at a substrate temperature of 25 °C, rather than 100 °C. In contrast, it is observed that the XRD spectra of the DPh-BTBT films on the silicon substrates are very similar for the two substrate temperatures, with a single dominant peak at 2θ = 4.65°, corresponding to molecules in an upright-standing configuration. Since this orientation is favorable to lateral carrier transport, this also explains the carrier mobilities of 0.56 and 1.1 cm^2/V s for DPh-BTBT TFTs on silicon substrates for substrate temperatures of 25 °C and 100 °C, respectively, and the fact that the transistor characteristics depend only weakly on the substrate temperature during the semiconductor deposition. Additional numerical data regarding the XRD spectra can be found in the Supporting Information (Table S2). This work aims to study the effect of substrate heating during the semiconductor deposition. A more systematic investigation of the influence of varying the substrate temperature would be required to deduce the optimum substrate temperature for the DPh-BTBT deposition. To the best of our knowledge, this anomalous behavior is unique to the semiconductor DPh-BTBT and remains unexplained; nevertheless, it helps to identify the conditions required for fabricating devices and circuits on these two types of substrate. These appropriate substrate temperatures (100 °C for the silicon substrates and 25 °C for the PEN substrates) were used to fabricate the TFTs described in the following section.

3.2. Effect of Fluoroalkylphosphonic Acid Chain Length. By using fluoroalkylphosphonic acids with different chain lengths, SAMs of varying thicknesses are formed, and the capacitance of the hybrid AlO_x/SAM dielectric can be tuned

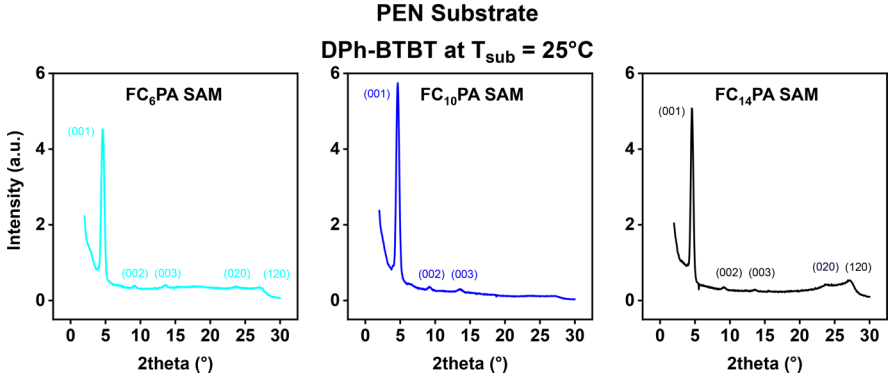

Figure 8. Out-of-plane XRD spectra measured on DPh-BTBT thin films deposited onto three different hybrid AlO_x/SAM dielectrics on PEN substrates.

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from 1.1 μF/cm^2 (with the FC_6PA SAM) to 0.61 μF/cm^2 (with the $FC_{14}PA$ SAM) (Table 2). Along with this, the different SAMs also influence the thin-film morphology of the semiconductor layer deposited onto them, which is crucial since the gate field-induced carrier channel is confined to the first one or two monolayers of the semiconductor layer close to the interface with the SAM.[30] Figure 4 shows the thin-film morphology of DPh-BTBT films with a nominal thickness of 25 nm deposited onto different SAMs. It is evident that, with increasing chain length of the fluoroalkylphosphonic acid, the film coverage decreases and the film appears to be more sparsely connected. However, as will be shown below, this has little effect on the charge-carrier mobilities of the TFTs, which suggests that all films are characterized by a sufficient degree of percolation.

Figure 5 shows the carrier mobility (Figure 5a) and turn-on voltage (Figure 5b) of the DPh-BTBT TFTs fabricated on silicon substrates as a function of the chain length of the fluoroalkylphosphonic acid. Results for DNTT TFTs are shown for comparison. For both semiconductors, the carrier mobility is relatively small when the chain length is either short (FC_6PA, FC_8PA) or long ($FC_{14}PA$), and it has a maximum value in the case of a medium chain length ($FC_{10}PA$, $FC_{12}PA$). Upon observing the same trend for both semiconductors, the influence of the chain length of the fluoroalkylphosphonic acid on the carrier mobility in the organic semiconductor layer is evident.

An interesting aspect of the combination of fluoroalkylphosphonic acid SAMs with the organic semiconductor DPh-BTBT is that the turn-on voltage is extremely close to 0 V, as compared to the significantly more positive turn-on voltages of the DNTT TFTs (Figure 5b). The near-zero turn-on voltage of the DPh-BTBT TFTs is highly beneficial for the design of low-voltage, low-power circuits, especially complementary inverters and complementary ring oscillators.[31] Figure 5c shows the transfer curves of five DPh-BTBT TFTs with an $AlO_x/FC_{10}PA$-SAM gate dielectric fabricated on the same silicon substrate; all TFTs have a turn-on voltage of exactly 0 V. Similarly, transfer curves of five DPh-BTBT TFTs with a hybrid AlO_x/SAM dielectric based on all fluoroalkylphosphonic acid molecules available as well as TFTs with a bare AlO_x dielectric have been included in the Supporting Information (Figure S2).

DPh-BTBT TFTs with AlO_x/SAM gate dielectrics based on fluoroalkylphosphonic acids with five different chain lengths were also fabricated on flexible PEN substrates without heating the PEN during the semiconductor deposition. Thirty TFTs were measured on each substrate to determine the influence of the chain length of the fluoroalkylphosphic acid on the TFT characteristics, such as the threshold voltage, the gate leakage current, the carrier mobility, and the on/off current ratio. This could be helpful in identifying the appropriate choice of the fluoroalkylphosphonic acid to meet the specific device or circuit design requirements. Figure 6a shows the transfer curves of these TFTs and the threshold voltage plotted as a function of the chain length of the fluoroalkylphosphonic acid. Compared to the TFTs with an AlO_x gate dielectric, that is, without a SAM (as indicated by a dashed red line), the fluoroalkylphosphonic acid SAM leads to a significant shift in threshold voltage toward more positive values (Figure 6b), producing a threshold voltage very close to 0 V. This phenomenon has also been observed for pentacene p-channel and $F_{16}CuPc$ n-channel TFTs[15] as well as for TFTs employing DNTT and its derivatives as the semiconductor.[32] As seen in Figure 6b, in spite of the hybrid AlO_x/SAM gate dielectric being thicker than the AlO_x gate dielectric, the threshold voltage of all the TFTs with the hybrid gate dielectrics is much closer to 0 V, indicating the influence of the SAM in controlling the threshold voltage of the TFTs. Figure 6c also shows the gate leakage current measured at the maximum gate−source voltage (V_{GS} = −3 V) plotted as a function of the chain length. The gate current of the TFTs with the hybrid AlO_x/SAM gate dielectrics are 1 to 2 orders of magnitude smaller compared to the TFT with the AlO_x gate dielectric, confirming the beneficial effect of the SAM in the hybrid gate dielectrics.

Both the carrier mobility (Figure 6d) and the on/off current ratio (Figure 6e) of the TFTs fabricated on PEN substrates have maximum values for a medium chain length (0.4 cm^2/V s and 5 × 10^5 for TFTs with the $FC_{10}PA$ SAM), similar to the TFTs fabricated on silicon substrates (Figure 5a). When alkylphosphonic acids of varying chain lengths (from 6 to 18 carbon atoms) were used for the hybrid AlO_x/SAM gate dielectrics in pentacene TFTs, the alkyl SAMs with a medium chain length (10 to 14 carbon atoms) were also reported to produce the best TFT performance.[16−18] This was attributed to the observation that SAMs based on molecules with medium chain lengths tend to form the most well-ordered and most densely packed monolayers.[33−35] Similar dynamics between the fluoroalkylphosphonic acids might be at play here, but a spectroscopic investigation would be required to gain more information on the packing density and the ordering of the monolayers.

Static water contact angles on different fluoroalkylphosphonic acid monolayer surfaces were measured on PEN substrates (Figure 7) to ensure the quality of the monolayers and estimate the ordering and packing density in the SAMs. Apart from verifying the hydrophobic nature of the different SAMs, the variation of the water contact angle with the chain length provides an insight into the relative surface energies and underlying molecular interactions in the SAM. A smaller water contact angle observed for the shorter and longer chain lengths indicates more wettability on these surfaces and a higher surface energy. In comparison, the medium-chain-length $FC_{10}PA$ SAM surface has the largest water contact angle, indicating a low-wettability surface with low surface energy. This could be correlated to the most well-ordered and densely packed monolayer with maximum cohesive forces among the individual fluoroalkylphosphonic acid molecules, thus lowering the energy of the surface.

Out-of-plane XRD measurements on DPh-BTBT thin films on different fluoroalkylphosphonic acid SAMs also give insight into the dependence of the carrier mobility on the chain length of the phosphonic acids (Figure 8). On the medium-chain-length $FC_{10}PA$ SAM, the DPh-BTBT molecules are predominantly standing upright, with a dominant diffraction peak at 2θ = 4.65°. On the shorter-chain-length FC_6PA and on the longer-chain-length $FC_{14}PA$ SAMs, the XRD spectra indicate additional peaks at 2θ = 23.9° and 26.95°. This indicates that a fraction of the DPh-BTBT molecules on these SAMs are lying face-down, which is unsuitable for efficient charge transport in the lateral direction. This could explain the observed dependence of the carrier mobility on the chain length of the gate dielectric SAM. Additional numerical data regarding the XRD spectra can be found in the Supporting Information (Table S3).

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ACS Appl. Mater. Interfaces 2019, 11, 27104−27111

4. CONCLUSIONS

In this work, we have investigated the relatively new organic semiconductor DPh-BTBT, in combination with hybrid gate dielectrics based on fluoroalkylphosphonic acid SAMs. We observed a peculiar dependence of the semiconductor morphology and the resulting TFT performance on the choice of the substrate (silicon or PEN) and the substrate temperature during the semiconductor deposition: for DPh-BTBT molecules to form a closed layer with optimum carrier mobility, the semiconductor deposition should be carried out with substrate heating on silicon substrates and without substrate heating on flexible PEN substrates. Furthermore, the chain length of the fluoroalkylphosphonic acid molecules forming the SAM has a strong influence on the thin-film morphology of the semiconductor and the corresponding TFT performance. We find that the TFTs with the medium-chain-length $FC_{10}PA$-SAM have the highest carrier mobility and the largest on/off current ratio. By employing DPh-BTBT in combination with fluoroalkylphosphonic acid gate dielectric SAMs, organic TFTs with a turn-on voltage of 0 V can be fabricated, which may be beneficial for low-voltage, low-power integrated circuits.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.9b04361.

Out-of-plane XRD spectra and scanning electron microscopy images of DPh-BTBT thin films deposited onto bare AlO_x dielectrics on silicon as well as PEN substrates held at temperatures of 100 and 25 °C each during the semiconductor deposition and corresponding numerical data for all XRD spectra measured identifying peak positions, heights, and FWHM values (PDF)

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Notes

The authors declare no competing financial interest.

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Supporting Information

Achieving Ultralow Turn-On Voltages in Organic Thin-Film Transistors: Investigating Fluoroalkylphosphonic Acid Self-Assembled Monolayer Hybrid Dielectrics

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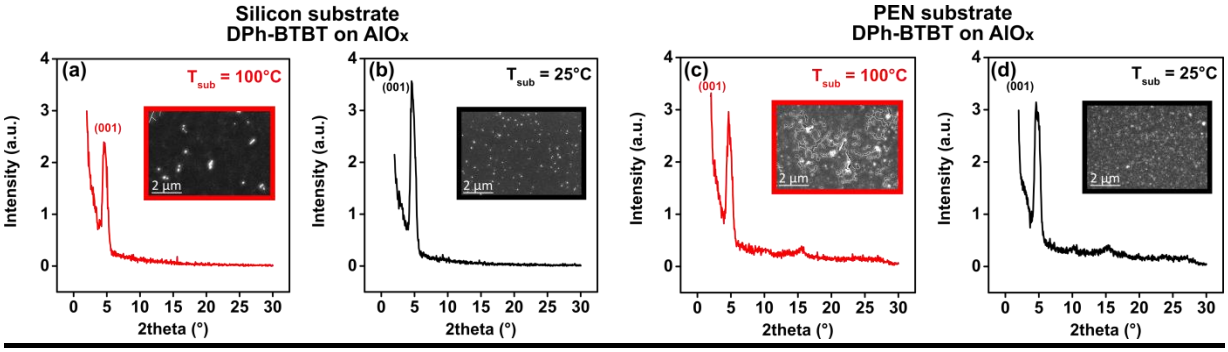

Figure S1: Out-of-plane XRD spectra and corresponding scanning electron microscopy images (insets) of DPh-BTBT thin-films deposited onto bare AlO_x dielectrics on silicon substrates held at temperatures of 100 °C (red line, (a)) and 25 °C (black line, (b)) and on PEN substrates held at a temperature of 100 °C (red line, (c)) and 25 °C (black line, (d)) during the semiconductor deposition.

Table S1: Corresponding numerical data for XRD spectra in Figure S1 measured on DPh-BTBT thin-films deposited on AlO_x dielectrics on silicon and PEN substrates at two different substrate temperatures during semiconductor deposition.

Substrate	T_{sub}	Peak	Peak position	Peak height	FWHM
Silicon	100 °C	(001)	4.55	478.28	0.8606
	25 °C	(001)	4.55	712.85	0.8717
PEN	100 °C	(001)	4.65	586.18	0.9998
		(003)	15.55	71.79	2.0054
	25 °C	(001)	4.6	623.31	1.0122
		(003)	15.35	76.97	2.2252

Table S2: Corresponding numerical data for XRD spectra in Figure 3 of main manuscript measured on DPh-BTBT thin-films deposited on AlO_x/$FC_{10}PA$ SAM hybrid dielectric on silicon and PEN substrates at two different substrate temperatures during semiconductor deposition.

Substrate	T_{sub}	Peak	Peak position	Peak height	FWHM
Silicon	100°C	(001)	4.65	21514.5845	0.54179
	25°C	(001)	4.65	34795.3858	0.52053
PEN	100 °C	(001)	4.55	11544.29	0.5688
		(020)	23.95	1872.35	4.5448
		(120)	27.05	2002.17	2.3494
	25 °C	(001)	4.65	28579.86	0.5436
		(002)	9.2	1675.85	4.2
		(003)	13.5	1369.72	3.8428

Table S3: Corresponding numerical data for XRD spectra in Figure 8 of main manuscript measured on DPh-BTBT thin-films deposited on three different AlO_x/SAM hybrid dielectrics on PEN substrates.

Phosphonic acid	Peak	Peak position	Peak height	FWHM
FC_6PA	(001)	4.6	22288.47	0.5588
	(002)	9.25	1629.37	1.45
	(003)	13.6	1749.81	11.75
	(020)	23.9	1532.15	3.95
	(120)	26.95	1422.24	1.95
$FC_{10}PA$	(001)	4.65	28579.87	0.5436
	(002)	9.2	1675.86	4.2
	(003)	13.5	1369.72	3.8428
$FC_{14}PA$	(001)	4.55	24915.34	0.4671
	(002)	9.15	1312.38	4.5
	(003)	13.65	976.37	4.85
	(020)	23.65	1676.39	3.9498
	(120)	26.9	2213.35	3.2441

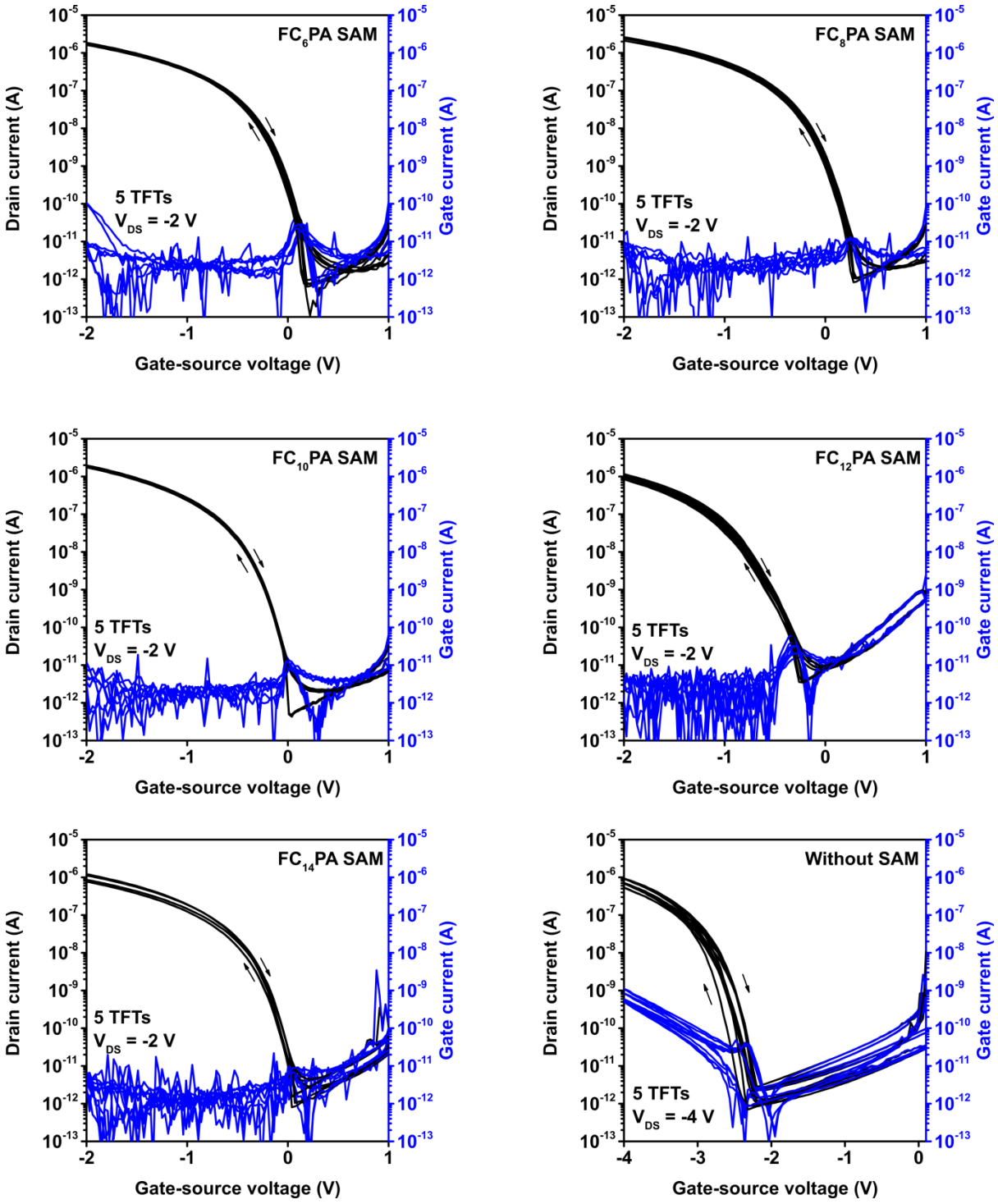

Figure S2: Transfer curves of five DPh-BTBT TFTs each with a hybrid AlO_x/SAM gate dielectric based on fluoroalkylphosphonic acids with five different chain lengths, along with a bare AlO_x dielectric (without SAM) fabricated on silicon substrates with substrate temperature at 100 °C during semiconductor deposition.