Accurate Capacitance Modeling and Characterization of Organic Thin-Film Transistors

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***Abstract*— This paper presents analysis of the charge storage behavior in organic thin-film transistors (OTFTs) by means of admittance characterization, compact modeling, and 2-D device simulation. The measurements are performed for frequencies ranging from 100 Hz to 1 MHz and bias potentials from zero to −3 V on top-contact OTFTs that employ air-stable and high-mobility dinaphtho-thieno-thiophene as the organic semiconductor. It is demonstrated that the dependence of the intrinsic OTFT gate–source and gate–drain capacitances on the applied voltages agrees very well with Meyer's capacitance model. Furthermore, the impact of parasitic elements, including fringe current and contact impedance, is investigated. The parameters used for the simulation and modeling of all the dynamic characteristics correspond closely to those extracted from static measurements. Finally, the implications of the admittance measurements are also discussed relating to the OTFTs dynamic performance, particularly the cutoff frequency and the charge response time.**

***Index Terms*— Admittance measurement, channel capacitance, device modeling and simulation, organic thin-film transistors.**

I. Introduction

ORGANIC thin-film transistors (OTFTs) are now making significant inroads into many new large-area applications, considering that they can be fabricated at low temperatures and with high throughput on a wide range of unconventional substrates, such as glass, plastic, fabric, and paper [1]. For further development, it is essential to understand the device physics and to study the limits of the device performance to be able to accurately model their behavior. The steady-state characteristics of the OTFTs have been extensively studied [2]–[4]. Vissenberg and Matters [2] have proposed an analytical model to describe the gate-voltage dependence of the field-effect mobility of OTFTs—an effect that was originally perceived by Brown *et al.* [3].

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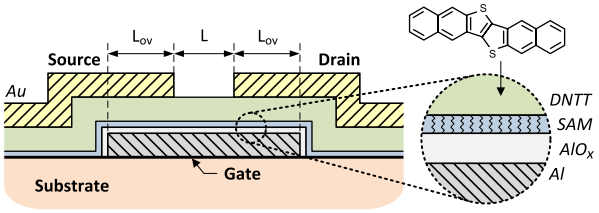

Fig. 1. Schematic cross section of the fabricated inverted-staggered (bottom-gate, top-contact) OTFT, where L is the channel length and L_{ov} is the gate-to-contact overlap. The molecular structure of the used dinaphtho-thieno-thiophene OSC is designated.

Based on that common point, Marinov and Deen [4] have derived an OTFT compact DC model that is valid for all operating regimes, i.e., linear and saturation above threshold, subthreshold, and reverse biasing. As for the dynamic characteristics of the OTFTs, recent works have reported *S*-parameter measurements of OTFTs to characterize the cutoff frequency [5], and also to study the influence of unintentional process misalignment between the device terminals on the dynamic performance [6]. Further investigations have used admittance measurements to model the OTFT channel and to describe the current injection mechanism through the contact interfaces between the metallic source/drain and the organic semiconductor (OSC) layers [7]–[11]. It has been proposed in [11] to adopt Meyer's model [12], which is used for silicon-based MOSFETs, to describe the charge storage effects of the OTFTs intrinsic capacitances. However, what is lacking at this point is a verification of this proposal by adequate comparison between capacitance measurements and simulations.

In this paper, we present experimental analysis of the OTFTs intrinsic capacitances at different biasing potentials and validate the results with accurate modeling as well as 2-D device simulations. Effects induced by the parasitic elements that extend beyond the periphery of the intrinsic transistor are carefully considered. We also investigate the frequency response of OTFTs by means of admittance measurements. A small-signal model is built to characterize both the resistive and the reactive parts of the measured device admittance.

II. OTFT Fabrication

As shown in Fig. 1, the inverted-staggered OTFT structure, which is also referred to as top-contact/bottom-gate configuration, was used for our OTFTs, as it offers better performance

compared to its coplanar counterparts [13], [14], i.e., staggered structures often have smaller contact resistance owing to the extended parts of the gate-induced channel beneath the contact regions [15]. Furthermore, dinaphtho[2, 3-b: 2′, 3′-f] thieno[3, 2-b]thiophene (DNTT) OSC was employed for our OTFTs as it features high intrinsic mobility, promising shelf-life and bias-stress stability, as well as little hysteresis behavior [16].

A set of three high-resolution silicon stencil masks was used to fabricate the fully patterned OTFTs on an alkali-free glass substrate that was coated with a 4-nm-thick adhesion layer of aluminum oxide formed by atomic layer deposition [17]. The OTFT layers, namely 30-nm-thick aluminum gate, 11-nm-thick DNTT, and 25-nm-thick gold source/drain contacts, were all deposited in vacuum through the shadow masks. Prior to the deposition of the DNTT, a hybrid dielectric (about 5.3-nm thick), which consists of an oxygen-plasma-grown AlO_x layer (3.6-nm thick) and a solution-processed self-assembled monolayer (SAM) of *n*-tetradecylphosphonic acid (1.7-nm thick), was formed. This hybrid gate dielectric features a high capacitance value ($\sim$560 nF/cm^2), which allows the OTFTs to operate at low supply voltages ($\leq$3 V) [16]. The OTFTs have channel widths (W) of 400 μm, channel lengths (L) of 200, 160, 140, 120, 100, 80, 50, and 30 μm, and gate-to-contact overlaps (L_{ov}) of 10 μm. Moreover, the OSC layer extends beyond the periphery of the intrinsic OTFTs by 30 μm on each side (also called fringe regions).

III. Experimental and Modeling Results

A. Static Characteristics

Static current–voltage (I–V) measurements were performed using a DC source/monitor unit (HP 4141B) on the chip, in the dark, in ambient air, and at room temperature. Using the transmission line method (TLM) analysis on our OTFTs at a drain–source voltage (V_{DS}) of -0.1 V, a set of parameters were extracted; an intrinsic charge carrier mobility (μ_o) of 2.1 cm^2/Vs and a threshold voltage (V_{TH}) of -1.04 V were calculated, and at a gate–source voltage (V_{GS}) of -3 V, a sheet resistance (R_{sh}) of 420 k$\Omega/\square$ and a contact resistance ($R_C \cdot W$) of 0.20 kΩcm were found. Fig. 2 shows the measured versus simulated data for the I–V output and transfer characteristics of the OTFT with $L = 200$ μm. Here we distinguish between two different simulations. The first is a 2-D device simulation developed on a Sentaurus Device simulator by Synopsys (designated as simulated in Fig. 2), while the second is a simple compact DC model adopted from silicon-based transistors and implemented on a SPICE simulator (designated as modeled in Fig. 2).

For the 2-D device simulation, the thin-film transistor (TFT) design was slightly simplified as illustrated in the inset of Fig. 2. However, comparative simulations for both structures showed negligible error. The used simulation parameters are summarized in Table I, noting that some of the values were extracted from admittance measurements as will be demonstrated further below. As for the compact DC model, the drain

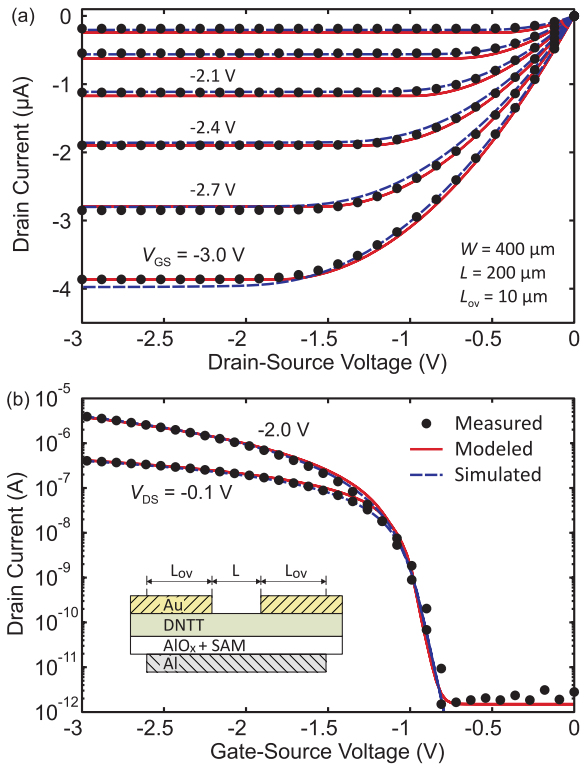

Fig. 2. Measured versus simulated (on Sentaurus Device) and modeled (on SPICE) static I–V characteristics of an OTFT ($W = 400$ μm, $L = 200$ μm). (a) Output characteristics. (b) Linear and saturation transfer characteristics. The inset shows the simplified OTFT schematic representation used for the simulation. The OTFT has an effective field-effect mobility (μ) of $\sim$2.0 cm^2/Vs, a turn-on voltage (V_{ON}) of -0.8 V, a threshold voltage (V_{TH}) of -1 V, and ON/OFF current ratios of 10^6 and 10^5 for the saturation and linear regimes, respectively.

current (I_D) of the OTFT above threshold is described by [4]

$$I_D = \begin{cases} \dfrac{\mu C_I}{2}\dfrac{W}{L}\left(2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2\right) \\ \quad \text{in linear; } V_{DS} < V_{GS} - V_{TH} \\ \dfrac{\mu C_I}{2}\dfrac{W}{L}(V_{GS} - V_{TH})^2 \\ \quad \text{in saturation; } V_{DS} \geq V_{GS} - V_{TH} \end{cases} \quad (1)$$

where μ is the effective charge carrier mobility and C_I is the dielectric capacitance per unit area. For the OTFT shown in Fig. 2, the following model parameters were used: $\mu = 1.9$ cm^2/Vs and $C_I = 560$ nF/cm^2 (Table I). Since the transistor has a relatively long channel length ($L = 200$ μm $\gg$ $L_{ov} = 10$ μm), contact effects are insignificant, and accordingly, the effective charge carrier mobility in both the saturation and linear operation regimes are very close to the intrinsic mobility and independent of the gate voltage. As depicted in Fig. 2, an excellent agreement between measured, simulated, and modeled data using the same device parameters was achieved.

B. Admittance Characteristics

Admittance (Y) measurements were conducted using an LCR meter (HP 4284A) at frequencies from 100 Hz up to 1 MHz under the same atmospheric conditions as in the

TABLE I
SIMULATION AND MATERIAL PARAMETERS

Parameter	Notation	Value
Al-gate work function	Φ_{Al}	4.1 eV
Au-contacts work function	$\Phi_{S/D}$	5.0 eV
DNTT-semiconductor thickness	d	11 nm
AlO_x-dielectric thickness	d_{ox}	3.6 nm
SAM-dielectric thickness	d_{SAM}	1.7 nm
AlO_x/SAM effective permittivity	ε_{is}	3.37
Dielectric capacitance per unit area	C_I	560 nF/cm^2
DNTT highest occupied molec. orbital	HOMO	−5.19 eV
DNTT lowest unoccup. molec. orbital	LUMO	−1.81 eV
DNTT band gap	E_G	3.38 eV
Intrinsic charge carrier mobility	μ_o	2.1 cm^2/Vs
Doping concentration in the OSC	N_A	1×10^{16} cm^{-3}
Fixed interface charges concentration[a]	N_{if}	5×10^{11} cm^{-2}

[a] A different value of $N_{if} = 1.1 \times 10^{12}$ cm^{-2} was used for dynamic simulations because the negative bias stress caused by $V_{GS} = -3$ V during the measurements resulted in a negative shift of V_{TH}.

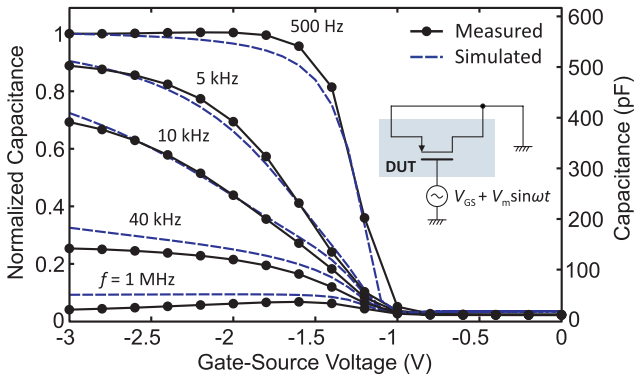

Fig. 3. Measured versus simulated capacitance–voltage (C–V) characteristics of an OTFT ($W = 400$ μm, $L = 200$ μm) as a function of gate bias and at different frequencies. The inset shows the used measurement setup, where the device under test (DUT) is the p-channel OTFT. The dashed line represents the simulations, assuming a mobility of $\mu = 2.0$ cm^2/Vs and a contribution of the fringe part of about 13%. Note that the simulations also fit well to the conductance–voltage (G–V) characteristics (not shown here).

static measurements. The capacitance (C) and the conductance (G) were calculated using equations $C = \mathrm{Im}(Y/\omega)$ and $G = \mathrm{Re}(Y)$, respectively, where ω is the angular frequency. To initially extract C_I, dedicated metal–insulator–metal (MIM) devices with different dimensions (200 × 200, 100 × 100, 50 × 50, and 10 × 10 μm^2) were fabricated on the same substrate. In principle, the MIM is a two-terminal pendant of the OTFT sharing the same layer structure except for the semiconductor. The average value measured for the MIMs with different areas was found to be $C_I = 560$ nF/cm^2 (Table I). With the hybrid insulator thickness of about $d_{is} = 5.3$ nm, an effective value of $\varepsilon_{is} = 3.37$ resulted for the relative dielectric constant.

Fig. 3 shows the capacitance–voltage (C–V) curves of the OTFT with $L = 200$ μm calculated from the measured admittance. For this setup, the source and drain contacts were electrically shorted and connected to the low terminal (virtual ground) of the LCR meter, while the gate electrode was connected to the high terminal. A DC potential sweep from zero to −3 V along with a superimposed AC voltage (V_m) of ±100 mV was applied to the gate. The C–V curves show a typical transition from depletion (at low absolute bias potential) to accumulation (at higher negative voltages), determined by the doping concentration of the semiconductor (Table I). Note that, as the frequency increases, the accumulated charges in the gate-induced channel cannot follow the signal. Considering the measurement at the frequency of $f = 500$ Hz, a maximum capacitance of $C_{max} = 566$ pF (in accumulation) and a minimum capacitance of $C_{min} = 13$ pF (in depletion) were measured. The value of C_{min} corresponds to the overlap capacitances ($2 \cdot C_{ov}$) between the gate and the source/drain contacts and can be modeled as a series sum of two dielectrics (with $\varepsilon_{is} = 3.37$ for the hybrid gate dielectric and $\varepsilon_{DNTT} = 2.84$ for the fully depleted layer of DNTT). On the other hand, the C_{max} is the geometrical capacitance between the gate and the channel and it is simply given by the hybrid dielectric capacitance per unit area C_I, while taking into consideration that the gate-induced channel extends beyond the periphery of the intrinsic OTFT through both the overlaps and the fringe regions. The pronounced ratio between the measured capacitances in the depletion and the accumulation modes (×44) is due to the patterning of the gate layer and the use of a relatively small gate overlap ($L_{ov} = 10$ μm $\ll L = 200$ μm) [11]. This helps in modeling the OTFT intrinsic capacitances accurately. Furthermore, Fig. 3 shows the results of the device simulation. At $f = 500$ Hz, the transition slope between accumulation and depletion is determined only by an unintentional doping (N_A). From the minimum capacitance, the effective layer thickness (d) of the OSC was estimated. At this frequency, the measured curve was well described with $N_A = 10^{16}$ cm^{-3} and $d = 11$ nm (Table I) with the exception of the transition region near −1 V; however, the error in this region is less than 10% and probably caused by the large voltage step in the measurement. To simulate correctly the flat band voltage a concentration of fixed interface charges of $N_{if} = 1.1 \times 10^{12}$ cm^{-2} was assumed. The frequency dependence of the C–V curves was well simulated by considering a mobility of $\mu = 2.0$ cm^2/Vs for the injected holes from the source/drain electrodes. For the highest frequencies (40 kHz and 1 MHz), a smaller contribution of the fringe part should be assumed to reduce the error. Nevertheless, the value of the mobility corresponds very well with the aforementioned TLM measurements and static simulation.

C. Frequency Response Analysis

To investigate the charge response behavior, the capacitance and the loss (G/ω) of the OTFT with $L = 200$ μm were measured as a function of frequency (Fig. 4). Similar to the previous setup (Fig. 3), the results include the intrinsic as well as the parasitic OTFT components, i.e., the fringe and overlap regions. Above threshold, the holes appear to respond well to the applied small signal up to a certain frequency depending on the gate potential; however, their responsiveness starts to degrade above this frequency due to limited lateral flow of holes [11]. At the said frequency, also referred to as relaxation or cutoff frequency (f_c), the measured capacitance decreases and the loss reaches a maximum. This kind of dispersion

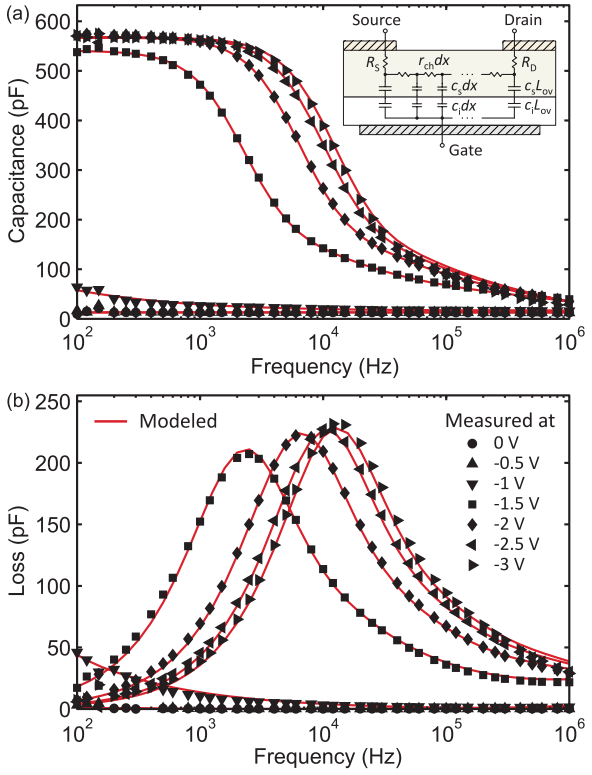

Fig. 4. Measured versus modeled admittance of an OTFT ($W = 400$ μm, $L = 200$ μm) as a function of frequency and at different gate biases. (a) Capacitance–frequency (C–f) characteristics, where $C = \mathrm{Im}(Y/\omega)$. (b) Loss–frequency ($G/\omega$–$f$) characteristics, where $G = \mathrm{Re}(Y)$. The OTFT small-signal equivalent circuit model is depicted in the inset.

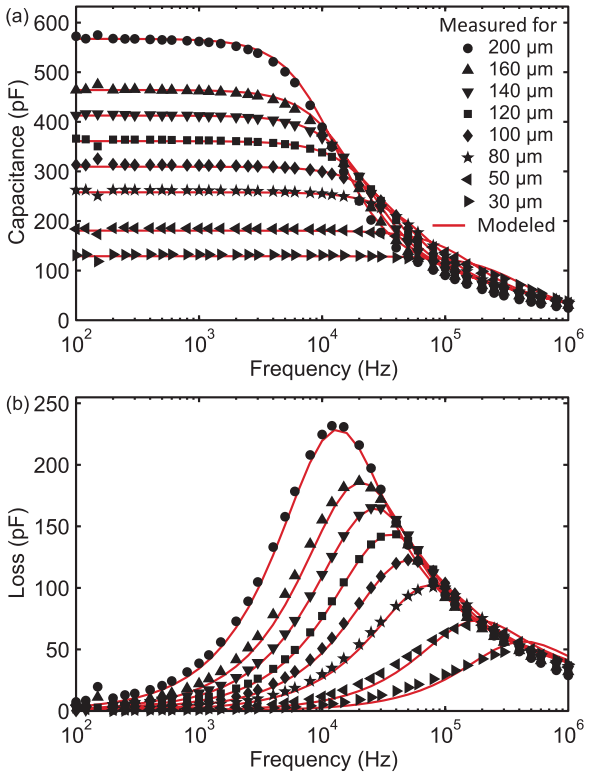

Fig. 5. Measured versus modeled admittance of several OTFTs ($W = 400$ μm, $L = 200$, 160, 140, 120, 100, 80, 50, and 30 μm) as a function of frequency and at a gate bias of $V_{\mathrm{GS}} = -3$ V. (a) Capacitance–frequency (C–f) characteristics, where $C = \mathrm{Im}(Y/\omega)$. (b) Loss–frequency ($G/\omega$–$f$) characteristics, where $G = \mathrm{Re}(Y)$. Note that the model (shown in the inset of Fig. 4) here used a constant set of parameters except for the channel length (L).

occurs as a result of the frequency- and voltage-dependent accumulation layer, while another dispersion is expected to occur above 1 MHz due to the overlap regions. For the latter case, the measured capacitances fall to zero.

A small-signal equivalent circuit was developed to explain the conduction mechanism and quantitatively evaluate the impact of the parasitic impedances. As depicted in the inset of Fig. 4, the model consists of a distributed circuit with parasitic resistances at the contact [8]–[11]. The channel and the fringe regions act as an RC transmission line owing to the distributed coupling between the gate electrode and the semiconductor. From the geometry, the contribution of the fringe part was found to be about 16.5%.

In total, the model consists of five parameters: source/drain contact resistances ($R_{\mathrm{S,D}}$), channel resistance per unit length (r_{ch}), dielectric capacitance per unit length (c_i), and semiconductor capacitance per unit length (c_s). The resistances $R_{\mathrm{S,D}} = R_C/2$ [Ω] and $r_{\mathrm{ch}} = R_{\mathrm{sh}}/W$ [Ω/cm] were directly obtained from the TLM measurements. Since there is no potential difference between the drain and source electrodes during this measurement, r_{ch} was assumed to be uniform along the whole channel. In accumulation, the influence of the semiconductor capacitance was negligible ($c_s \gg c_i$). In depletion, the capacitance c_s governs the change in the depletion layer thickness depending on the gate voltage. Finally, the capacitance $c_i = C_I \cdot W$ [F/cm] was acquired from the capacitance measurements of the MIM structures. At $V_{\mathrm{GS}} = -3$ V, the following values were used: $R_C \cdot W = 0.24$ kΩcm, $R_{\mathrm{sh}} = 500$ k$\Omega/\square$, and $C_I = 560$ nF/cm^2 (there is only a slight difference of <20% to the values extracted from TLM). As shown in Fig. 4, the model shows good agreement with both the capacitance and loss of the measured admittance over the complete frequency range (100 Hz–1 MHz).

Furthermore, the measured admittance at $V_{\mathrm{GS}} = -3$ V for all the fabricated OTFTs with channel lengths of $L = 200$, 160, 140, 120, 100, 80, 50, and 30 μm was compared with the small-signal equivalent circuit as shown in Fig. 5. A reliable and precise fit of the model to the experimental data was obtained. The measurements shown in Figs. 4(b) and 5(b) verify that the cutoff frequency, which was estimated at the peak of G/ω, increases with decreasing channel length and with increasing gate bias. This approximately conforms with the expression $f_c \simeq \mu(V_{\mathrm{GS}} - V_{\mathrm{TH}})/(2\pi L^2)$ [8].

The dynamic performance of the intrinsic OTFT can be estimated by the response time of the gate-induced charges in the channel [9]. Evaluation of the RC transmission line model (Fig. 4) of the channel in [18] has yielded the following expressions for the gate-to-channel capacitance (C_{ch}) and loss (G_{ch}/ω):

$$C_{\mathrm{ch}} = \frac{C_I W L}{\alpha} \cdot \left(\frac{\sinh\alpha + \sin\alpha}{\cosh\alpha + \cos\alpha} \right) \tag{2}$$

$$\frac{G_{\mathrm{ch}}}{\omega} = \frac{C_I W L}{\alpha} \cdot \left(\frac{\sinh\alpha - \sin\alpha}{\cosh\alpha + \cos\alpha} \right) \tag{3}$$

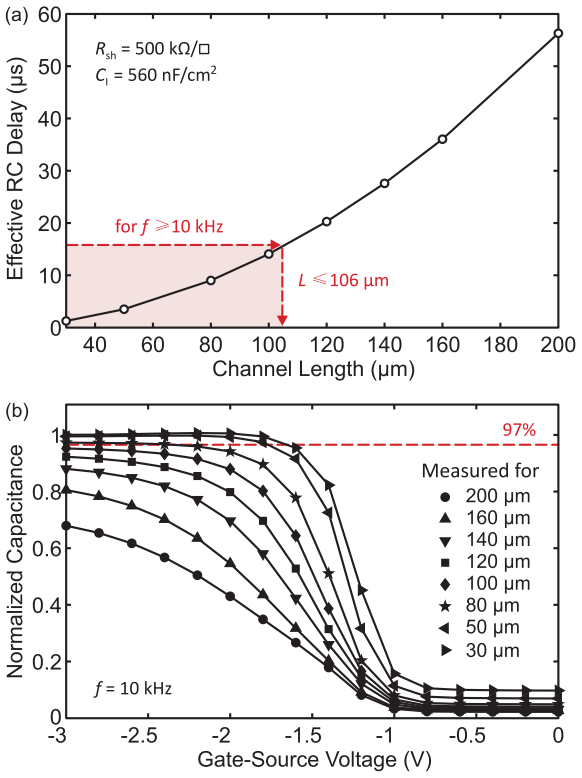

Fig. 6. (a) Calculated effective delay (τ) for 97% of the total charges in the OTFT channel to be induced and effectively responding. (b) Normalized C–V measurements at $f = 10$ kHz. The contribution of the fringe part was assumed to be constant (16.5%) for all channel lengths, and the normalization was done by dividing the measurement results by $1.165\,C_I W(L+2L_{ov})$. There is an error of $< 3\%$ because of this assumption.

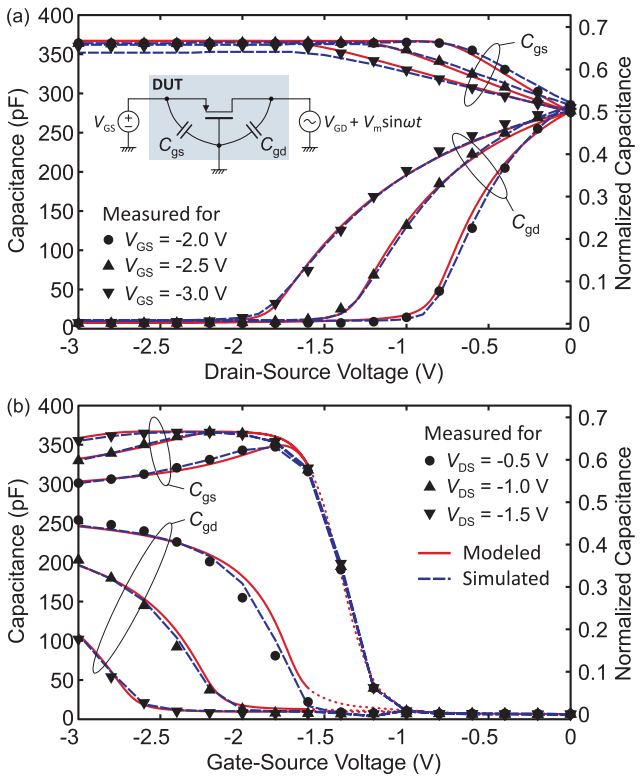

Fig. 7. Measured gate–source (C_{gs}) and gate–drain (C_{gd}) capacitances along with modeled and simulated results of an OTFT ($W = 400$ μm, $L = 200$ μm). (a) C_{gs} and C_{gd} as a function of V_{DS}. (b) C_{gs} and C_{gd} as a function of V_{GS}. Note that the modeled curves are represented by (4) and (5), which are valid above threshold (solid lines). The voltage-dependent fringe factor of the simulated curves was calculated by dividing the measured value of C_{gs} by the simulated intrinsic value. The inset shows the used measurement setup.

where $\alpha = \sqrt{\omega C_I R_{sh} L^2/2}$. A delay time ($\tau$), needed for 97% (when $\alpha = 1$) of the total charges in the channel to be induced and effectively responding, is accordingly determined as $\tau = 1/\omega = R_{sh} C_I L^2/2$ (the relation is slightly different from the one given in [9] because of the different device structure used). Fig. 6(a) shows the calculated τ as a function of L using the same modeling parameters $R_{sh} = 500$ kΩ/□ and $C_I = 560$ nF/cm^2, from which information about the maximum f achieved for a given minimum L and/or maximum L needed for a given f can be deduced. For example, one can estimate from Fig. 6(a) that for operation at $f = 10$ kHz, the OTFTs should have $L \leq 106$ μm. This corresponds closely with the normalized C–V measurements of the OTFTs at 10 kHz as depicted in Fig. 6(b).

D. Meyer's Capacitance Model

In principle, the application of a drain–source bias to the OTFT results in a nonuniform distribution of charges along the channel. An accurate description of this effect requires a distributed capacitance model, which can in practice be simplified into lumped capacitive elements between the source, drain, and gate terminals. In this case, the resulting errors in circuit simulations are typically small [19]. We have been considering so far admittance measurements with shorted source and drain contacts; however, a different setup was used here to account for the variations in the stored charges of the OTFT at different V_{DS} and V_{GS}. Accordingly, the gate electrode was connected to the low terminal of the LCR meter, while the source and drain contacts were connected alternatively to the high terminal of the LCR meter and a DC voltage source [11]. The DC voltages V_{DS} and V_{GS} were both swept from zero to −3 V, and an AC signal of ±100 mV with $f = 500$ Hz was applied to either the source or the drain.

Fig. 7 shows the measured gate–source (C_{gs}) and gate–drain (C_{gd}) capacitances along with modeled and simulated results for the OTFT with $L = 200$ μm. Again, the data include both the intrinsic and parasitic components. Similar to the previous measurements, the parasitic component is composed of about 16.5% for the fringe region and a constant 6.5 pF (C_{ov}) for each of the gate–source and gate–drain overlap areas. By excluding the parasitic components, it was found that $C_{gs} = C_{gd} = 1/2\,C_{ch}$ at $V_{DS} = 0$ V, while C_{gs} and C_{gd} approach $2/3\,C_{ch}$ and zero, respectively, at $V_{DS} > V_{GS} - V_{TH}$ (saturation regime). This charge storage effect complies with Meyer's capacitance model, which was developed originally for silicon-based MOSFETs [12]. Moreover, the result indicates that a small change in the applied V_{DS} when the channel is pinched off during saturation regime does not have an impact on the gate or channel charges; however, the channel is completely assigned to the source terminal, resulting in a maximum value for C_{gs} [19].

According to the Meyer's capacitance model, the distributed intrinsic capacitances C_{gs} and C_{gd} above threshold are given by [12], [19]

$$C_{gs} = \frac{\partial Q_G}{\partial V_{GS}}\bigg|_{V_{GD}} = \frac{2}{3} C_I W L \left[1 - \left(\frac{V_{GT} - V_{DSe}}{2V_{GT} - V_{DSe}}\right)^2\right] \quad (4)$$

$$C_{gd} = \frac{\partial Q_G}{\partial V_{GD}}\bigg|_{V_{GS}} = \frac{2}{3} C_I W L \left[1 - \left(\frac{V_{GT}}{2V_{GT} - V_{DSe}}\right)^2\right] \quad (5)$$

where $V_{GT} = V_{GS} - V_{TH}$, and V_{DSe} is the effective drain–source voltage that is equal to V_{DS} for $V_{DS} < V_{GT}$ and is equal to V_{GT} for $V_{DS} > V_{GT}$. V_{DSe} is actually used to avoid discontinuity at the onset of the saturation region and it is expressed as [19]

$$V_{DSe} = \frac{1}{2}\left[V_{DS} + V_{GT} - \sqrt{V_\delta^2 + (V_{DS} - V_{GT})^2}\right] \quad (6)$$

where V_δ is a constant voltage that determines the width of the transition region. In principle, Meyer's model does not guarantee charge conservation and there have been attempts in [20] and [21] to derive other models for the OTFTs intrinsic capacitances. However, we preferred to use here the simple Meyer's model because the resulting errors in circuit simulations are usually small. Using $C_I = 580$ nF/cm^2, $V_{TH} = -1.18$ V, and $V_\delta = 0.1$ V, in addition to multiplying both (4) and (5) by 1.165 for the fringe region and adding 6.5 pF for the overlap capacitance (C_{ov}), a precise fit between the modeled and measured data was accomplished as depicted in Fig. 7.

Furthermore, the measured and modeled characteristics were compared with the device simulation results as demonstrated in Fig. 7. Using the same simulation parameters given in Table I, excellent agreement for all voltage regions was obtained for both C_{gs} and C_{gd}. It was necessary here to include a voltage-dependent fringe factor because otherwise the results were not well described. The reason is simply the smaller influence of fringe effects for small intrinsic capacitances, which occurs in the case of the subthreshold or the linear operation regions.

IV. Conclusion

Frequency response analysis on top-contact OTFTs based on DNTT by means of admittance measurements were performed. A small-signal equivalent circuit based on a distributed transmission line model was used to produce a good fit to the data for different operating frequencies (100 Hz–1 MHz), biasing potentials (−3 V to zero), and channel lengths (30–200 μm). Material parameters extracted from the dynamic *C–V* measurements were similar to the ones obtained from the static *I–V* characteristics, except for the density of fixed interface states, which was due to the negative bias stress imposed during the dynamic measurements. Moreover, the charge storage behavior in the OTFT was very well described by 2-D simulation as well as compact modeling. The dependence of the intrinsic capacitances C_{gs} and C_{gd} on the applied voltages V_{GS} and V_{DS} showed excellent agreement with Meyer's capacitance model, which can in principle be easily incorporated into a SPICE simulator. All the necessary parameters employed by the simulation and modeling conformed closely to the values extracted from the static measurements.

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