Compact DC Modeling of Organic Thin-Film Transistors Including Their Parasitic Non-Linear Contact Effects Based on a Novel Extraction Method

Samar Elsaegh, Ute Zschieschang, James W. Borchert, Hagen Klauk, Hans Zappe, and Yiannos Manoli

***Abstract*— This article presents a novel generic method for the extraction of the current–voltage characteristics of organic thin-film transistors (TFTs) that specifically accounts for the individual contributions of the source and drain contacts and their nonlinear behavior. Based on this extraction method, an analytical model has been derived that describes the behavior of the intrinsic TFT and of the source and drain contacts both in the linear and the saturation regimes. The essential feature of the proposed extraction method is that it does not depend on or assume any physical phenomena underlying the electrical characteristics of the contacts. Instead, it extracts the current–voltage characteristics of the contacts which can then be fit to any physics-based TFT model. This is beneficial both for circuit designers and for those developing physics-based TFT models. The proposed extraction method has been applied to organic TFTs fabricated on flexible plastic substrates in the staggered and coplanar device architectures using two different small-molecule organic semiconductors. The compact dc model has been used to simulate organic TFTs with channel lengths ranging from 4 to 100 μm and a transimpedance amplifier circuit based on TFTs with different channel lengths, and the results are in good agreement with the measurements.**

***Index Terms*— Compact modeling, contact resistances, extraction method, modeling contact effects, organic thin-film transistors (TFTs).**

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I. Introduction

ORGANIC thin-film transistors (TFTs) can usually be fabricated at temperatures around or below 100 °C and, therefore, on a variety of unconventional substrates, such as plastics and paper. This makes them good candidates for large-area and flexible electronic systems, such as sensor arrays and active-matrix displays. For many of these applications, it is desirable to utilize TFTs with small device dimensions in order to exploit the area efficiently and to achieve a small device capacitance and thus a high operating frequency [1]. However, when the channel length (L_{ch}) of the TFTs is small, the impact of the nonlinear contact resistances on the overall device behavior is quite severe and may dominate over the channel resistance [2], [3]. These nonlinear contact resistances must thus be properly accounted for in-circuit simulations and hence in the underlying device models.

The dc characteristics of organic TFTs can in principle be described by adapting the models originally developed for single-crystal (MOSFETs) [4]. However, when considering the contact effects, modeling becomes significantly more challenging, due to the lack of a full description of the device physics and due to the wide variety of organic semiconductors, contact materials, TFT architectures, film thicknesses and process methods involved in the fabrication of TFTs [3].

Currently, two approaches to modeling the dc characteristics of TFTs can be found in the literature. One approach consists of analyzing the structure of the TFTs and understanding the physical phenomena that determine their behavior. For this, complete knowledge of all device parameters is required. In addition, a number of assumptions have to be made, for example, that the contact resistance is independent of the channel length [5], [6] or that the value of the mobility-enhancement factor is known [1]. Three such models were reviewed and summarized by Kim et al. [3]. A wide range of physical phenomena controlling the behavior of organic TFTs and their contacts have been introduced and modeled separately or collectively, usually by fitting the parameters of the proposed equations to the measurement results.

Some of the physical interpretations that have been proposed are described below.

1) The widely used variable range hopping (VRH) model describes the dependence of the intrinsic charge-carrier mobility in the organic semiconductor on the applied gate–source voltage [7] through an empirical power law, and this power-law dependence has been adopted in most organic-TFT models, including the models developed by Marinov and Deen [5] and by Sohn et al. [8].
2) The space-charge-limited current (SCLC) model describes the charge transport near the interface between the semiconductor and the contacts using the Mott–Gruney law [9] and is used in a number of organic-TFT models (e.g., [8] and [10]).
3) Some models describe the exchange of charge carriers between the contact metal and the organic semiconductor using exponential or power-law [10] Schottky-barrier equations.

The main disadvantage of this physical interpretation approach to TFT modeling is that a large number of trial-and-error iterations are required in order to fit the parameters to the measurement data, which can lead to large parameter errors if the proposed physical description is not sufficiently accurate. The other modeling approach consists of utilizing a method for extracting the electrical characteristics and the parameters of the intrinsic TFTs and their contacts. The advantage of the latter approach is that it does not require any physical understanding or any material-specific investigations to derive the TFT equations and extract the device parameters.

This article features an original generic method that aims at separately extracting the current–voltage characteristics and the related parameters of the intrinsic TFT and of the source and drain contacts, without making any assumptions regarding the physicals underlying their electrical characteristics. This method can be applied to any TFT that shows clearly defined linear and saturation regions in the output characteristics. Based on this method, a compact dc model has been derived for p-channel TFTs fabricated in the staggered and the coplanar device architectures using vacuum-deposited small-molecule semiconductors [11]. The derived model has been verified by comparing the simulation results to measurements of an organic-TFT-based transimpedance amplifier.

The article is organized as follows. In Section II, the technique that is most frequently employed to extract the contact resistance of TFTs is briefly reviewed, highlighting the drawbacks of this method. In Section III, the new extraction method is proposed and explained in detail. In Section IV, the new method is applied to organic TFTs fabricated in the staggered and coplanar device architectures, and the extracted TFT parameters are compared. In Section V, simulations using the new compact model are performed on individual TFTs and on analog circuits, and the results are compared to the measurement results. Section VI provides a conclusion.

II. Problem Definition

Existing contact-resistance-extraction methods can be divided into two categories: single-transistor methods [12], [13] and channel-length-scaling methods [14]. However, as discussed in [15], none of these methods is able to describe and model the current–voltage characteristics reliably. The most widely used method is the transmission line method (TLM) [14], [16] which belongs to the category of channel-length-scaling methods. This method is briefly discussed in this section.

The concept of the TLM derives from the fact that the total resistance (R_t) of the TFT is the sum of the channel resistance (R_{ch}) and the contact resistances (R_c): $R_t = R_c + R_{ch}$. These resistances are usually normalized to the channel width (W_{ch}): $R_t \cdot W_{ch} = R_c \cdot W_{ch} + R_{sheet} \cdot L_{ch}$, where R_{sheet} is the sheet resistance of the organic semiconductor ($R_{sheet} = R_{ch} \cdot (W_{ch}/L_{ch})$). When the width-normalized total resistance ($R_t \cdot W_{ch}$), measured under certain biasing conditions, is plotted versus the channel length (L_{ch}), it is possible to estimate the sheet resistance (R_{sheet}) and the total contact resistances (R_c) from the slope and the y-intercept of the plot.

However, the TLM makes a number of assumptions and simplifications that complicate the full extraction and a complete understanding of the contact behavior. For example, the TLM assumes that the contact resistance is independent of the channel length at a constant drain–source voltage [15], which is an unrealistic simplification, especially when the channel length is small. This is due to the nonlinearity of the contact characteristics which implies that the contact resistance depends on the voltage drop across the contacts and, thus, on the channel length [10]. This unrealistic assumption can lead to a nonlinear relation between R_t and L_{ch} when a linear relation is expected, as in [8, Fig. 10]. To correct for this, R_c and R_{sheet} should be extracted at each channel length from the slope of the R_t-versus-L_{ch} curve at this channel length. The second disadvantage of the TLM is that it cannot relate the extracted contact resistances to the voltage that drops across the contacts, as this voltage drop is not accessible from the external nodes of the transistor. Furthermore, the TLM method can be applied only in the deep linear regime where the current–voltage characteristics are dependent on both the intrinsic TFT and the source and drain contacts [15]. This makes it impossible to analyze the behavior of each contact separately. For these reasons, the TLM cannot provide the information required to develop accurate models for the source contact, the drain contact and the intrinsic TFT separately.

III. Methodology Description

Our methodology is based on the fact that the saturation drain current (I_{sat}) of a TFT is affected only by the intrinsic TFT parameters and the source contact, but not by the drain contact. This is illustrated in Fig. 1 which shows simplified schematics of TFTs with different contact contributions. Fig. 1(a) illustrates an intrinsic field-effect transistor (FET) without any contact resistances, so I_{sat} is directly proportional to the square of the effective gate–source voltage. For a FET with a drain resistance, shown in Fig. 1(b), I_{sat} will not be affected by this resistance, because the effective gate–source voltage is independent of the drain resistance. However, as seen in Fig. 1(c), the effective gate–source voltage applied

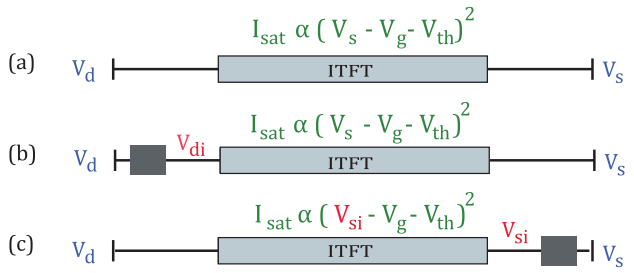

Fig. 1. Illustration of the idea underlying the parameter-extraction methodology. (a) FET without any parasitic contact effects. (b) FET with parasitic drain resistance. (c) FET with parasitic source resistance.

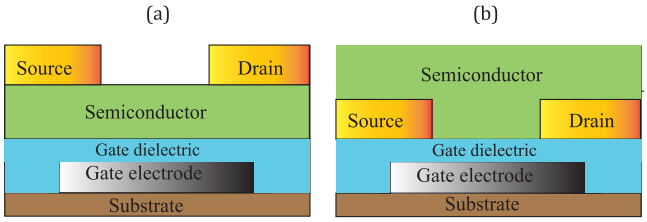

Fig. 2. Schematic cross sections of organic TFTs fabricated in the (a) inverted staggered device architecture and (b) inverted coplanar architecture.

across the intrinsic part of the TFT depends on the source resistance, and so does I_{sat} [10]. The parameter extraction is a three-step process.

1) The intrinsic TFT parameters are extracted from the measured output characteristics (drain current as a function of the drain–source voltage for various gate–source voltages).
2) The current–voltage curve of the source contact is derived from the saturation regime obtained from (1).
3) The current–voltage curve of the drain contact is obtained from the linear regime estimated from (1) and (2).

In this article, no assumptions were made regarding initial device parameters or charge-transport physics. The only assumptions are that the current–voltage characteristics of the intrinsic organic TFT follow the equations derived for the ideal MOSFET and that all deviations from the ideal (i.e., intrinsic) transistor behavior arise from the source and drain contacts. We demonstrate the parameter-extraction procedure on p-channel TFTs fabricated in the inverted staggered architecture using dinaphtho[2,3-b:2',3'-f]thieno [3,2-b]thiophene (DNTT), as shown in Fig. 2(a). The TFTs were fabricated on flexible polyethylene naphthalate (PEN) substrates. Aluminum gate electrodes were deposited in vacuum. The gate dielectric is a combination of 3.6-nm-thick oxygen-plasma-grown AlO_x and a 1.7-nm-thick tetradecylphosphonic acid self-assembled monolayer (SAM) [11]. Gold source and drain contacts of 25 nm thick were deposited in vacuum. All layers were patterned using shadow masks [11], with gate-to-source and gate-to-drain overlaps (L_{ov}) of 20 μm. Each set of output characteristics analyzed throughout the extraction procedure is an average of measurements performed on five to ten TFTs in order to reduce the effect of process variations.

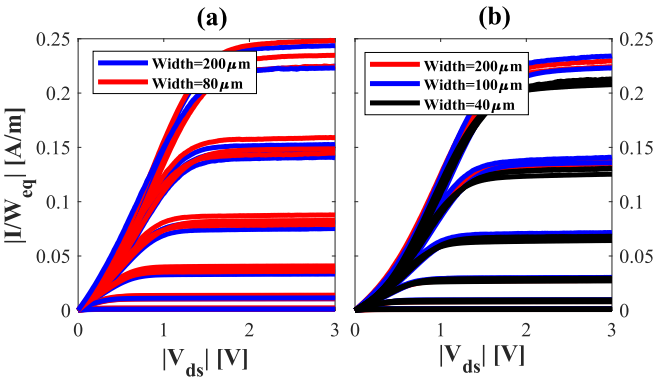

Fig. 3. Normalization of the equivalent width of (a) six TFTs with a channel width of 80 or 200 μm ($L_{ch} = 4$ μm), and (b) seven TFTs with a channel width of 40, 100, or 200 μm ($L_{ch} = 8$ μm).

A. Fringe-Current Modeling

Before starting the extraction procedure, the measured TFT characteristics are normalized to the channel width (W_{ch}) in order to obtain a generic model for all W_{ch} and L_{ch}. However, despite the fact that the intrinsic TFT, the source resistance and the drain resistance are all affected by W_{ch} in the same manner, the normalization should not be done by simply dividing by W_{ch}, because this would ignore the contribution of the fringe currents [17]. The influence of these fringe currents can be modeled as an extension of W_{ch} by the fringe width (W_{fringe}) [18], which can be determined by superimposing the measured output characteristics of TFTs with different channel widths after normalizing the drain current to the equivalent width ($W_{eq} = W_{ch} + W_{fringe}$) for the same channel length and the same biasing conditions, as shown in Fig. 3. According to [16], W_{fringe} is a function of W_{ch}, L_{ch} and L_{ov}. For the TFTs employed in this article, W_{fringe} was found to range from 8 μm for $L_{ch} = 4$ to 15 μm for $L_{ch} = 100$ μm. For the sake of simplicity, an average value of *10* μm has been found to provide good fits for all TFT dimensions employed in this article ($L_{ch} = 4$ to 100 μm, $W_{ch} = 20$ to 200 μm, $L_{ov} = 20$ to 30 μm). Also, the linear relationship between W_{fringe} and L_{ch} ($W_{fringe} = 7.7\mu\text{m} + 0.073 \cdot L_{ch}$) has been found to provide very good fits for all TFT dimensions.

B. Intrinsic TFT

To extract the correct parameters of the intrinsic TFT, it is necessary to consider the effects of the contacts and of the fringe currents. The analysis is thus performed in the saturation regime, rather than the linear regime, since the drain current in the saturation region is not affected by the drain contact, as discussed in the beginning of Section III. This leaves the effect of the source contact. For an ideal MOSFET, the drain current in the saturation regime can be written as

$$I_{sat} = \frac{1}{2}\frac{W_{eq}}{L_{ch}}\mu_0 C_{diel}(V_{si} - V_g + V_{th})^2 \quad (1)$$

where μ_0 is the intrinsic charge-carrier mobility, C_{diel} is the gate-dielectric capacitance per unit area, V_{th} is the threshold voltage, and V_{si} is the potential of the gate-field-induced carrier channel at the location closest to the source contact.

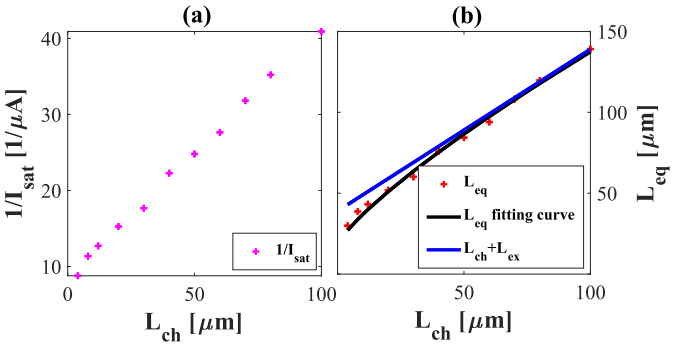

Fig. 4. (a) Inverse of the saturation drain current I_{sat} measured for $V_g = -3$ V, $V_d = -3$ V, $V_s = 0$ V and plotted versus the channel length L_{ch}. (b) Equivalent channel length L_{eq} (which is proportional to $1/I_{sat}$) plotted versus L_{ch} in order to extract the value of the extension length L_{ex} by extrapolating the linear function $L_{ch} + L_{ex}$ from the fit to the data at large channel lengths to $L_{ch} = 0$.

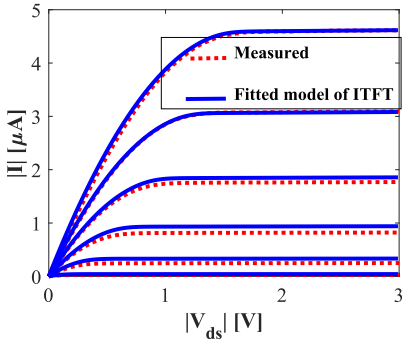

Fig. 5. Fitting the parameters of (6) with $W_{eq} = 210$ μm, $L_{eq} = 140$ μm to the output characteristics of a TFT with $W_{ch} = 200$ μm, $L_{ch} = 100$ μm measured for $|V_g| = 1.5$ to 3 V in steps of 0.3 V.

For simplicity, the source contact effect can be considered as an extension length (L_{ex}) in series with the intrinsic channel length L_{ch}. Equation (1) can thus be written as

$$I_{sat} = \frac{1}{2}\frac{W_{eq}}{L_{ch} + L_{ex}}\mu_0 C_{diel}(V_s - V_g + V_{th})^2 \tag{2}$$

where $L_{ch} + L_{ex}$ is the equivalent length (L_{eq}) that replaces L_{ch} in order to account for the effect of the source-contact resistance. To extract the value of L_{ex}, the inverse of the saturation drain current I_{sat} measured at a particular biasing condition in the saturation regime ($V_g = -3$ V, $V_d = -3$ V, $V_s = 0$ V) is plotted as a function of the channel length L_{ch}; see Fig. 4(a)]. The equivalent length L_{eq}, which is directly proportional to the inverse of I_{sat}, is then plotted versus L_{ch} where its slope matches the slope of the linear function $L_{ch}+L_{ex}$ at large channel lengths. The linear function $L_{ch} + L_{ex}$ is then extrapolated to $L_{ch} = 0$, yielding the value of L_{ex} as the y-intercept [see Fig. 4(b)]. As can be seen in Fig. 4(b), the source-contact effect is completely accounted for with the expression $L_{eq} = L_{ch} + L_{ex}$ by using $L_{ex} = 40$ μm for $L_{ch} > 60$ μm ($L_{ch} < 60$ μm will be discussed later). Consequently, the parameters of the intrinsic TFT can be extracted by fitting the measured output characteristics of the TFT with the largest channel length ($L_{ch} = 100$ μm) at $V_g = -3$ V to (3), used to describe the dc behavior in the linear and saturation regimes, while using the value of W_{eq} instead of W_{ch} (to account for the fringe currents) and L_{eq} instead of L_{ch} (to account for the source-contact resistance)

$$I = \frac{1}{2}\frac{W_{eq}}{L_{eq}}\mu_0 C_{diel}[(V_s - V_g + V_{th})^2 - (V_d - V_g + V_{th})^2] \tag{3}$$

where I is the current flowing through the source and drain terminals of the transistor. V_d is equal to the applied drain voltage in the linear regime and equal to $V_g - V_{th}$ in the saturation regime. In [5], the subthreshold regime was included in (3) through an interpolation function for the overdrive source and drain voltages (4). In addition, this interpolation function smoothens the transition between the linear and saturation regimes, which leads to (5)

$$f(V, V_g) = V_{ss} ln\left[1 + e^{\frac{V - V_g + V_{th}}{V_{ss}}}\right] \tag{4}$$

where V is V_s or V_d, and V_{ss} is a voltage parameter whose value can be determined from the subthreshold slope [5]

$$I = \frac{1}{2}\frac{W_{eq}}{L_{eq}}\mu_0 C_{diel}[(f(V_s, V_g))^2 - (f(V_d, V_g))^2]. \tag{5}$$

To include the contribution of the channel-length modulation, (5) has been modified according to [5], which results in the following expression that covers all three regimes of operation of any intrinsic TFT:

$$I = \frac{1}{2}\frac{W_{eq}}{L_{eq}}\mu_0 C_{diel}(1 + \lambda(V_s - V_d))[(f(V_s, V_g))^2 - (f(V_d, V_g))^2] \tag{6}$$

where λ is the channel-length-modulation coefficient. In Fig. 5, the intrinsic-TFT-model parameters developed using (6) (μ_0, V_{th}, λ, and V_{ss}) have been extracted by fitting (6) with $W_{eq} = 210$ μm and $L_{eq} = 140$ μm to the characteristics for a TFT with $W_{ch} = 200$ μm and $L_{ch} = 100$ μm measured at $V_g = -3$ V. For $C_{diel} = 0.7$ μ F/cm^2 and $L_{ov} = 20$ μm, the intrinsic parameters of DNTT TFTs fabricated in the inverted staggered architecture are as follows: $\mu_0 = 3.3$ cm^2/Vs, $V_{th} = -1$ V, $\lambda = 0.01$, and $V_{ss} = 0.09$ V. These are essentially identical to the parameters extracted in [15] and [16] for TFTs based on the same architecture and materials.

C. Source Contact

Having determined the intrinsic parameters of the current–voltage behavior of the TFTs makes it possible to extract the effects of the source and drain contacts separately. As discussed earlier, the value of the saturation drain current I_{sat} is affected only by the source contact, not by the drain contact. As shown in Fig. 5, the source resistance can be properly accounted for by assuming an extension length (L_{ex}) of 40 μm. However, this value of L_{ex} does not provide a good fit when $|V_g|$ is small (see Fig. 5) or when $L_{ch} < 60$ μm at $|V_g| = 3$ V [see Fig. 4(b)]. Therefore, the value of L_{ex} (and thus also the value of L_{eq}) are extracted

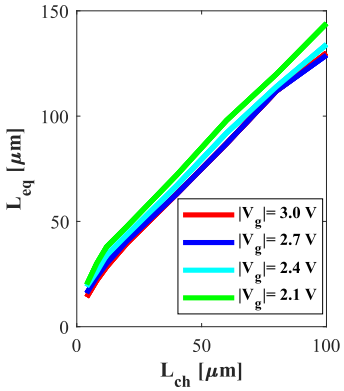

Fig. 6. Extracting L_{eq} for each channel length at $|V_g|$ = 2.1, 2.4, 2.7 and 3 V.

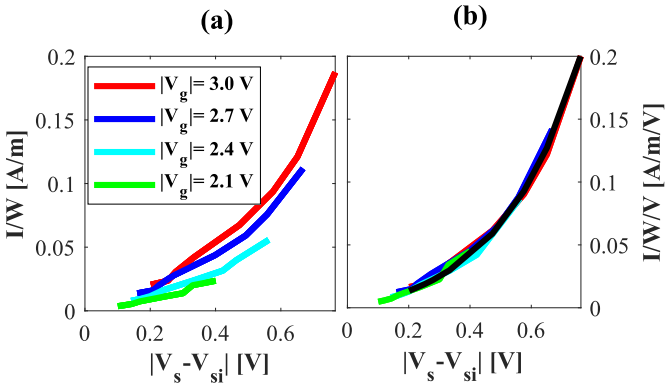

Fig. 7. Width-normalized current–voltage characteristics of the source contact (a) for $|V_g|$ = 2.1, 2.4, 2.7, and 3 V, and (b) normalized to the gate-field-accumulated charge density by dividing by $(V_{si}\text{-}V_g\text{+}V_{th})^{0.8}$.

by fitting (6), utilizing the extracted intrinsic parameters, to match the measured saturation drain current at each L_{ch} and each V_g, as shown in Fig. 6. Solving (1) (with the channel length L_{ch} and the channel voltage at the location closest to the source contact V_{si}) and (2) (with the equivalent length $L_{eq} = L_{ch} + L_{ex}$ and the applied source voltage V_s) simultaneously with V_s grounded, we can derive the value of V_{si} for the corresponding $I_{D,sat}$ as in (7)

$$V_{si} = (V_{th} - V_g)\left(\sqrt{\frac{L_{ch}}{L_{eq}}} - 1\right). \tag{7}$$

In Fig. 7(a), the voltage drop across the source contact ($|V_s\text{-}V_{si}|$) is plotted versus the corresponding drain current normalized to the equivalent width for different absolute values of the gate voltage $|V_g|$. As expected, the source resistance increases with decreasing $|V_g|$. The reason is that $|V_g|$ controls the density of charges available at the interface between the source contact and the semiconductor. To normalize this effect, each drain-current point along the curve is divided by the corresponding effective gate–source-overdrive voltage ($V_{si}\text{-}V_g + V_{th}$), which is directly proportional to the charge density. However, at least for the TFTs investigated here (inverted staggered DNTT TFTs with gate-to-contact overlaps of 20 μm), the best fit was obtained by normalizing the drain current to the gate–source-overdrive voltage raised to the power 0.8, $(V_{si}\text{-}V_g + V_{th})^{0.8}$, Fig. 7(b). The physical interpretation of this power factor is illustrated in Fig. 8 where it can be seen that the channel voltage under the source is not constant along the length of the gate-to-contact overlap L_{ov}. Instead, it has a certain value V_{si} at the leading edge of the contact (labeled point A in Fig. 8) and decreases monotonically to zero (at point B) along the contact. Consequently, the value of 0.8 for the power factor is a good average to account for this contact–voltage variation.

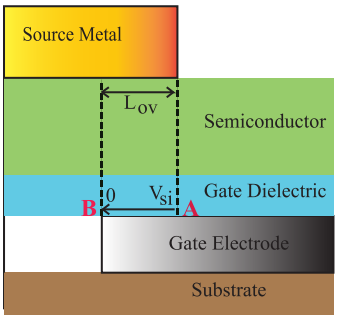

Fig. 8. Schematic cross section of the source-contact region of an inverted staggered TFT. The channel source voltage is not constant along the length of the gate-to-source overlap L_{ov}. This variation of the contact voltage affects the value of the power factor that produces the most accurate results when the current is normalized to the charge density in Fig. 7(b).

If so desired, the curves in Fig. 7(b) can be fit to various equations depending on the physical phenomenon assumed to be governing the TFT characteristics. In this article, the curves are fit to an exponential expression according to a reverse-biased Schottky-diode model [black line in Fig. 7(b)]. As a result, the overall expression for the current–voltage characteristics of the source contact is

$$I = L_{ov} J_{os} (W_{ch} + W_{fringe}) \left(e^{\frac{V_s - V_{si}}{\eta_s V_T}} - 1\right) (V_{si} - V_g + V_{th})^{P_{snorm}} \tag{8}$$

where J_{os} is the current density underneath the gate-to-source overlap, V_T is the thermal voltage (25.9 mV at room temperature), η_s is the nonideality factor, and P_{snorm} is the charge-normalization power factor at the source contact. For the inverted staggered p-channel DNTT TFTs with $L_{ov} = 20$ μm utilized in this article, the extracted parameters for the current–voltage characteristics of the source contact are as follows: $J_{os} = 1800$ A/m^2, $\eta_s = 21.45$, and $P_{snorm} = 0.8$.

D. Drain Contact

An electrical model is developed that combines the current–voltage characteristics of the source contact and of the intrinsic TFT described by (8) and (9), respectively, by solving the two equations simultaneously

$$I = \frac{1}{2}\frac{W_{eq}}{L_{ch}} \mu_0 C_{diel} (1 + \lambda (V_{si} - V_d))[(f(V_{si}, V_g))^2 - (f(V_d, V_g))^2]. \tag{9}$$

As illustrated in Fig. 9, when comparing the measured output characteristics with those predicted by the model that includes

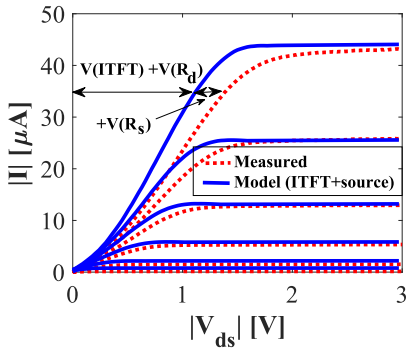

Fig. 9. Output characteristics of an organic TFT with W_{ch} = 200 μm and L_{ch} = 4 μm (red), and output characteristics calculated using an electrical model that takes into account the intrinsic TFT and the source-contact behavior (blue).

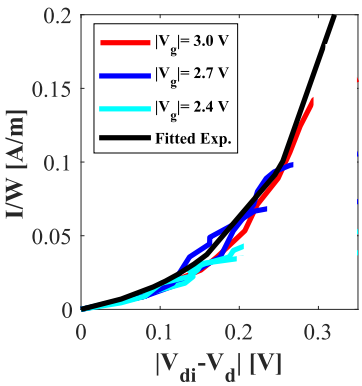

Fig. 10. Width-normalized current–voltage characteristics of the drain contact normalized to the gate-field-induced charge density by dividing by $(V_{di}\text{-}V_g\text{+}V_{th})^{0.8}$, together with the fit exponential curve (black).

the intrinsic TFT and the source contact, one notices that the agreement is satisfactory only in the saturation regime, but not in the linear regime. The reason is that the model so far ignores the drain resistance which affects the linear regime, but not the saturation regime. The drain resistance can thus be extracted from the difference between the drain–source voltage for a specific drain current in the linear regime predicted by the model (which accounts for the intrinsic TFT and the source contact, but not for the drain contact) and the drain–source voltage for the same drain current in the linear regime in the measured output characteristics (which are affected by the drain resistance); this difference is the voltage drop across the drain contact (see Fig. 9). Similar to the source-contact effect, the current–voltage characteristics of the drain contact are obtained, normalized to W_{eq} and to the gate-field-induced charge density, and plotted as shown in Fig. 10. The notable nonlinearity in the curves in Fig. 10 is due to the unavoidable device-to-device variations usually experienced in thin-film technologies, where each point of these curves is deduced from different transistors. An exponential expression has been fit to the curves, shown in black. As a result, the expression that describes the current–voltage characteristics of the drain contact is

$$I = L_{ov} J_{od} (W_{ch} + W_{fringe}) \left(e^{\frac{V_{di}-V_d}{\eta_d V_T}} - 1 \right) (V_{di} - V_g + V_{th})^{P_{dnorm}} \tag{10}$$

where J_{od} is the current density underneath the gate-to-drain overlap, η_d is the non-ideality factor, and P_{dnorm} is the charge-normalization power factor. For the TFTs used in this article, $J_{od} = 27250$ A/m^2, $\eta_d = 4$, $P_{dnorm} = 0.8$.

IV. Inverted Staggered and Coplanar TFTs Models

The extraction method proposed in this article has been applied to two types of TFTs: 1) p-channel TFTs fabricated in the inverted staggered architecture using DNTT as the semiconductor [11] and 2) p-channel TFTs fabricated in the inverted coplanar architecture using 2,9-diphenyl-DNTT (DPh-DNTT) as the semiconductor [19], both with L_{ov} =20 μm. The extracted generic equations that describe the intrinsic TFT and the source and drain contacts in both architectures are summarized in following equations:

$$I = \frac{1}{2} \frac{W_{eq}}{L_{ch}} \mu_0 C_{diel} (1 + \lambda (V_{si} - V_{di})) \times [(f(V_{si}, V_g))^2 - (f(V_{di}, V_g))^2] \tag{11}$$

$$I = t J_{os} W_{eq} \left(e^{\frac{V_s - V_{si}}{\eta_s V_T}} - 1 \right) (V_{si} - V_g + V_{th})^{P_{snorm}} \tag{12}$$

$$I = t J_{od} W_{eq} \left(e^{\frac{V_{di} - V_d}{\eta_d V_T}} - 1 \right) (V_{di} - V_g + V_{th})^{P_{dnorm}} \tag{13}$$

where t is the effective injection length. In the case of inverted staggered TFTs, t is equal to L_{ov} (20 μm in this work). In the case of inverted coplanar TFTs, t is the thickness of the source/drain contacts (30 nm in this work).

The values extracted for the various TFT parameters are summarized in Table I. As can be seen, the intrinsic channel mobility of DPh-DNTT is 40% larger than that of DNTT. More importantly, the injection current density J_{os} is three orders of magnitude larger in the coplanar DPh-DNTT TFTs than in the staggered DNTT TFTs. The impact of the drain contact on the TFT performance is negligible in the case of the coplanar DPh-DNTT TFTs, in contrast to the staggered DNTT TFTs, where the effect of the drain contact is significant, as seen in Fig. 9. This difference in the effect of the contacts is due in part to the difference in device architecture, the difference in the semiconductor material and the thickness of the semiconductor layer that plays a significant role in the high contact resistances experienced in the staggered architecture. Furthermore, it can be seen that the charge-normalization-power factor applied for the staggered architecture ($P_{snorm} = 0.8$) is not encountered in the coplanar architecture ($P_{snorm} = 1$). This is because, in the latter, there is no V_{si} gradient along the contact.

V. Extraction Method and Model Verification

The model equations and parameters for the inverted staggered p-channel TFTs, extracted in Section IV, have been implemented in Verilog-A for computer simulations and solved, simultaneously, using the Cadence design framework. Simulations have been carried out for individual TFTs with

TABLE I
COMPARISON BETWEEN THE EXTRACTED ORGANIC TFT (OTFT) PARAMETERS FOR INVERTED STAGGERED AND INVERTED COPLANAR CONFIGURATIONS

Parameters	μ_o [cm^2/Vs]	V_{th} [V]	W_{fringe} [μm]	λ [1/V]	J_{os} [A/m^2]	η_s -	P_{snorm} -	J_{od} [A/m^2]	η_d -	P_{dnorm} -
Inverted staggered p-channel OTFT	3.3	-1	10	0.01	1.8x10^3	21.45	0.8	27250	4	0.8
Inverted coplanar p-channel OTFT	4.715	-0.815	10	0.01	2.8x10^6	21.45	1	-	-	-

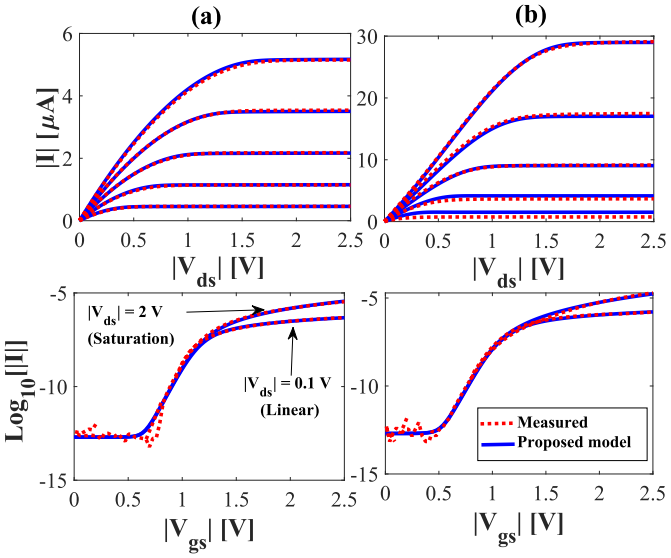

Fig. 11. Measured and simulated output characteristics (top) and transfer characteristics (bottom) of a TFT with (a) L_{ch} = 100 μm, W_{ch} = 200 μm and (b) L_{ch} = 4 μm, W_{ch} = 200 μm.

different channel lengths L_{ch}. As illustrated in Fig. 11, the simulation results are in excellent agreement with the measured characteristics for the entire range of channel lengths using the parameters in Table I.

Moreover, to evaluate our new compact model for circuits, the gain-boosted common-gate transimpedance amplifier first reported in [20] has been implemented with different TFT dimensions using the model, as shown in Fig. 12. This circuit is an analog amplifier designed to transform the dc current generated by a photodetector into a dc voltage. As shown in Fig. 12, the transimpedance amplifier consists of two parts, namely, a common-gate input stage and a voltage-controlled resistor (VCR), both of which are implemented here using only organic TFTs. This circuit is well suited for evaluating our new compact TFT model, since the VCR contains a transistor (T_2) that operates in the linear regime, while all other transistors operate in saturation regime. Therefore, we are able to investigate the model for TFTs working in the saturation regime as well as for TFTs working in the linear regime. Also, by implementing two versions of the circuit, one in which L_{ch} of T_2 equals 4 μm and another in which L_{ch} equals 20 μm, we can verify the model for different channel lengths.

The potentials present at three different nodes of the circuit have been considered in this test for an input-current

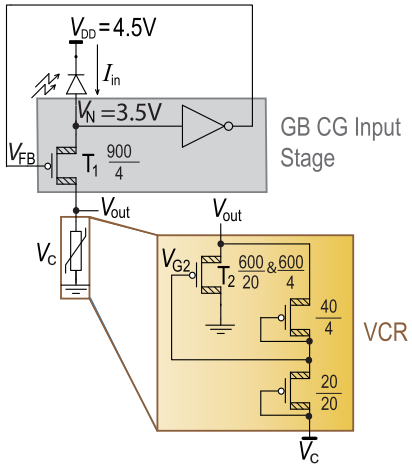

Fig. 12. Circuit schematic of a gain-boosted common-gate transimpedance amplifier, first reported in [20] and utilized here to evaluate the model.

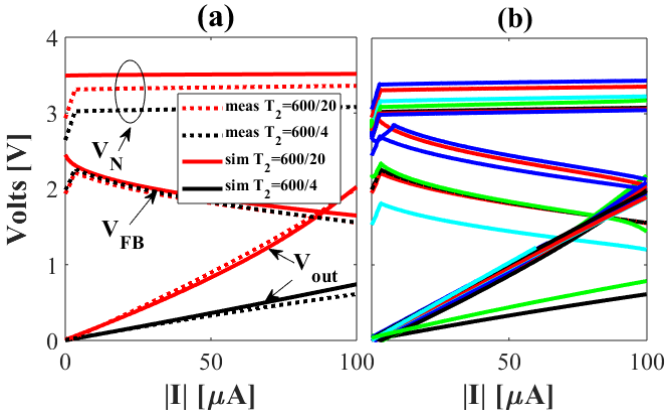

Fig. 13. (a) Measured (dotted lines) and simulated (continuous lines) potentials at three nodes of the gain-boosted common-gate transimpedance amplifier from Fig. 12: V_{out}, V_{FB}, and V_N. Transistor T_2 has a channel length of either 4 μm (black lines) or 20 μm (red lines). (b) Results of measurements performed on seven circuits in which transistor T_2 has a channel length of 20 μm and on two circuits in which T_2 has a channel length of 4 μm. The simulation results coincide approximately with the average of the measurement results.

sweep from 0 to 100 μ A, namely, the output-voltage node (V_{out}), the input node (V_N), and the feedback node (V_{FB}). In Fig. 13(a), the measured and simulated voltages at these three nodes are plotted versus the input current, once for a circuit in which transistor T_2 has a channel length of 20 μm and once for a circuit in which T_2 has a channel length of

4 μm (the channel width is 600 μm in both cases). The results show that the model describes the dc behavior of the circuit accurately, even when the channel length of the TFTs is small (4 μm). Fig. 13(b) shows the results of measurements performed on seven circuits in which T_2 has a channel length of 20 μm and on two circuits in which T_2 has a channel length of 4 μm, including the two circuits in Fig. 13(a) (the channel width is 600 μm in all cases). The results demonstrate that the simulation results coincide approximately with the average of the measurement results. One should note that although the internal nodes (V_N and V_{FB}) deviate among the individual devices, the output voltage (V_{out}) is fairly constant across the samples.

VI. Conclusion

In this article, we have proposed a new generic approach for extracting the current–voltage characteristics of organic TFTs that explicitly take into account the effects of the source and drain contacts. This approach is applicable to any TFT, regardless of the device architecture, materials, layer thicknesses, and fabrication process. The extraction method has been applied to TFTs fabricated in the inverted staggered architecture using DNTT semiconductor and to TFTs fabricated in the inverted coplanar architecture using DPh-DNTT semiconductor. A compact analytical model that describes the static behavior of the two types of organic TFTs has been derived and implemented for computer simulations using Verilog-A. The model has been used successfully to compare simulations to measurements of individual TFTs with channel lengths ranging from 4 to 100 μm and to transimpedance amplifiers based on organic TFTs with different channel lengths.

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