

A 3-V, 6-Bit C-2C Digital-to-Analog Converter Using Complementary Organic Thin-Film Transistors on Glass

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Abstract—A 3-V, 6-bit DAC is designed using complementary organic thin-film transistors on a glass substrate. The p-channel and n-channel transistors utilize dinaphthothienothiophene (DNTT) and hexadecafluorocopperphthalocyanine ($F_{16}CuPc$) as the organic semiconductors, respectively. A low-temperature process compatible with flexible plastic substrates is used to fabricate the circuit. The DAC utilizes switched capacitors to circumvent the large transistor-current variations, and a C-2C structure to avoid the large capacitances that would otherwise be required in the thin-film process. With calibration, the DAC achieves DNL and INL of less than 1 LSB at a conversion rate of 100 Hz.

Index Terms—C-2C ladder, digital-to-analog converter, organic integrated circuits, organic thin-film transistors.

I. INTRODUCTION

THE recent development of low-voltage p-channel and n-channel organic thin-film transistors (OTFTs) offers potential for many novel applications. Because OTFTs can be manufactured at or near room temperature, they allow integrated circuits to be made on flexible plastic substrates that do not withstand the high processing temperatures used for silicon-based devices. Furthermore, the ability to print organic OTFTs advances the prospect of inexpensive large-area electronics [1]. This mechanical flexibility and large-area coverage make OTFTs naturally compatible to integration with innovative organic materials such as artificial muscles [2], polymer actuators [3] and chemical sensors [4]. In these applications, data converters are the essential links between the digital processors and the inherently analog interfaces.

This paper reports on the design of an organic 6-bit digital-to-analog converter (DAC) [5]. Since accurate conversions require a linear transfer function between digital inputs and analog outputs, precise matching between circuit elements is crucial. Unfortunately, OTFTs suffer from large device-to-de-

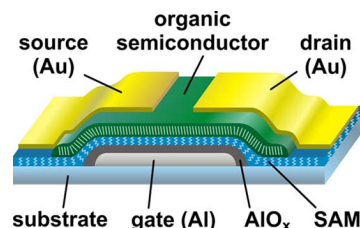


Fig. 1. Cross-sectional view of an OTFT, the organic semiconductor can be either p-type (DNTT) or n-type ($F_{16}CuPc$). source and drain metals are gold; gate metal is aluminium.

vice variations, often orders of magnitude greater than that of silicon transistors [6]. As a result, organic analog circuits have only been sparsely reported due to the difficulty of working with the inconsistencies of organic transistors [7]–[10]. However, with careful process-device-circuit co-design, moderate precision analog circuitry is within reach.

The design described in this paper uses both p-channel and n-channel OTFTs to achieve complementary operation. Although n-channel OTFTs typically have much lower mobility than p-channel OTFTs, the complementary circuit allows for a larger signal swing than a p-channel-only circuit. Furthermore, recent work has shown consistent increases in the mobility of n-channel OTFTs [11] and [12]. It is our expectation that n-channel OTFTs will soon approach the performance of p-channel OTFTs. In the presented DAC, the OTFTs are fabricated on a glass substrate with a maximum process temperature of 90 °C. A high-capacitance gate dielectric allows for supply voltages as low as 3 V, suitable for battery-powered applications. To minimize the impact of transistor mismatch, the DAC operates in the switched-capacitor mode, where linearity is determined by the more tractable capacitor matching. The relatively large minimum feature size of our organic thin-film process (20 μm) necessitates the C-2C structure for the DAC. Calibration is added to enhance the linearity performance.

Section II of this paper describes the organic thin-film fabrication process. Section III presents the detailed circuit design, including analyses on DAC linearity, matching properties of organic components, and the limits on operational speed. Section IV summarizes the measurement setup and results.

II. FABRICATION PROCESS

As shown in Fig. 1, our OTFTs use an inverted staggered (bottom-gate, top-contact) device structure. A 40-nm-thick

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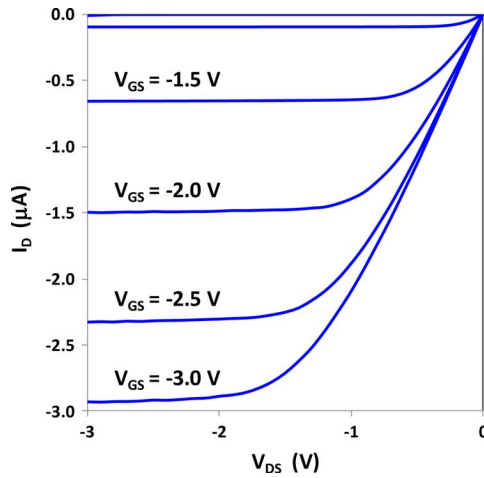


Fig. 2. Measured output characteristics of a p-channel OTFT (length = $20\ \mu\text{m}$, width = $400\ \mu\text{m}$) with V_{GS} swept from 0 to $-3\ \text{V}$ in $-0.5\ \text{V}$ increments.

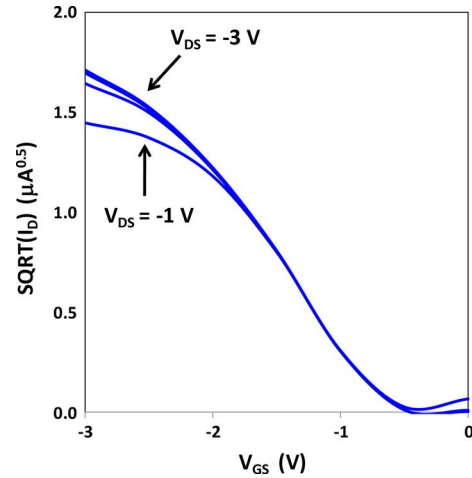


Fig. 4. Measured transfer characteristics of a p-channel OTFT (length = $20\ \mu\text{m}$, width = $400\ \mu\text{m}$) with V_{DS} swept from -1 to $-3\ \text{V}$ in $-0.5\ \text{V}$ increments.

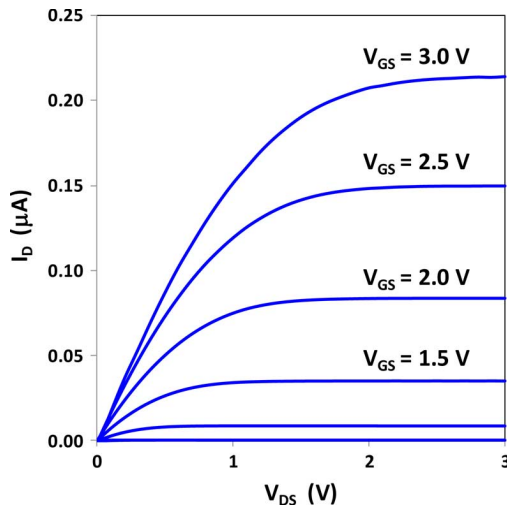


Fig. 3. Measured output characteristics of an n-channel OTFT (length = $20\ \mu\text{m}$, width = $400\ \mu\text{m}$) with V_{GS} swept from 0 to $3\ \text{V}$ in $0.5\ \text{V}$ increments.

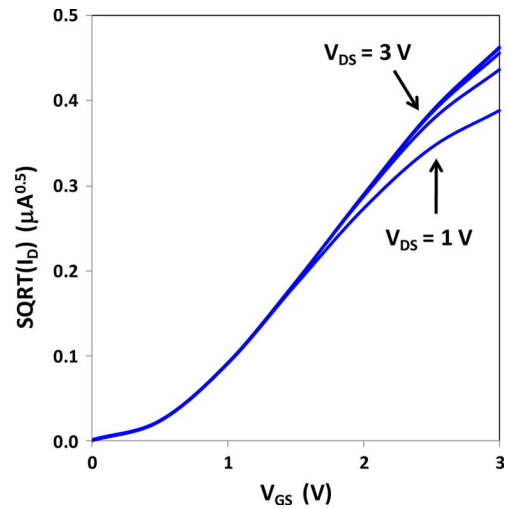


Fig. 5. Measured transfer characteristics of an n-channel OTFT (length = $20\ \mu\text{m}$, width = $400\ \mu\text{m}$) with V_{DS} swept from 1 to $3\ \text{V}$ in $0.5\ \text{V}$ increments.

Ti–Au interconnect layer was first deposited by evaporation onto the glass and patterned by photolithography and wet etching. 50-nm-thick aluminum was then deposited by thermal evaporation through a shadow mask to define the gate electrodes of the OTFTs. The substrate was briefly exposed to oxygen plasma to create a 3.6-nm-thick AlO_x layer and immersed in a 2-propanol solution of octadecylphosphonic acid, allowing a 2.1-nm-thick organic self-assembled monolayer (SAM) to form on the aluminum oxide. The total thickness of the AlO_x /SAM dielectric is 5.7 nm, with a capacitance of $7\ \text{fF}/\mu\text{m}^2$. This dielectric serves as the gate dielectric for the OTFTs. 30-nm-thick DNTT [13] and F_{16}CuPc [14] were then deposited in vacuum through shadow masks to form the semiconductors for the p-channel and n-channel OTFTs, respectively. Finally, 30-nm-thick gold was evaporated through a fourth shadow mask to provide the source and drain contacts of the OTFTs. The use of shadow masks has the advantage that

the source and drain contacts can be prepared on top of the organic semiconductors—providing better injection efficiency compared with bottom contacts—without exposing the organic semiconductors to deleterious chemicals [15]. Connections between devices are made via traces on the interconnect layer. The measured output characteristics of a p-channel OTFT and of an n-channel OTFT are shown in Figs. 2 and 3, respectively. The measured transfer characteristics of the OTFTs are shown in Figs. 4 and 5, respectively. Both devices exhibit the typical OTFT behaviors, including non-idealities such as contact resistance and gate-bias-dependent mobility [16].

The capacitors are created simultaneously with the OTFTs by intersecting an aluminum trace (deposited with the OTFT gate) with a gold trace (deposited with OTFT source and drain contacts). The aluminum trace serves as the bottom electrode; the gold trace serves as the top electrode. The capacitors share the same AlO_x /SAM dielectric as the OTFTs.

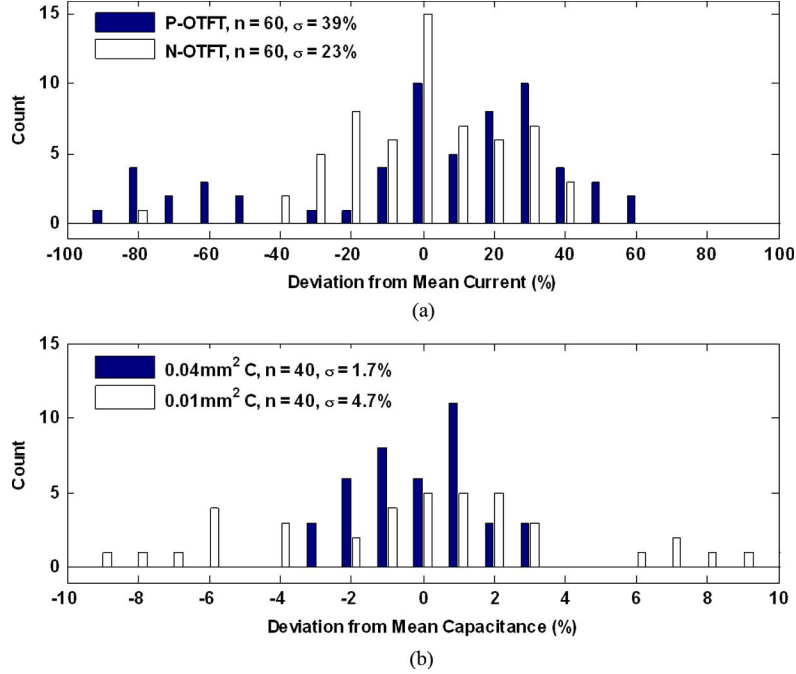


Fig. 6. Distributions of (a) OTFT drain currents and (b) unit capacitances.

III. CIRCUIT DESIGN

A. DAC Architecture

Numerous DAC architectures exist, including current-steering and switched-capacitor types. For a current-steering DAC, the critical parameter is the matching of the drain currents between the elemental transistors that make up the array. For a B -bit binary-weighted DAC, the maximum allowed current mismatch can be calculated using the following expressions [17]:

$$\sigma_{\text{INL}} = \frac{\text{INL}}{\sqrt{2}(\text{erfinv}(Y))} \quad (1)$$

$$\sigma_{\text{DNL}} = \frac{\text{DNL}}{\sqrt{2}(\text{erfinv}(Y))} \quad (2)$$

$$\sigma_{u\text{-INL}} \approx \frac{2\sigma_{\text{INL}}}{\sqrt{2^B}} \quad (3)$$

$$\sigma_{u\text{-DNL}} \approx \frac{\sigma_{\text{DNL}}}{\sqrt{2^B - 1}} \quad (4)$$

where erfinv is the inverse error function, and $\sigma_{u\text{-INL}}$ and $\sigma_{u\text{-DNL}}$ represent the standard deviations (σ) of the transistor-current mismatches that lead to INL error and DNL error, respectively. With $B = 6$, $\text{INL} < 1 \text{ LSB}$, $\text{DNL} < 1 \text{ LSB}$ and $Y = 0.95$ (corresponding to a confidence interval of 2 sigma), we obtain $\sigma_{u\text{-INL}} < 12.7\%$ and $\sigma_{u\text{-DNL}} < 6.4\%$. However, in our organic thin-film process, the use of shadow masks and non-uniformities in device mobility introduce transistor mismatches far greater than 6.4%. Measurement of 60 p-channel and 60 n-channel OTFTs on one substrate shows $1\text{-}\sigma$ drain-current mismatches of 39% and 23%, respectively [see Fig. 6(a)]. Because of these large variations, the current-steering architecture is at present not suitable for our organic transistor technology.

In a switched-capacitor DAC, because the transistors function as switches, the precision of their currents has little impact on the output. Rather, the critical parameter is the matching between capacitors in the array. Although capacitors also suffer mismatches due to shadow mask processing, their precision is far higher than that of transistor currents because of the capacitor's simple square geometry. Furthermore, because the capacitors are fabricated by intersecting two metal traces, they are immune to x-y mask misalignments. Measurement of 120 capacitors shows $1\text{-}\sigma$ capacitance mismatches of 8.4% for 0.0025-mm² capacitors (17.5 pF), 4.7% for 0.01-mm² capacitors (70 pF) and 1.7% for 0.04-mm² capacitors (280 pF) [see Fig. 6(b)]. From these measurements, we observed that the mismatch distribution follows approximately the well-known area-scaling rule [18]

$$\sigma \approx \frac{k}{\sqrt{\text{Area}}} \quad (5)$$

where k is a process parameter. This result illustrates that our organic thin-film process exhibits a similar characteristic as a typical silicon CMOS process—the mismatch between capacitors can be reduced by increasing their areas.

For a 6-bit switched-capacitor DAC, a requirement of less than 1 LSB INL and 1 LSB DNL, and 95% yield, the maximum mismatch of binary-weighted capacitors can also be calculated using (1)–(4), giving $\sigma_{u\text{-INL}} < 12.7\%$ and $\sigma_{u\text{-DNL}} < 6.4\%$. For a 6.4% mismatch, 0.01-mm² unit capacitors are chosen, with a unit capacitance of 70 pF. However, in a binary-weighted DAC, the largest capacitance is $2^{(B-1)}$ times the unit capacitance, equal to 2240 pF for 6 bits. This large capacitance, together with the relatively high on-resistances of the OTFTs, results in a large DAC settling time and low operating speed. An alternative DAC architecture is thus needed to reduce the capacitance, leading to our calibrated C-2C design. In a C-2C DAC,

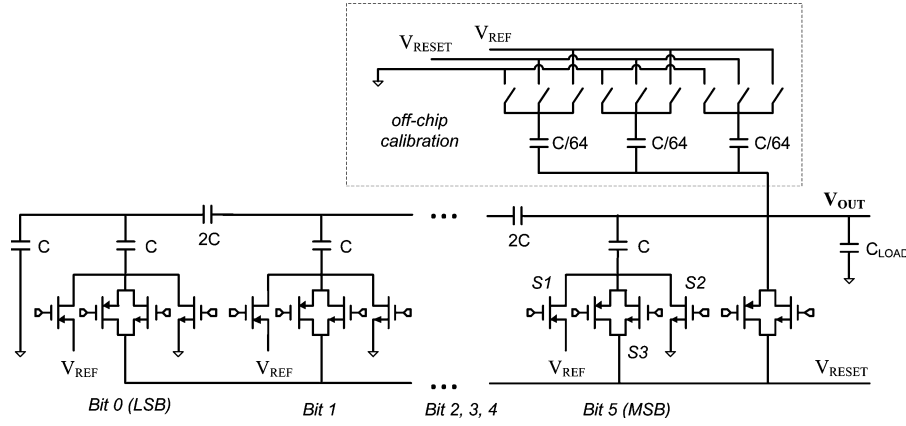


Fig. 7. Circuit schematic of the C-2C DAC; $V_{REF} = 3$ V, $V_{RESET} = 1.5$ V.

at any node in the circuit the largest capacitance is no more than twice that of the unit capacitor and thus significantly reducing the time constants. Furthermore, a 6-bit binary-weighted DAC requires 64 unit capacitors, which is a large sum that is difficult to accomplish with high yield at this nascent stage of process development. A 6-bit C-2C DAC only requires 17 unit capacitors, which is a quantity easier to fabricate with high yield.

In the silicon CMOS process, the C-2C topology typically suffers from parasitic capacitances between the summing nodes and the silicon substrate [19]. But with our organic process, the substrate is insulating glass or plastic and does not contribute to parasitic capacitances. A schematic of our DAC circuit is shown in Fig. 7: S1 and S2 are the pull-up and pull-down switches, respectively; S3 is a complementary switch for sampling a reset voltage V_{RESET} (the need to sample V_{RESET} is described in the following subsection on capacitor leakage). Since the capacitor network is linear, we can apply superposition to calculate the DAC output voltage V_{OUT} to be

$$V_{OUT} = \frac{C_{LOAD}}{C_{OUT} + C_{LOAD}} V_{RESET} + \frac{C_{OUT}}{C_{OUT} + C_{LOAD}} V_{REF} \sum_{i=0}^{B-1} b_i 2^{-(B-i)}. \quad (6)$$

C_{OUT} is the equivalent output capacitance of the DAC, equal to $2C_u$, where C_u is the capacitance of one unit capacitor. C_{LOAD} is the load capacitance at the DAC output, equal to approximately $4C_u$ in our design. B is the number of bits, and b_i is the i th bit, either 1 or 0. V_{REF} equals 3 V, and V_{RESET} equals 1.5 V in our design.

To select the appropriate unit-capacitor size, we calculate the DNL of the C-2C DAC. The DNL at the major transition determines the matching requirement at a given yield. Similar to a binary-weighted DAC, the maximum DNL of the C-2C DAC occurs at midcode transition, i.e., from 011111 to 100000. Detailed analysis shows that the maximum allowed unit-capacitor mismatch can be calculated from the following expressions:

$$\sigma_{DNL}^2 \approx \frac{1}{4} \sigma_{u_DNL}^2 2^{2B} \quad (7)$$

$$\sigma_{DNL} \approx \frac{1}{2} \sigma_{u_DNL} 2^B = \frac{DNL}{\sqrt{2}(\text{erfinv}(Y))} \quad (8)$$

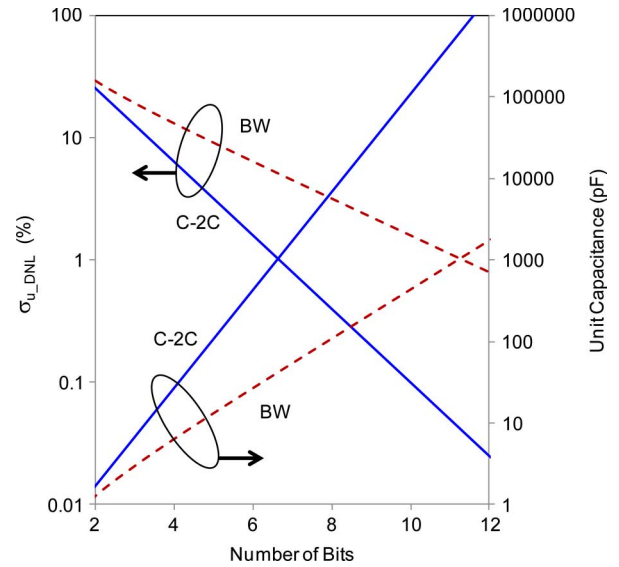


Fig. 8. Comparison of the unit capacitor matching (σ_{u_DNL}) and the corresponding unit capacitance required for C-2C and binary-weighted DACs in our organic process (for DNL = 1, yield = 95%).

where σ_{DNL} is the standard deviation of the DNL at the major transition and σ_{u_DNL} is the standard deviation of the unit-capacitor mismatch. For $B = 6$, $DNL < 1$ LSB and a yield of 95%, $\sigma_{u_DNL} = 1.6\%$, a much more stringent requirement than that for a binary-weighted DAC. This need for better matching in a C-2C DAC is the result of having a lower output capacitance—instead of spreading the DNL over 2^B times the unit capacitance as in a binary-weighted DAC, the C-2C DAC can only spread the DNL over 2 times the unit capacitance. Comparing (4) and (8), a C-2C DAC requires a unit-capacitor matching that is approximately square-root (2^{B-1}) times better than that of the binary-weighted DAC. To achieve 1.6% matching, 0.04-mm^2 unit capacitors are chosen with a unit capacitance of 280 pF. Fig. 8 illustrates the relationships between the number of bits, the unit capacitor matching σ_{u_DNL} , and the unit capacitances for C-2C and binary-weighted DACs. Compared to a binary-weighted DAC, although the unit-capacitor size of a C-2C DAC is larger, the capacitance needing to be switched at the MSB node is significantly smaller: 280 pF for

C-2C versus 2240 pF for binary-weighted (32×70 pF). This reduced switching capacitance results in faster DAC speed. In terms of the total capacitance in the DAC, the C-2C contains 4760 pF, whereas the binary-weighted contains 4410 pF. Thus, the C-2C DAC is only slightly larger in capacitor area than the binary-weighted DAC.

B. Calibration

To correct any realistic deviations from analysis and process parameters, a two-bit calibration circuit is added externally at the output of the C-2C DAC, shown in Fig. 7. The calibration circuit consists of three thermometer-coded elements, each represented by a 4.7-pF capacitor that is approximately 1/64th of the C-2C unit capacitor. Although the calibration is implemented off-chip with discrete CMOS switch arrays and discrete capacitors, the concept can be readily fabricated as a part of the organic DAC: the smallest individual capacitor that can be fabricated in our organic thin-film process is 2.8 pF (limited by the minimum opening in the shadow masks); and thermometer coding guarantees monotonicity despite any large mismatches between the calibration capacitors.

C. Limits on Operational Speed

A common measure of the maximum operational speed of a transistor is the transit frequency f_t , that is, the frequency at which the (extrapolated) transistor current-gain drops to unity. As shown in Figs. 4 and 5, our OTFTs exhibit the quadratic $I_D - V_{DS}$ behavior to a first-order approximation. Thus, the transit frequency can be computed using the following [20]:

$$f_t \cong \frac{g_m}{2\pi C_{gg}} = \frac{\mu}{2\pi L (2L_{\text{overlap}} + \frac{2}{3}L)} (V_{GS} - V_{TH}) \quad (9)$$

$$g_m \cong \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \quad (10)$$

$$C_{gg} \cong 2C_{\text{overlap}} + \frac{2}{3}WLC_{ox} \\ = 2WL_{\text{overlap}}C_{ox} + \frac{2}{3}WLC_{ox}. \quad (11)$$

In an OTFT, f_t is determined by materials properties (mobility μ and threshold voltage V_{TH}) as well as by process parameters (channel length L and gate-source overlap L_{overlap}). In our design, $|V_{GS_max}| = 3$ V, $L = 20$ μm , $L_{\text{overlap}} = 20$ μm , $V_{THP} = -0.5$ V, $V_{THN} = 0.5$ V, $\mu_p = 0.08$ $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, $\mu_n = 0.008$ $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$. These give a maximum f_t of approximately 3 kHz for p-channel transistors and 300 Hz for n-channel transistors. As seen in (9), the operational speed is primarily limited by semiconductor mobility and device feature sizes: channel length and gate overlap length. With improved mobility and further refined fabrication process, recent works have shown μ_p and μ_n in excess of 1 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ [11] and [12] and channel length of 1 μm [1], organic circuits can potentially reach speeds over 1 MHz. Indeed, several groups have already demonstrated ring oscillators with sub-microsecond stage delays [21] and [22].

The maximum speed of our DAC design is determined by the settling time at the output. For a C-2C DAC, the settling at the output node is approximately equal to the settling of the

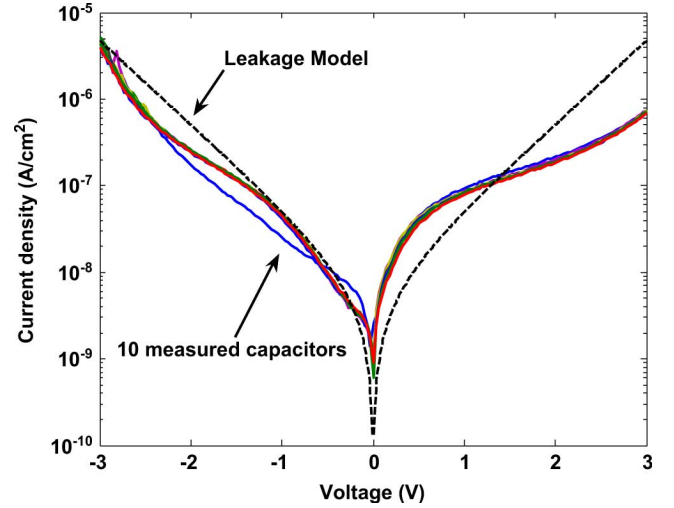


Fig. 9. Comparison of measured leakage current density and the leakage model.

MSB node because any settling errors at lower bits are attenuated by the C-2C network. The time t required to settle to within 1 LSB of a B -bit DAC can be calculated using the following expression:

$$t = B \ln(2) R_{ON} C_{TOTAL} \quad (12)$$

where R_{ON} is the on-resistance of the p-channel or n-channel OTFT switch at MSB (S1 or S2 in Fig. 7) and C_{TOTAL} is the total load capacitance to this OTFT. R_{ON} can be calculated from the following expression:

$$R_{ON} = \frac{1}{\mu C_{ox} (W/L) (V_{GS} - V_{TH})}. \quad (13)$$

With the aforementioned device parameters, to obtain equal R_{ON} , the width of the n-channel OTFT (W_n) needs to be ten times the width of the p-channel OTFT (W_p). As a reasonable compromise that avoids excessively large devices, we use $W_n = 5W_p$ in our design. With $W_p = 200$ μm , $W_n = 1000$ μm , and $V_{GS} = 3$ V, we obtain the approximate on-resistances of 714 k Ω and 1428 k Ω , for the p-channel and n-channel OTFTs, respectively. C_{TOTAL} in (11) equals approximately 620 pF (the sum of $C_U = 280$ pF and all overlap capacitances at the OTFT drain node equals approximately 340 pF). Thus, the maximum operational speed of our 6-bit DAC is $1/(2t) \approx 132$ Hz. (Although the overlap capacitances are substantial, because they are not connected to the charge conservation nodes between the C and 2C capacitors, they do not affect the 1:2 ratio required for the C-2C operation.)

A lower limit on the operational speed is governed by the leakage current through the capacitors. In our organic thin-film process, the leakage current through a capacitor is nonlinearly related to the applied capacitor voltage [23], resulting in input-dependent output errors. The slower the operation and the longer the capacitors lose charge through leakages, the greater the errors. Fig. 9 shows the measured leakage current density as a function of applied voltage on ten capacitors. Although the leakage current density is about 1000 times less than that of 90-nm silicon CMOS [24], because of the low operating

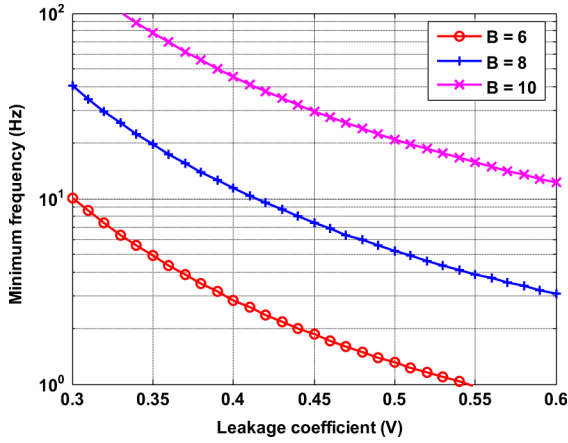


Fig. 10. Minimum DAC frequency required for 1 LSB output error due to capacitor leakage (8-bit and 10-bit are included for comparison).

speed, the accumulated leakage charges can result in substantial errors. To quantify the amount of errors and thus establish a lower bound on the operational speed, we now estimate the change in the DAC output voltage as a function of the leakage current and the DAC clock rate.

Empirical curve-fitting of the measured data in Fig. 9 shows that the leakage current through a unit capacitor is approximately exponential to the applied voltage V_C :

$$I_{\text{LEAK}} \approx I_0 (e^{V_C/a} - 1) \quad (14)$$

where $I_0 = 0.6$ pA and the leakage coefficient $a = 0.45$ V. The leakage charge on a unit capacitor is

$$\Delta Q = I_{\text{LEAK}} \Delta t = C \Delta V. \quad (15)$$

At the DAC output, the error in the output voltage is a weighted function of all capacitor leakages. Calculating the exact worst case value of the error is difficult to obtain analytically. However, we can simplify the analysis by recognizing that the MSB capacitor leakage holds the greatest contribution to the output voltage error, since the C-2C network attenuates the effects of all other capacitor leakages. Therefore, by only considering the MSB capacitor, we arrive at a simple estimate for the minimum frequency f_{\min} of the DAC:

$$f_{\min} = \frac{1}{2\Delta t} = \frac{I_{\text{LEAK}}}{2C\Delta V_{\text{OUT}}} \quad (16)$$

$$f_{\min} = \frac{1}{2C_U} I_0 (e^{V_C/a} - 1) \frac{2^B}{\varepsilon} \quad (17)$$

where ε is the allowed output error due to leakage. Although this result is a simplified estimate, it offers insight into the relationship between the minimum speed limit of the DAC and its dependencies. For $C_U = 280$ pF, $V_C = 1.5$ V and $\varepsilon = 1$ LSB, Fig. 10 plots f_{\min} as a function of the leakage coefficient a . In our empirical leakage model, $a = 0.45$ V; thus the minimum operating frequency of our 6-bit DAC is estimated to be 1.8 Hz. This minimum frequency is small because we designed the dynamic range of the DAC output such that the maximum V_C is 1.5 V. At $V_C = 2.5$ V, the leakage would have been ten times greater, and thus the minimum frequency would be a more detrimental 18 Hz. Further, variations in I_0 or the leakage

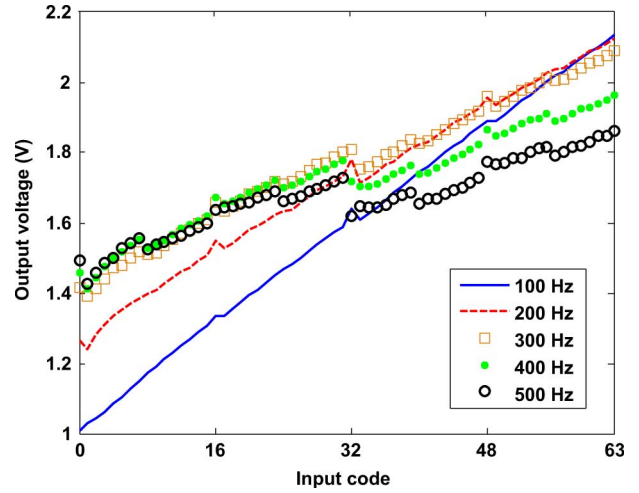


Fig. 11. Measured DAC transfer function (before calibration) becomes increasingly nonlinear as the clock rate increases.

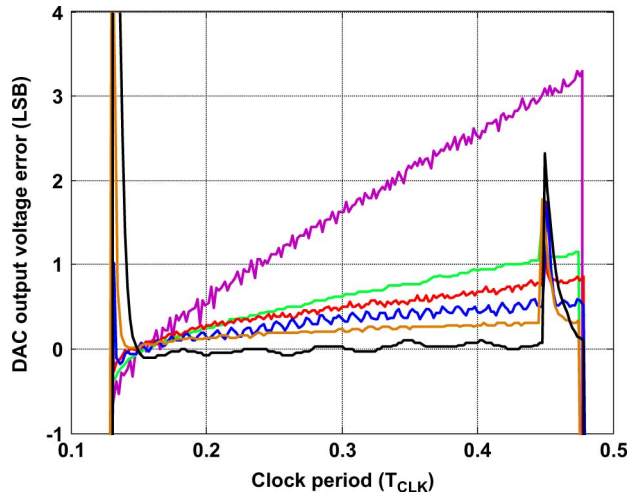


Fig. 12. Measured DAC output voltage error (code 63, before calibration) as a function of clock rate; from top to bottom: 0.1 Hz, 0.5 Hz, 1 Hz, 2 Hz, 5 Hz, and 10 Hz.

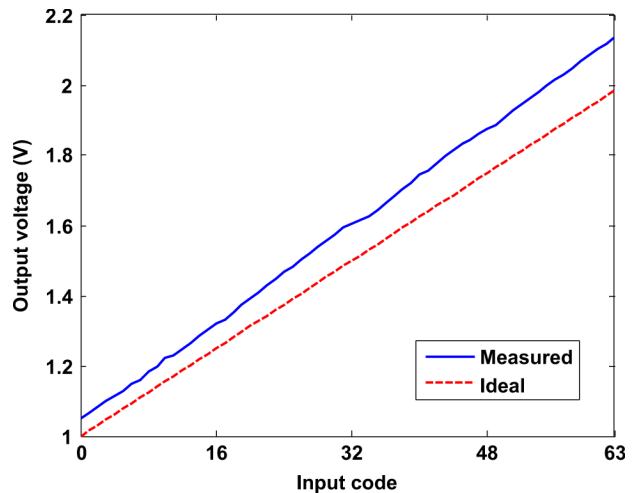


Fig. 13. Ideal and measured (after calibration) DAC transfer functions with 100 Hz clock.

coefficient a (due to temperature or process) can significantly alter this minimum frequency, as shown in Fig. 10. To prevent

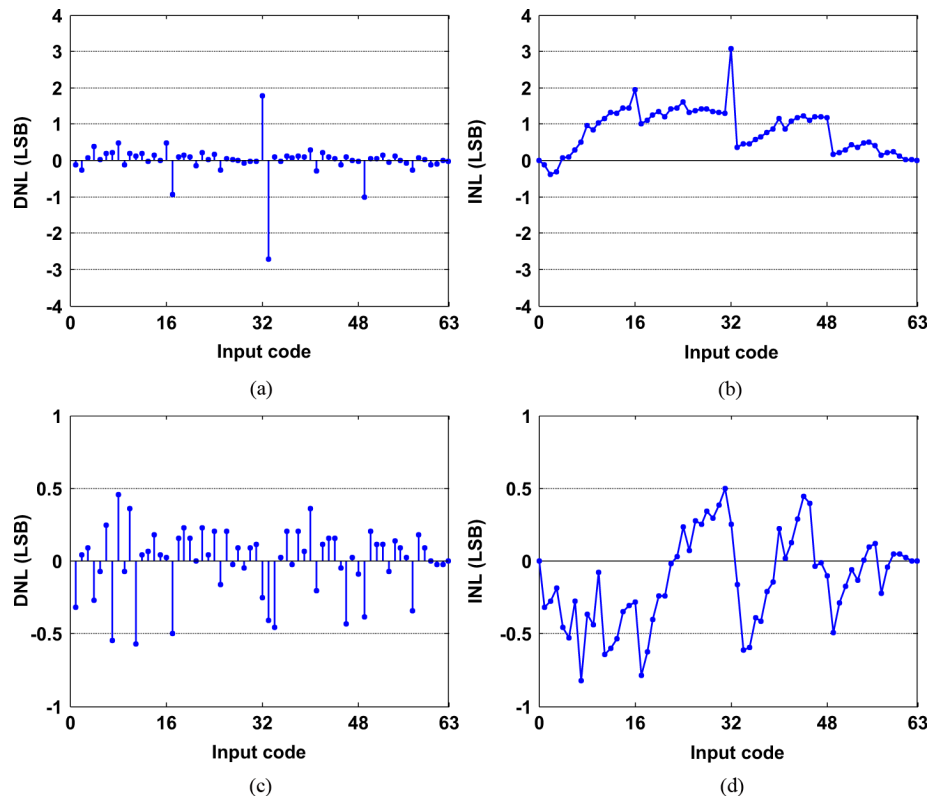


Fig. 14. DAC DNL and INL before calibration [(a) and (b)] and after calibration [(c) and (d)].

leakage errors from accumulating over multiple clock cycles, the DAC recharges all capacitors by sampling V_{RESET} every clock cycle, as shown in Fig. 7.

IV. MEASUREMENT RESULTS

A. Measurement Setup

The DAC is fabricated on a commercial LCD glass substrate. The glass is placed on a probe station for measurement. Two custom-designed multi-probe handlers (MPHs) provide the interface contacts. Wire bonding was attempted but was unsuccessful due to insufficient adhesion between the gold pads and the glass surface. (Subsequent experiment showed that wire bonding was feasible with thicker pads.) The MPHs are connected to the FPGA board via an adapter card. The FPGA provides the digital signals to the DAC. All signals are loaded with appropriate capacitances on the adapter card to reflect realistic OTFT conditions. The DAC output is connected to an oscilloscope. All measurements were performed in ambient air and at room temperature.

B. Mismatches in the Circuit

The DAC contains 12 capacitors: seven 280-pF unit capacitors and five 560-pF capacitors, each formed from two unit capacitors. To increase the sample size, two DACs were measured. (One capacitor was damaged during measurement for a total sample size of 23.) The standard deviation of the unit capacitor mismatches is 3.4%, twice as much as that of the test capacitors. There are two possibilities for the wider distribution: 1) in the actual circuit, the shadow mask openings for capacitors

are more difficult to control due to adjacent circuitry, and 2) the dielectric thickness may vary across the circuit. (For the process utilized in this work, possibility 1 is more likely.) However, the mismatch standard deviation of the 560-pF capacitors is 2.1%, equal to 0.62 of the mismatch standard deviation of the 280-pF capacitors, approximately conforming to the area-scaling rule (square root of $280/560 = 0.707$).

C. Transfer Function, Static and Dynamic Performances

Figs. 11 and 12 illustrate the upper and lower speed limits of the DAC. In Fig. 11, as the clock rate increases above 100 Hz, the measured DAC transfer function becomes increasingly distorted, as predicted by (12) and (13). In Fig. 12, as the clock rate decreases below 10 Hz, the leakage error progressively increases. At 2 Hz, the leakage error is approximately 0.5 LSB, whereas (14)–(17) predicted a 1 LSB error. Fig. 13 shows the measured DAC transfer function after calibration, together with the ideal characteristic described by (6). Compared to the ideal transfer function, the measured transfer function has a 60 mV offset and an 8% gain error. The offset results from calibration; and the gain error results from the imprecise estimation of C_{LOAD} . Fig. 14 shows the static linearity of the DAC, as measured by DNL and INL at a conversion rate of 100 Hz. Before calibration, the maximum DNL and INL are -2.8 LSB and $+3.1$ LSB, respectively. After calibration, the maximum DNL and INL are -0.6 LSB and -0.8 LSB, respectively. Fig. 15 shows the spectrum of two output sinusoids at 10 Hz and 45 Hz, synthesized at the conversion rate of 100 Hz. The harmonic spurs of the sinusoids are clearly visible. For the 10-Hz output,

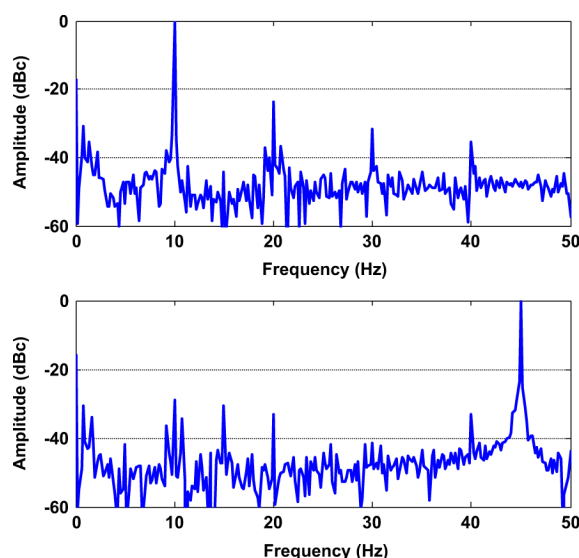


Fig. 15. DAC output spectrum for 10 Hz and 45 Hz sinusoids (500-point FFT).

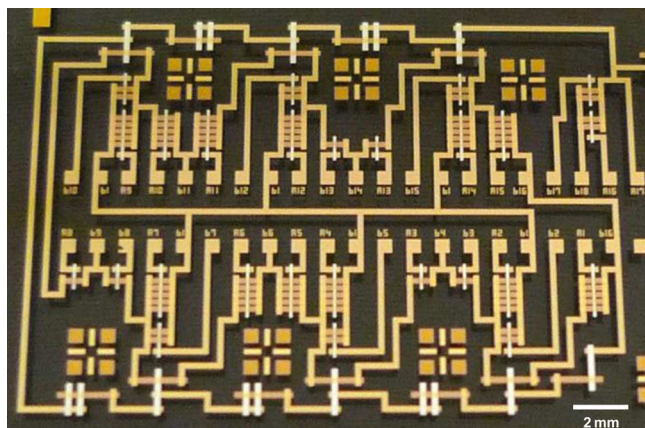


Fig. 16. Photograph of the DAC on glass substrate.

the highest spur is at -24 dBc. For the 45-Hz output, the highest spur is at -29 dBc. For sinusoids between 1 Hz to 49 Hz, the worst case occurs at 10 Hz. Thus, the minimum spurious-free dynamic range (SFDR) of the DAC is 24 dB.

A photograph of the DAC is shown in Fig. 16. The circuit contains 13 p-channel OTFTs, 13 n-channel OTFTs, and 17 unit capacitors. The total area of the DAC is $28 \text{ mm} \times 14 \text{ mm}$.

V. CONCLUSION

A 3-V, 6-bit DAC was implemented using p-channel and n-channel organic thin-film transistors on glass. The circuit was fabricated at low temperature in a process that is compatible with plastic substrates. The large undesirable drain-current variations of the organic transistors led to the switched-capacitor architecture, where precision depended on the superior matching of capacitors. By appropriately scaling capacitor sizes to reduce mismatch and applying calibration, the DAC achieved a DNL/INL of $-0.6/-0.8$ LSB, respectively, at a conversion rate of 100 Hz.

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