A 3.3 V 6-Bit 100 kS/s Current-Steering Digital-to-Analog Converter Using Organic P-Type Thin-Film Transistors on Glass

Tarek Zaki, *Student Member, IEEE*, Frederik Ante, Ute Zschieschang, Joerg Butschke, Florian Letzkus, Harald Richter, Hagen Klauk, *Member, IEEE*, and Joachim N. Burghartz, *Fellow, IEEE*

***Abstract*—A 3.3 V 6-bit binary-weighted current-steering digital-to-converter converter (DAC) using low-voltage organic p-type thin-film transistors (OTFTs) is presented. The converter marks records in speed and compactness owing to an OTFT fabrication process that is based on high-resolution silicon stencil masks. The chip has been fabricated on a glass substrate and consumes an area of 2.6×4.6 mm^2. The converter has a maximum update rate of 100 kS/s and a maximum output voltage swing of 2 V. The measured DNL and INL at an update rate of 1 kS/s are -0.69 and 1.16 LSB, respectively. A spurious-free dynamic range (SFDR) of 32 dB has been measured for output sinusoids at 31 Hz (update rate of 1 kS/s) and 3.1 kHz (update rate of 100 kS/s).**

***Index Terms*—Current-steering, digital-to-analog converter (DAC), organic integrated circuits, organic thin-film transistors (OTFTs), stencil masks.**

I. Introduction

INTEGRATED circuits based on organic thin-film transistors (OTFTs) have recently shown a rapid progressive development towards higher level of integration and better performance. In contrast to inorganic transistors, OTFTs have been promising on account of their low cost, low temperature, fast manufacturability, and especially their compatibility with mechanically flexible and lightweight polymeric substrates [1]. Accordingly, OTFTs offer prospects in realizing large-area, bendable, and rollable applications such as electronic papers and panel displays [2]. In addition, the low-voltage operation competence of recent OTFTs opens the possibility to integrate hybrid solutions combining large-area organic electronics with high-performance thin silicon chips [3] and also makes them well-suited for battery-powered or frequency-coupled portable devices, such as radio frequency identification (RFID) tags [4]. Finally, OTFTs are also exploited in chemical and biological sensors owing to the chemical interactivity of the organic semiconductors with numerous solvent vapors [5]. In all such applications, data conversion to interface digital processors with the analog world is an essential necessity.

Work on digital-to-analog converters (DACs) [6], analog-to-digital converters (ADCs) [7], [8], and digital processors [9] based on organic transistors have been recently introduced. Hereby, the first demonstration of an organic-based 6-bit current-steering DAC is reported [10]. In the current-steering topology, device matching is essential to meet a certain intrinsic accuracy and to minimize nonlinearity errors. Since OTFT fabrication processes have been prone to large device-to-device variations, the early approach to OTFT DACs used the switched-capacitor architecture, which is less sensitive to transistor mismatching [6]. By comparing the two approaches, the presented current-steering DAC offers a dramatic performance boost (1000 times faster) and greatly reduced area consumption (30 times smaller). These considerable improvements are attributed to a new OTFT fabrication process based on high-resolution silicon stencil masks that provide submicrometer channel length capability and excellent transistor matching [11], thus making it possible to exploit the fast and compact current-steering topology.

The OTFT fabrication technology using silicon stencil masks is briefly described in Section II. For reliable computer-aided simulations of the designed DAC, an accurate OTFT dc model that combines the concepts of enhanced carrier mobility at higher gate overdrive voltage and the field-dependent contact resistances has been implemented. The model is presented and validated in Section III. The complete design and floorplan of the DAC are introduced in detail in Section IV. Note that the design of the DAC includes a unique highly linear current-to-voltage converter, which employs only two p-type OTFTs. In Section V, the measurement setup and results are summarized. Finally, conclusions follow in Section VI.

II. Stencil-Mask-Based OTFT Technology

Using high-resolution silicon stencil (shadow) masks and a low-temperature ($\sim 90\,^{\circ}$C) fabrication process, low-voltage top-contact OTFTs have been fabricated [11]. The transistors employ the inverted staggered (bottom-gate, top-contact) device structure as they provide better injection efficiency compared with their staggered (top-gate, bottom-contact) contenders [12]. Thus, the use of shadow masks offers a virtue in patterning the source/drain contacts on the top of small-molecule organic semiconductors without the need of solvents or elevated temperatures. Fig. 1 shows a scanning electron microscope (SEM) image depicting the detail of a silicon stencil mask [Fig. 1(a)],

Manuscript received May 01, 2011; revised July 05, 2011; accepted September 05, 2011. Date of current version December 23, 2011. This paper was recommended by Guest Editor Satoshi Shigematsu.

T. Zaki and J. N. Burghartz are with the Institute for Microelectronics Stuttgart (IMS CHIPS), 70569 Stuttgart, Germany, and also with the University of Stuttgart, 70569 Stuttgart, Germany (e-mail: zaki@ims-chips.de).

F. Ante, U. Zschieschang, and H. Klauk are with the Max Planck Institute for Solid State Research, 70569 Stuttgart, Germany.

J. Butschke, F. Letzkus, and H. Richter are with the Institute for Microelectronics Stuttgart (IMS CHIPS), 70569 Stuttgart, Germany.

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Digital Object Identifier 10.1109/JSSC.2011.2170639

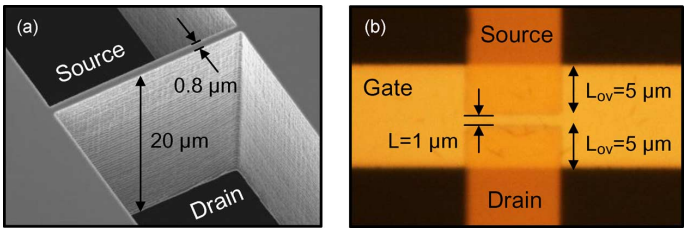

Fig. 1. (a) SEM image of a high-resolution silicon stencil mask by which the source and drain contacts of an OTFT are patterned. (b) Photograph of a top-contact OTFT fabricated on a glass substrate.

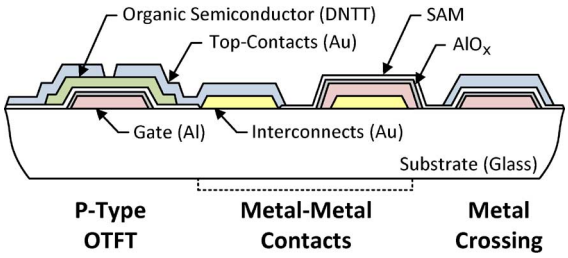

Fig. 2. Cross-sectional view of a p-type OTFT, metal–metal contacts and metal crossing. The materials are designated.

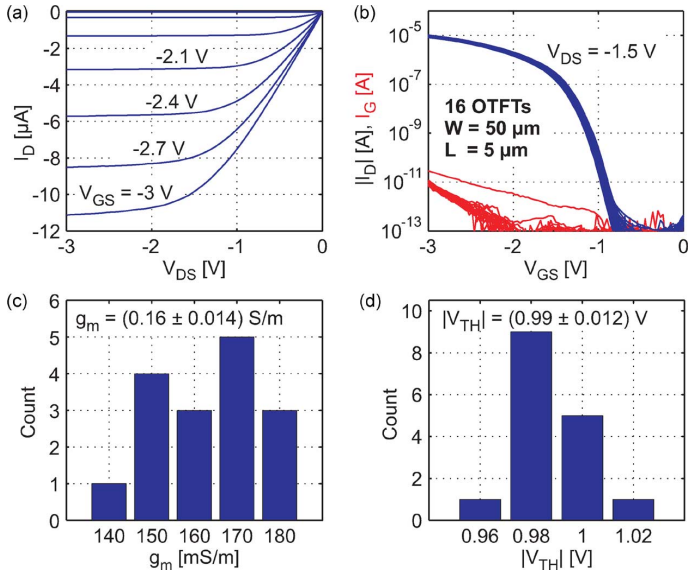

Fig. 3. Measured electrical characteristics of 16 p-type OTFTs: (a) output characteristics of one of the OTFTs, (b) transfer characteristics and gate leakage currents, (c) transconductances, and (d) threshold voltages.

by which the source–drain contacts of OTFTs with a channel length of 0.8 μm are patterned, and the micrograph of a top-contact OTFT fabricated on a glass substrate [Fig. 1(b)]. It is worth noting that the process is compatible with mechanically flexible plastic substrates [13]. Fig. 1(a) and (b) shows the sharp edges of both the silicon stencil as well as the source/drain contacts on the substrate (the edge roughness is below 50 nm, [14]), which lead to an excellent transistor matching that allows the implementation of circuit topologies that would not be feasible otherwise (e.g., current-steering topology).

A. Fabrication Process

The high-resolution silicon stencil masks were fabricated on silicon-on-insulator (SOI) wafers, where the buried SiO_2 layer serves as an etch stop during the manufacturing process. The apertures in the silicon stencil mask, through which the OTFT layers were evaporated and patterned, were defined by electron-beam lithography in combination with dry etching from the wafer front side [15], [16]. After back-side etching, a 20-μm -thick silicon membrane with an area of, but not limited to, 20×20 mm^2 remains anchored to a robust 5-mm-wide wafer frame. The OTFT process used here requires a total of only four masks that were simultaneously fabricated on one 150-mm wafer.

Referring to Fig. 2, an alkali-free glass coated with a thin adhesion layer of 4-nm-thick aluminum oxide formed by atomic layer deposition was utilized as the substrate. Initially, 30-nm-thick interconnect traces consisting of thermally evaporated gold were patterned by the first stencil mask. Subsequently, the OTFT layers were formed by vacuum deposition and patterned by using the remaining three stencil masks, including 30-nm-thick aluminum for the gate electrode, 30-nm-thick dinaphtho-thieno-thiophene (DNTT) for the p-type organic semiconductor, and 30-nm-thick gold for the source/drain contacts. Prior to the organic semiconductor deposition, a 5.3-nm-thick hybrid dielectric that consists of an oxygen-plasma-grown AlO_x layer (3.6-nm-thick) and a solution-processed self-assembled monolayer (SAM) of n-tetradecylphosphonic acid (1.7-nm-thick [13]) was formed. This hybrid dielectric with a capacitance of 800 nFcm^{-2} serves as the gate dielectric, enabling low-voltage operation for the integrated circuits at a supply voltage of about 3 V. However, it also serves as the interconnect insulator that causes significant metal–metal parasitic capacitances at interconnect crossings.

B. Electrical Characterization

The electrical characteristics of 16 p-type OTFTs with a channel length of 5 μm manufactured on the same substrate are shown in Fig. 3. The drain current in the output characteristics shows a linear increase for small drain–source voltages and good current saturation for large drain–source voltages. The transistors show excellent matching with an average transconductance of (0.16 ± 0.01) Sm^{-1} and an average threshold voltage (defined as the gate-source voltage for which $I_D = 100$ pA) of (-0.99 ± 0.01) V. The threshold voltage variation is less than one percent with respect to the maximum supply voltage of 3 V. From the transfer characteristics a hole mobility of ~ 0.6 cm^{2}V^{-1}s^{-1}, a subthreshold slope of 90 mV/decade, and an on/off current ratio of more than 10^8 are extracted.

In contrast to the polyimide shadow mask technology, which provides a minimum of 20 μm for both the channel length and the gate-overlap [6], the high-resolution silicon stencil mask technology allows minimum channel length and gate-overlap down to 0.8 and 2 μm, respectively [11]. Accordingly, a dramatic improvement of the transistor's dynamic performance is observed. The maximum operational speed of the p-type transistor, which is commonly measured by the transit frequency f_t, is improved from 3 kHz to 5.3 MHz; f_t is given as [6]

$$f_t \cong \frac{g_m}{2\pi C_{gg}} = \frac{\mu}{2\pi L\left(2L_{ov} + \frac{2}{3}L\right)}(V_{\mathrm{GS}} - V_{\mathrm{TH}}) \quad (1)$$

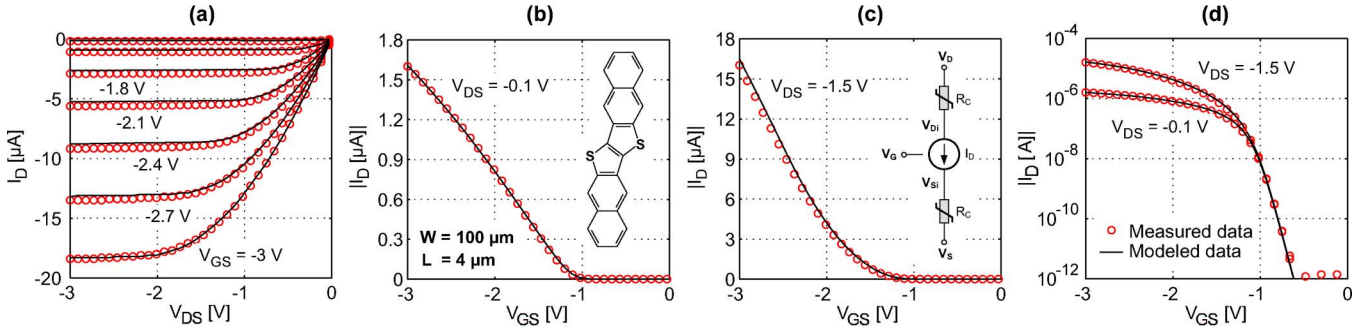

Fig. 4. Measured versus modeled I–V characteristics for a p-type OTFT (100 μm/4 μm): (a) output characteristics, (b) linear transfer characteristics, (c) saturation transfer characteristics, and (d) subthreshold region. The insets show the molecular structure of the p-type organic semiconductor (DNTT) and the OTFT dc model schematic.

$$g_m \cong \mu C_i \frac{W}{L}(V_{\rm GS} - V_{\rm TH}) \tag{2}$$

$$C_{gg} \cong 2WL_{ov}C_i + \frac{2}{3}WLC_i \tag{3}$$

where W is the channel width, L is the channel length, L_{ov} is the gate-overlap, μ is the carrier mobility, C_i is the gate capacitance per unit area, $V_{\rm TH}$ is the threshold voltage, and $V_{\rm GS}$ is the gate–source voltage. In this case, $L = 0.8$ μm, $L_{ov} = 2$ μm, $V_{\rm GS} = 3$ V, $V_{\rm TH} = 0.99$ V, and $\mu = 0.6\,{\rm cm^2V^{-1}s^{-1}}$, thus $f_t = 5.3$ MHz. However, one should note that a minimum channel length of $L_{\rm min} = 4$ μm ($f_t = 112$ kHz) has been utilized in the converter circuit to ensure proper device matching.

III. OTFT DC Model

The design and optimization of the DAC circuit relied heavily on simulations where an accurate OTFT model was highly desired. An adopted metal–oxide–semiconductor (MOS) model has been used for a long time for the TFT devices [17]. However, this simplified model lacks the main common point observed in the behavior of all OTFTs, i.e., charge carrier mobility enhancement at higher gate overdrive voltage [18]. Consequently, the model for the current–voltage characteristics of the OTFTs used here is based on a recently published OTFT compact dc model [19], which includes the aforementioned mobility behavior; $\mu \propto (V_G - V_{\rm TH})^{\gamma}$, where γ is defined as the mobility enhancement factor ($\gamma > 0$). The validity of the model for the technology presented is justified herein.

The OTFT drain current I_D is given by the following expression [19]:

$$I_D = \mu C_i \cdot \frac{W}{L} \cdot \frac{[V_E(V_{Si})]^{(\gamma+2)} - [V_E(V_{Di})]^{(\gamma+2)}}{\gamma+2} \tag{4}$$

$$V_E(V) = V_{\rm SS} ln\left[1 + exp\left(\frac{V_G - V_{\rm TH} - V}{V_{\rm SS}}\right)\right] \cong \begin{cases} V_{\rm SS} exp\left(\frac{V_G - V_{\rm TH} - V}{V_{\rm SS}}\right), \\ \quad \text{for subthreshold regime;} \\ \quad (V_G - V_{TH} - V) < -V_{\rm SS} \\ (V_G - V_{\rm TH} - V) \\ \quad \text{for above-threshold regime;} \\ \quad (V_G - V_{\rm TH} - V) > V_{\rm SS} \end{cases} \tag{5}$$

where $V_{\rm SS}$ is defined as the subthreshold slope voltage, which is related to the slope in the semi-logarithmic OTFT transfer characteristic [see Fig. 4(d)]. Note that the subscript i is indicated for the internal source–drain potentials present after the contact resistances [see Fig. 4(c)]. Moreover, to include the channel-length modulation effect, the channel length L can be replaced by the following:

$$L\left(1 - \frac{\Delta L}{L}\right) \cong \frac{L}{1 + \lambda|V_{Di} - V_{Si}|} \tag{6}$$

where λ is the channel-length modulation coefficient.

TABLE I
Extracted Model Parameters for a P-Type OTFT

Parameter	Notation	Value
Channel Length	L	$4\,\mu m$
Channel Width	W	$100\,\mu m$
Gate-overlap	L_{ov}	$20\,\mu m$
Carrier Mobility	μ	$0.6\,cm^2/Vs$
Gate Capacitance per Unit Area	C_i	$800\,nF/cm^2$
Threshold Voltage	V_{TH}	$-0.99\,V$
Mobility Enhancement Factor	γ	0.3
Sub-threshold Slope Voltage	V_{SS}	$0.09\,V$
Channel Length Modulation Coefficient	λ	-0.0134

The equations above are valid for all operating regimes of n-type OTFTs, namely linear and saturation above threshold regimes, subthreshold regime, and reverse-biased regime; for p-type OTFTs the polarities of currents and voltages are inverted.

The model parameters, excluding the contact resistances, have been extracted according to the methods proposed in [20]. Since the compact dc model presented in [19] does not take into account the field dependence in the contact resistances, they were extracted from the total series resistance at different gate voltages as a function of the channel length [21] and accordingly modeled. The total series resistance is given by $R_t = 2R_c + R_{\rm ch}$, where R_c is the contact resistance and $R_{\rm ch}$ is the channel resistance, thus $R_c(V_{\rm GS})$ is extracted from the y-intercept of the R_t-versus-L plot at $L = 0$.

The model has been implemented in a SPICE simulator. Fig. 4 depicts the measured versus simulated data for the current-voltage output and transfer characteristics of a p-type OTFT with a channel length of 4 μm and a channel width of 100 μm. The corresponding extracted parameter set is summarized in Table I. The accurate agreement of the simulated to the measured data justifies the reliability of the model needed to carry out more complex simulations for the DAC circuit.

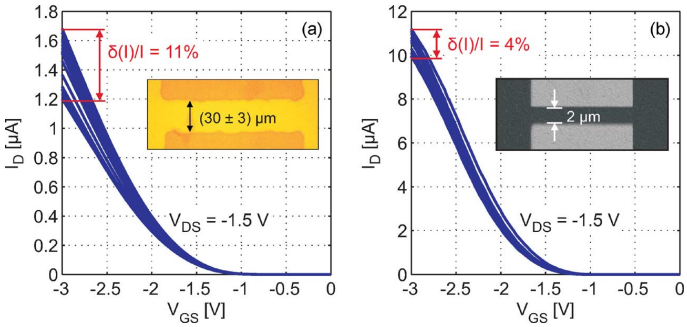

Fig. 5. Comparison between the measured saturation transfer characteristics of 16 identical p-type OTFTs fabricated by two different technologies: (a) conventional polyimide shadow masks and (b) high-resolution silicon stencil masks. The insets show the dimensions and edge features of both technologies, exhibiting noticeable edge roughness in case (a) and very smooth edges in case (b).

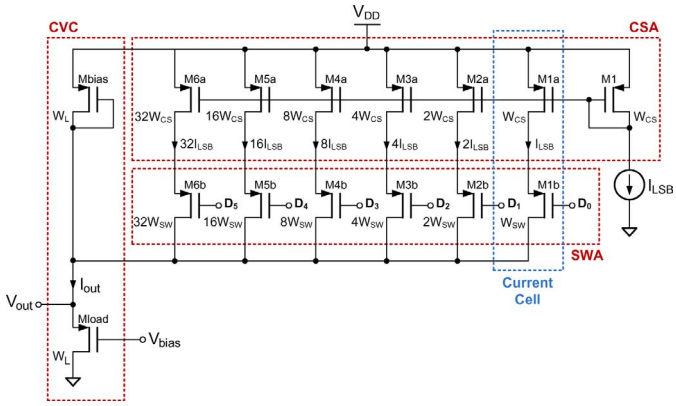

Fig. 6. Schematic diagram of the 6-bit binary-weighted current-steering DAC. The schematic is composed of a CSA with $(W/L)_{\rm CS} = 100\ \mu{\rm m}/15\ \mu{\rm m}$, an SWA with $(W/L)_{\rm SW} = 40\ \mu{\rm m}/4\ \mu{\rm m}$, and a CVC with $(W/L)_L = 100\ \mu{\rm m}/5\ \mu{\rm m}$.

IV. DAC Circuit

A. Converter Architecture

Depending on the electrical reference quantity, DACs are classified into three main classes, namely resistive, capacitive, and current-steering architectures. By comparing the three classes, the current-steering architecture is known to be superior in speed and compactness. However, excellent device matching in this architecture is an essential necessity for the DAC linearity; the matching requirements are evaluated for an N-bit binary-weighted current-steering DAC by the following [6], [22]:

$$\sigma_{\rm INL} = \frac{\rm INL}{\sqrt{2}\,(erfinv(Y))} = \frac{\sqrt{2^N}}{2} \cdot \frac{\sigma_I}{I} \tag{7}$$

$$\sigma_{\rm DNL} = \frac{\rm DNL}{\sqrt{2}\,(erfinv(Y))} = \sqrt{2^N - 1} \cdot \frac{\sigma_I}{I} \tag{8}$$

where INL is the integral nonlinearity, DNL is the differential nonlinearity, and σ_I/I is the current relative standard deviation (transistor's current mismatch). Thus, for $N = 6$-bit, INL $\leq$ 1 LSB, DNL $\leq$ 1 LSB, and $Y = 0.95$, which corresponds to a confidence interval of 2-σ, the required current mismatch should be $\sigma_I/I \leq 6.4\%$ which is the minimum value resulting from (7) and (8).

Fig. 5 depicts a comparison between the conventional polyimide shadow mask and the high-resolution silicon stencil mask OTFT technologies [11], [13]. The figure shows that the 16 OTFTs fabricated by the polymide shadow masks with a channel length of 30 μm have $\sigma_I/I = 11\%$, which exceeds already the upper limit calculated above, and the 16 OTFTs fabricated by the silicon stencil masks with a channel length of only 2 μm have $\sigma_I/I = 4\%$. Because of the large device-to-device variations resulting from the older OTFT fabrication processes, the first approach to realize an organic-based DAC used the capacitive (switched-capacitor C-2C) architecture which is less sensitive to the poor transistor matching; nevertheless, featuring the following limitations [6]: 1) a reset phase is needed every conversion clock cycle to prevent accumulating leakage errors which were expected to be up to 0.6 LSB at 100 Hz; 2) the leakage error constricts the lower speed limit of the DAC to be around 10 Hz; and 3) the use of n-type OTFTs, that feature low carrier mobility of 0.005 cm^2/Vs limits the maximum update rate to 100 Hz and results in a relatively large DAC area of 28×14 mm^2. On the other hand, the comparison showed that the silicon stencil masks provide much improved transistor matching even for smaller device geometries, thus allowing the realization of the current-steering architecture at considerably higher sampling rate and smaller chip-area consumption.

The schematic diagram of the 6-bit current-steering DAC is shown in Fig. 6. The binary-weighted current-steering architecture is employed because of its lower complexity, smaller area consumption, and lower power dissipation since no decoding logic is necessary compared with its unary current-steering counterpart. The converter consists of three main blocks; a current-source array (CSA) that contains the binary-weighted current sources and an input current mirror, a switch array (SWA) that contains the binary-weighted analog switches, and a current-to-voltage converter (CVC) at the output. Note that, for current source $\rm M_i$, 2^{i-1} identical parallel transistors are used to provide $2^{i-1}I_{\rm LSB}$, where $I_{\rm LSB}$ is the least significant bit current. This similarly applies for all of the binary-weighted analog switches; this results in a total of 129 transistors. Finally, the converter is designed with only p-type OTFTs because of their faster operational speed and smaller area, this is mainly owed to the considerably higher carrier mobility in the p-type channel regions $(\mu_p \geq 10\mu_n)$ and thus proportionally larger drive current.

B. Current Cell

The current cell comprises a current-source transistor and an analog switch; see Fig. 6. The dimensions of the current-source transistor typically depend on the technology with which the chip will be fabricated [23]. As mentioned above, the LSB current mismatch should be $\sigma_I/I \leq 6.4\%$ for proper DAC linearity. Therefore, a sufficiently large current-source transistor with a channel length of 15 μm and a channel width of 100 μm has been utilized to guarantee even better matching than the value displayed in Fig. 5(b).

As long as the voltage swing at the drain nodes of the current-source transistors is reduced during switching, the considerable capacitance of the current sources will not be charged

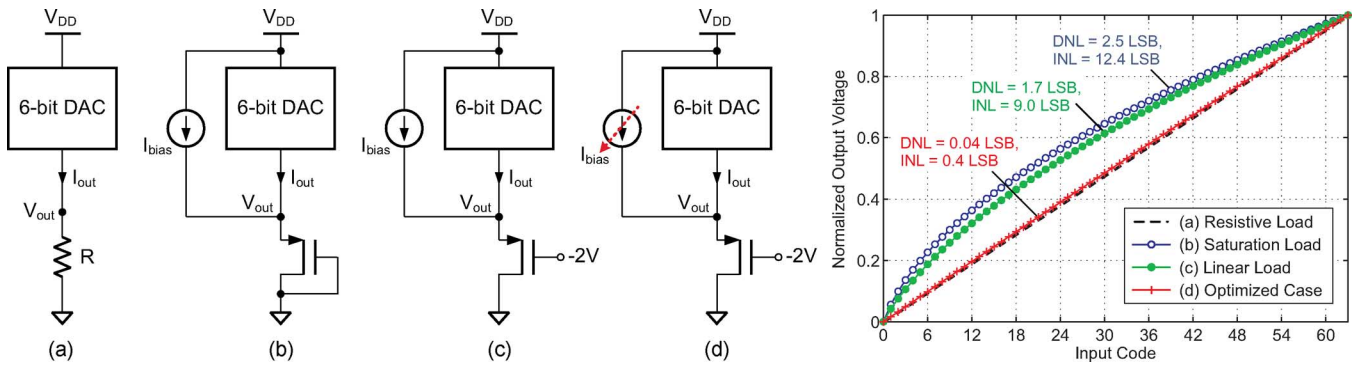

Fig. 7. Schematic and simulation results for different CVC designs: (a) ideal passive resistive load, (b) saturation diode-connected load, (c) linearly operating load, and (d) proposed optimized design with a linearly operating load and a variable biasing current source.

and discharged, thus the dynamic performance will not be degraded. This would have been achieved by using differential analog switches with reduced cross-point voltage at their control signals [24]. By doing so, the interconnect crossings, featuring very high parasitic capacitances (800 nFcm^{-2}) and degrading the circuit performance, would have been indispensable. Therefore, single-ended analog switches have been used mainly to avoid interconnect crossings and also to minimize chip area. In addition, the analog switches were designed to be operating in the saturation mode during the full output voltage swing. This approach avoids the use of cascode current sources, which require larger chip area and limit the output swing, while maintaining the shielding effect of the cascode structure by isolating the drain nodes of the current source transistors from the variant output node. Additionally, the nonlinearities of the output current–voltage characteristics of the OTFTs at low drain bias due to the non-ohmic contacts can be avoided.

The above operating conditions put a constraint on the switch input ON voltages $(V_{\mathrm{sw,on}})$ to keep both the current source and analog switch transistors in the saturation mode. For proper circuit operation and in close agreement with simulations, the analog switch transistors are designed with a channel length of 4 μm and a channel width of 40 μm, and the switch input ON voltage is set to be 1 V.

C. Current-to-Voltage Converter

The linearity of the CVC is essential as it directly affects the DAC static performance. An ideal CVC would have been implemented by using a passive resistor element; however, resistors are so far difficult to be realized in the organic technology. For this reason, an OTFT-based transimpedance circuit has been realized.

As shown in the schematic diagram (Fig. 6), the CVC consists of only two p-type transistors (100 μm/5 μm); one transistor is biased in the linear regime with a gate voltage of $V_{bias} = -2$ V, while the other transistor is diode-connected to serve as a variable current source. This design followed series of comparison steps which are elucidated by the simulations shown in Fig. 7. The ideal case with the passive resistor element [Fig. 7(a)] experiences very low linearity error, taking into account that device mismatch is not considered in the simulations. The second case [Fig. 7(b)] involves a p-type load transistor that is diode-connected, thus operating in the saturation mode. In this case, the CVC relation is controlled by the OTFT saturation equation

$$I_{\mathrm{D,sat}} = -\mu C_i \frac{W}{L} \frac{(-V_{\mathrm{GS}} + V_{\mathrm{TH}})^{(\gamma+2)}}{\gamma+2} \tag{9}$$

$$V_{\mathrm{out}} = \left((\gamma+2) \cdot \frac{I_{\mathrm{out}}}{\mu C_i (W/L)}\right)^{\frac{1}{\gamma+2}} - V_{\mathrm{TH}} \tag{10}$$

This nonlinear relation directly reflects the high output linearity error obtained by the simulation. In the third case [Fig. 7(c)], a linearly operating p-type load transistor is used. The gate bias voltage (-2 V) is set in a way to ensure that the gate-source voltage will not exceed the breakdown voltage ($\sim$6 V) during the complete output swing. Owing to the field-dependence in the OTFT contact resistance $(R_c(V_{\mathrm{GS}}))$, which decreases as the gate–source voltage increases, the DAC linearity is perturbed. Therefore, it is proposed in the fourth case [Fig. 7(d)] to use a variable current source, which decreases at higher DAC output voltage, to compensate for the nonlinearity of the load. Consequently, the DAC linearity is optimized. Using a diode-connected OTFT, as shown previously in the schematic (Fig. 6), the variable current source is realized. In this case, the gate-source voltage of the diode-connected OTFT, operating in the saturation mode for $V_{\mathrm{GS}} = V_{\mathrm{DS}}$, is expressed as $V_{\mathrm{GS}} = V_{\mathrm{out}} - V_{\mathrm{DD}}$. Therefore, the absolute value of the saturation current $I_{\mathrm{D,sat}}$ passing through the transistor given in (9) decreases as the DAC output voltage V_{out} increases.

D. Layout and Floorplan

Device matching and data interference have a strong impact on the DAC performance. Consequently, strict requirements apply to the design of the DAC layout and floorplan due to the relatively large number of transistors employed, especially for an organic-based analog circuit. Fig. 8 shows two possible approaches for the floorplan, namely merged SWA-CSA and separated SWA-CSA [23]. In the merged SWA-CSA, each unit cell comprises both the current source and the analog switch transistors. This approach has a simplified layout; however, it increases the distances between the current source transistors and so the layout will be potentially more susceptible to the systematical gradient effects. As for the separated SWA-CSA, the identical transistors are placed in separate arrays, thus

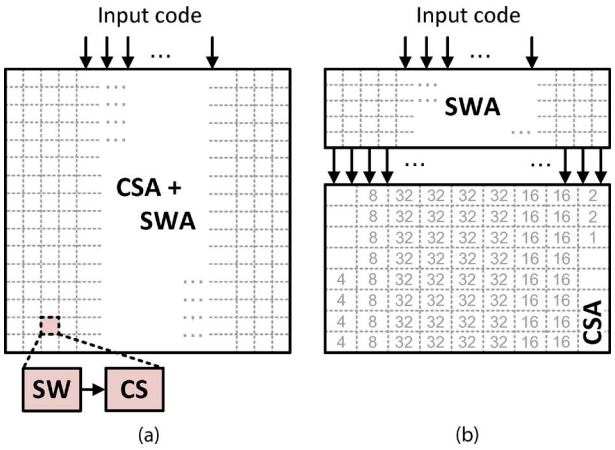

Fig. 8. DAC floorplans: (a) merged SWA-CSA and (b) separated SWA-CSA.

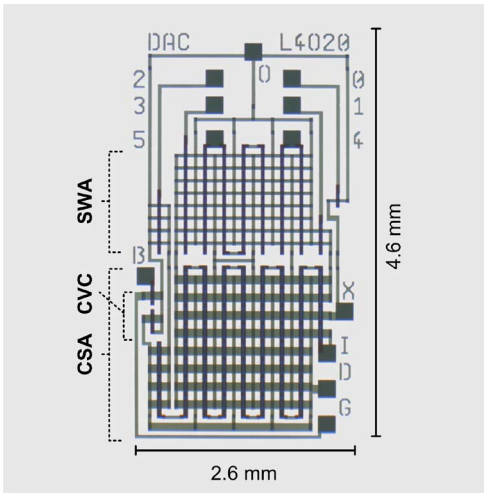

Fig. 9. Photograph of the 6-bit current-steering DAC fabricated on a glass substrate.

ensuring better device matching, easing power routing, and minimizing signal interference due to the division of the digital and the analog parts. In spite of the increased layout complexity in the latter approach [Fig. 8(b)], it has been used here as it offers a substantially better conversion performance. Furthermore, the transistors are placed in a matrix-like orientation in each array to keep the identical transistors in closer proximity. This makes it possible to exploit the excellent feature size control enabled by the stencil mask technology regardless of the non-uniformity introduced by material deposition through evaporation. Fig. 8(b) shows clearly the arrangement of the transistors in the CSA by designating the binary-weights. In this way, the complexity of the routing matrix between the SWA and the CSA is minimized. With this careful layout and floorplan design, no interconnect crossings that feature high parasitic capacitances have been comprised.

Using the OTFT process technology presented in Section II, the DAC has been fabricated on a glass substrate. The die photograph of the realized design is shown in Fig. 9. The total area of the DAC including the contact pads is only 2.6×4.6 mm^2.

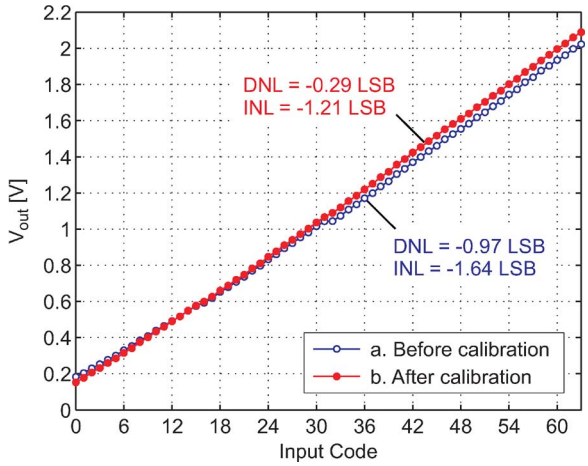

Fig. 10. Measured DAC dc transfer characteristics: (a) before calibration and (b) after calibration.

E. Calibration

After the chip has been fabricated, multiple DACs have been measured and a noticeable non-linearity error is observed in the transfer characteristics only during the transition of the input bit stream from "011111" to "100000." Therefore, the DAC is calibrated by tuning manually the switch input ON voltage for the most significant bit (MSB) to be 0 V instead of 1 V. By doing so, a slightly larger current for the MSB is enabled to the output, hence the DAC linearity is optimized. The calibration method used here has a lower complexity compared to [6] where a 2-bit off-chip calibration circuit has been employed.

V. Measurement Results

A. Measurement Setup

The chip has been measured in a manual probe station with a careful connection between the probeheads and the 55-nm-thick gold pads. The 6-bit digital input stream has been provided by a data generator, while the remaining four inputs $(V_{\mathrm{DD}}, V_{\mathrm{GND}}, V_{\mathrm{bias}}, I_{\mathrm{LSB}})$ have been supplied by a source measure unit (SMU). During dc analyses, the output data were captured by the SMU. In transient analyses the frequency with which the input bit stream is applied to the DAC is adjusted in the data generator, and the DAC output was connected to an oscilloscope. All measurements were performed in ambient air, at room temperature, and at relatively dimmed light environment.

B. Static and Dynamic Performances

Fig. 10 shows the measured DAC dc transfer function before and after calibration and the corresponding static linearity evaluated by the DNL and INL. Before calibration, an undesired abrupt step at the digital input code "32" was observed, resulting in a degraded static linearity; maximum DNL and INL were -0.97 and -1.64 LSB, respectively. However, after calibration, the transfer function shows a monotonic behavior, where the maximum output voltage swing is 1.94 V with a power dissipation of 260 μW and an improved static linearity is obtained;

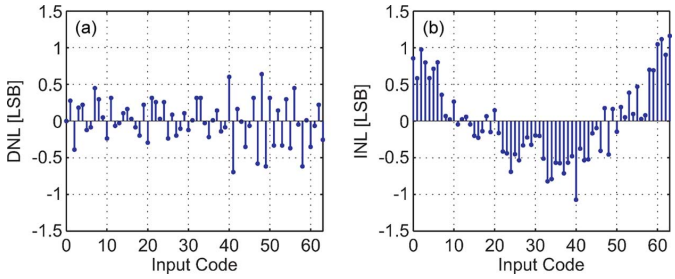

Fig. 11. Measured DAC nonlinearity errors at an update rate of 1 kS/s, after calibration, and at an output swing of 1.3 V: (a) differential nonlinearity (DNL) and (b) integral nonlinearity (INL).

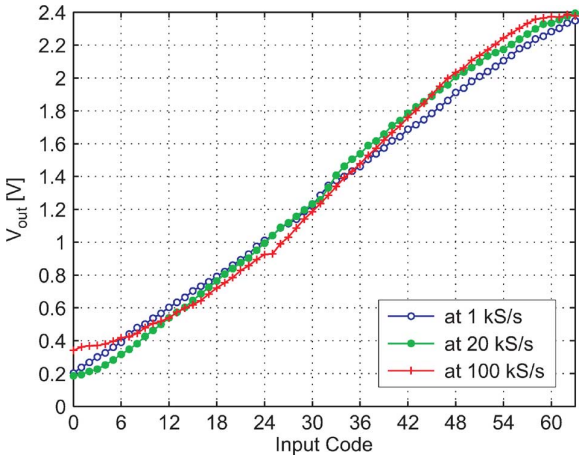

Fig. 12. Measured DAC transfer characteristics at an update rate of 1, 20, and 100 kS/s. The DAC was operating in worst case conditions: before calibration and slightly above the maximum output voltage swing ($\gtrsim$2 V).

maximum DNL and INL are -0.29 and -1.21 LSB, respectively. Furthermore, Fig. 11 shows the measured DNL and INL at an update rate of 1 kS/s, after calibration and at an output swing of 1.3 V; the resulting maximum DNL and INL are -0.69 and 1.16 LSB, respectively.

Fig. 12 illustrates the upper speed limit of the DAC in worst case conditions, i.e., the DAC was operating before calibration and slightly above the maximum output voltage swing ($\gtrsim$2 V). As shown in the figure, as the update rate increases above $\sim$20 kS/s, the measured transfer function exhibits higher distortion, whereas, at a swing of only 1 V and after calibration, the DAC was able to operate at a maximum update rate as high as 100 kS/s without strong deterioration.

Finally, for the evaluation of the spurious-free dynamic range (SFDR), Fig. 13 shows the spectrum of two measured output sinusoids at 31.25 Hz (update rate of 1 kS/s) and 3.125 kHz (update rate of 100 kS/s). The SFDR is found to be 32 dB for both outputs.

C. Benchmarking

Table II benchmarks the 6-bit current-steering DAC presented in this work against the recently published 6-bit switched-capacitor (C-2C) organic-based DAC [6]. The comparison clearly depicts that the current-steering DAC consumes 30 times smaller chip area and achieves 1000 times higher maximum update rate than the state of the art. This dramatic performance boost results from the OTFT fabrication process based on high-resolution silicon stencil masks that makes it possible to use transistors with smaller dimensions and far improved matching. In addition, the current-steering DAC achieves a maximum output voltage swing of 2 V, which is as high as double the swing generated by the C-2C DAC. Owing to the nonlinear leakage error generated by the capacitors, the lower speed limit of the C-2C DAC is constricted to 10 S/s, while the current-steering DAC can operate at DC. Although the power dissipation of the current-steering DAC is relatively high (260 μW), the power–delay product is still smaller than that of the C-2C DAC.

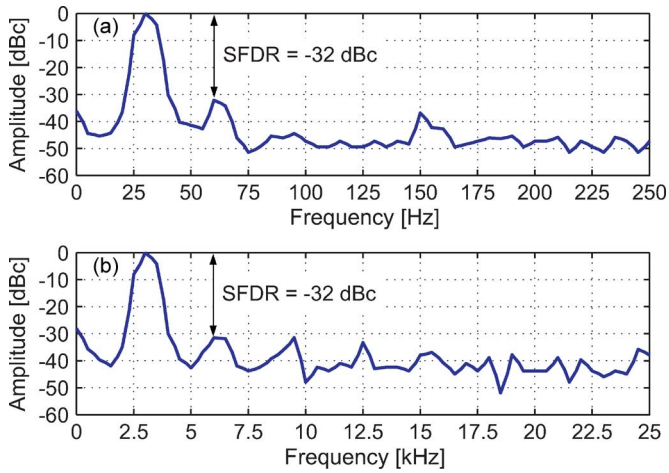

Fig. 13. Measured DAC output spectrum for two output sinusoids at: (a) 31.25 Hz (update rate of 1 kS/s) and (b) 3.125 kHz (update rate of 100 kS/s).

TABLE II
BENCHMARKING TABLE AND DAC CHARACTERISTICS SUMMARY

Design Parameter	[6]	This Work
Architecture	Switched-Capacitor	Current-Steering
Technology	Complementary OTFTs	P-type OTFTs
Resolution	6-bit	6-bit
Min. Feature	20 μm	4 μm
Transistor Count	26	129
Capacitor Count	17	0
Chip Area	$28 \times 24\,mm^2$	$2.6 \times 4.6\,mm^2$
Supply Voltage	3 V	3.3 V
Output Swing	$\sim 1\,V$	$\sim 2\,V$
Update Rate	10 S/s-100 S/s	DC-100 kS/s
Power×Delay	7 nWs (1 V swing)[1]	1.8 nWs (1 V swing)[2] 2.6 nWs (2 V swing)
Max. DNL	-0.6 LSB (at 100 S/s)	-0.69 LSB (at 1 kS/s)
Max. INL	-0.8 LSB (at 100 S/s)	+1.16 LSB (at 1 kS/s)
SFDR	24 dB (at 10 Hz) 29 dB (at 45 Hz)	32 dB (at 31 Hz & at 3.1 kHz)

[1] Deduced from [7] at 100 S/s and the input bit stream is not stated
[2] Measured at 100 kS/s and at the input bit stream of "111111"

VI. CONCLUSION

A record in performance and compactness for an organic integrated circuit has been introduced in this work by using an OTFT fabrication process that is based on high-resolution silicon stencil masks. Such a process offers submicron channel lengths and superb transistor matching, thus allowing the use of circuit topologies that are not feasible otherwise. Accordingly, the first 3.3 V 6-bit 100 kS/s current-steering DAC using p-type OTFTs has been demonstrated. The chip has been fabricated on

a glass substrate with an area of 2.6×4.6 mm^2. Measurement results show that the converter is 1000 times faster and 30 times smaller than the state of the art.

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Tarek Zaki (S'07) received the B.Sc. degree (with highest honors) in information engineering and technology from the German University, Cairo, Egypt, in 2009, and the M.Sc. degree (with distinction) in information technology from the University of Stuttgart, Stuttgart, Germany, in 2010, where he is currently working toward the Ph.D. degree.

Since 2010, he has been a Researcher at the Institute for Microelectronics Stuttgart (IMS CHIPS), Stuttgart, Germany. His research interest is the design of mixed-signal circuits based on organic semiconductors.

Frederik Ante received the Diploma degree in physics from the University of Würzburg, Würzburg, Germany, in 2007. He is currently working toward the Ph.D. degree in physics from the École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland.

He is currently a Scientist with the Organic Electronics Group, Max Planck Institute for Solid State Research, Stuttgart, Germany. His research interests include organic devices and circuits, doping of organic semiconductors, and high-resolution patterning techniques.

Ute Zschieschang received the Diplomingenieur degree in mechanical engineering from Mittweida University of Applied Sciences, Mittweida, Germany, in 2000, and the Ph.D. degree in chemistry from the Technical University Bergakademie, Freiberg, Germany, in 2006.

Since 2005, she has been a Scientist with the Organic Electronics Group, Max Planck Institute for Solid State Research, Stuttgart, Germany. Her research interests include high-performance conjugated semiconductors, self-assembled monolayers, and micropatterning techniques for organic devices and circuits.

Joerg Butschke received the Ph.D. degree in mechanical engineering from the University of Stuttgart, Stuttgart, Germany, in 2003.

He joined the Institute for Microelectronics Stuttgart (IMS CHIPS), Stuttgart, Germany, in 1996 as a Research Engineer and was involved in the development of the SOI stencil mask technology. His current work covers data preparation, electron beam lithography, and registration metrology. He has authored and coauthored several papers on NGL mask technology. Since 2010, he has been head of the Lithography Department.

Florian Letzkus received the M.S. degree in physics from the University of Tübingen, Tübingen, Germany, in 1996, and the Ph.D. degree from the University of Stuttgart, Stuttgart, Germany, in 2003. His dissertation focused on dry and wet etch processes for stencil mask making.

In 1997 he joined the Institute for Microelectronics Stuttgart (IMS CHIPS), Stuttgart, Germany, where he is currently head of the Nanoprocess Department and responsible PMLII project-manager. He authored and coauthored more than 60 publications in the field of NGL mask technology.

Harald Richter received the diploma in semiconductor physics from the University of Kaiserslautern, Kaiserslautern, Germany, in 1980, and the Ph.D. degree in physics from the University of Stuttgart, Stuttgart, Germany, in 1983.

In 1983, he was with the Xerox Research Center, Rochester, NY, studying surface properties of various semiconductors. From 1984 to 1986, he held a postdoctoral position with the Max Planck Institute for Semiconductor Research, Stuttgart, Germany, before joining the Institute for Microelectronics Stuttgart (IMS CHIPS) in 1986. He held several positions in the Technology and the Systems division before being nominated Head of System Division in 2005. In this division, both CMOS imager circuits and structured ASICs are developed and fabricated in small volumes.

Hagen Klauk (S'97–M'99) received the Diplomingenieur degree from Chemnitz University of Technology, Chemnitz, Germany, in 1995, and the Ph.D. degree from the Pennsylvania State University (Penn State), University Park, in 1999, both in electrical engineering.

From 1999 to 2000, he was a Postdoctoral Researcher with the Center for Thin Film Devices at Penn State. In 2000, he joined Infineon Technologies, Erlangen, Germany. Since 2005, he has been head of the Organic Electronics Group, Max Planck Institute for Solid State Research, Stuttgart, Germany. His research focuses on flexible transistors and circuits based on organic semiconductors, carbon nanotubes, and inorganic semiconductor nanowires.

Joachim N. Burghartz (M'90–SM'92–F'02) was born in Aachen, Germany, in 1956. He received the M.Sc. (Dipl. Ing.) degree from the RWTH Aachen, Germany, in 1982, and the Ph.D. (Dr.-Ing.) degree from the University of Stuttgart, Stuttgart, Germany, in 1987, both in electrical engineering.

From 1982 to 1987, he was a Research Assistant with the University of Stuttgart, where he developed sensors with integrated signal conversion with a special focus on magnetic-field sensors. From 1987 to 1998, he was with the IBM Thomas J. Watson Research Center, Yorktown Heights, NY. His earlier research work at IBM included device applications of selective epitaxial growth of silicon, Si and SiGe high-speed transistor design and integration processes, and deep submicrometer CMOS technology. He and his colleagues at IBM Research demonstrated the first SiGe bipolar technology setting the basis for IBM's SiGe commercialization. From 1994 to 1998, he was interested in the development of circuit building blocks for SiGe RF front-ends, with a special interest in the integration of high-quality passive components on silicon, and in particular the optimization of integrated spiral inductors. In 1998, he moved to The Netherlands to become a full Professor with Delft University of Technology (TU Delft). There he was chairing the High-Frequency Technology and Components (HiTeC) group. His research interests continued to be on silicon RF technology ranging from investigations on materials to the design of RF circuit building blocks. Since 1995, he has been setting several milestones in the development of integrated spiral inductors for high-frequency applications. From March 2001 until September 2005, he was the Scientific Director of the Delft Institute of Microelectronics and Submicron Technology (DIMES). Since October 1, 2005, he has been Director and Chairman of the Board of the Institute for Microelectronics Stuttgart (IMS CHIPS) and full Professor with the University of Stuttgart. Since March 1, 2006, he has been the head of the Institute of Nano- and Microelectronic Systems (INES) at the University of Stuttgart. In Stuttgart he is leading a research program that is focused on industrial contract research in the areas silicon technologies, advanced lithography, CMOS imagers, ASIC design and continued education. Recently, his special research interest is on a new manufacturing technology for ultrathin chips aimed at 3D-ICs, flexible and ultra-small electronics and other applications. He also continues to supervise several Ph.D. students at TU Delft working on projects related to RF silicon technology. He has published more than 300 reviewed articles and holds 22 patents.