Modified Bootstrap Switching Scheme for Organic Digital Integrated Circuits

Masoud Seifaei, Daniel Schillinger, Matthias Kuhl, Matthias Keller, Ute Zschieschang, Hagen Klauk, and Yiannos Manoli

***Abstract*—The design and implementation of a modified bootstrap switching circuit based on p-channel organic thin-film transistors and integrated thin-film resistors that addresses the lack of high-performance n-channel organic transistors is presented. Using the bootstrap technique, the fall time of the output stage is decreased by more than a factor of 10, resulting in a 10.39 times higher operating frequency for a load capacitance of 10 nF, and rail-to-rail output swing is achieved. A minimum-area inverter and a Schmitt-trigger-based inverter are presented that serve as references for comparison and as small-footprint alternatives to the bootstrap circuit. The dynamic performance of the proposed circuits is validated by comparing three different ring oscillator implementations.**

***Index Terms*—Bootstrap, digital inverter, flexible electronics, organic electronics, ring oscillator, Schmitt-trigger.**

I. Introduction

ORGANIC thin-film transistors (TFTs) are potentially useful for flexible electronics applications, such as large-area sensors, smart textiles, and rollable active-matrix displays. While p-channel organic TFTs with sufficient performance and stability can be fabricated on a variety of substrates [1], the performance and stability of n-channel organic TFTs is still relatively poor [2], which poses a number of challenges for the design of integrated circuits. For example, in analog circuits, the lack of adequate n-channel TFTs makes it difficult to implement high-impedance loads, which results in poor signal gain. This problem has recently been addressed using integrated thin-film resistors, resulting in amplifiers with high gain, large bandwidth, and small footprint [3]. Digital organic circuits often rely on diode-connected, zero-V_{GS} [4], [5] or biased-load designs [6] and thus suffer from asymmetric paths for the charging and discharging of the load capacitance C_L, resulting in a fall time (t_f) that is longer than the rise time (t_r).

In this letter, we present a modified version of the bootstrap switching circuit [7], depicted in Fig. 1. This circuit provides symmetric paths for the charging and discharging of C_L, which leads to very short t_f and high switching frequencies. A minimum-area inverter [Fig. 2(a)] and a Schmitt-trigger-based inverter [Fig. 2(a)], designed and fabricated using integrated thin-film resistors, are presented as small-footprint alternatives for lower-frequency digital implementation. The minimum-area inverter and a Schmitt-trigger-based inverter are designed using minimum-sized p-channel TFTs, i.e., W/L = 50 μm/20 μm, and a load resistance of 1 MΩ and 1.5 MΩ, respectively. Three types of ring oscillators using the mentioned inverter architectures are implemented as an application example.

Manuscript received May 29, 2019; revised August 12, 2019 and September 16, 2019; accepted September 19, 2019. Date of publication October 1, 2019; date of current version October 30, 2019. This article was approved by Associate Editor Samuel Palermo. This work was supported by the German Research Foundation under Grant MA 2193/17-1, Grant MA 2193/17-2, Grant KL 2223/6-1, and Grant KL 2223/6-2 (SPP "FFlexCom"). *(Corresponding author: Masoud Seifaei.)*

M. Seifaei, D. Schillinger, and M. Keller are with the Fritz Huettinger Chair of Microelectronics, IMTEK, University of Freiburg, 79110 Freiburg, Germany (e-mail: masoud.seifaei@imtek.uni-freiburg.de).

M. Kuhl is with the Institute for Integrated Circuits, Hamburg University of Technology, 21073 Hamburg, Germany.

U. Zschieschang and H. Klauk are with the Organic Electronics Research Group, Max Planck Institute for Solid State Research, 70569 Stuttgart, Germany.

Y. Manoli is with the Fritz Huettinger Chair of Microelectronics, IMTEK, University of Freiburg, 79110 Freiburg, Germany, and also with Hahn-Schickard, 78052 Villingen-Schwenningen, Germany.

Digital Object Identifier 10.1109/LSSC.2019.2944854

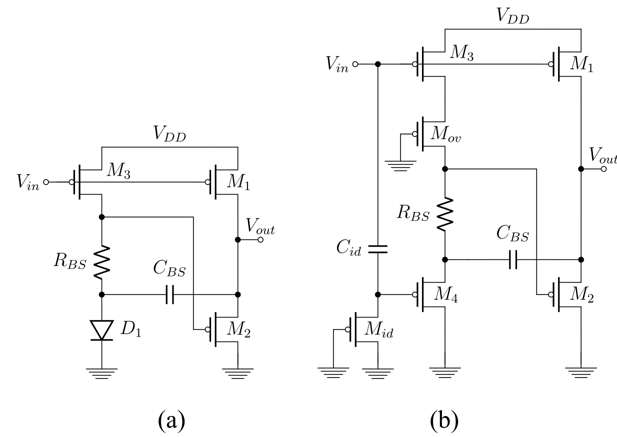

Fig. 1. Since high-quality diodes are difficult to fabricate on flexible substrates, the diode in the conventional bootstrap circuit (a) is replaced by an active transistor architecture (b). In addition, a cascode isolating TFT, M_{ov}, is added in order to protect the gate-drain junction of M_3.

The circuits were fabricated using p-channel organic TFTs with a minimum channel length of 20 μm and gate-to-contact overlaps of 30 μm, based on the vacuum-deposited small-molecule semiconductor dinaphtho[2,3−b : 2',3'−f]thieno[3,2−b]thiophene (DNTT) [8] and thin-film resistors based on vacuum-deposited carbon [3]. The TFTs have a threshold voltage V_{th} of −1 V, a carrier mobility μ_{eff} of 2 cm^2/Vs and a gate-dielectric capacitance C_I of 600 nF/cm^2. The circuits were fabricated on flexible polyethylene naphthalate (PEN) substrates using polyimide shadow masks [8].

A meaningful comparison between inverter architectures is difficult to perform if the circuits are fabricated using different semiconductors or processes. We will therefore limit the comparison to the biased-load, zero-V_{GS}, pseudo-E, and pseudo-D architectures reported in [6], as these were implemented using the same materials and a similar fabrication process as the circuits presented here; the only differences are the minimum channel length (5 μm in [6], 20 μm here) and gate-to-contact overlaps (20 μm in [6], 30 μm here).

In Section II the modified bootstrap circuit is explained in detail. Implementations and measurement results of the bootstrap circuit are given in Section III. The application examples are presented in Section IV. The results are summarized in Section V.

II. Modified Bootstrap Switching Scheme

The main idea behind the bootstrap circuit, shown in Fig. 1(a), is to charge C_{BS} to $V_{DD} - V_{D,on}$ when $V_{in} = 0$, and then put C_{BS} in parallel with C_{SG} of M_2 when $V_{in} = V_{DD}$, in order to charge C_{SG} to $V_{DD} - V_{D,on}$ and drive M_2 deep into the linear regime.

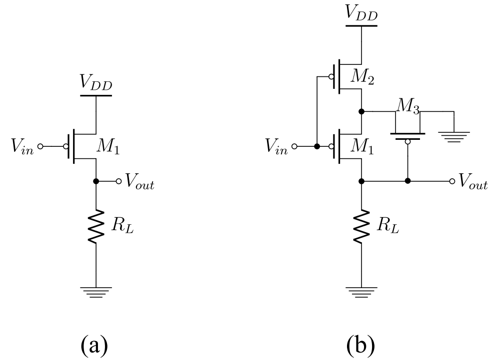

Fig. 2. (a) Minimum-area inverter and (b) Schmitt-trigger-based inverter implemented using resistive loads.

Since high-quality diodes are difficult to implement on flexible substrates, the diode employed in the conventional bootstrap circuit [Fig. 1(a)] is implemented using the components available in our technology, i.e., p-channel TFTs, metal–insulator-metal (MIM) capacitors, and thin-film carbon resistors. Using simply a diode-connected TFT is not desirable, since the large turn-on voltage would reduce the V_{SG} of M_2, causing significant performance degradation.

The proposed solution is the charge-pump circuit consisting of C_{id} and a diode-connected TFT M_{id}, as depicted in Fig. 1(b). As M_{id} has no DC bias current, it acts as a diode with $V_{D,on} = V_{th}$, thus the gate voltage of M_4 will swing from $|V_{th}|$ to $-(V_{DD} - |V_{th}|)$ as V_{in} swings from V_{DD} to GND and vice versa. For this purpose, the capacitance of C_{id} should be much larger than the sum of the parasitic capacitances seen on the gate of M_4. With a proper design of R_{BS}, $V_{DS,4}$ can reach near-zero volts, as the gate of M_4 is pulled to $-(V_{DD} - |V_{th}|)$.

In addition, when $V_{in} = V_{DD}$, M_3 and M_1 turn off and $V_{G,2}$ changes to approximately $-V_{DD}$, making $V_{GD,3}$ nearly equal to $2V_{DD}$, which could easily destroy the TFTs. In order to prevent this issue, M_{ov} is used as a cascode isolating transistor, by means of which the voltage difference between the terminals of M_3 is limited to V_{DD}.

III. Bootstrap Inverter Implementation and Measurement Results

The concept of modified bootstrap switching and the use of integrated thin-film carbon resistors as the load elements in minimum-area and Schmitt-trigger-based inverters are demonstrated and compared by means of three different inverter implementations, with the circuit schematics shown in Fig. 1(b) and Fig. 2(a) and (b), respectively.

The falling-edge waveforms of the three inverters with a load capacitance of 1 nF are shown in Fig. 3(a), showing significantly reduced t_f and rail-to-rail output swing for the bootstrap inverter. The reason for the swing improvement is the push–pull behavior of the output stage.

The t_f and t_r of the bootstrap and of the minimum-area resistive-load inverters measured for different load capacitances are shown in Fig. 3(b). As expected, the t_f of the bootstrap inverter is more than one order of magnitude smaller than that of the minimum-area resistive-load inverter. The falling edge of the Schmitt-trigger-based inverter and the minimum-area inverter are nearly the same, because the discharging path for both of the circuits is implemented using the integrated carbon resistors. Thus, the analysis of the fall time of the minimum-area inverter is also valid for the Schmitt-trigger-based inverter.

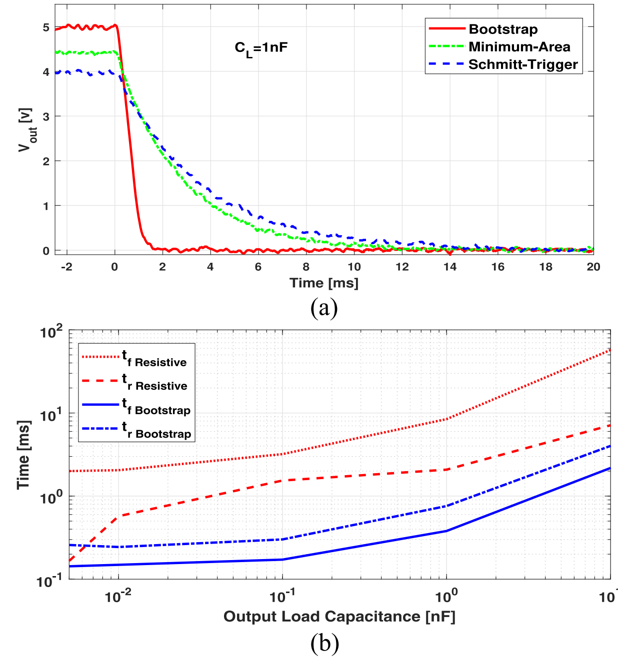

Fig. 3. (a) Measured falling edge of the output signal of inverters implemented in three different architectures. The bootstrap design produces the smallest t_f and rail-to-rail swing of the output signal. (b) Comparison of t_f and t_r of the minimum-area resistive-load inverter and the bootstrap inverter as a function of the load capacitance, showing that the t_f of the bootstrap circuit is smaller by a factor of 10 over the entire range of load capacitances.

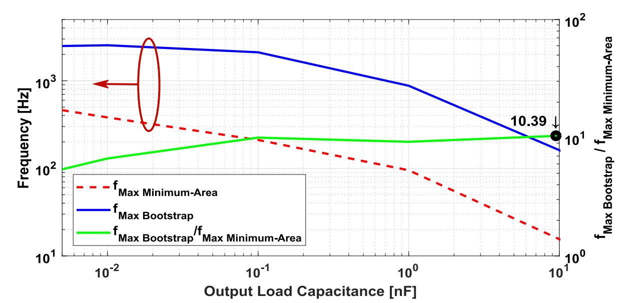

Fig. 4. Maximum operating frequency of the minimum-area resistive-load inverter and of the bootstrap inverter as a function of the load capacitance. For $C_L = 10$ nF, the maximum operating frequency of the bootstrap inverter is 10.39 times higher than that of the resistive-load inverter.

The t_r of the resistive-load inverter without load is smaller than that of the bootstrap circuit, because of the smaller parasitic capacitance. With increasing load capacitance, the t_r of the minimum-area inverter increases more rapidly than that of the bootstrap inverter, because of the larger channel width of the output TFT of the bootstrap inverter. Furthermore, due to the fact that C_{BS} has to be charged at the rising edge of the output signal, the t_f of the bootstrap inverter is smaller than its t_r.

The advantage of the bootstrap inverter over the resistive-load inverter in terms of the maximum operating frequency increases with increasing load capacitance, as shown in Fig. 4. For $C_L = 10$ nF, the maximum operating frequency of the bootstrap inverter is 10.39 times higher than that of the resistive-load inverter.

Table I compares the key parameters of different inverter architectures to the proposed architectures at a load capacitance of 16 pF. As mentioned in the introduction, all of the inverters were fabricated using the same process and the same semiconductor, but using

TABLE I
COMPARISON OF DIFFERENT INVERTER ARCHITECTURES

Parameter	This work	This work	This work	[6] [4]	[6]	[6] [5]	[6] [5]
Architecture	Bootstrap	Minimum-Area	Schmitt-Trigger	Zero-V_{GS}	Biased-Load	Pseudo-D	Pseudo-E
L_{min} (L_{OV})	20 μm (30 μm)	20 μm (30 μm)	20 μm (30 μm)	5 μm (20 μm)	5 μm (20 μm)	5 μm (20 μm)	5 μm (20 μm)
Area	1.8 mm^2	0.21 mm^2	0.58 mm^2	0.1 mm^2	0.122 mm^2	0.21 mm^2	0.275 mm^2
# Supplies	1	1	1	1	2	1	2
Rise time [a]	255 μs	700 μs	1387 μs	43 μs	29 μs	53 μs	61 μs
Fall time [a]	155 μs	2245 μs	3253 μs	368 μs	144 μs	345 μs	147 μs
t_f / t_r [c]	0.61	3.2	2.4	8.6	4.9	6.5	2.4
$V_{out, min}$	≈ 0 V	≈ 0 V	≈ 0 V	≈ 0 V	≈ 0 V	≈ 0 V	≈ 0 V
$V_{out, max}$	5 V	4.45 V	4 V	3 V [b]	≈ 2.38 V [b]	3 V [b]	≈ 2.8 V [b]
Supply	5 V [c]	5 V [c]	5 V [c]	3 V	3 V	3 V	3 V

[a] The values were measured with a load capacitance of 16 pF.
[b] Estimated from the output waveform diagrams in [6].
[c] The circuits are operational with supply voltages down to 2 V.

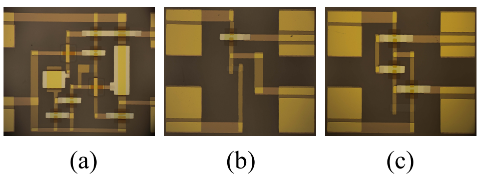

Fig. 5. Photographs of (a) bootstrap inverter, (b) minimum-area resistive-load inverter, and (c) Schmidt-trigger resistive-load inverter.

different channel lengths and larger gate-to-contact overlaps. The larger channel length and gate-to-contact overlaps, which are the main source of the parasitic capacitances, are the reason behind the larger rise times of the proposed architectures in comparison to the inverters in [6]. The bootstrap circuit exhibits an impressively small fall time in comparison to its rise time and a rail-to-rail output voltage swing. Simulation results using the minimum channel length and gate-to-contact overlaps used in [6] have shown a 9.3 times shorter fall time for the bootstrap inverter compared to the biased-load inverter.

The minimum-area resisitive-load inverter can be an ideal candidate for small-area and lower-frequency applications. Because of the negligible parasitic capacitance and relatively small footprint of the integrated carbon resistors, by assuming the same process and critical dimensions, the minimum-area inverter can have a smaller area and a higher operating frequency than the conventional architectures. In comparison to the biased-load inverter which requires two power supplies and has a gain of 6 dB [6], the minimum-area inverter uses a single supply and in [3] has shown a gain of more than 29 dB. Although the Schmitt-trigger-based resistive-load inverter has inferior dynamic performance, its hysteresis characteristics make it attractive for signal-conditioning circuits and ring oscillators.

Photographs of the bootstrap, the minimum-sized resistive-load, and the Schmitt-trigger resistive-load inverters are shown in Fig. 5.

IV. APPLICATION EXAMPLES

In certain types of analog or digital circuits, the active push–pull behavior of the output stage is of crucial importance. An example is the ring oscillator, where the symmetry of the falling and rising edges and the amplitude of the output-voltage swing are two important factors. Another example are dynamic logic circuits which can be implemented using the bootstrap architecture.

A. Bootstrap-Based 7-Stage Ring Oscillator

In order to evaluate the performance of the proposed inverter architectures, 7-stage ring oscillators based on the bootstrap, the minimum-area, and the Schmitt-trigger-based inverters were implemented, as shown in Fig. 7. All circuits were designed for minimum circuit area. The output waveforms of the ring oscillators measured with a supply voltage of 5 V are shown in Fig. 6. Table II summarizes the parameters of the three implementations. The bootstrap-based ring oscillator has approximately symmetric t_r and t_f and oscillates with the highest frequency and with rail-to-rail output swing.

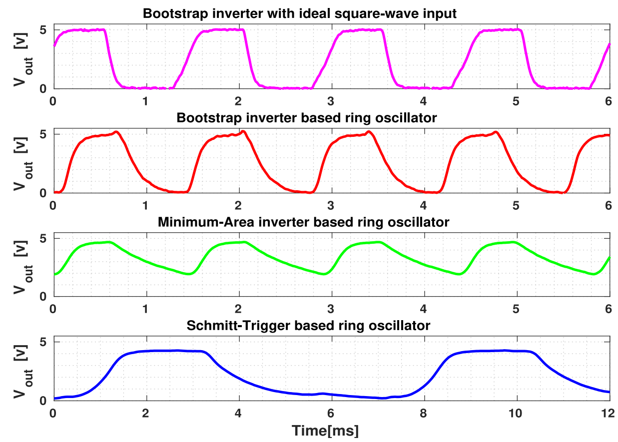

Fig. 6. Measured output waveforms of the bootstrap-based inverter with ideal square-wave input and 7-stage ring oscillators based on the bootstrap-based inverter, the minimum-area resistive-load inverter, and the Schmitt-trigger-based resistive-load inverter. The bootstrap-based ring oscillator exhibits rail-to-rail output swing and more symmetric rising and falling edges than the other designs.

TABLE II
COMPARISON TABLE OF THREE DIFFERENT RING-OSCILLATOR IMPLEMENTATIONS

Parameter	Bootstrap	Minimum-Area	Schmitt-Trigger
$V_{out, min}$	21 mV	1.4 V	0.2 V
$V_{out, max}$	5.2 V	4.69 V	4.27 V
Frequency	732 Hz	685 Hz	141 Hz
Power	150 μW	80 μW	85 μW
Supply	5 V	5 V	5 V
Area	17.6 mm^2	2.35 mm^2	5.25 mm^2

Closer inspection shows that in the bootstrap-based ring oscillator, the fall time is slightly longer than the rise time ($t_f > t_r$), whereas in the bootstrap-based inverter, the opposite is true ($t_f < t_r$; see Table I). The reason is that the discharge path relies on the charge-pump circuit, which is edge-sensitive, so the fall time of the output signal depends on the rise time of the input signal. The inverter measurements were performed with a square-wave input signal, so that $V_{GS,M2}$ increases promptly and M_2 rapidly reaches its maximum current-driving capability for discharging the output capacitor, resulting in a short fall time. In contrast, the signal in the ring oscillator

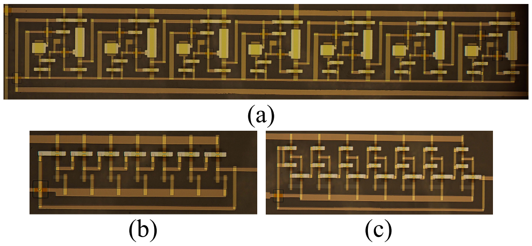

Fig. 7. Photographs of 7-stage ring oscillators based on (a) bootstrap inverter, (b) minimum-area resistive-load inverter, and (c) Schmitt-trigger resistive-load inverter.

is not a square wave, so it takes longer for $V_{GS,M2}$ to increase and for M_2 to discharge the output capacitor, resulting in a longer fall time. Symmetric rise and fall times can in principle be achieved by optimizing the device sizing, but this is currently quite difficult due to the significant variations of the carrier mobility of the TFTs, of the parasitic capacitance of the TFTs (because that the masks are aligned manually) and of the resistance of the thin-film resistors (due to significant thickness nonuniformity of the vacuum-deposited carbon layer). Also note that in the minimum-area ring oscillator, the fall time (2.25 ms) is longer than the oscillation period (1.46 ms), so that the output signal never reaches 0 V; this issue can be solved by increasing the number of inverter stages in order to increase the oscillation period. Finally, the Schmitt-trigger-based ring oscillator has by far the lowest oscillation frequency, but it generates a better formed output signal, owing to its hysteresis characteristics.

B. Dynamic Logic

The relative overhead of the bootstrap technique is minimized when implementing complex logic functions. In a p-channel-organic-TFT technology, the logic function of a dynamic logic circuit can be implemented using only p-channel TFTs, but the lack of high-performance and stable n-channel organic TFTs makes an efficient implementation of a reset circuit very problematic or even impossible. However, due to its superior push–pull behavior the bootstrap architecture can be used for the reset part of dynamic logic.

V. Conclusion

A modified bootstrap switching circuit with superior dynamic performance, push–pull behavior, and rail-to-rail output swing even for high capacitive loads has been presented. The t_f is reduced by more than a factor of 10 and the maximum operating frequency for a load capacitance of 10 nF is 10.39 times larger compared to a resistive-load circuit. The minimum-sized resistive-load and Schmitt-trigger resistive-load inverter architectures are presented as lower-frequency and small-area alternatives for the common inverter architectures. The dynamic performance of the proposed circuits is demonstrated by implementing a ring oscillator. The bootstrap-based ring oscillator generates the highest frequency and symmetric rise and fall times along with a rail-to-rail output signal. The Schmitt-trigger-based ring oscillator has a square-wave output signal, as expected due to its hysteresis characteristics.

References

[1] U. Kraft *et al.*, "Low-voltage, high-frequency organic transistors and unipolar and complementary ring oscillators on paper," *Adv. Electron. Mater.*, vol. 5, no. 2, 2019, Art. no. 1800453. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/aelm.201800453

[2] U. Zschieschang, J. W. Borchert, M. Geiger, F. Letzkus, J. N. Burghartz, and H. Klauk, "Stencil lithography for organic thin-film transistors with a channel length of 300nm," *Org. Electron.*, vol. 61, pp. 65–69, Oct. 2018. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1566119918303446

[3] M. Seifaei *et al.*, "Stable, self-biased and high-gain organic amplifiers with reduced parameter variation effect," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Tainan, Taiwan, Nov. 2018, pp. 119–122.

[4] D. Raiteri, P. van Lieshout, A. van Roermund, and E. Cantatore, "Positive-feedback level shifter logic for large-area electronics," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 524–535, Feb. 2014.

[5] T.-C. Huang *et al.*, "Pseudo-CMOS: A design style for low-cost and robust flexible electronics," *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 141–150, Jan. 2011.

[6] M. Elsobky *et al.*, "A digital library for a flexible low-voltage organic thin-film transistor technology," *Org. Electron.*, vol. 50, pp. 491–498, Nov. 2017. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1566119917304275

[7] "HV floating MOS-gate driver ICs, in IR," Application Note AN-978, Int. Rectifier Corprat., El Segundo, CA, USA, 2007.

[8] U. Zschieschang and H. Klauk, "Low-voltage organic transistors with steep subthreshold slope fabricated on commercially available paper," *Org. Electron.*, vol. 25, pp. 340–344, Oct. 2015.