Unipolar Sequential Circuits Based on Individual-Carbon-Nanotube Transistors and Thin-Film Carbon Resistors

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ABSTRACT A fabrication process for the monolithic integration of field-effect transistors based on individual carbon nanotubes and load resistors based on vacuum-evaporated carbon films into fast unipolar logic circuits on glass substrates is reported for the first time. The individual-carbon-nanotube transistors operate with relatively small gate-source and drain-source voltages of 1 V and combine large transconductance (up to 6 μS), large ON/OFF ratio (>10^4), and short switching delay time constants (12 ns). The thin-film carbon load resistors provide linear current–voltage characteristics and resistances between 300 kΩ and 100 MΩ, depending on the layout of the resistors and the thickness of the vacuum-evaporated carbon films. Various combinational circuits (NAND, NOR, AND, OR gates) as well as a sequential circuit ($\bar{S}\bar{R}$ NAND latch) have been fabricated and characterized. Although these unipolar circuits cannot compete with optimized complementary circuits in terms of integration density and static power consumption, they offer the possibility of realizing air-stable, low-voltage integrated circuits with promising static and dynamic performance on unconventional substrates for large-area electronics applications, such as displays or sensors.

KEYWORDS: carbon-nanotube transistors · thin-film carbon resistors · unipolar circuits · sequential circuits

Nanoscale field-effect transistors that employ an individual semiconducting carbon nanotube as the charge-carrier channel hold great potential for the realization of high-performance digital or analog circuits on arbitrary substrates, such as glass or flexible plastics. Individual-carbon-nanotube p-channel transistors have been realized by many groups and have shown excellent static characteristics, including large transconductance (up to 40 μS),[1−6] large ON/OFF ratio ($\geq 10^7$),[7−12] and steep subthreshold swing (<80 mV/decade).[1,3,7,8,12−17] Unlike discrete transistors, integrated circuits based on individual-carbon-nanotube transistors are more challenging to realize. Because n-channel carbon-nanotube transistors often suffer from a lack of air stability,[3,13,18−20] poor ON/OFF ratio ($\leq 10^4$),[5,13,20−24] or the need for a thick gate dielectric to support large gate voltages for the conversion from p-channel to n-channel operation,[25] there are only a limited number of reports of air-stable, low-voltage complementary circuits based on carbon-nanotube transistors.[18−28]

In contrast to complementary circuits, unipolar circuits utilize only transistors of one carrier type and thus do not require n-channel transistors. Although this presents a possible advantage in terms of process complexity, unipolar circuits are in principle inferior to optimized complementary circuits, especially in terms of integration density and static power consumption. However, in light of the above-mentioned difficulties in producing n-channel carbon-nanotube transistors with adequate performance and stability, unipolar carbon-nanotube circuits are considered as a viable alternative to complementary carbon-nanotube circuits until high-performance, air-stable n-channel carbon-nanotube transistors become more commonplace. In fact, in the first report of integrated circuits based on individual-carbon-nanotube transistors, Bachtold *et al.* fabricated unipolar circuits.[29] In Bachtold's work, the load devices were implemented in the form of commercially available, fully packaged bulk resistors, which were connected to the carbon-nanotube transistors using coaxial cables. The circuits had excellent static characteristics, but because of the large parasitic capacitances introduced by the off-chip cable connections, the circuits were relatively slow (less than 100 Hz).

Here we report on a fabrication process for the realization of unipolar integrated circuits on glass substrates by integrating field-effect transistors based on individual semiconducting carbon nanotubes with load resistors based on thin vacuum-evaporated

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and lithographically patterned carbon films. For the realization of the load resistors we take advantage of the fact that thin films of vacuum-evaporated carbon have a relatively large ohmic resistance that matches well with the ON-state and OFF-state resistances of the individual-carbon-nanotube transistors. Owing to the large transconductance (6 μS) of the carbon-nanotube transistors and the fact that the load resistors are integrated on the same substrate, inverter circuits can be switched with a frequency as high as 2 MHz. In addition to simple combinational circuits (NAND, NOR, AND, OR gates) we also report on the first sequential logic circuits realized using individual-carbon-nanotube transistors.

RESULTS AND DISCUSSION

To fabricate, characterize, and integrate a large number of individual-carbon-nanotube transistors and thin-film carbon resistors, we first defined an array of metal probe pads and alignment markers on the glass substrate. The schematic process flow for the carbon-nanotube transistors is shown in Figure S1 (Supporting Information). For each transistor we defined a narrow gate electrode by electron-beam lithography and vacuum evaporation of 30 nm thick aluminum, so that each gate electrode is connected to one of the probe pads allocated for each transistor. The gate electrodes were then covered with a thin gate dielectric composed of oxygen-plasma-grown AlO_x (3.6 nm thick) and an octadecylphosphonic acid self-assembled monolayer (2.1 nm thick).[12,30] The electron-beam resist was then removed by lift-off. Single-walled carbon nanotubes produced either by the arc-discharge method or the HiPCO method and purchased from commercial sources were then randomly dispersed on the substrate from a liquid suspension that had been thoroughly sonicated and centrifuged prior to use. Using scanning electron microscopy (SEM) we located one individual carbon nanotube on each of the patterned gate electrodes, registered its precise location and orientation with respect to the alignment markers, and defined a pair of Ti/AuPd source and drain contacts by electron-beam lithography for each transistor. The channel length of the transistors is 300 to 400 nm.

Note that the density of carbon nanotubes in the liquid suspension was sufficiently large so that on average more than one nanotube was found on each gate electrode, but sufficiently small to allow an individual nanotube to be selected for each transistor. Although this method of locating and contacting individual nanotubes cannot be easily scaled to the mass production of sophisticated integrated circuits, it facilitates the investigation of the intrinsic properties of individual-nanotube devices and circuits without having to account for charge transport through a large number of nanotubes having different properties or

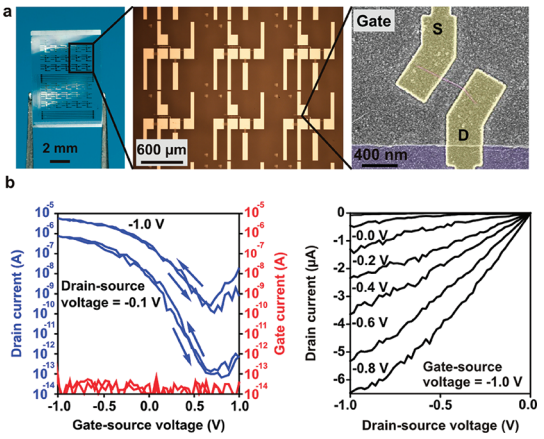

Figure 1. (a) Photograph of a glass substrate, optical microscopy image of an array of carbon-nanotube transistors and thin-film carbon load resistors, and SEM image of a carbon-nanotube transistor. The local gate electrode, the source and drain contacts, and the gate/source and gate/drain overlap areas are clearly visible. (b) Transfer and output characteristics of a field-effect transistor based on an individual semiconducting carbon nanotube produced by the arc-discharge method and fabricated on a glass substrate.

across nanotube−nanotube junctions.[31,32] Also note that it has been shown by Raman spectroscopy that carbon nanotubes can be damaged during SEM imaging,[33] although it is unclear how severe this damage is, considering that excellent electrical performance has been reported for transistors based on carbon nanotubes located by SEM.[34] For our experiments, we utilized a field-emission SEM operated with an acceleration voltage of 800 eV, a magnification of 15 000×, and an electron current of 185 pA.

To fabricate the load resistors, rectangular areas or meanders overlapping two adjacent probe pads were defined by electron-beam lithography, and a thin layer of carbon with a specific thickness was then deposited by vacuum evaporation and patterned by lift-off. Figure 1a shows a photograph of a glass substrate, an optical microscope image of an array of transistors and load resistors on a glass substrate, and an SEM image of a carbon-nanotube transistor. Each substrate contains up to 35 nanotube transistors and up to 105 thin-film carbon resistors.

The current−voltage characteristics of all transistors and resistors in each array were then measured in ambient air at room temperature. The yield of functional nanotube transistors with an ON/OFF ratio $\geq 10^4$ (for $V_{DS} = -0.1$ V) is usually around 30% in the case of mixed (semiconducting and metallic) carbon nanotubes produced by the HiPCO method, 50% in the case of mixed nanotubes produced by the arc-discharge method, and about 80% in the case of sorted semiconducting nanotubes (IsoNanotubes-S, provided by NanoIntegris). Statistics of 1131 individual-carbon-nanotube transistors we have fabricated with this method are shown in Figure S2 (Supporting Information).

By moving from mixed to sorted semiconducting nanotubes, the yield of transistors with a usefully large ON/OFF ratio is significantly increased. Figure 1b shows the current–voltage characteristics of a transistor based on a semiconducting carbon nanotube produced by the arc-discharge method fabricated on a glass substrate. This transistor has an ON/OFF ratio of 10^7 for $V_{DS} = -0.1$ V and an ON/OFF ratio of 5×10^4 for $V_{DS} = -1$ V. The transconductance is 6 μS, and the subthreshold swing is 80 mV/decade.

Unipolar integrated circuits with load resistors operate properly only if the resistance of the load resistors is smaller than the OFF-state resistance of the transistors, but larger than the ON-state resistance.[29,30] This means that the resistance of the load resistor must be selected carefully. Our carbon-nanotube transistors usually have an ON-state resistance below 1 MΩ and an OFF-state resistance above 1 GΩ. Therefore, our load resistors should have a resistance in the range of 1 MΩ to 1 GΩ. To realize such load resistors on a glass substrate, we initially considered long, narrow, thin metal meanders fabricated by electron-beam lithography, metal evaporation, and lift-off. However, common metals and metal alloys have very small resistivity (*e.g.*, titanium ~42 $\mu\Omega$cm, Nichrome ~110 $\mu\Omega$cm), so to make a resistor with a resistance of 10 MΩ would require a length/width ratio of more than 10^5, even if the film thickness was extremely small. For example, assuming a film thickness of 15 nm and a line width of 25 nm, the meander would have a length of almost 1 cm. At such extreme dimensions it is very difficult to obtain resistors with high yield and reproducibility, as shown in Figure S3 (Supporting Information).

As an alternative to metals and metal alloys, we have therefore fabricated load resistors based on vacuum-evaporated carbon films. The resistivity of vacuum-evaporated carbon is 4 to 6 orders of magnitude larger than the resistivity of metals, so it is much simpler to fabricate resistors with large resistance (>1 MΩ). Indeed, we found that the yield, uniformity, and reproducibility of vacuum-evaporated carbon-film resistors are much better than those of thin, narrow metal meanders. The resistivity of carbon depends on several parameters, such as the ratio between the number of sp^2-hybridized and sp^3-hybridized carbon atoms and the amount of structural disorder. The resistivity of carbon can be as small as 10^{-4} Ωcm in the case of graphite and as large as 10^{18} Ωcm in the case of diamond.[35] In this work, we have employed thermal evaporation of carbon from a 1 mm thick carbon wire in a vacuum evaporator with a background pressure of about 10^{-4} mbar. Figure 2a shows the Raman spectrum of a 20 nm thick carbon film evaporated onto a glass substrate. By fitting the measured Raman spectrum we obtain a ratio between the intensity of the D-band (centered at 1395 cm^{-1}) and the intensity of the G-band (centered at 1563 cm^{-1}) of about 0.9,

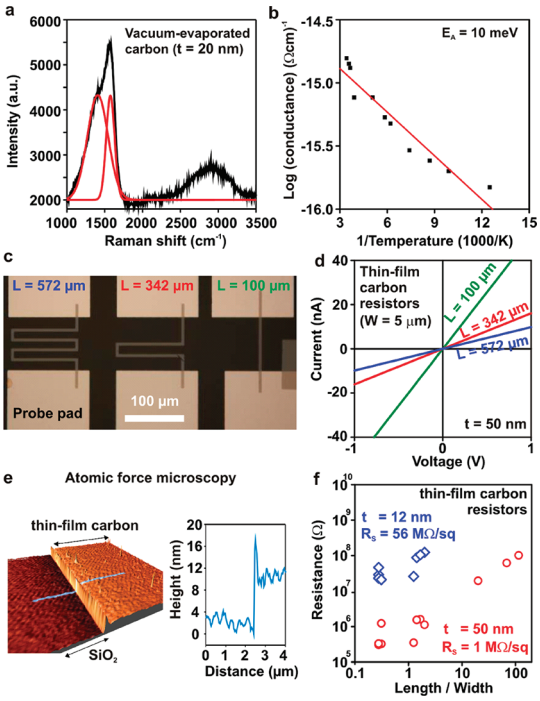

Figure 2. (a) Raman spectrum of a 20 nm thick carbon film deposited onto a glass substrate by vacuum evaporation from a carbon wire. The ratio between the intensity of the D-band (centered at 1395 cm^{-1}) and the intensity of the G-band (centered at 1563 cm^{-1}) is approximately 0.9. (b) Temperature dependence of the electrical conductance of a 20 nm thick vacuum-evaporated carbon film, indicating an activation energy of 10 meV. (c) Optical microscopy image of three thin-film carbon resistors with the same lithographically defined width (5 μm), but different length. (d) Current–voltage characteristic of three resistors. (e) AFM image and height profile of a patterned carbon film with a thickness of 12 nm. (f) Resistance *versus* length/width ratio of 21 thin-film carbon resistors with two different carbon thicknesses (12 and 50 nm).

which confirms that the evaporated carbon films contain significant structural disorder.[36,37] This was also confirmed by temperature-dependent conductance measurements, which indicate that carrier transport in the carbon films is thermally activated with an activation energy of about 10 meV (see Figure 2b).

To fabricate load resistors with well-defined ohmic resistance, a thin film of carbon was vacuum-evaporated onto the same substrate as the carbon-nanotube transistors and patterned by electron-beam lithography and lift-off, and a pair of adjacent AuPd probe pads was used as the contacts. Figure 2c shows a photograph of three carbon resistors with a carbon film thickness of 50 nm on a glass substrate. Each resistor has a lithographically defined width of 5 μm and a length of either 100, 342, or 572 μm. Figure 2d shows the current–voltage characteristics of these three resistors, confirming the excellent linearity of the resistance. Depending on the lithographically defined geometry, the resistance is between 20 and 100 MΩ. From the dimensions and the measured resistance, a sheet resistance of 1 MΩ/sq and a resistivity of 5 Ωcm

(for a carbon film thickness of 50 nm) are calculated. Figure 2e shows an atomic force microscopy (AFM) image and a height profile of an evaporated and patterned carbon film with a thickness of 12 nm, showing a well-defined line edge and relatively small surface roughness. Figure 2f summarizes the measured resistances of 21 resistors with various lengths, widths, and carbon film thicknesses, showing that depending on the geometry and thickness, resistors with a resistance between 300 kΩ and 100 MΩ can be fabricated with relaxed lateral dimensions. Figure S4 (Supporting Information) shows statistics of the measured resistances of 22 resistors with nominally identical width (30 μm), length (75 μm), and thickness (13 nm). The average resistance is 56 MΩ, with a standard deviation of 4%, confirming the good reproducibility of the fabrication process. Resistors with a smaller footprint can also be fabricated. As an example, Figure S5 shows a photograph and the current−voltage characteristics of a resistor that has a length and width of 2 μm and a resistance of 10 MΩ.

The simplest integrated circuit is the inverter, which consists only of a field-effect transistor and a load resistor. Figure 3a shows the circuit schematic and a photograph of an inverter based on an individual-carbon-nanotube transistor and a thin-film carbon load resistor with a resistance of 120 MΩ fabricated on a glass substrate. Because the load resistors are patterned directly between the probe pads for the output node (V_{OUT}) and the supply voltage (V_{DD}) node, there is no need for an additional process step to define interconnects. Figure 3b shows the static transfer characteristics and the small-signal gain of this inverter measured at a supply voltage of −1 V. As can be seen, the output signal swings completely from 0 V to V_{DD} (>0.99 V) as the input voltage is changed between the ON-state and the OFF-state of the transistor. The small-signal gain reaches about 15.

The exact shape of the inverter transfer curves depends on the load resistance. Figures S6 through S9 (Supporting Information) show that if the load resistance is too small or too large in comparison to the ON-state or OFF-state resistance of the transistor, the output swing of the inverter may be significantly smaller than the supply voltage. Given the significant variations of the electrical properties of transistors based on carbon nanotubes with different chiralities, the optimum load resistance is therefore different for each inverter, making the systematic design of robust integrated circuits very difficult. However, the uniformity of the characteristics of carbon-nanotube transistors and hence the prospects of carbon-nanotube integrated circuits are expected to greatly improve once carbon nanotubes with a single, well-defined chirality become available.[38]

Owing to the fact that the load resistors are monolithically integrated with the transistors on a glass substrate, the parasitic capacitances are very small, and so the integrated inverters are able to switch large signals with relatively short delay. Figure 3c shows the dynamic response of an inverter to an input signal with a frequency of 2 MHz. When the input potential is changed from −1 V to +1 V, the transistor switches from the ON-state to the OFF-state, and since the load resistance is smaller than the OFF-state resistance of the transistor, the output node is charged through the load resistor to the supply potential (−1 V). To minimize the time required for this transition, which is determined not only by the parasitic capacitances but also by the load resistance, the load resistor of this inverter was designed to have a relatively small resistance (1.2 MΩ). The signal delay associated with charging the output node through the load resistor can be estimated by fitting an exponential function to the falling edge of the output signal of the inverter. In Figure 3c this yields a signal delay of 100 ns, which is significantly shorter than the signal delay of the carbon-nanotube circuits reported by Bachtold *et al.*,[29]

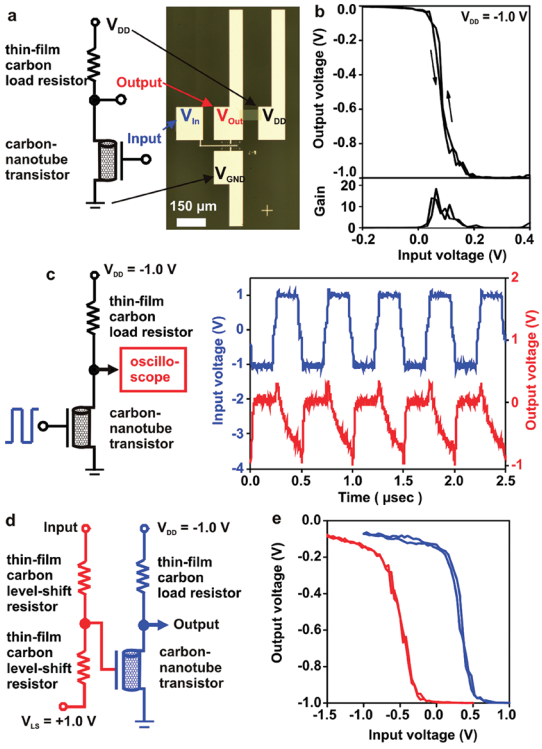

Figure 3. (a) Schematic and optical microscopy image of an inverter composed of a carbon-nanotube transistor and a thin-film carbon load resistor. (b) Static transfer characteristics of an inverter with a load resistance of 120 MΩ. (c) Output-voltage response of a carbon-nanotube inverter fabricated on a glass substrate to a square-wave input signal with a frequency of 2 MHz. The load resistance is 1.2 MΩ. By fitting an exponential function to the rising edge of the output signal, a time constant of 12 ns is extracted for the switching delay of the transistor. (d) Circuit schematic of an inverter with an integrated level-shift stage that consists of two additional thin-film carbon resistors. (e) Static transfer characteristics of an inverter without level-shifting (blue line) and of an inverter with integrated level-shift stage (red line).

which were limited by the parasitic capacitances associated with the cables connecting the transistors to external load resistors. When the input potential is changed from +1 V to −1 V, the transistor switches from the OFF-state to the ON-state, and since the ON-state resistance of the transistor is smaller than the load resistance, the output node is discharged through the transistor to ground potential. The signal delay associated with this transition can be estimated by fitting an exponential function to the rising edge of the output signal of the inverter. In Figure 3c this yields a signal delay of 12 ns, which is close to the signal delay of the complementary carbon-nanotube ring oscillator reported by Chen *et al.* (2 ns).[23]

The minimum signal delay (τ) of a field-effect transistor is determined by its transconductance (g_m) and gate capacitance (C_G): $\tau > \pi C_G/g_m$. The largest contribution to the gate capacitance of our individual-carbon-nanotube transistors is the overlap between the source and drain contacts and the gate electrode. Depending on the gate width and the orientation of the carbon nanotube on the patterned metal gate electrode, this overlap area is usually between 1 and 7 μm^2, so the gate capacitance is usually between 7 and 50 fF. For a transconductance of 6 μS this yields a theoretical lower limit for the signal delay of our transistors of about 5 to 30 ns.

The inverters shown in Figure 3b and c require a positive input voltage (>0.2 V) to switch the transistor into the OFF-state, but the output voltage of the inverter is never positive, which means that the input and output voltages of these inverters do not match. As a result, this type of inverter cannot be cascaded; that is, the output of this inverter cannot drive the input of an identical inverter. The reason for the positive switching voltage of these inverters is that our carbon-nanotube transistors often (although not always) have a slightly positive threshold voltage (about +0.2 V for the transistor shown in Figure 1b). Therefore we have designed and fabricated inverters with an integrated level-shift stage that consists of two thin-film carbon resistors (see Figure 3d). The purpose of the level-shift stage is to shift the (negative) input signal by a few hundred millivolts toward a more positive potential required to switch the transistor into the OFF-state.[39] As a result, inverters with an integrated level-shift stage have matching input and output levels; that is, inverters with level-shifting switch for input voltages between 0 V and −1 V and produce output voltages between 0 V and −1 V (see red curve in Figure 3e).

In addition to inverters, we have also fabricated and characterized four different unipolar combinational logic gates (a NAND gate, a NOR gate, an AND gate, and an OR gate). Figure 4 shows the circuit schematics and the transfer characteristics of these circuits, confirming the correct logic function according to the truth table. For simplicity, these circuits were realized without

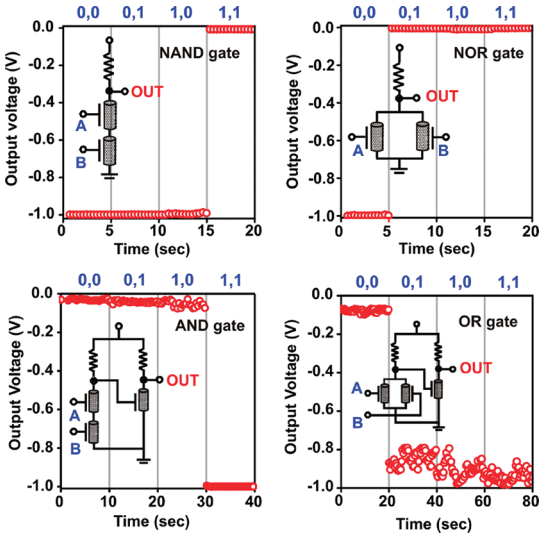

Figure 4. Circuit schematics and transfer functions of a NAND gate, a NOR gate, an AND gate, and an OR gate realized using individual-carbon-nanotube transistors and thin-film carbon resistors.

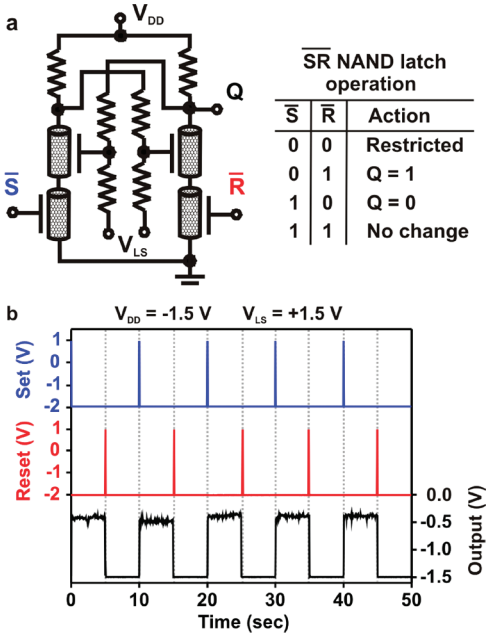

Figure 5. Circuit schematic and input−output characteristics of an $\overline{SR}$ NAND latch realized using individual-carbon-nanotube transistors and thin-film carbon resistors.

level-shift stage; that is, they were operated with input signals of −1 V and +1 V, and transistors with near-zero threshold voltage were chosen for the output stage of the AND gate and the OR gate.

Finally, we have also realized a sequential circuit. In sequential circuits, the output signal depends not only on the present input (as in combinational circuits) but also on the history of the input. A sequential circuit fabricated using transistors based on random networks of semiconducting carbon nanotubes was recently reported by Sun *et al.*[40] Sequential circuits of transistors

based on individual-carbon nanotubes have to our knowledge not been previously reported. Figure 5 shows the circuit schematic and the electrical response of an $\bar{S}\bar{R}$ NAND latch (a type of flip-flop) based on individual-carbon-nanotube transistors and thin-film carbon resistors. The circuit operates as follows: Applying a brief LOW pulse (pulse width 20 ms) to the $\bar{S}$ input causes the output (Q) to switch from the HIGH state (−1.5 V) to the LOW state (~0 V). This state information is stored in the latch, so that the output remains LOW until a LOW signal is applied to the $\bar{R}$ input, which switches the latch (and the output) back to the HIGH state (see Figure 5).

CONCLUSIONS

We have fabricated unipolar combinational and sequential logic circuits using field-effect transistors based on individual carbon nanotubes with large transconductance (>1 μS), large ON/OFF ratio (>10^4), and short switching delay time constants (12 ns). Load resistors were realized using vacuum-evaporated and lithographically patterned carbon films that provide a resistance between 300 kΩ and 100 MΩ and good linearity of the current−voltage characteristics. To account for the slightly positive threshold voltage of the transistors, an integrated level-shift stage based on two additional thin-film carbon resistors was implemented. Both the combinational and the sequential circuits show the correct logic functions. Fast integrated circuits like these are potentially useful for a variety of large-area electronics applications on arbitrary substrates, for example flexible information displays or conformable sensor arrays.

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Supporting Information Available: Additional description of the process flow to fabricate the carbon-nanotube transistors, statistics of the properties of carbon-nanotube transistors and thin-film carbon load resistors, yield issues with metal meander load resistors, characteristics of carbon resistors with reduced lateral dimensions, and relationship between load resistance and inverter output swing. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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Supporting Information

Sequential Circuits with Transistors based on Individual Carbon Nanotubes and Thin-Film Carbon Resistors

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1. **Process flow for carbon-nanotube transistors**
2. **Statistics of the ON/OFF ratio of individual-carbon-nanotube transistors**
3. **Yield issues with metal meander load resistors**
4. **Statistics of the resistance of thin-film carbon resistors**
5. **Thin-film carbon load resistors with reduced lateral dimensions**
6. **Relationship between load resistance and inverter output characteristics**

1. Process flow for carbon-nanotube transistors

Figure S1 shows the process flow to fabricate the individual-carbon-nanotube transistors. The metal probe pads, the gate electrodes, and the source/drain contacts are all patterned by electron-beam lithography. To avoid charge build-up in the resist during electron-beam lithography on the glass substrates, the resist (poly(methyl methacrylate), PMMA) is covered with a thin layer of a conducting polymer (ESPACER, provided by Showa Denko, Japan). After e-beam exposure, the conducting polymer is removed in deionized water, and the PMMA resist is developed in methyl isobutyl ketone (MIBK; 25 vol% in 2-propanol). The gate electrodes are 30 nm thick, thermally evaporated aluminum. The gate dielectric is a combination of a 3.6 nm thick layer of oxygen-plasma-grown aluminum oxide (AlO_x) and a 2.1 nm thick self-assembled monolayer (SAM) of octadecylphosphonic acid. The carbon nanotubes are randomly deposited from a liquid suspension. The source and drain contacts consist of a 0.3 nm thick titanium (to improve adhesion on the glass substrate) and 33 nm thick AuPd, both deposited by thermal evaporation.

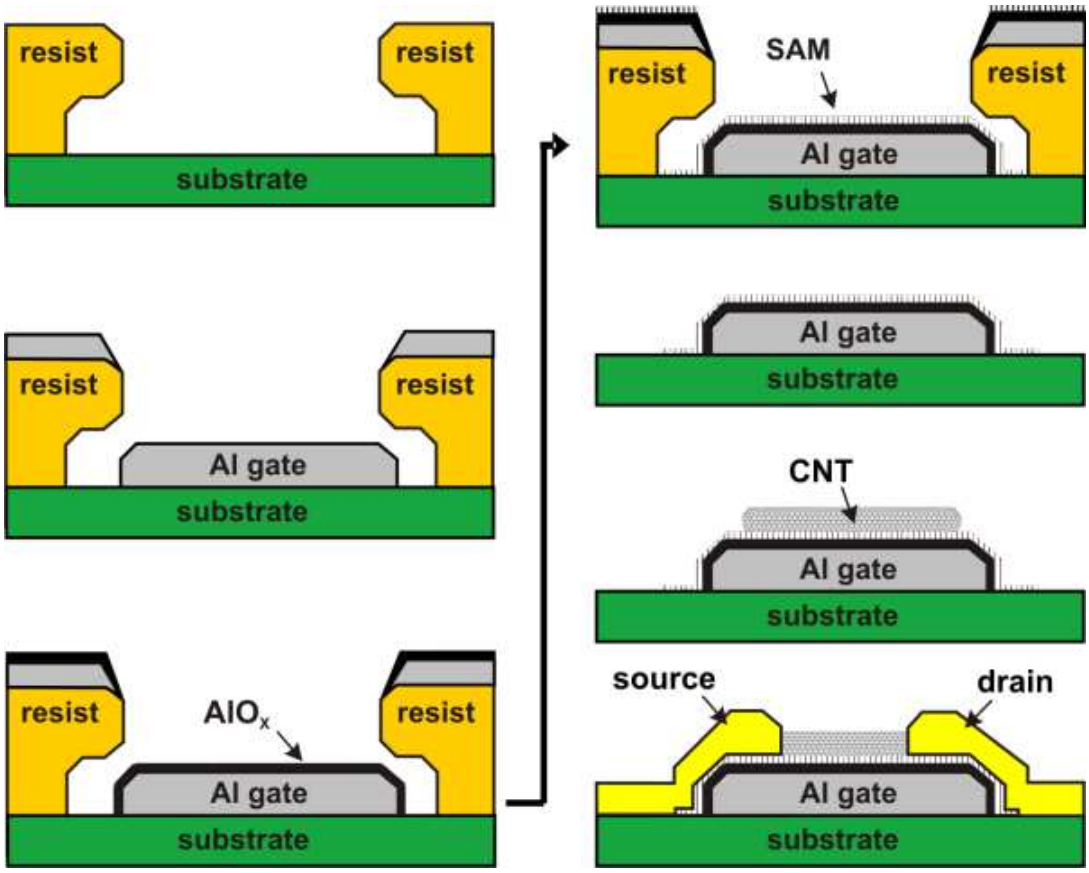

Figure S1. Process flow to fabricate individual-carbon-nanotube transistors.
1) pattern gate electrodes by electron-beam lithography;
2) deposit 30 nm thick aluminum gate electrodes;
3) create a 3.6 nm thick AlO_x layer by plasma oxidation as the first part of the gate dielectric;
4) allow an organic monolayer to self-assemble as the second part of the gate dielectric;
5) remove the resist and the aluminum outside of the gate areas by lift-off;
6) disperse the carbon nanotubes from a liquid suspension;
7) define Ti/AuPd source/drain contacts by e-beam lithography, evaporation and lift-off.

2. Statistics of the ON/OFF ratio of individual-carbon-nanotube transistors

Figure S2 shows statistics of 1131 transistors fabricated using carbon nanotubes produced either by the HiPCO or arc-discharge method or using sorted semiconducting carbon nanotubes (IsoNanotubes-S, provided by NanoIntegris).

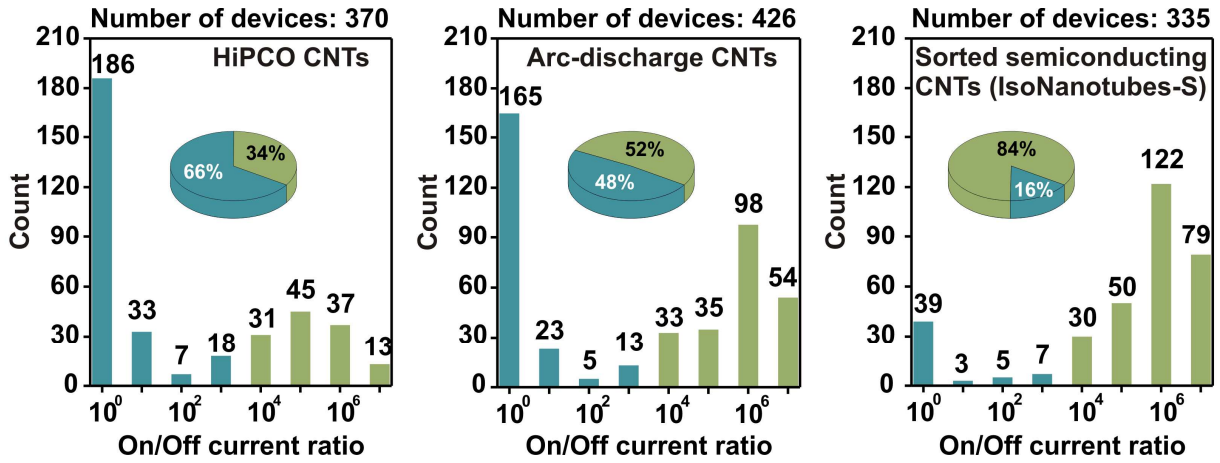

Figure S2. Statistics of the ON/OFF ratio measured at a drain-source voltage of -0.1 V of 370 transistors based on individual carbon nanotubes produced by the HiPCO method, 426 transistors based on individual carbon nanotubes produced by the arc-discharge method, and 335 transistors based on individual sorted semiconducting carbon nanotubes (IsoNanotubes-S, provided by NanoIntegris). The pie charts summarize the percentage of transistors with an ON/OFF ratio greater than 10^4 (green) and smaller than 10^4 (blue) measured at a drain-source voltage of -0.1 V.

3. Yield issues with metal meander load resistors

The resistance of the load resistors must be smaller than the OFF-state resistance of the transistors, but larger than the ON-state resistance of the transistors, i.e. between about 1 MΩ and 1 GΩ. To realize such resistors on glass substrates, we initially considered long, narrow, thin metal meanders manufactured by electron-beam lithography, vacuum deposition, and lift-off.

The resistance is determined by the resistivity of the metal (ρ), the length of the meander (L), the width of the meander (W) and the thickness of the metal (t):

$$R = \rho \cdot \frac{L}{W \cdot t}$$

Considering titanium (Ti), which has a bulk resistivity of 42 μΩcm, and assuming that meanders with a thickness of t = 15 nm and a width of W = 25 nm can be defined by electron-beam lithography, vacuum deposition and lift-off, this implies a length of about 1 cm to realize a resistance of 10 MΩ. In this case, the metal thickness (15 nm) is about half of the electron mean free path [S1], so that the resistance will be increased by surface scattering [S2] and the minimum required meander length will be somewhat smaller, perhaps a few millimeters. Meanders with such dimensions (t ~ 15 nm, W ~ 25 nm, L ~ 1 .. 10 mm) can indeed be defined by electron-beam lithography, but the process yield after metal deposition and lift-off is very poor. Figure S2 shows three SEM images highlighting some of the yield issues we have encountered in the fabrication of such extreme meanders, including missing lines, broken lines, and distorted lines.

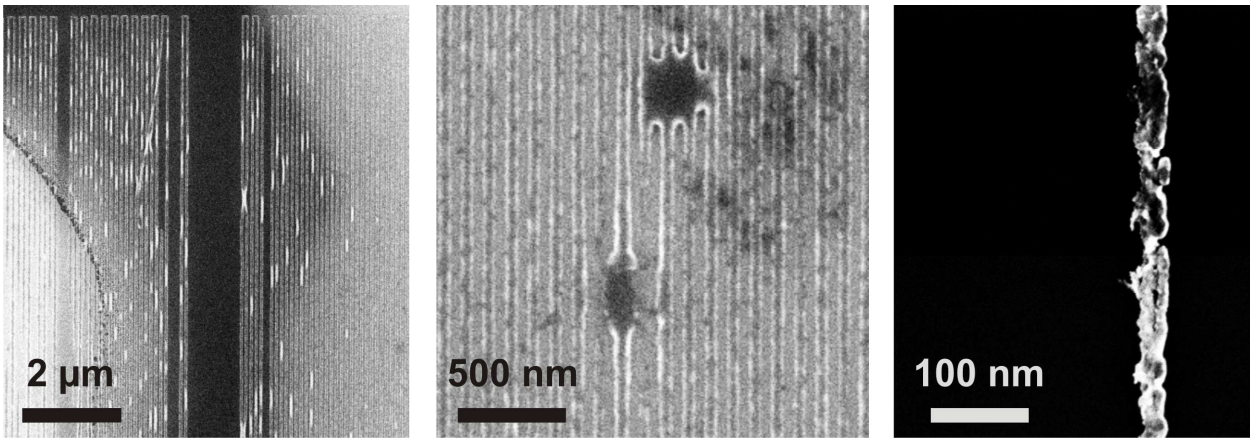

Figure S3. SEM images showing yield problems encountered during the fabrication of long, narrow, thin titanium meanders, which were initially considered as load resistors.
Left: missing lines; **center**: broken lines; **right**: distorted line.

Better yield is expected if the width W and/or the thickness t are increased, but this would substantially increase the foot print of the resistors and make the realization of useful integrated circuits impractical.

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4. Statistics of the resistance of thin-film carbon resistors

Figure S4 shows statistics of the measured resistances of 22 vacuum-evaporated thin-film carbon resistors with nominally identical (lithographically defined) width (30 µm) and length (75 µm), and nominally identical carbon film thickness (13 nm). The average resistance is 56 MΩ, and the standard deviation is only 4%. This confirms the good reproducibility of the fabrication process.

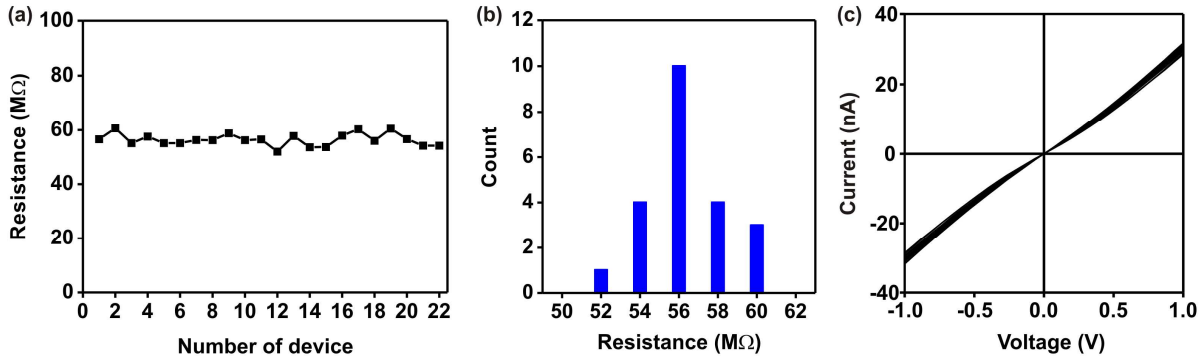

Figure S4. (a), (b) Statistics of the measured resistances of 22 thin-film carbon resistors. The average resistance is 56 MΩ, and the standard deviation is 4%.
(c) Current-voltage characteristics of all 22 resistors, confirming the good linearity of the resistance.

5. Thin-film carbon load resistors with reduced lateral dimensions

Figure S5 shows an optical microscopy image and the current-voltage characteristics of a thin-film carbon load resistor with a carbon film thickness of 15 nm and lithographically defined length and width of 2 µm.

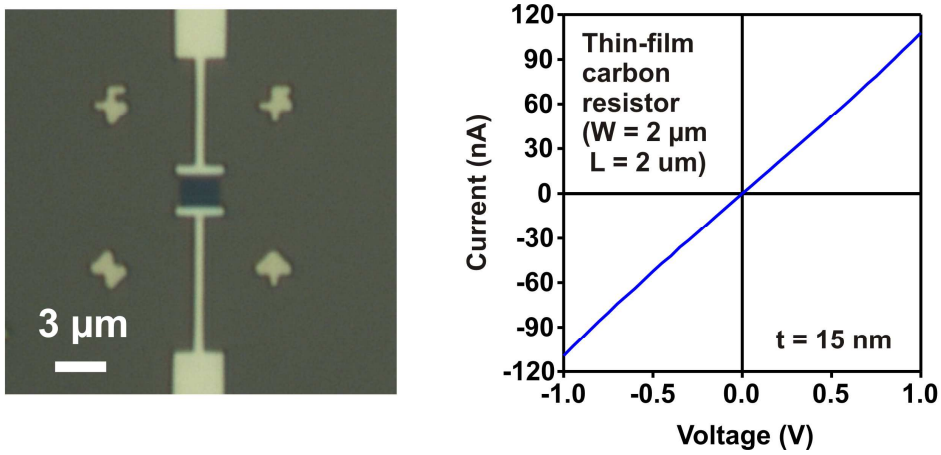

Figure S5. Optical microscopy image and the current-voltage characteristics of a thin-film carbon load resistor with a carbon film thickness of 15 nm and lithographically defined length and width of 2 µm.

6. Relationship between load resistance and inverter output characteristics

Figures S6-S9 show how the choice of the load resistance affects the shape of the inverter transfer curve, depending on the ratios between ON-state and OFF-state resistances of the transistor and load resistance, and depending on how pronounced the ambipolar behavior of the transistor is. For the simulation of the inverter transfer curves, the following equation was used: $V_{OUT} = R_{Transistor} \cdot V_{DD} / (R_{Transistor} + R_{Load})$.

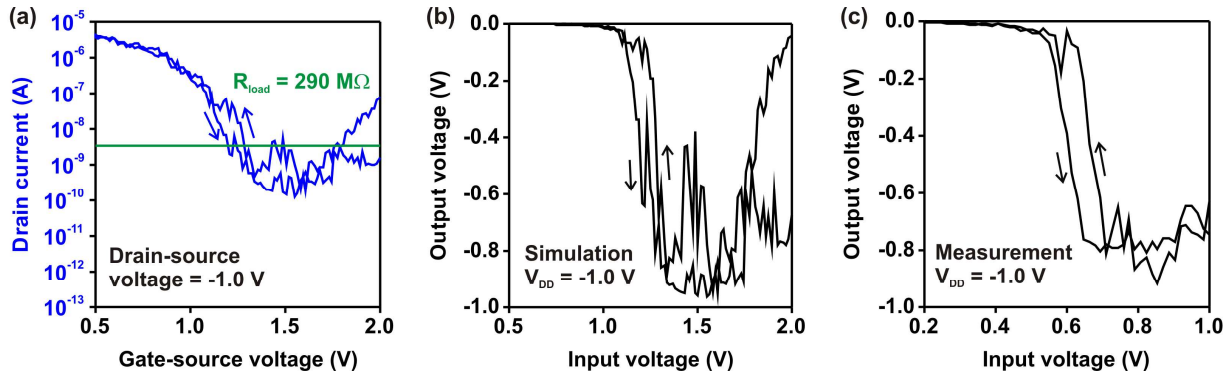

Figure S6. (a) Transfer characteristics of a transistor with an ON-state resistance of about 300 kΩ and an OFF-state resistance of about 1 GΩ that was integrated with a load resistance of 290 MΩ.
(b) Simulated inverter transfer characteristics.
(c) Measured inverter transfer characteristics.
The load resistance is much larger than the ON-state resistance of the transistor, so the LOW output signal is equal to ground potential (0 V), but at the same time the load resistance is very close to the OFF-state resistance of the transistor, so the HIGH output signal does not reach V_{DD} (-1.0 V), and the output swing is only about 0.8 V.

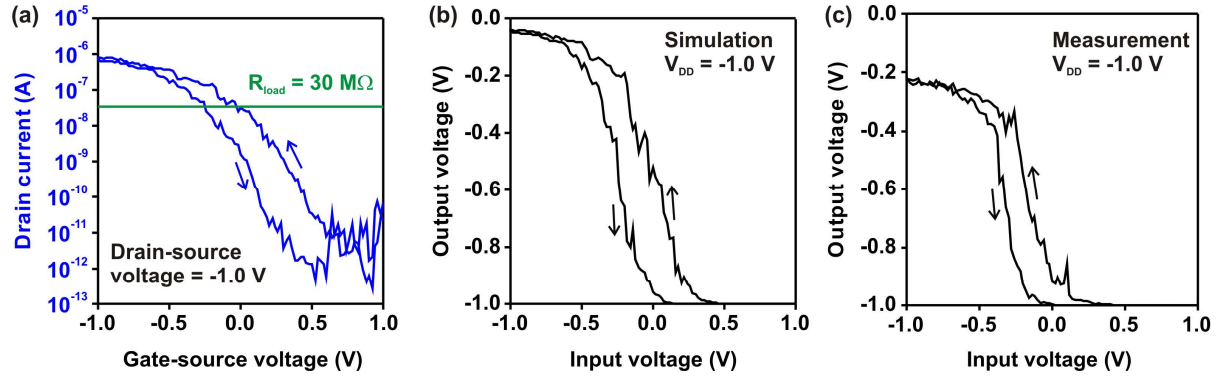

Figure S7. (a) Transfer characteristics of a transistor with an ON-state resistance of about 1 MΩ and an OFF-state resistance of about 100 GΩ that was integrated with a load resistance of 30 MΩ.
(b) Simulated inverter transfer characteristics.
(c) Measured inverter transfer characteristics.
The load resistance is much smaller than the OFF-state resistance of the transistor, so the HIGH output signal is equal to V_{DD} (-1.0 V), but at the same time the load resistance is quite close to the ON-state resistance of the transistor, so the LOW output signal does not reach ground potential (0 V), and the output swing is only about 0.8 V.

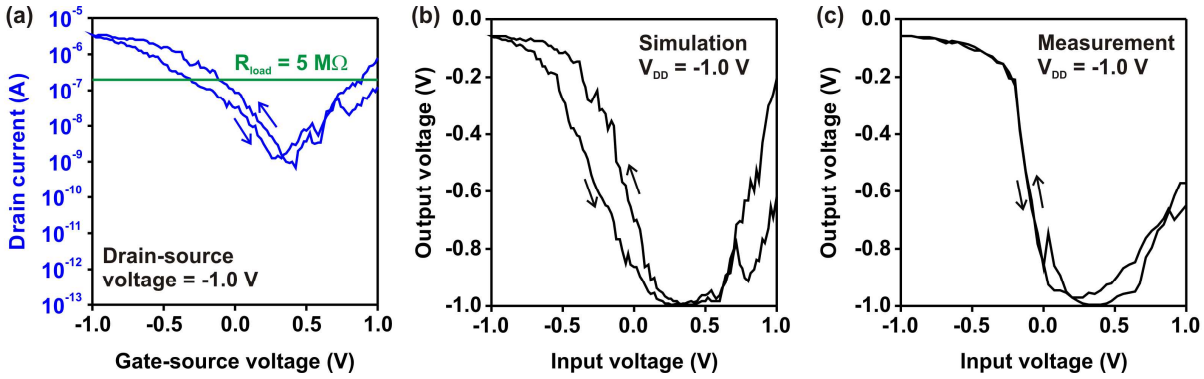

Figure S8. (a) Transfer characteristics of a carbon-nanotube transistor with a pronounced ambipolar behavior that results in a relatively small OFF-state resistance at large positive gate-source voltages (about 2 MΩ at V_{GS} = +1.0 V), despite the fact that the resistance of the transistor is fairly large (about 1 GΩ) at gate-source voltages around 0 V. This transistor was integrated with a thin-film carbon load resistor having a resistance of 5 MΩ.
(b) Simulated inverter transfer characteristics.
(c) Measured inverter transfer characteristics.
As a result of the pronounced ambipolar behavior of the carbon-nanotube transistor, the OFF-state resistance of the transistor drops below the load resistance at large positive gate-source voltages, so the HIGH output signal deviates significantly from V_{DD} (-1.0 V) at large positive gate-source voltages.

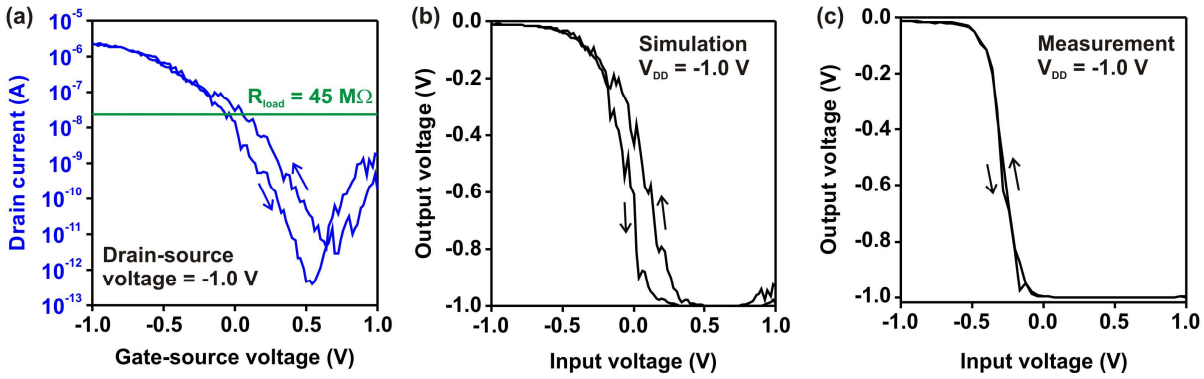

Figure S9. (a) Transfer characteristics of a carbon-nanotube transistor with a less pronounced ambipolar behavior that results in a relatively large OFF-state resistance (about 1 GΩ) even at large positive gate-source voltages. This transistor was integrated with a thin-film carbon load resistor having a resistance of 45 MΩ.
(b) Simulated inverter transfer characteristics.
(c) Measured inverter transfer characteristics.
The load resistance is much smaller than the OFF-state resistance and much larger than the ON-state resistance of the transistor over the entire range of gate-source voltages, so the LOW output signal reaches ground potential (0 V), the HIGH output signal reaches V_{DD} (-1.0 V), and the output swing is identical to V_{DD}.