Nanotechnology **21** (2010) 475207 (5pp) doi:10.1088/0957-4484/21/47/475207

Logic circuits based on individual semiconducting and metallic carbon-nanotube devices

Hyeyeon Ryu[1], Daniel Kälblein[1], R Thomas Weitz[2], Frederik Ante[1], Ute Zschieschang[1], Klaus Kern[1,3], Oliver G Schmidt[4,5] and Hagen Klauk[1]

[1] Max Planck Institute for Solid State Research, Heisenbergstraße 1, 70569 Stuttgart, Germany
[2] Department of Physics, Harvard University, Cambridge, MA 02138, USA
[3] Institut de Physique de la Matière Condensée, Ecole Polytechnique Fédérale de Lausanne, Switzerland
[4] Faculty of Electrical Engineering and Information Technology, Chemnitz University of Technology, 09107 Chemnitz, Germany
[5] Institute for Integrative Nanosciences, IFW Dresden, 01069 Dresden, Germany

E-mail: H.Ryu@fkf.mpg.de

Received 28 July 2010, in final form 12 September 2010
Published 29 October 2010
Online at stacks.iop.org/Nano/21/475207

Abstract
Nanoscale transistors employing an individual semiconducting carbon nanotube as the channel hold great potential for logic circuits with large integration densities that can be manufactured on glass or plastic substrates. Carbon nanotubes are usually produced as a mixture of semiconducting and metallic nanotubes. Since only semiconducting nanotubes yield transistors, the metallic nanotubes are typically not utilized. However, integrated circuits often require not only transistors, but also resistive load devices. Here we show that many of the metallic carbon nanotubes that are deposited on the substrate along with the semiconducting nanotubes can be conveniently utilized as load resistors with favorable characteristics for the design of integrated circuits. We also demonstrate the fabrication of arrays of transistors and resistors, each based on an individual semiconducting or metallic carbon nanotube, and their integration on glass substrates into logic circuits with switching frequencies of up to 500 kHz using a custom-designed metal interconnect layer.

S Online supplementary data available from stacks.iop.org/Nano/21/475207/mmedia

(Some figures in this article are in colour only in the electronic version)

Field-effect transistors in which the semiconducting channel is an individual carbon nanotube have demonstrated very promising static performance, including transconductance up to 30 μS [1–5], an ON/OFF ratio as large as 10^7 [6–11] and a subthreshold swing near the room-temperature limit of 60 mV/decade [1, 6, 7, 11–15]. The realization of integrated circuits based on individual nanotube transistors, however, remains a challenge. In terms of power consumption and immunity against electronic noise, complementary circuits have the most desirable characteristics [16]. However, complementary circuits require both p-channel and n-channel transistors, the latter of which are very difficult to realize with carbon nanotubes. In fact, only a few groups have successfully fabricated n-channel carbon-nanotube transistors. For example, Javey *et al* have converted p-channel nanotube transistors into n-channel nanotube transistors by chemical doping with potassium [3] or by heating to 400 °C in hydrogen [12]. However, both these effects vanish upon air exposure [3, 12], so that these n-channel transistors can only be operated in vacuum, not in air, which makes them less useful for practical applications. Javey *et al* have also produced n-channel carbon-nanotube transistors by applying a gate voltage of 40 V to p-channel nanotube transistors [17]. Unfortunately, this method can only be employed if the gate

dielectric is at least 50 nm thick, and it requires that the gate electrodes of all the transistors in the complementary circuit can be accessed individually. Chen *et al* have reported that n-channel transistor characteristics can be induced by employing a low-workfunction metal, such as aluminum, for the gate electrodes [18]. However, other authors have shown that aluminum gate electrodes do not necessarily produce n-channel transistor characteristics [11]. These observations suggest that the realization of n-channel carbon-nanotube transistors and complementary carbon-nanotube circuits with useful performances and stabilities is not at all straightforward.

Unlike complementary circuits, unipolar circuits require only one type of transistor, which greatly simplifies the realization of integrated circuits based on carbon-nanotube devices. Instead of transistors of the opposite carrier type, unipolar circuits employ 'passive' load devices. In unipolar circuits based on organic thin-film transistors, for example, passive load devices are often implemented using transistors (of the same carrier type as the drive transistors) that have their gate electrode connected to their source or drain contact [19, 20].

The simplest passive load device, however, is a resistor. In the first report of integrated circuits based on carbon-nanotube transistors, Bachtold *et al* employed commercially available, fully packaged bulk resistors and connected them to their carbon-nanotube transistors using coaxial cables [21]. The circuits had excellent static characteristics, but due to the large parasitic capacitances associated with the off-chip connections, the maximum frequency of these circuits was limited to less than 100 Hz.

To implement load resistors directly on the substrate along with the nanotube transistors for monolithic circuit integration, we have exploited the fact that carbon nanotubes are usually produced as a mixture of semiconducting and metallic nanotubes. When the nanotubes are dispersed on the substrate for device fabrication, a significant number of metallic nanotubes become available on the substrate. Since the electric current through a metallic nanotube cannot be modulated by a transverse electric field, metallic nanotubes are not useful for transistors and have therefore been ignored in all previous reports on integrated circuits based on carbon-nanotube transistors. However, many of the metallic carbon nanotubes can in fact be used to fabricate load resistors, and these can be integrated with transistors based on semiconducting nanotubes to design unipolar circuits with good static and dynamic performance.

To facilitate the fabrication, characterization and integration of a large number of nanotube devices, we first defined an array of probe pads on the substrate. Each device in the array has a narrow aluminum gate electrode that is connected to one of the three probe pads allocated for each device. The gate electrodes were covered with a thin gate dielectric composed of oxygen-plasma-grown AlO_x (3.6 nm thick) and an organic self-assembled monolayer (2.1 nm thick) [11, 22–25]. Single-walled carbon nanotubes produced by the HiPCO process and purchased from commercial sources were then deposited from a liquid suspension that was thoroughly sonicated and centrifuged prior to use. No attempts were made to separate the

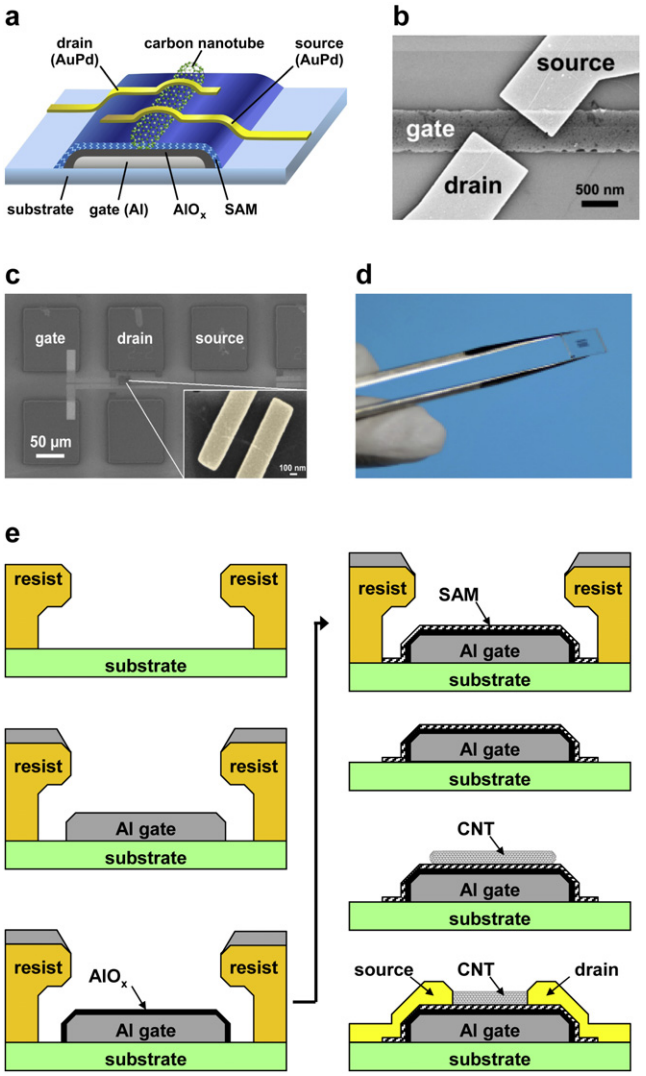

Figure 1. Device structure and fabrication process. (a) Schematic device structure. (b) SEM image of a carbon-nanotube device. The local gate electrode, the source and drain contacts, and the overlap area are clearly visible. (c) SEM image showing two carbon-nanotube devices within an array of 32 devices. (d) Photograph of a glass substrate with arrays of carbon-nanotube devices. (e) Fabrication process.

semiconducting and metallic nanotubes, or to obtain nanotubes longer than a few microns. One individual nanotube was identified on each of the patterned gates, and the AuPd contacts were defined by electron-beam lithography. Figure 1 shows the schematic device structure and several electron microscopy images; the fabrication process is described in more detail in the supplementary information (available at stacks.iop.org/Nano/21/475207/mmedia).

The current–voltage characteristics of all devices in the array were measured to identify those that were semiconducting and those that were metallic. All measurements were performed in air. With the HiPCO nanotubes utilized and the sonication/centrifugation protocol employed in this work, about 40% of the devices display a gate-bias-dependent current modulation (ON/OFF ratio $> 10^3$), indicating a semiconducting nanotube. Figure 2 shows the characteristics

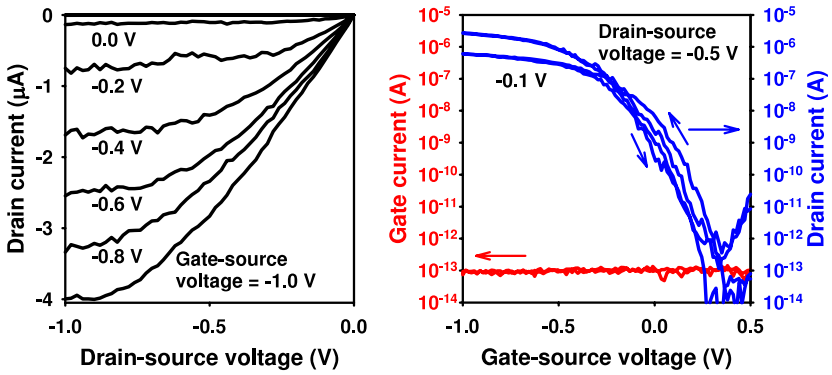

Figure 2. Electrical characteristics of carbon-nanotube transistors. Output and transfer characteristics of a field-effect transistor based on an individual semiconducting single-walled carbon nanotube on a glass substrate.

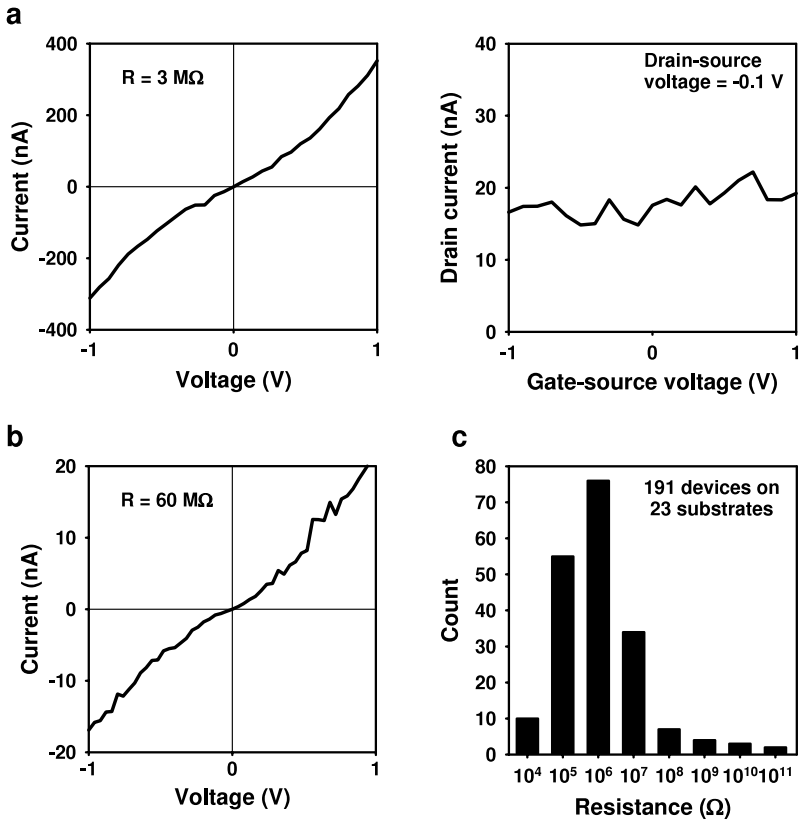

Figure 3. Electrical characteristics of resistive load devices. (a) Current–voltage characteristics of a load resistor based on a metallic carbon nanotube with a resistance of 3 MΩ. (b) Current–voltage characteristics of a load resistor based on a metallic carbon nanotube with a resistance of 60 MΩ. (c) Distribution of the resistance of 191 metallic nanotube devices on 23 substrates.

of a transistor based on a semiconducting carbon nanotube obtained by this method. The transistor has a transconductance of 4 μS, a subthreshold swing of 70 mV/decade, an ON/OFF ratio of 10^6 for $V_{DS} = -0.5$ V and an ON/OFF ratio of 2×10^3 for $V_{DS} = -1$ V.

The largest contribution to the gate capacitance of these transistors is the overlap between the source and drain contacts and the gate electrode. Depending on the gate width and the orientation of the nanotube on the gate, the overlap area can be as small as 0.2 μm^2 (see figure1(b)). For most of our transistors the overlap area is between 2 and 6 μm^2, so the gate capacitance is usually between 15 and 50 fF. For a transconductance of 4 μS this yields a theoretical upper limit for the cutoff frequency of about 10–40 MHz ($f_T \sim g_m/2\pi C_G$) and a theoretical lower limit for the signal delay of about 10–40 ns ($\tau = 1/2f_T$).

Figure 3 shows the current–voltage characteristics of two devices based on metallic carbon nanotubes. The current in these devices is not modulated by the gate–source voltage (indicating a metallic nanotube), but varies approximately linearly with the lateral drain–source voltage. Thus, these devices can in principle be used as load resistors. However, in order for the circuits to show the correct logic function, the resistance of the load devices must be larger than the

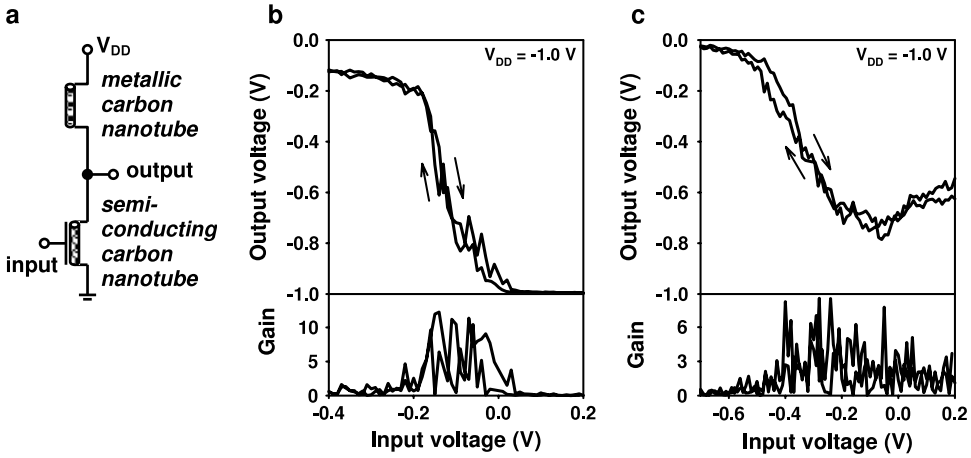

Figure 4. Static characteristics of carbon-nanotube inverters. (a) Circuit schematic of an inverter with a resistive load. (b) Static transfer characteristics of an integrated inverter on a glass substrate with a load resistance of about 10^7 Ω. (c) Static transfer characteristics of an integrated inverter on a glass substrate with a load resistance of about 10^8 Ω.

ON-state resistance of the transistors, but smaller than the OFF-state resistance of the transistors. The nanotube transistors we have selected to implement circuits have a maximum drain current of 2–5 μA at $V_{GS} = V_{DS} = -1$ V (ON-state resistance 200–500 kΩ) and a minimum drain current of 1–5 nA at $V_{GS} \sim 0$ and $V_{DS} = -1$ V (OFF-state resistance 200 MΩ–1 GΩ). Therefore, the load devices should have a resistance between about 1 and 100 MΩ. The resistance of a defect-free metallic single-walled carbon nanotube with perfect contacts is 6.25 kΩ [26], so obtaining a resistance above 1 MΩ may seem unrealistic. However, as figure 3(c) shows, most of our metallic nanotube devices in fact have resistances above 1 MΩ. The larger resistance is possibly due to defects induced by the sonication process and non-ideal metal contacts; similar observations have also been made for semiconducting nanotubes (see supplementary information, figure S1 available at stacks.iop.org/Nano/21/475207/mmedia).

The simplest logic circuit is the inverter, which consists of one transistor and one load resistor (see figure 4(a)). We have implemented inverters by connecting a drive transistor (based on a semiconducting nanotube with a transconductance between 1 and 4 μS) and a load resistor (based on a metallic nanotube with a resistance between 1 and 100 MΩ) using an interconnect layer fabricated by electron-beam lithography, metal deposition, and lift-off. This process of connecting individual devices into circuits with a custom-designed interconnect layer is somewhat similar to the process of individualizing commercially manufactured silicon gate array circuits.

Figures 4(b) and (c) show the transfer characteristics of two resistive load inverters. In figure 4(b) the transistor has an ON-state resistance of 500 kΩ and an OFF-state resistance of 1 GΩ, and the load resistance is 3 MΩ. In figure 4(c), the ON-state and OFF-state resistances are 500 kΩ and 200 MΩ, and the load resistance is 60 MΩ. Both inverters show a useful small-signal gain (∼5–10) for a supply voltage $V_{DD} = -1$ V. The output voltage at a high input voltage ($V_{IN} = -1$ V) is determined by the ratio between the ON-state resistance of the transistor and the load resistance, while the output voltage at a low input voltage ($V_{IN} = 0$ V) depends on the ratio between the OFF-state resistance and the load resistance (see supplementary information available at stacks.iop.org/Nano/21/475207/mmedia). The inverter in figure 4(b) has an output swing of 0.87 V, and the inverter in figure 4(c) has an output swing of 0.77 V. Note that the ratio between the output swing and supply voltage (87% for the inverter in figure 4(b)) is only slightly smaller than that of the complementary nanotube inverters reported by Javey *et al* (∼93%; [17]), which shows that the static characteristics of unipolar circuits with resistive load devices can be almost as good as those of complementary circuits.

Figure 5 shows the dynamic switching characteristics of the inverter from figure 4(b). An approximately rectangular output signal is obtained for a square-wave input signal with a frequency as high as about 500 kHz. Because the load resistors and the interconnects were realized directly on the glass substrate, rather than using coaxial cables, the maximum frequency is significantly higher compared with the carbon-nanotube circuits reported by Bachtold *et al* [21] and Javey *et al* [17]. The time constants of the output signal transitions in figure 5 are approximately 220 ns when the transistor switches from the ON-state to the OFF-state (in this case the output node is charged through the load resistor, so the time constant is limited by the load resistance) and about 120 ns when the transistor switches from the OFF-state to the ON-state (in this case the output node is discharged through the transistor and the time constant is limited by the intrinsic delay and the ON-state resistance of the transistor).

With a time constant of 120 ns our transistors are more than an order of magnitude slower than the nanotube transistors reported by Chen *et al* [18]. The reason for the high speed of their transistors is the small gate overlap and thus very small gate capacitance (∼1 fF) achievable with their high-resolution top-gate process. In our bottom-gate process, the source and drain contacts overlap the gate by as much as half the width of the gate, depending on the orientation of the nanotube on the gate, so the gate capacitance is usually much larger (15–50 fF), and this explains the longer signal delay. Nonetheless,

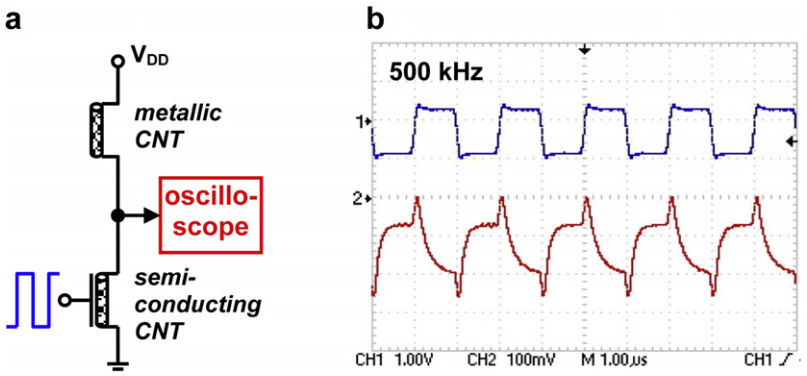

Figure 5. Dynamic characteristics of carbon-nanotube inverters. (a) Measurement schematic. (b) Output voltage response of a carbon-nanotube inverter on a glass substrate to a square-wave input signal with a frequency of 500 kHz.

this is the best dynamic performance reported so far for a unipolar circuit based on carbon-nanotube transistors, and the first report of a circuit in which both semiconducting and metallic carbon nanotubes are utilized.

In summary, we have reported on the fabrication and characterization of unipolar logic circuits that consist of field-effect transistors based on individual semiconducting single-walled carbon nanotubes and resistive load devices based on individual metallic single-walled carbon nanotubes. The devices and circuits have good static and dynamic characteristics, including a transconductance of up to 4 μS, a subthreshold swing as small as 70 mV/decade, an ON/OFF ratio greater than 10^3 (for a drain–source voltage of -1 V), and a switching time constant as short as 120 ns. The reproducibility of the performance characteristics of the transistors, resistors, and inverters is limited by the significant variations in the electrical parameters of the carbon nanotubes and in the quality of the electrical contacts made to the nanotubes. However, by utilizing some of the metallic nanotubes as load resistors, this process allows a larger portion of the nanotubes to be included in the circuit design, thus making better use of the nanotubes available on the substrate.

Acknowledgment

RTW acknowledges the support of the Alexander von Humboldt Foundation for a Feodor Lynen Research Fellowship.

References

[1] Javey A, Guo J, Farmer D B, Wang Q, Wang D W, Gordon R G, Lundstrom M and Dai H 2004 *Nano Lett.* **4** 447
[2] Javey A, Guo J, Farmer D B, Wang Q, Yenilmez E, Gordon R G, Lundstrom M and Dai H 2004 *Nano Lett.* **4** 1319
[3] Javey A, Tu R, Farmer D B, Guo J, Gordon R G and Dai H 2005 *Nano Lett.* **5** 345
[4] Zhang Z Y, Wang S, Ding L, Liang X L, Xu H L, Shen J, Chen Q, Cui R L, Li Y and Peng L M 2008 *Appl. Phys. Lett.* **92** 133117
[5] Zhang Z Y *et al* 2008 *Nano Lett.* **8** 3696
[6] Appenzeller J, Lin Y M, Knoch J and Avouris P 2004 *Phys. Rev. Lett.* **93** 196805
[7] Chen J, Klinke C, Afzali A and Avouris P 2005 *Appl. Phys. Lett.* **86** 123108
[8] Chen Z, Appenzeller J, Knoch J, Lin Y and Avouris P 2005 *Nano Lett.* **5** 1497
[9] Kim W, Javey A, Tu R, Cao J, Wang Q and Dai H 2005 *Appl. Phys. Lett.* **87** 173101
[10] Tulevski G, Hannon J, Afzali A, Chen Z, Avouris P and Kagan C R 2007 *J. Am. Chem. Soc.* **129** 11964
[11] Weitz R T, Zschieschang U, Forment-Aliaga A, Kälblein D, Burghard M, Kern K and Klauk H 2009 *Nano Lett.* **9** 1335
[12] Javey A, Kim H, Brink M, Wang Q, Ural A, Guo J, McIntyre P, McEuen P, Lundstrom M and Dai H 2002 *Nat. Mater.* **1** 241
[13] Lu Y, Bangsaruntip S, Wang X, Zhang L, Nishi Y and Dai H 2006 *J. Am. Chem. Soc.* **128** 3518
[14] Yang M H, Teo K B K, Gangloff L, Milne W I, Hasko D G, Robert Y and Legagneux P 2006 *Appl. Phys. Lett.* **88** 113507
[15] Weitz R T, Zschieschang U, Effenberger F, Klauk H, Burghard M and Kern K 2007 *Nano Lett.* **7** 22
[16] Bode D, Rolin C, Schols S, Debucquoy M, Steudel S, Gelinck G H, Genoe J and Heremans P 2010 *IEEE Trans. Electron Devices* **57** 201
[17] Javey A, Wang Q, Ural A, Li Y M and Dai H 2002 *Nano Lett.* **2** 929
[18] Chen Z H, Appenzeller J, Lin Y M, Sippel-Oakley J, Rinzler A G, Tang J Y, Wind S J, Solomon P M and Avouris P 2006 *Science* **311** 1735
[19] Gelinck G H *et al* 2004 *Nat. Mater.* **3** 106
[20] Myny K, Steudel S, Vicca P, Beenhakkers M J, van Aerle N A J M, Gelinck G H, Genoe J, Dehaene W and Heremans P 2009 *Solid-State Electron.* **53** 1220
[21] Bachtold A, Hadley P, Nakanishi T and Dekker C 2001 *Science* **294** 1317
[22] Klauk H, Zschieschang U, Pflaum J and Halik M 2007 *Nature* **445** 745
[23] Kang H, Han K K, Park J E and Lee H H 2007 *Org. Electron.* **8** 460
[24] Goetting L B, Deng T and Whitesides G M 1999 *Langmuir* **15** 1182
[25] Jedaa A, Burkhardt M, Zschieschang U, Klauk H, Habich D, Schmid G and Halik M 2009 *Org. Electron.* **10** 1442
[26] Anantram M P and Govindan T R 1998 *Phys. Rev.* B **58** 4882

Supplementary Information

Logic circuits based on individual semiconducting and metallic carbon nanotube devices

Hyeyeon Ryu, Daniel Kälblein, R. Thomas Weitz, Frederik Ante, Ute Zschieschang, Klaus Kern, Oliver G. Schmidt, and Hagen Klauk

Device Fabrication

First, an array of alignment markers and probe pads (pad area: 100×100 μm^2) is defined on the glass substrate by electron-beam lithography, metal evaporation, and lift-off. For each device in the array, a set of three adjacent probe pads is allocated for connecting the gate electrode, the source contact, and the drain contact of each device. Electron-beam lithography is then used to define the areas for the gate electrodes (and to connect each gate to one of the three probe pads), and 30 nm thick aluminum is deposited by thermal evaporation. The substrate is then briefly exposed to an oxygen plasma in order to increase the thickness of the native aluminum oxide layer from about 1.5 nm to about 3.6 nm [ref. 22,23]. The oxygen plasma also creates a large density of hydroxyl groups on the AlO_x surface, which is beneficial for the formation of a high-quality self-assembled monolayer (SAM) in the next process step. For this, the substrate is immersed in a 2-propanol solution of n-tetradecylphosphonic acid ($C_{14}H_{29}PO(OH)_2$; purchased from PolyCarbon Industries) for about one hour, then rinsed with 2-propanol and baked on a hotplate at 100 ºC to stabilize the phosphonic-acid monolayer assembled on the AlO_x surface [ref. 24]. The tetradecylphosphonic acid SAM has a thickness of 1.7 nm, so the total thickness of the AlO_x/SAM gate dielectric is 5.4 nm. The capacitance per unit area of the AlO_x/SAM gate dielectric is 800 nF/cm^2 [ref. 25]. During the oxygen-plasma treatment and the SAM formation, the areas outside the aluminum gate electrodes remain covered by electron-beam resist, so that the hydrophobic SAM is formed only on the gate electrodes, while the rest of the substrate is left hydrophilic [ref. 11]. The latter is useful, since a hydrophobic substrate would be more difficult to coat with resist for the following process step.

After formation of the AlO_x/SAM gate dielectric, the electron-beam resist is stripped in order to remove the aluminum outside of the gate areas. Single-walled carbon nanotubes grown by high-pressure conversion of carbon monoxide (HiPCO) and obtained from commercial sources are suspended in deionized water with 1 wt% sodium dodecyl-sulfate (SDS) as a surfactant. The suspension is thoroughly sonicated and centrifuged. The substrate is then immersed in the carbon-nanotube suspension which leads to a preferred deposition of carbon nanotubes on the hydrophobic, SAM-covered gate electrodes [ref. 11]. No attempts are made to separate semiconducting and metallic nanotubes, or to obtain nanotubes longer than a few microns. Using atomic force microscopy (AFM) or scanning electron microscopy (SEM), one individual carbon nanotube is identified on each of the patterned gate electrodes, and its position and orientation is registered with respect to the alignment markers. This step is necessary, since the location of the nanotubes on the gate electrodes after dispersion is essentially random. The substrate is again coated with resist, and areas for the source and drain contacts are opened by electron-beam lithography, so that one individual carbon nanotube is contacted on each gate electrode, and the source contact and the drain contact are connected to probe pads. Finally, a 30 nm thick layer of gold/palladium is deposited by thermal evaporation, and the resist is stripped to remove the metal outside of the contact regions. The channel length of the devices is usually around 400 nm.

Electrical Characterization

To identify those devices that are semiconducting and those that are metallic, the current-voltage characteristics of all devices in the array are recorded by measuring the drain current (I_D) as a function of gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}). The measurements are carried out using a semiconductor parameter analyzer (Agilent 4156C) in air at room temperature.

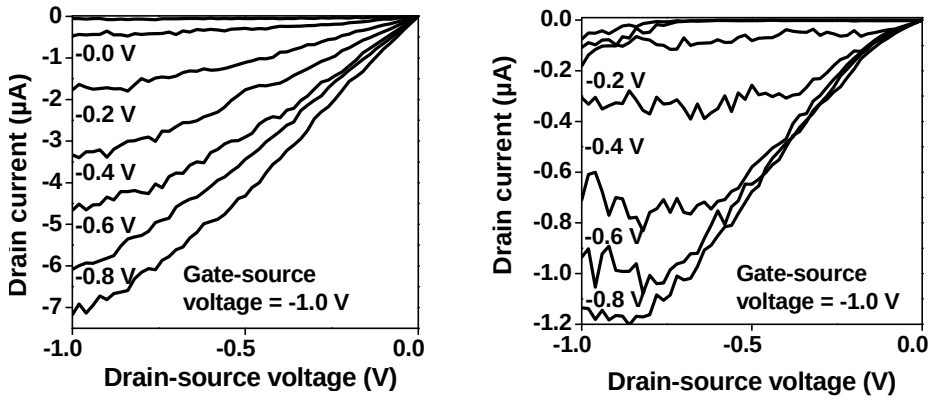

Figure S1. Left: Output characteristics of a semiconducting carbon-nanotube device with "good" characteristics (i.e., small contact resistance, large transconductance, low noise). Right: Output characteristics of a semiconducting carbon-nanotube device with "poor" characteristics (i.e., large contact resistance, reduced transconductance, large noise).

Circuit Fabrication

To fabricate circuits, transistors (based on a semiconducting carbon nanotube) and resistive load devices (based on a metallic carbon nanotube having a resistance in the range of 1 MΩ to 100 MΩ) are connected using a custom-designed on-chip interconnect layer. For this, the substrate is coated with resist, the interconnect layer is defined by electron-beam lithography and metal evaporation, and the resist (along with the metal outside of the desired interconnects) is removed.

Analytical Description of the Inverter Voltage Transfer Characteristics

The electric potential at the inverter's output node (V_{OUT}) is determined by the supply voltage (V_{DD}) and the ratio between the resistance of the drive transistor (R_{FET}) and that of the load (R_L):

$$\frac{V_{OUT}}{V_{DD}} = \frac{R_{FET}}{R_{FET} + R_L}$$

When the inverter's input voltage is high (V_{IN} = -1 V), the transistor is in the ON-state, so that the resistance of the transistor (R_{ON}) is much smaller than that of the load and the output is pulled towards the ground potential ($V_{OUT,LOW} \rightarrow 0$ V):

$$\frac{V_{OUT,LOW}}{V_{DD}} = \frac{R_{ON}}{R_{ON} + R_L}$$

When the input is low (V_{IN} = 0 V), the transistor is in the OFF-state, so that the resistance of the transistor (R_{OFF}) becomes much larger than that of the load and hence the output is pulled towards the supply potential ($V_{OUT,HIGH} \rightarrow V_{DD}$):

$$\frac{V_{OUT,HIGH}}{V_{DD}} = \frac{R_{OFF}}{R_{OFF} + R_L}$$

For logic-level conservation in a digital circuit it is desirable to make the difference between the high output voltage ($V_{OUT,HIGH}$) and the low output voltage ($V_{OUT,LOW}$), i.e., the inverter's output swing, as large as possible:

$$\frac{\Delta V_{OUT}}{V_{DD}} = V_{OUT,LOW} - V_{OUT,HIGH} = \frac{R_{ON}}{R_{ON} + R_L} - \frac{R_{OFF}}{R_{OFF} + R_L} \quad (1)$$

From Equation (1) it follows that the ON/OFF ratio of the transistor should be as large as possible and that for any combination of ON-state and OFF-state resistance of the transistor there is a optimum load resistance that will provide the maximum output swing. For example, if the transistor has an ON-state resistance of 500 kΩ and an OFF-state resistance of 1 GΩ (as in Figure 4b), the optimum load resistance is 20 MΩ and provides an output swing of 0.95 V. If the ON-state resistance is 500 kΩ and the OFF-state resistances 200 MΩ (as in Figure 4c), the maximum output swing that can be obtained is a little smaller (0.91 V) and is given for a load resistance of 10 MΩ.

During dynamic characterization the inverter output swing is somewhat smaller (about 0.2 V; see Figure 5). Chen et al. [ref. 18] made a similar observation for their complementary inverters, although in their case the reduction in output swing was more dramatic, from 0.8 V during static characterization to 140 μV during dynamic characterization [ref. 18].