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Charge-Based Compact Modeling of Capacitances in Staggered Multi-Finger OTFTs

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ABSTRACT This journal paper introduces a charge-based approach for the calculation of charges and capacitances in staggered organic thin-film transistors (OTFTs). Based on an already existing DC model, the charges are yielded in an analytical and compact form. A linear charge partitioning scheme is applied to ascribe charges to the drain/source side of the channel. The final equation is only dependent on geometrical parameters and the charge densities at the drain/source end of the channel. Furthermore, the fringing regions in fabricated devices are taken into account. The compact model is implemented in Verilog-A and the capacitances are compared to Sentaurus TCAD simulation results as well as measurement data. Additionally, simulation results for a differential amplifier are compared to measurements. The advantage of this model is its unique formulation covering all operation regimes.

INDEX TERMS Capacitance, charge-based model, compact modeling, OTFT.

I. INTRODUCTION

Over the last decades, the interest in organic semiconductors (OSCs) has increased because of the falling costs in the fabrication process. This makes them interesting for large-scale, low-cost applications [1]–[3]. In OTFTs, the crystalline semiconductor is replaced by an OSC like pentacene or DNTT and the source/drain (S/D) electrodes consist of a metal like gold. In contrast to crystalline semiconductors, OSCs do not have a band-structure. Each molecule is characterized by molecular orbitals. In some orbitals, electrons behave like bound electrons and in some other orbitals with higher energy, they can be characterized as quasi-mobile charges. The highest occupied molecular orbital (HOMO) is the highest orbital in which an electron behaves like a bound electron. In contrast, the lowest unoccupied molecular orbital (LUMO) is the lowest orbital in which an electron behaves like a quasi-mobile charge. The energy difference between HOMO and LUMO can be compared to the bandgap of a crystalline semiconductor. In OSC layers, charge carriers can hop between adjacent molecules, and this process can be described by a variable range hopping transport model [4]. Usually, the whole OSC is modeled by the band model with the HOMO-LUMO distance as bandgap [5], [6], whereby in comparison to a band-like transport due to hopping transport the effective mobility is quite low (up to $\approx 20\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ [7]). Furthermore, OTFTs are operated in the accumulation regime [8]. Whether an OTFT is an n- or p-type transistor, depends on the work function of the electrode metal of source and drain in comparison to the energy levels of the OSC. If the work function of the metal is close to the HOMO level, the OTFT acts like a p-type transistor and if the work function is close to the LUMO level, it acts like an n-type transistor [9].

In the channel of the transistor, there is a certain amount of charge carriers which varies in dependence of the applied terminal voltages. This causes capacitive charging currents which mainly influence the dynamic performance of the device. Hence, for circuit simulation, it is mandatory to have

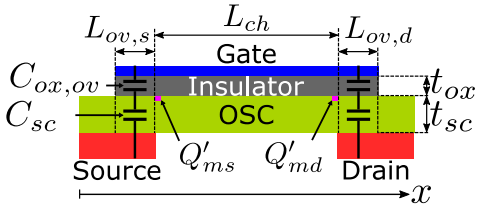

FIGURE 1. Sketch of the staggered OTFT showing structural parameters and as well capacitances and charge densities.

a compact model covering both the DC and the AC behavior. There already exists a variety of different capacitance and charge models for OTFTs [2], [3], [10]–[15]. However, these models distinguish between different operation regimes such as weak and strong accumulation and provide a transition between them. In this work, a completely charge-based model is proposed which covers every operation regime in one unique equation. The DC model presented in [6] serves as a basis for this work and will thus quickly be reviewed in the following section. The charge model is derived and the verification is presented. The OTFTs under investigation (see Fig. 1) are p-type devices. This journal paper is an extended version of the work presented in [16].

II. CHARGE-BASED DC MODEL

The DC model in [6] is a charge-based model, which means that the current is calculated based on the charge densities Q'_{ms} and Q'_{md} on the source and the drain end of the channel (see Fig. 1). These charge densities are calculated as follows:

$$Q'_{ms/d} = \frac{S}{\ln(10)} \cdot C'_{ox} \cdot \mathcal{L}\left\{\exp\left(\frac{V_{gs/d} - V_{T0}}{S/\ln(10)}\right)\right\}, \tag{1}$$

where $\mathcal{L}$ is the first branch of the Lambert W function, C'_{ox} is the capacitance of the gate dielectric per gate area, and the parameters S and V_{T0} are the inverse sub-threshold slope factor and the threshold voltage. The model takes into account the hopping transport by a field-dependent mobility [17]:

$$\mu = \kappa \cdot \left(\frac{Q'_{ms}}{C'_{ox}}\right)^{\beta}, \tag{2}$$

where $\kappa\,[\mathrm{cm^2V^{\beta-1}s^{-1}}]$ is a proportionality factor and β is the power-law factor. The Schottky barrier at the source/channel interface as well as Ohmic contact resistances are taken into account by modifying the effective mobility [18]:

$$\mu_{eff} = \frac{\mu}{1 + \mu \cdot \frac{W_{ch}}{L_{ch}} \cdot (R_c + R_{sb}) \cdot Q'_{ms}}, \tag{3}$$

where R_{sb} is the non-linear resistance of the Schottky barrier and R_c is the Ohmic part of the resistance. Finally, the drain current reads as follows:

$$I_{ds} = \mu_{eff} \cdot W_{ch} \cdot \left(\frac{k_B \cdot T}{q} \cdot \frac{Q'_{ms} - Q'_{md}}{L_{ch}} + \frac{Q'^2_{ms} - Q'^2_{md}}{2 \cdot L_{ch} \cdot C'_{ox}}\right) \times (1 + \lambda \cdot (V_{ds} - V_{dsat})), \tag{4}$$

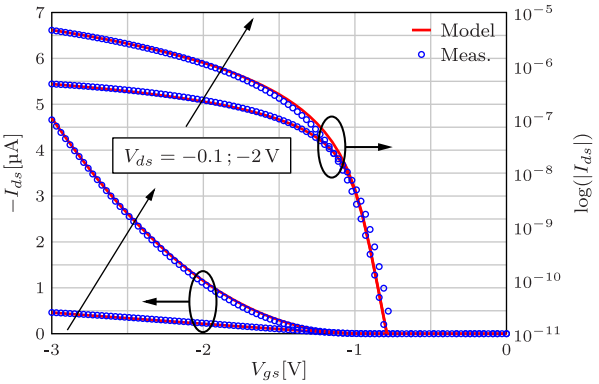

FIGURE 2. Transfer characteristics of a staggered OTFT. The compact model is compared to measurement data [12]. The parameters of the transistor are: $L_{ch} = 200\,\mu\mathrm{m}$, $W_{ch} = 400\,\mu\mathrm{m}$, $L_{ov,s} = L_{ov,d} = 10\,\mu\mathrm{m}$. The proportionality factor for the mobility in the compact model is set to $\kappa = 2.05\,\mathrm{cm^2V^{\beta-1}s^{-1}}$ and the power-law factor is set to $\beta = 0.03$. $V_{T0} = -0.94\,\mathrm{V}$ and $S = 70\,\mathrm{mV/dec}$. DNTT is used as OSC.

where L_{ch} and W_{ch} are the channel length and width, V_{dsat} is the saturation voltage, and λ is the channel length modulation factor. The saturation voltage is given by

$$V_{dsat} = \frac{1}{C'_{ox}} \cdot (Q'_{ms} - Q'_{md}). \tag{5}$$

At the interface between the S/D electrodes and the OSC there can occur Schottky barriers. This is the case if there is a mismatch of the work functions. The Schottky barrier at the source to OSC junction creates an additional, non-linear resistance (R_{sb}) for the injection of holes. This resistance lies in series with the Ohmic channel resistance (R_{ch}). This effect only plays a dominating role, if R_{sb} is high in comparison to R_{ch}. The longer the channel, the higher becomes R_{ch}. In this paper, the transistors are long-channel devices. Hence, the influence of the Shottky barrier is neglected in this work. As it can be seen in Fig. 2, the model reproduces the current transfer characteristics of a measured device well. In the ON state the relative error of the model compared to measurements is less than 10 % for $V_{ds} = -0.1\,\mathrm{V}$. This also holds true for $V_{ds} = -2\,\mathrm{V}$ if V_{gs} is less than $-1.5\,\mathrm{V}$. Close to the threshold voltage the error increases to 20 %. Below the threshold voltage, the transfer curves have a shift of $\approx 0.04\,\mathrm{V}$ regarding V_{gs}, which is due to hysteresis effects during measurements [19].

III. MODELING OF INTRINSIC CAPACITANCES

In this section, the derivation of the quasistatic charges and capacitances is presented. Quasistatic means that the charges and currents in any operation point are assumed to be the same as in a steady-state condition.

A. INTRINSIC CHARGES

The total number of charges in the channel is calculated by integrating the charge density per gate area over the channel length. The linear charge partitioning scheme according to Ward and Dutton [20] is applied to find expressions of the charges associated with drain and source. The procedure is

based on the approach presented in [21]. The three terminal charges of a transistor can be calculated as follows:

$$Q_c = W_{ch} \cdot \int_0^{L_{ch}} Q'_m(x)\, dx, \tag{6}$$

$$Q_d = W_{ch} \cdot \int_0^{L_{ch}} \frac{x}{L_{ch}} \cdot Q'_m(x)\, dx, \tag{7}$$

$$Q_s = W_{ch} \cdot \int_0^{L_{ch}} \left(1 - \frac{x}{L_{ch}}\right) \cdot Q'_m(x)\, dx, \tag{8}$$

with x as an arbitrary position along the channel and $Q'_m(x)$ as the density of quasi-mobile charges per gate area at position x. The difficulty is that the charge densities are only known at the source and drain end of the channel according to Eq. (1). In order to make use of this, the integration variable of the charge equations has to be changed from dx to dQ'_m. First, the drift-diffusion model is used:

$$dx = \left(\frac{W_{ch} \cdot \mu_{eff}}{I_{ds}} \cdot Q'_m(x)\right) dV, \tag{9}$$

where dV is a voltage drop in the direction of the channel and μ_{eff} is the effective mobility. Equation (9) contains both, the drift and the diffusion components and shows that the overall current is proportional to the gradient of the channel voltage which is a quasi-Fermi potential and not the electrostatic potential [22]. In [6], a differential which links a change of the gate voltage with respect to a point in the channel to the change in the density of accumulated charges is derived:

$$\frac{dQ'_m}{dV_g} = \frac{1}{\frac{\tilde{\alpha} \cdot V_{th}}{Q'_m(x)} + \frac{1}{C'_{ox}}}, \tag{10}$$

where $\tilde{\alpha} = {}^{S}/_{(\ln(10) \cdot V_{th})}$ is the slope degradation factor with V_{th} as the thermal voltage. dV_g is the change of the gate voltage with respect to an arbitrary point in the channel. The differential in Eq. (9), contains a voltage drop dV in the direction of the channel and not from the gate to the channel. However, the differentials can be linked together: When the channel potential increases by a certain amount, the voltage between gate and channel is decreased by the same amount. Thus, $dV = -dV_g$. Making use of this and rearranging Eq. (10), both differentials can be linked:

$$dx = -\left(\frac{W_{ch} \cdot \mu_{eff}}{I_{ds}} \cdot Q'_m(x)\right) \cdot \left(\frac{\tilde{\alpha} \cdot V_{th}}{Q'_m(x)} + \frac{1}{C'_{ox}}\right) \cdot dQ'_m. \tag{11}$$

In order to solve the charge equations for the drain and source sides of the channel (Eqs. (7) and (8)), an expression for x in dependence on $Q'_m(x)$ is calculated by integrating Eq. (11) over the charges from Q'_{ms} at the source end to $Q'_m(x)$:

$$x = +\frac{W_{ch} \cdot \mu_{eff}}{I_{ds}} \cdot \left[\tilde{\alpha} \cdot V_{th} \cdot Q'_m(x) + \frac{Q'^2_m(x)}{2 \cdot C'_{ox}}\right]_{Q'_m(x)}^{Q'_{ms}}. \tag{12}$$

Equation (6), Eq. (7) and Eq. (8) can now be solved analytically by integrating over $Q'_m(x)$ from Q'_{ms} to Q'_{md}. The solutions of these equations are given in Appendix A. As the equation for the source charge Q_s is very long, it is not presented there. The source charge can be calculated by making use of the fact that $Q_s = Q_c - Q_d$.

B. OVERLAP CHARGES

In staggered transistors, there exists an overlap between the source/drain electrodes and the gate, as it can be seen in Fig. 1. The overlaps are considered symmetric in this case, and thus $L_{ov,s} = L_{ov,d} = L_{ov}$. The overlapping electrodes are separated from each other by a staggering of the gate dielectric and the OSC. This can be regarded as a series connection of two capacitors which can both be calculated by the plate capacitor formula:

$$C_{sc} = \frac{\varepsilon_{sc}}{t_{sc}} \cdot L_{ov} \cdot W_{ch}, \tag{13}$$

$$C_{ox,ov} = C'_{ox} \cdot L_{ov} \cdot W_{ch} = \frac{\varepsilon_{ox}}{t_{ox}} \cdot L_{ov} \cdot W_{ch}. \tag{14}$$

If the transistor is biased in weak accumulation, the OSC behaves like an insulator with a certain dielectric constant ε_{sc} and the voltage drop over the series connection of capacitors causes a certain amount of charge to be stored. However, if the transistor is biased in strong accumulation, there are additional charges accumulated in the OSC at the insulator interface and the OSC no longer behaves like an insulator. Furthermore, the surface potential is nearly constant and does not follow the gate-source voltage [11]. Hence, it leads to wrong results if it is assumed that the voltage V_{gs} or V_{gd} drops over the series connection of C_{sc} and $C_{ox,ov}$ at the source/drain end of the channel. In order to overcome this, the voltage drop is limited to

$$V'_{gs} = V_{gs} - \frac{Q'_{ms}}{C'_{ox}} \tag{15}$$

for the source side. V'_{gs} follows V_{gs} for small values of V_{gs} and saturates to V_{T0} in the strong accumulation. Now, another assumption is made: The charge density Q'_{ms} at the source end of the channel is supposed to be present in the whole overlap region and thus, the total amount of charges stored in the overlap regions can be calculated as the sum of the charges in the series connection and these accumulation charges:

$$\begin{aligned} Q_{s,ov} &= \frac{C_{sc} \cdot C_{ox,ov}}{C_{sc} + C_{ox,ov}} \cdot V'_{gs} + Q'_{ms} \cdot L_{ov} \cdot W_{ch} \\ &= \frac{C_{ox,ov}}{C_{sc} + C_{ox,ov}} \cdot \left(C_{sc} \cdot V_{gs} + Q'_{ms} \cdot L_{ov} \cdot W_{ch}\right). \end{aligned} \tag{16}$$

A similar consideration holds true for the drain end of the channel which leads to

$$Q_{d,ov} = \frac{C_{ox,ov}}{C_{sc} + C_{ox,ov}} \cdot \left(C_{sc} \cdot V_{gd} + Q'_{md} \cdot L_{ov} \cdot W_{ch}\right). \tag{17}$$

The overlap charges are added to the intrinsic charges.

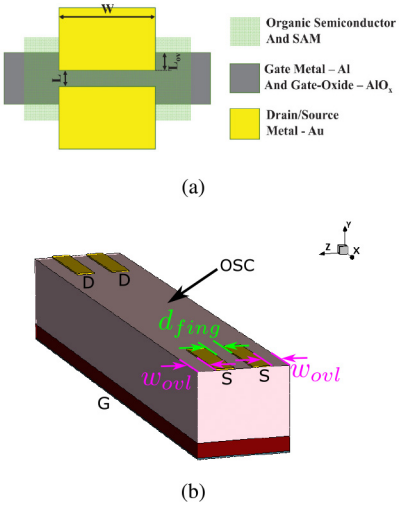

FIGURE 3. **(a) Layout of a fabricated single-finger OTFT [25]. The OTFT layers, which are aluminum gate, DNNT (OSC), and gold S/D contacts are evaporated through silicon stencil masks in the vacuum. After the aluminum deposition, the aluminum is oxidized and afterwards, a self-assembled monolayer (SAM) of n-tetradecylphosphonic acid is formed. Together, the aluminum oxide and the SAM form a hybrid dielectric [12]. (b) Sketch of a multi-finger OTFT.**

C. CAPACITANCES

The capacitances of the transistor are defined as the change of the charge at terminal i with respect to the change of the voltage at terminal j [23]:

$$C_{ij} = \begin{cases} -\frac{\delta Q_i}{\delta V_j} & i \neq j \quad i,j = g,s,d \\ \frac{\delta Q_i}{\delta V_j}, & i = j. \end{cases} \tag{18}$$

The equations for the capacitances can be obtained by differentiating the charge expressions with respect to the terminal voltages. However, this is not necessary, because in the Verilog-A implementation, only the charges at each operation point are needed.

IV. FRINGING REGIONS

A. GENERAL OBSERVATIONS

In many OTFTs reported in literature, the OSC layer extends beyond the channel and the gate-to-contact overlap regions [24], [25] [see Fig. 3(a)]. For stability reasons of the evaporation masks, there is a limitation for the channel width that can be fabricated. If a greater channel width is desired, the OTFT is fabricated as a multi-finger device. In Fig. 3(b) a structure of a double-finger device is shown. In both structures shown in Fig. 3, there are regions where the OSC layer overlaps the gate electrode (separated by the gate dielectric) but which are not part of the overlap between source/drain and the gate or the channel region. These regions are called fringing regions. In Fig. 4(a) the length of the fringing regions is denoted as w_{ovl}. Sentaurus TCAD simulations have shown that the fringing regions, however, have a huge influence on both the DC and the AC characteristics. The reason is that charges are accumulated everywhere where the OSC overlaps with the gate stack, which can be seen in Fig. 4(b). This opens additional paths

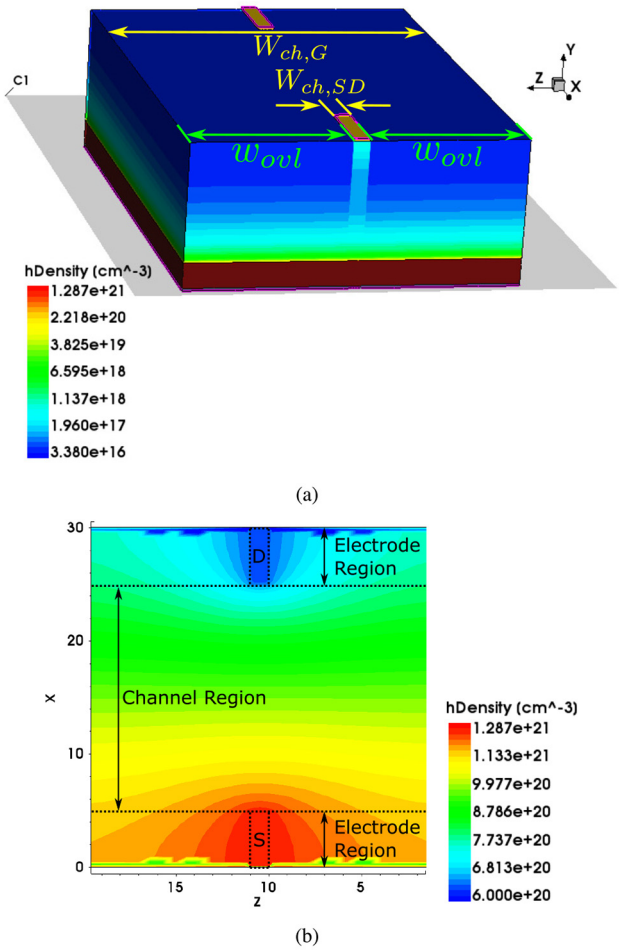

FIGURE 4. **TCAD Sentaurus simulation of a single-finger OTFT with fringing regions. $V_{gs} = -4$ V, $V_{ds} = -1$ V. (a) shows a 3D sketch of the transistor (not to scale) and (b) shows the cutplane in the OSC directly at the OSC/dielectric interface which is denoted as C1 in (a). The color encodes the density of accumulated holes. The scales are different in both plots. In (b) it can be seen that in the channel region the density of holes is only dependent on the x-position and nearly independent of the z-position. Hence, a current can flow at each z-position and the charges contribute to the total charges in the device. In the electrode region the charge density is dependent on the z-position to a certain degree.**

for the current. Furthermore, the amount of accumulated charge in fringing regions has to be taken into account for the charge calculations. The observations in Fig. 4 show that modeling the fringing regions is essential for the correct device characterization. As the fringing regions influence both, the DC and the AC model, changes to both models have to be done.

B. ENHANCEMENT OF THE DC MODEL

The fringing regions open additional paths for the current which can be denoted as a current spreading. However, the current density in the fringing regions will be lower than in the channel, especially in regions far away from the channel center due to a weaker electric field. The reason is that the path a charge carrier travels is longer if it takes a detour through the fringing region instead of flowing directly from

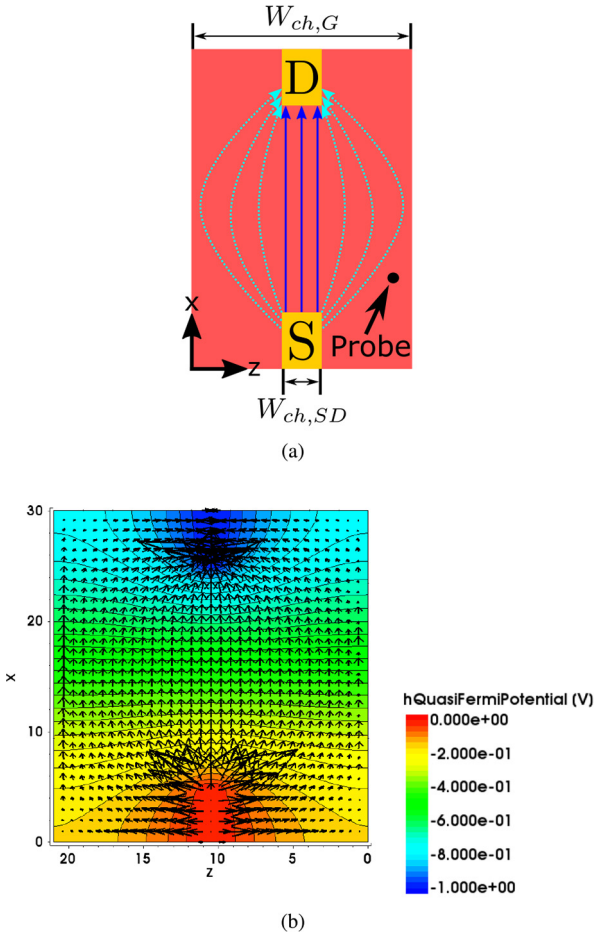

FIGURE 5. **(a) Schematic of the current flowing in a planar OTFT. If there are fringing regions, the current not only flows directly from source to drain (solid arrows), but also in the fringing regions (dotted arrows). As the paths through the fringing regions are longer, the current density in the fringing regions is lower than in the center of the channel. At the probe point, the current density is assumed to be low. However, the density of accumulated quasi-mobile charges is assumed to be the same as in the center of the channel. (b) Quasi-Fermi potential for holes in a cutplane at the OSC/dielectric interface of the same TCAD simulation as in Fig. 4. The arrows in (b) show the vector data for the hole current density in the plane. The current flows between regions with different Fermi potentials, as predicted.**

the source to the drain electrode. The current spreading is schematically shown in Fig. 5. The behavior is modeled as a change in the effective channel width for the current. Hence, the drain current presented in Eq. (4) is modified. It is assumed that the effective channel width lies between $W_{ch,SD}$ and $W_{ch,G}$. Thereby, as can be seen in Fig. 4(a) and Fig. 5, $W_{ch,SD}$ is the channel width as seen from the S/D electrodes and $W_{ch,G}$ is the width including the overlaps w_{ovl}. Furthermore, the sum of the distances between the fingers (in case of a multi-finger device) is included in $W_{ch,G}$. The following function for the effective gate width is defined:

$$W_{ch,eff} = \delta_{fit} \cdot \left(W_{ch,G} - W_{ch,SD}\right) + W_{ch,SD}, \tag{19}$$

where $\delta_{fit} \in [0, 1]$ is a fitting parameter and $W_{ch,G}$ is defined as

$$W_{ch,G} = N_{fing} \cdot W_{ch,SD} + 2 \cdot w_{ovl} + \left(N_{fing} - 1\right) \cdot d_{fing}, \tag{20}$$

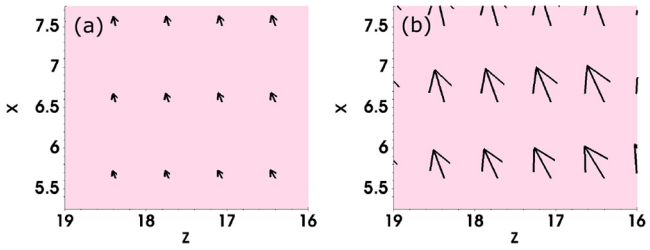

FIGURE 6. **Electric field vectors in a small cutplane close to the OSC/insulator interface of the same transistor as in Fig. 4 for (a) $V_{gs} = -1.333$ V and (b) $V_{gs} = -4$ V. The drain voltage is $V_{ds} = -1$ V in (a) and (b). For both gate voltages, the arrows point in the same directions, but their lengths are different. This shows that a higher gate bias does not influence the orientation of the field lines.**

with N_{fing} as the number of fingers and d_{fing} as the distance between two fingers [see Fig. 3(b)]. The fitting parameter δ_{fit} might be bias-dependent. However, as we show in Fig. 6, a change in the gate voltage V_{gs} does not change the directions of the field vectors, but only their lengths. Hence, the current spreading is assumed to be bias-independent. Furthermore, the electric field in the OSC close to the insulator interface is independent of the OSC thickness t_{sc} and the relative dielectric permittivity of the OSC. Please note that δ_{fit} is only used to capture the effect that the current spreads over a certain region beyond the channel center. Later, we will show that in the charge equations δ_{fit} does not play a role. This is because the density of accumulation charges at a specific point does not depend on the current density at this point. The effective channel width is now used in the current equation which then reads as follows:

$$I_{ds} = \mu_{eff} \cdot W_{ch,eff} \cdot \left(\frac{k_B \cdot T}{q} \cdot \frac{Q'_{ms} - Q'_{md}}{L_{ch}} + \frac{Q'^2_{ms} - Q'^2_{md}}{2 \cdot L_{ch} \cdot C'_{ox}} \right) \times \left(1 + \lambda \cdot (V_{ds} - V_{dsat})\right). \tag{21}$$

C. ENHANCEMENT OF THE CHARGE MODEL

C.1. INTRINSIC CHARGES

The intrinsic charges are as well affected by the fringing regions. First, the three integrals for the total charges are modified:

$$Q_c = W_{ch,G} \cdot \int_0^{L_{ch}} Q'_m(x)\, dx, \tag{22}$$

$$Q_d = W_{ch,G} \cdot \int_0^{L_{ch}} \frac{x}{L_{ch}} \cdot Q'_m(x)\, dx, \tag{23}$$

$$Q_s = W_{ch,G} \cdot \int_0^{L_{ch}} \left(1 - \frac{x}{L_{ch}}\right) \cdot Q'_m(x)\, dx. \tag{24}$$

In these equations, the geometric gate width $W_{ch,G}$ is used and not the effective gate width. The reason for this is that the charges are accumulated all along the channel width, as well in the regions where the current density due to the current spreading is low. Looking at Fig. 5, this can be seen. It is assumed that at the probe point the density of accumulated charges is the same as at any other z-position.

This can be verified by observing Fig. 4(b): In the channel region, the contour lines are nearly horizontal which means that the density of accumulated holes is equal in the channel center and in the fringing regions. TCAD simulations have shown that this is also true for very long fringing lengths w_{ovl} in the range of several tens of micrometers.

In the next step, the differential shown in Eq. (9) has to be adapted. As due to current spreading effects the current is dependent on the effective gate width $W_{ch,eff}$ (given by Eq. (19)), this differential is:

$$dx = \left(\frac{W_{ch,eff} \cdot \mu_{eff}}{I_{ds}} \cdot Q'_m(x) \right) dV \tag{25}$$

and together with Eq. (10), this becomes

$$dx = -\left(\frac{W_{ch,eff} \cdot \mu_{eff}}{I_{ds}} \cdot Q'_m(x) \right) \cdot \left(\frac{\tilde{\alpha} \cdot V_{th}}{Q'_m(x)} + \frac{1}{C'_{ox}} \right) \cdot dQ'_m. \tag{26}$$

The variable x is then expressed as

$$x = +\frac{W_{ch,eff} \cdot \mu_{eff}}{I_{ds}} \cdot \left[\tilde{\alpha} \cdot V_{th} \cdot Q'_m(x) + \frac{Q'^2_m(x)}{2 \cdot C'_{ox}} \right]_{Q'_m(x)}^{Q'_{ms}}. \tag{27}$$

After these minor modifications to the equations, the integrals Eq. (22), Eq. (23) and Eq. (24) can be solved again. The solution of them is given in Appendix B. Looking at the results in Appendix B, one interesting fact becomes visible: The effective channel width $W_{ch,eff}$ and the drain current I_{ds} always appear on opposite sides of the fraction with the same exponent. As I_{ds} is linearly dependent on $W_{ch,eff}$, this means that $W_{ch,eff}$ is practically canceled in the charge equations. Or, in other words: The total charges are independent of the effective channel width $W_{ch,eff}$ and hence independent of the factor δ_{fit}. However, the fringing regions influence the total charges through the gate width $W_{ch,G}$ which includes the fringing length w_{ovl} and the distances between the fingers d_{fing}.

C.2. OVERLAP CHARGES

The charges in the overlap regions also have to be adapted to the new model. The staggered structure of C_{sc} and $C_{ox,ov}$ (see Fig. 1) depends on the dimensions of the S/D electrodes. Hence, in these equations, the electrode width $W_{ch,SD}$ is used:

$$C_{sc} = \frac{\varepsilon_{sc}}{t_{sc}} \cdot L_{ov} \cdot W_{ch,SD}, \tag{28}$$

$$C_{ox,ov} = C'_{ox} \cdot L_{ov} \cdot W_{ch,SD} = \frac{\varepsilon_{ox}}{t_{ox}} \cdot L_{ov} \cdot W_{ch,SD}. \tag{29}$$

These formulas are only valid for ideal plate capacitors, where the electric field is assumed to be homogeneous in the capacitor and zero outside the capacitor. This assumption is also kept here, since the additional field lines beyond the S/D electrodes are assumed to have a small influence. This is because the layer thickness is assumed to be much less than the lateral dimensions of the S/D electrodes. As shown in Fig. 4(b), the density of accumulation charges in the OSC is in the same order of magnitude in the whole overlap region for each electrode, although it varies a little bit with the z-position. For simplification purposes, the charge densities are assumed equal in the whole overlap regions. Thus, Eq. (16) and Eq. (17) are modified as follows:

$$\begin{aligned} Q_{s,ov} &= \frac{C_{sc} \cdot C_{ox,ov}}{C_{sc} + C_{ox,ov}} \cdot V'_{gs} + Q'_{ms} \cdot L_{ov} \cdot W_{ch,G} \\ &= \frac{C_{ox,ov}}{C_{sc} + C_{ox,ov}} \cdot \left(C_{sc} \cdot V_{gs} + Q'_{ms} \cdot L_{ov} \cdot W_{ch,G} \right), \end{aligned} \tag{30}$$

$$Q_{d,ov} = \frac{C_{ox,ov}}{C_{sc} + C_{ox,ov}} \cdot \left(C_{sc} \cdot V_{gd} + Q'_{md} \cdot L_{ov} \cdot W_{ch,G} \right). \tag{31}$$

V. MODEL VERIFICATION

In this section, the model is verified using TCAD Sentaurus [26] 2D and 3D simulations, capacitance measurements and measurements on a differential amplifier.

A. TCAD

A.1. 2D SIMULATION

A 2D simulation of OTFTs has been conducted with TCAD Sentaurus. The OSC is simulated as a conventional semiconductor with some changes in order to reproduce the physical effects that occur in OSCs. The mobility for holes is set to a very low value and the band diagram is adapted so that the valence band has the energy of the HOMO level of the OSC and the conduction band has the energy of the LUMO level. The TCAD simulations yield the internodal capacitances of the transistor. As the compact model has total charges as outputs and not capacitances, the charges are numerically derived with respect to the terminal voltages. The TCAD simulations are conducted for a very low frequency of 0.01 Hz in order to simulate only quasistatic effects. As it can be seen in Fig. 7, the compact model reproduces the capacitances well, especially at the plot over V_{ds}. In OTFTs, the overlap lengths of the S/D electrodes are often long in comparison to the channel length. Hence, a remarkable amount of charge is stored in the overlap regions. Figure 8 shows the capacitances for a transistor with a shorter channel and comparatively long S/D overlaps. As it can be seen, the model fits well, especially for the OFF-State ($V_{gs} = 0\,\mathrm{V}$) and the very linear operation regime ($V_{gs} = -4\,\mathrm{V}$). This shows that the modeling of the overlap charges fits the simulation data well.

A.2. 3D SIMULATION

For the verification of the fringing model, a 3D TCAD simulation has been conducted. A single-finger OTFT is simulated with different fringing lengths w_{ovl} in order to see the influence on the DC currents and the capacitances. The parameter δ_{fit} which has been introduced in the modeling section has to be determined for each fringing length. Therefore, each simulated current transfer curve is compared to the compact model and the parameter δ_{fit} is manually determined so that the model and the simulation curves fit. Figure 9 shows the normalized drain current of a single-finger OTFT with different fringing lengths w_{ovl} and the extracted value

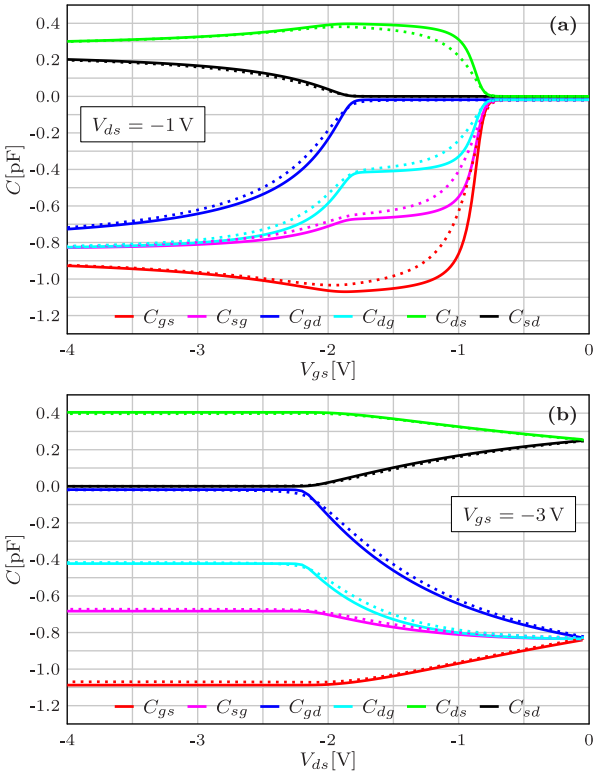

FIGURE 7. Capacitances of the compact model (solid lines) of a staggered device in comparison with a 2D TCAD simulation (dashed lines) for $f = 0.01\,\mathrm{Hz}$. In (a), the capacitances are plotted over V_{gs} for $V_{ds} = -1\,\mathrm{V}$. In (b), the capacitances are plotted over V_{ds} for $V_{gs} = -3\,\mathrm{V}$. The parameters of the transistor are: $V_{T0} = -0.86\,\mathrm{V}$, $L_{ch} = 200\,\mu\mathrm{m}$, $W_{ch} = 1\,\mu\mathrm{m}$, $L_{ov,s} = L_{ov,d} = 10\,\mu\mathrm{m}$, $S = 60\,\mathrm{mV/dec}$. The mobility for holes in TCAD is set to $\mu_p = 1\,\mathrm{cm^2V^{-1}s^{-1}}$ and the mobility in the compact model is set to a constant value of $\kappa = 0.96\,\mathrm{cm^2V^{-1}s^{-1}}$ with $\beta = 0$. In a 2D simulation, no fringing regions are present and hence, the simple current and charge equations are used.

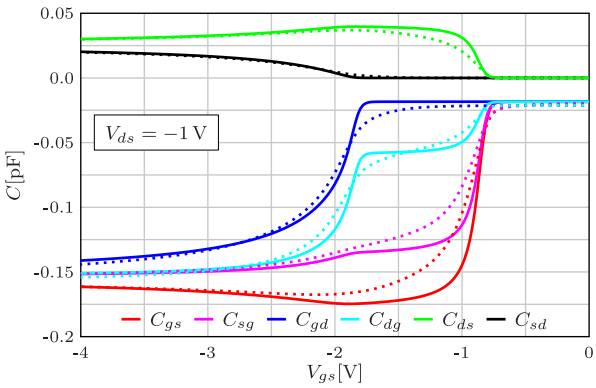

FIGURE 8. Capacitances of the compact model (solid lines) of a staggered device in comparison with a 2D TCAD simulation (dashed lines) for $f = 0.01\,\mathrm{Hz}$. The parameters of the transistor are similar to that in Fig. 7, but the channel length is in this case $L_{ch} = 20\,\mu\mathrm{m}$ and $\lambda = 0.031\,\mathrm{V^{-1}}$.

for δ_{fit}. The drain current is normalized with respect to the value at $w_{ovl} = 0\,\mu\mathrm{m}$ for each drain voltage. It has proven out that the extracted value for δ_{fit} is the same for both drain voltages. This shows that δ_{fit} can be assumed to be independent on V_{ds}. The drain current values reveal that if the

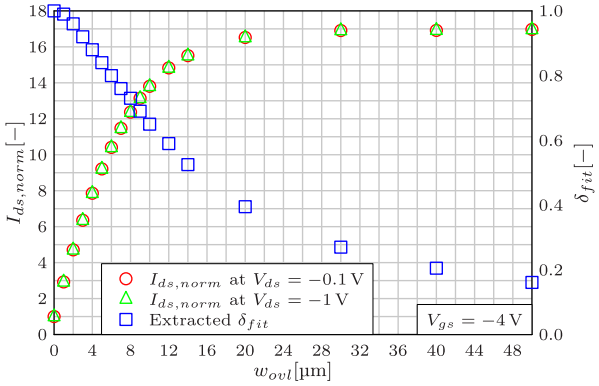

FIGURE 9. Simulated drain current of a single-finger OTFT at the bias point $V_{gs} = -4\,\mathrm{V}$ for different fringing lengths w_{ovl} for $V_{ds} = -0.1\,\mathrm{V}$ (red circles) and $V_{ds} = -1\,\mathrm{V}$ (green triangles). The drain current is normalized with respect to the current of a transistor with $w_{ovl} = 0\,\mu\mathrm{m}$ for both drain voltages. The extracted values for δ_{fit} are shown in blue squares. The transistor parameters are: $L_{ov,s} = L_{ov,d} = 5\mu\mathrm{m}$, $L_{ch} = 20\,\mu\mathrm{m}$, $t_{ox} = 5.3\,nm$, $W_{ch,SD} = 1\,\mu\mathrm{m}$, $\mu_p = 1\,\mathrm{cm^2V^{-1}s^{-1}}$. In the compact model, the mobility is set to $\kappa = 0.93\,\mathrm{cm^2V^{-1}s^{-1}}$ with $\beta = 0$.

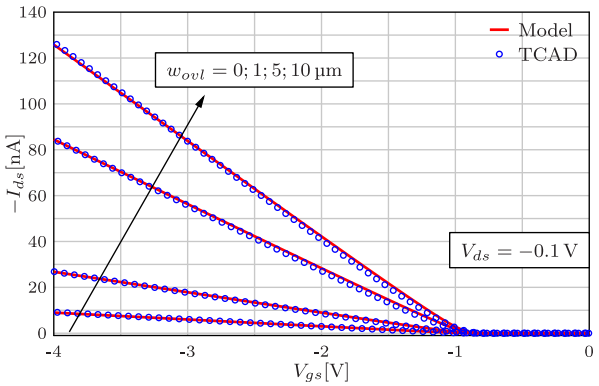

FIGURE 10. TCAD simulation of the current transfer characteristics of a single-finger OTFT (blue circles) with different fringing lengths w_{ovl} and manually fitted compact model curves (red solid lines). The values for δ_{fit} that have been used to fit the curves are shown in Fig. 9. The other transistor parameters are the same as in Fig. 9.

fringing length becomes greater than $20\,\mu\mathrm{m}$, the current is only slightly increased. Hence, the current spreading reaches some kind of saturation.

As it can be seen in Fig. 10, the fringing model fits the simulated current transfer characteristics well. For each curve, a constant, bias-independent value for δ_{fit} has been determined. This proves that modeling a bias-dependence is not necessary. In Fig. 11, it is shown that the fringing model fits the simulated capacitances, too. However, for high drain voltages and large fringing regions, the capacitances of the model show some deviations in comparison to the simulation results. The reason for this is that at higher drain voltages the charge distribution, especially in the electrode regions, is dependent on the z-position [see Fig. 4(b)]. This has been neglected in the overlap charges.

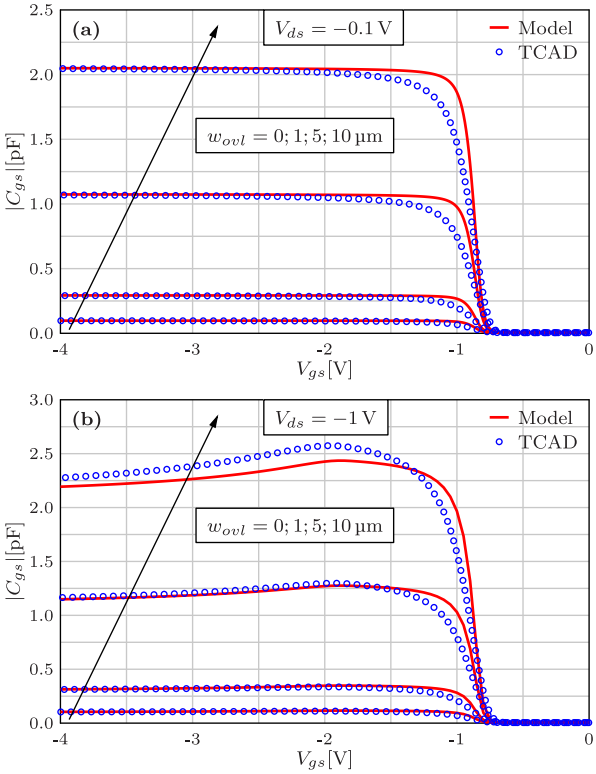

FIGURE 11. TCAD simulation of the capacitance C_{gs} of a single-finger OTFT (blue circles) with different fringing lengths w_{ovl} compared to compact model curves (red solid lines) for (a) $V_{ds} = -0.1$ V and (b) $V_{ds} = -1$ V. The transistor parameters are the same as in Fig. 9. The parameter δ_{fit} has no influence on the capacitances, since the effective channel width is canceled in the final charge equation.

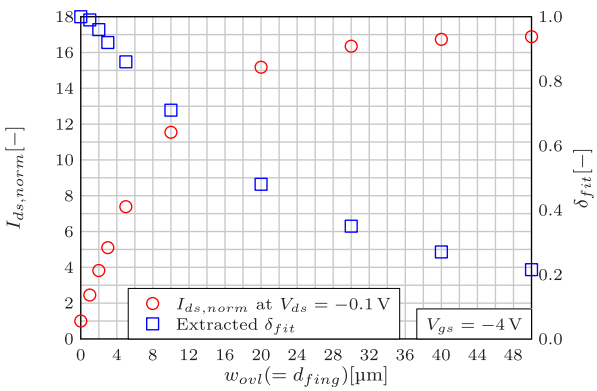

FIGURE 12. Simulated drain current of a double-finger OTFT at the bias point $V_{gs} = -4$ V for different fringing lengths w_{ovl} for $V_{ds} = -0.1$ V (red circles). The drain current is normalized with respect to the current of a transistor with $w_{ovl} = 0\,\mu$m. The extracted values for δ_{fit} are shown in blue squares. The transistor parameters are the same as for the single-finger OTFT in Fig. 9. Here, the device has two fingers, where each finger has a width of 1 µm. The overlap width w_{ovl} is varied simultaneously with d_{fing}.

The model also works for multi-finger devices. In Fig. 12 it can be seen that a variation of the fringing length and finger distance also leads to a change in the current which can be captured by a fitting of δ_{fit}. Nevertheless, the parameter δ_{fit} is an empirical fitting parameter. For the future, it might be interesting to find an even more physics-based way to calculate the effective channel width for the current.

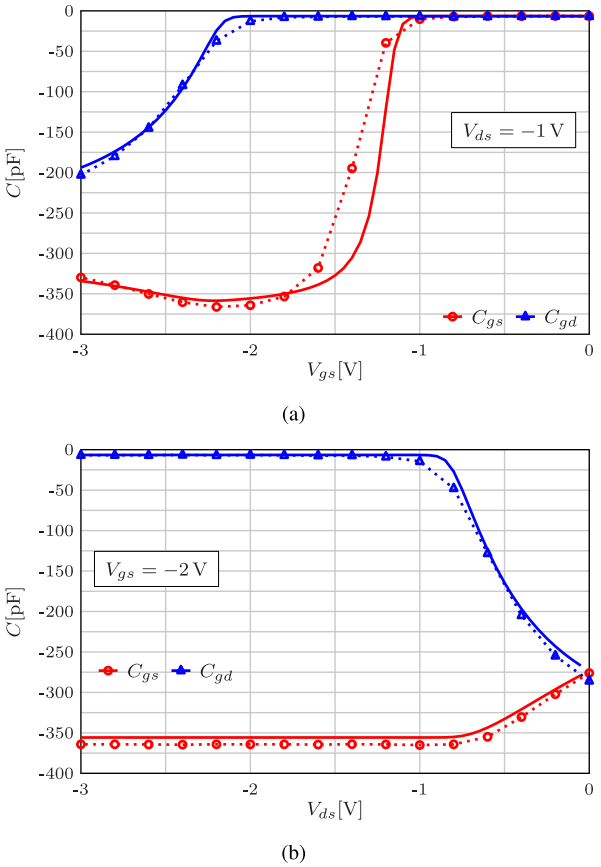

FIGURE 13. Capacitances of the compact model (solid lines) of a staggered device in comparison with measurement data (symbols with dotted lines) [12] for $f = 500$ Hz. In (a), the capacitances are plotted over V_{gs} for $V_{ds} = -1$ V. In (b), the capacitances are plotted over V_{ds} for $V_{gs} = -2$ V. The S/D channel width is $W_{ch,SD} = 400\,\mu$m, the fringing length is $w_{ovl} = 30\,\mu$m and $\delta_{fit} = 0.27$. The value for δ_{fit} does not play a role. However, a value has to be provided. The value of 0.27 is taken from Fig. 9. The threshold voltage is $V_{T0} = -1.2$ Volt and the mobility is set to $\kappa = 2.05\,\mathrm{cm^2 V^{\beta-1} s^{-1}}$ with $\beta = 0.03$. The transistor data are the same as in Fig. 2.

B. CAPACITANCE MEASUREMENTS

In this section, the capacitance model is compared to the measurements of a single-finger device presented in [12]. In Fig. 2, the fitting of the compact model to the measured current transfer characteristics is shown. However, at this stage, the model not considering the fringing regions has been used. As it can be seen, the transfer curves fit, though. The reason is that neglecting the fringing regions leads to a higher mobility value in the compact model [24]. An increase of the mobility has the same effect on the current as an increase of the effective channel width. Hence, it is difficult to separately extract the mobility and the parameter δ_{fit}, if there is only one transistor with a certain fringing length. As described in the modeling section, the parameter δ_{fit} has no influence on the capacitance model which can thus be verified without fitting δ_{fit}. As it can be seen in Fig. 13, the compact model reproduces the measured capacitances well. The capacitances from [12] have been measured

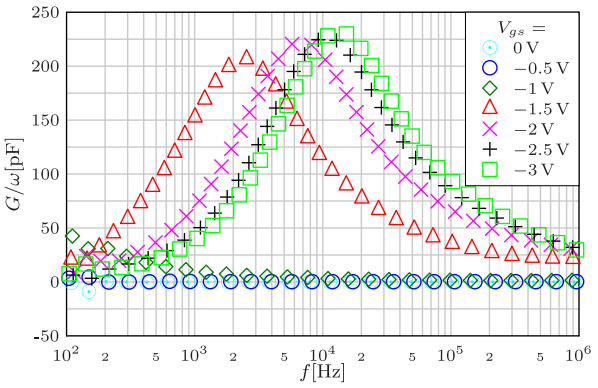

FIGURE 14. Measured loss of the transistor presented in Fig. 13. The loss is defined as G/ω, where $G = \mathrm{Re}(Y)$ and ω is the angular frequency.

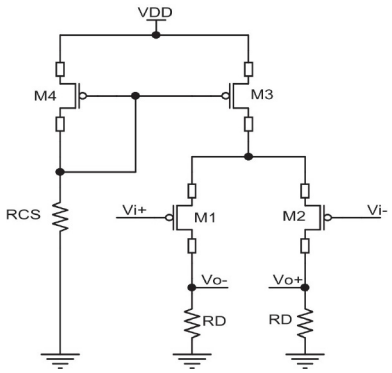

FIGURE 15. Schematic of the differential amplifier [25].

at a frequency of 500 Hz using an LCR meter (HP 4284A). The amplitude of the superimposed AC signal is 100 mV. Compensation of the parasitic capacitances due to the field lines between the probe tips is done. However, measurement errors are inevitable but are expected to be small because of the relatively long channel of the transistor. The LCR meter determines the complex admittance Y at each operation point. From this, the capacitance and the conductance can be determined. Although the compact model presented in this work only models the capacitances, the measured conductances can be of interest as well. In Fig. 14, the measured loss G/ω is presented. OTFTs based on DNTT are sensitive to bias stress which means that an applied gate voltage over a certain time may cause a shift of the threshold voltage [12], [19]. As a consequence, the threshold voltage which is used to fit the current transfer characteristics is different from the threshold voltage used for the capacitance measurements as they have been conducted at different times.

C. DIFFERENTIAL AMPLIFIER

The compact model for the OTFTs has been implemented in the hardware description language Verilog-A. In [25] design and measurements on differential amplifiers based on OTFTs are presented. The model has been used in the circuit simulator Cadence Virtuoso [27] to simulate the differential amplifiers. In Fig. 15, a sketch of the differential amplifier is shown. The transistors M3 and M4 constitute a current

TABLE 1. Parameters of the two differential amplifiers.

	Diff. Amp. 1	Diff. Amp. 2
$W_{ch,SD,M3/M4}$	2000 µm	1000 µm
$W_{ch,SD,M1/M2}$	1000 µm	500 µm
w_{ovl}	50 µm	50 µm
$N_{fing,M3/M4}$	20	10
$N_{fing,M1/M2}$	10	5
d_{fing}	50 µm	50 µm
R_D	22 MΩ	4 MΩ
R_{CS}	22 MΩ	4 MΩ
L_{ch}	20 µm	20 µm

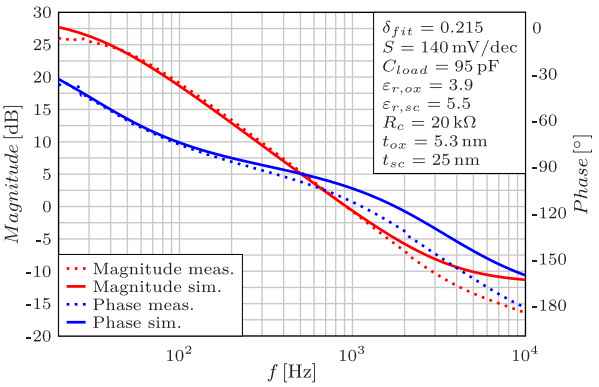

FIGURE 16. Magnitude response and phase response of the differential amplifier 1. The measurements [25] (dotted lines) are compared to the simulation results (solid lines). The inset of the graph shows further parameters which are valid for all transistors in the circuit.

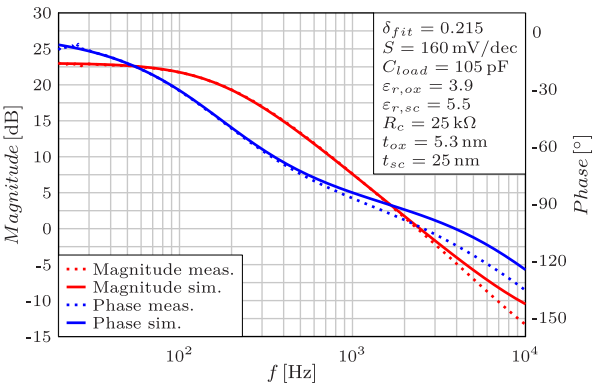

FIGURE 17. Magnitude response and phase response of the differential amplifier 2. The measurements [25] (dotted lines) are compared to the simulation results (solid lines).

mirror which provides a constant current for the differential pair consisting of M1 and M2. As the current flowing through M3 has to flow through M1 and M2, the channel width of M3 is chosen to be two times the channel width of M1 and M2. There have been fabricated two amplifiers with the parameters shown in Tab. 1. If no transistor is mentioned in the index, it means that the value holds true for all four transistors.

The differential amplifiers are loaded with a capacitor of 20 pF. However, the connector cables also have a capacitance. Hence, the effective load capacitance can be regarded as a fitting parameter. As it can be seen in Fig. 16 and Fig. 17, the simulated amplifier circuit has a good match

with the measured results with regards to both, the gain and the phase. However, for higher frequencies, the model has some deviations in comparison to the measurements. The reason for this is that the compact model is only valid for a quasistatic operation. However in OTFTs, a frequency dependency of the capacitances is observed. In [13], it is reported that already in the kilohertz regime the frequency dependency start to play an important role.

VI. CONCLUSION

In this paper, a charge-based compact model for the total charges in staggered OTFTs including multi-finger structures has been presented. Furthermore, the DC current model has been extended to take into account current spreading effects. The model includes the calculation of fringing regions which appear in fabricated devices. The compact model has been verified by comparing the capacitances to Sentaurus TCAD simulations and capacitance measurements. Furthermore, a differential amplifier based on OTFTs has been simulated with the compact model and has been compared to measurements of a fabricated circuit. The model reproduces the simulation and measurement data well.

APPENDIX A
CHARGE EQUATIONS WITHOUT FRINGING EFFECTS

The solutions of the three integrals in Eqs. (6)-(8) are:

$$Q_c = -\frac{W_{ch}^2 \mu_{eff}}{I_{ds}} \left(\frac{Q_{md}'^3}{3C_{ox}'} - \frac{Q_{ms}'^3}{3C_{ox}'} + \frac{Q_{md}'^2 V_{th}\tilde{\alpha}}{2} - \frac{Q_{ms}'^2 V_{th}\tilde{\alpha}}{2} \right), \tag{32}$$

$$\begin{aligned} Q_d = -\frac{W_{ch}^3 \mu_{eff}^2}{I_{ds}^2 L_{ch}} \Bigg(& \frac{Q_{md}'^3 Q_{ms}'^2}{6C_{ox}'^2} - \frac{Q_{ms}'^5}{15C_{ox}'^2} - \frac{Q_{md}'^5}{10C_{ox}'^2} - \frac{Q_{md}'^3 V_{th}^2 \tilde{\alpha}^2}{3} \\ & - \frac{Q_{ms}'^3 V_{th}^2 \tilde{\alpha}^2}{6} - \frac{3Q_{md}'^4 V_{th}\tilde{\alpha}}{8C_{ox}'} - \frac{5Q_{ms}'^4 V_{th}\tilde{\alpha}}{24C_{ox}'} \\ & + \frac{Q_{md}'^2 Q_{ms}' V_{th}^2 \tilde{\alpha}^2}{2} + \frac{Q_{md}'^2 Q_{ms}'^2 V_{th}\tilde{\alpha}}{4C_{ox}'} \\ & + \frac{Q_{md}'^3 Q_{ms}' V_{th}\tilde{\alpha}}{3C_{ox}'} \Bigg), \end{aligned} \tag{33}$$

$$Q_s = Q_c - Q_d. \tag{34}$$

APPENDIX B
CHARGE EQUATIONS WITH FRINGING EFFECTS

The solutions of the three integrals in Eqs. (22)-(24) are:

$$\begin{aligned} Q_c = & -\frac{W_{ch,G} W_{ch,eff} \mu_{eff}}{I_{ds}} \\ & \times \left(\frac{Q_{md}'^3}{3C_{ox}'} - \frac{Q_{ms}'^3}{3C_{ox}'} + \frac{Q_{md}'^2 V_{th}\tilde{\alpha}}{2} - \frac{Q_{ms}'^2 V_{th}\tilde{\alpha}}{2} \right), \end{aligned} \tag{35}$$

$$\begin{aligned} Q_d = & -\frac{W_{ch,G} W_{ch,eff}^2 \mu_{eff}^2}{I_{ds}^2 L_{ch}} \\ & \times \Bigg(\frac{Q_{md}'^3 Q_{ms}'^2}{6C_{ox}'^2} - \frac{Q_{ms}'^5}{15C_{ox}'^2} - \frac{Q_{md}'^5}{10C_{ox}'^2} - \frac{Q_{md}'^3 V_{th}^2 \tilde{\alpha}^2}{3} \\ & - \frac{Q_{ms}'^3 V_{th}^2 \tilde{\alpha}^2}{6} - \frac{3Q_{md}'^4 V_{th}\tilde{\alpha}}{8C_{ox}'} - \frac{5Q_{ms}'^4 V_{th}\tilde{\alpha}}{24C_{ox}'} \\ & + \frac{Q_{md}'^2 Q_{ms}' V_{th}^2 \tilde{\alpha}^2}{2} + \frac{Q_{md}'^2 Q_{ms}'^2 V_{th}\tilde{\alpha}}{4C_{ox}'} + \frac{Q_{md}'^3 Q_{ms}' V_{th}\tilde{\alpha}}{3C_{ox}'} \Bigg), \end{aligned} \tag{36}$$

$$Q_s = Q_c - Q_d. \tag{37}$$

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REFERENCES

[1] J. E. Anthony, "Functionalized acenes and heteroacenes for organic electronics," *Chem. Rev.*, vol. 106, no. 12, pp. 5028–5048, 2006.
[2] O. Marinov and M. J. Deen, "Quasistatic compact modelling of organic thin-film transistors," *Organic Electron.*, vol. 14, no. 1, pp. 295–311, 2013.
[3] L. Li, H. Marien, J. Genoe, M. Steyaert, and P. Heremans, "Compact model for organic thin-film transistor," *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 210–212, Mar. 2010.
[4] G. Horowitz, "Organic field-effect transistors," *Adv. Mater.*, vol. 10, no. 5, pp. 365–377, 1998.
[5] J. L. Brédas, J. P. Calbert, D. A. da Silva Filho, and J. Cornil, "Organic semiconductors: A theoretical characterization of the basic parameters governing charge transport," *Proc. Nat. Acad. Sci. USA*, vol. 99, no. 9, pp. 5804–5809, May 2002.
[6] F. Hain, M. Graef, B. Iñíguez, and A. Kloes, "Charge based, continuous compact model for the channel current in organic thin-film transistors for all regions of operation," *Solid-State Electron.*, vol. 133, pp. 17–24, Jul. 2017.
[7] A. F. Paterson *et al.*, "Recent progress in high-mobility organic transistors: A reality check," *Adv. Mater.*, vol. 30, no. 36, 2018, Art. no. 1801079.
[8] H. L. Gomes, "Organic field effect transistors," in *Organic and Printed Electronics Fundamentals and Applications*, G. Nisato, D. Lupo, and S. Ganz, Eds. Boca Raton, FL, USA: Taylor & Francis, 2016, pp. 147–197.
[9] C. H. Kim, D. Tondelier, B. Geffroy, Y. Bonnassieux, and G. Horowitz, "Operating mechanism of the organic metal-semiconductor field-effect transistor (OMESFET)," *Eur. Phys. J. Appl. Phys.*, vol. 56, Dec. 2011, Art. no. 34105.
[10] F. Torricelli, Z. M. Kovacs-Vajna, and L. Colalongo, "A charge-based OTFT model for circuit simulation," *IEEE Trans. Electron Devices*, vol. 56, no. 1, pp. 20–30, Jan. 2009.
[11] L. Wang, N. Lu, L. Li, Z. Ji, W. Banerjee, and M. Liu, "Compact model for organic thin-film transistor with Gaussian density of states," *AIP Adv.*, vol. 5, no. 4, 2015, Art. no. 047123.
[12] T. Zaki *et al.*, "Accurate capacitance modeling and characterization of organic thin-film transistors," *IEEE Trans. Electron Devices*, vol. 61, no. 1, pp. 98–104, Jan. 2014.
[13] S. Scheinert, T. Zaki, R. Rödel, I. Hörselmann, H. Klauk, and J. N. Burghartz, "Numerical analysis of capacitance compact models for organic thin-film transistors," *Organic Electron.*, vol. 15, no. 7, pp. 1503–1508, Jul. 2014.
[14] A. Castro-Carranza *et al.*, "Organic thin-film transistor bias-dependent capacitance compact model in accumulation regime," *IET Circuits Devices Syst.*, vol. 6, no. 2, pp. 130–135, Mar. 2012.
[15] A. Castro-Carranza *et al.*, "Compact capacitance model for OTFTs at low and medium frequencies," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 638–642, Feb. 2014.
[16] J. Leise, J. Pruefer, G. Darbandy, and A. Kloes, "Charge-based compact modeling of capacitances in staggered OTFTs," in *Proc. Lat. Amer. Electron Devices Conf. (LAEDC)*, Armenia, Colombia, Feb. 2019, pp. 1–4.
[17] G. Horowitz, M. E. Hajlaoui, and R. Hajlaoui, "Temperature and gate voltage dependence of hole mobility in polycrystalline oligothiophene thin film transistors," *J. Appl. Phys.*, vol. 87, no. 9, pp. 4456–4463, 2000.

[18] J. Pruefer, B. Iniguez, H. Klauk, and A. Kloes, "Compact modeling of non-linear contact resistance in staggered and coplanar organic thin-film transistors," in *Proc. ICOE*, Bordeaux, France, 2018.
[19] G. Darbandy *et al.*, "Characterization of the charge-trap dynamics in organic thin-film transistors," in *Proc. 26th Int. Conf. Mixed Design Int. Circuits Syst. (MIXDES)*, Rzeszow, Poland, Jun. 2019, pp. 76–80.
[20] D. E. Ward and R. W. Dutton, "A charge-oriented model for MOS transistor capacitances," *IEEE J. Solid-State Circuits*, vol. SSC-13, no. 5, pp. 703–708, Oct. 1978.
[21] T. Holtij, "Analytical compact modeling of nanoscale multiple-gate MOSFETs," Ph.D. dissertation, Dept. Elect. Elect. Autom. Control Eng., Univ. Rovira I Virgili, Tarragona, Spain, 2014.
[22] C. C. Enz and E. A. Vittoz, *Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design*. Chichester, U.K.: Wiley, Aug. 2006.
[23] N. Arora, *MOSFET Modeling for VLSI Simulation*. Singapore: World Sci., 2007.
[24] K. Pei, M. Chen, Z. Zhou, H. Li, and P. K. L. Chan, "Overestimation of carrier mobility in organic thin film transistors due to unaccounted fringe currents," *ACS Appl. Electron. Mater.*, vol. 1, no. 3, pp. 379–388, 2019.
[25] M. Seifaei *et al.*, "Stable, self-biased and high-gain organic amplifiers with reduced parameter variation effect," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Tainan, Taiwan, Nov. 2018, pp. 119–122.
[26] *TCAD Sentaurus™ Device User Guide, Version O-2018.06*, Synopsys Inc., Mountain View, CA, USA, 2018.
[27] *Virtuoso® Analog Design Environment, Version IC6.1.6.*, Cadence Design Syst. Inc., San Jose, CA, USA, 2013.