Flexible low-voltage high-frequency organic thin-film transistors

James W. Borchert1,2*, Ute Zschieschang1, Florian Letzkus3, Michele Giorgio4,5, R. Thomas Weitz6,7,8, Mario Caironi4, Joachim N. Burghartz2, Sabine Ludwigs2, Hagen Klauk1*

The primary driver for the development of organic thin-film transistors (TFTs) over the past few decades has been the prospect of electronics applications on unconventional substrates requiring low-temperature processing. A key requirement for many such applications is high-frequency switching or amplification at the low operating voltages provided by lithium-ion batteries (~3 V). To date, however, most organic-TFT technologies show limited dynamic performance unless high operating voltages are applied to mitigate high contact resistances and large parasitic capacitances. Here, we present flexible low-voltage organic TFTs with record static and dynamic performance, including contact resistance as small as 10 Ω·cm, on/off current ratios as large as 10⁸, subthreshold swing as small as 59 mV/decade, signal delays below 80 ns in inverters and ring oscillators, and transit frequencies as high as 21 MHz, all while using an inverted coplanar TFT structure that can be readily adapted to industry-standard lithographic techniques.

INTRODUCTION

Flexible electronics (1–3) are currently a $20-billion-per-year industry driven mainly by the recent trend of manufacturing active-matrix organic light-emitting diode (AMOLED) smartphone displays on polyimide substrates. Of the 600 million AMOLED displays manufactured in 2018, approximately 60% were made on polyimide rather than glass, and this share is projected to further increase (4). Among the many challenges associated with this transition was to reduce the process temperature of the thin-film transistor (TFT) technology based on low-temperature polycrystalline silicon (LTPS) from 550° to 450°C to make it compatible with polyimide substrates without compromising TFT characteristics (5). Further progress toward fully bendable androllable active-matrix displays on a wider range of polymeric substrates has incentivized the search for an alternative TFT technology that has a lower-thermal-budget process compared with LTPS. Amorphous metal oxide TFTs, such as those based on indium gallium zinc oxide (IGZO), have already seen some market success and typically outperform organic TFTs in terms of charge-carrier mobility and dynamic performance. However, process temperatures above 150°C are often still required, whereas organic TFTs can often be fabricated at temperatures below 100°C (6). The most critical issue preventing the adoption of organic TFTs in high-frequency, low-voltage applications such as mobile AMOLED displays is that the contact resistance between the source and drain contacts and the organic semiconductor (Rc) is often very high when compared to IGZO and LTPS TFTs (7). The fundamental reason that a small contact resistance is so critical for high-frequency TFT applications is that as the channel length (L) is reduced to increase the maximum operation frequency, the TFT enters a contact-limited regime where the contact resistance constitutes a substantial portion of the total resistance of the TFT. This effectively nullifies any potential benefits of, e.g., increasing the intrinsic carrier mobility (μ0) in the organic-semiconductor channel. Channel-width-normalized contact resistances (Rc/W) of organic TFTs typically fall into the range of 10² to 10⁵ Ω·cm. Several factors contribute to the contact resistance, including the TFT architecture (8–12), the semiconductor-thin-film morphology at the contact interface (9, 13), and the energetic injection barrier arising from the mismatch between the work function of the contact metal and the organic-semiconductor transport levels. Effective barrier heights of several 100 meV or more are often observed (8, 14). Despite substantial efforts to improve charge injection in organic TFTs via various methods over the past 20 years, only a handful of reports have shown contact resistances below 100 Ω·cm (Fig. 1D). Excepting the electrolyte-gated polymer TFTs presented by Braga et al. (15) (denoted by a star in Fig. 1D), the lowest contact resistance reported for organic TFTs so far (29 Ω·cm) was achieved in inverted coplanar TFTs by using a very thin gate dielectric and gold source and drain contacts modified with a chemisorbed layer of pentafluorobenzenethiol (PFBT) (12). The improvement in contact resistance over comparable inverted staggered TFTs (56 Ω·cm) was attributed primarily to a stronger influence of the electric field imposed by the applied potentials in the coplanar device architecture (11). The lowest contact resistance reported for staggered organic TFTs (46.9 Ω·cm) was achieved by using a bilayer of highly crystalline organic semiconductor monolayers in combination with contact doping using 2,3,5,6-tetrafluoro-7,7,8,8-tetracyanoquinodimethane (Fc-TCNQ) (16). Both of these results, while representing a substantial advance in the quest for low contact resistance in organic TFTs, are still larger by at least an order of magnitude compared to IGZO TFTs (17) and several orders of magnitude compared to silicon transistors (18).

Here, we further demonstrate the capabilities of our previously reported method for fabricating low-voltage organic TFTs with record low contact resistance (12) to enhance the static and dynamic performance characteristics of both individual TFTs and circuits. The TFTs and circuits were fabricated on flexible polyethylene...
naphthalate (PEN) sheets using high-resolution silicon stencil masks (see Fig. 1, A to C), to pattern all device layers (19–21). The small-molecule organic semiconductors 2,9-didecyl-dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (C10-DNTT) or 2,9-diphenyl-dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DPh-DNTT) were used as the active layer (22). Transmission line method (TLM) analysis of the transfer characteristics of the TFTs in the linear regime of operation indicates a width-normalized contact resistance of 35 Ω·cm, in close agreement with our previous report for similarly fabricated TFTs (12). By combining this low contact resistance with a small channel length and small gate-to-contact overlaps, the TFTs and circuits show record static and dynamic performance by several metrics. The TFTs show on/off current ratios as high as $10^{10}$ and subthreshold swings as small as $(59 \pm 2)$ mV/decade, within measurement error of the theoretical limit of 58.6 mV/decade at the temperature at which the measurements were conducted (292 K). Biased-load inverters switch with rise and fall time constants as short as 19 and 56 ns, respectively. An 11-stage ring oscillator operates with a signal propagation delay per stage of 79 ns at a supply voltage of 4.4 V. The dynamic performance of individual TFTs, including the unity-current gain (transit) frequency, was measured using two-port network analysis of a set of TFTs operated in the saturation regime. By analyzing the channel-length dependence of the transit frequency, a width-normalized contact resistance of $(10 \pm 2)$ Ω·cm was determined; the fact that this value is smaller than the contact resistance determined by TLM in the linear regime is related to the non-Ohmic nature of the contact resistance. Last, a transit frequency as high as 21 MHz was measured at gate-source and drain-source voltages of −3 V, corresponding to a record voltage-normalized transit frequency of 7 MHz/V. These characteristics represent important proof of concepts for the development of low-power flexible circuits using organic TFTs and for applications in flexible AMOLED displays (23–25). A literature overview and comparison to our results are provided for the contact resistance, ring oscillator stage delay, and voltage-normalized transit frequency in Fig. 1 (D to F).

**RESULTS AND DISCUSSION**

**Static TFT performance**

The static performance characteristics of DPh-DNTT TFTs fabricated on flexible PEN substrates are summarized in Fig. 2. Figure 2A shows the transfer characteristics of a DPh-DNTT TFT with a channel length of 8 μm, a total gate-to-contact overlap $(L_{ov,total} = L_{ov,GS} + L_{ov,GD})$ of 4 μm, and a channel width of 200 μm. The transfer curves show negligible hysteresis and a gate-leakage current of less than 10 pA over the gate-source voltage $(V_{GS})$ measurement range. When measured in the saturation regime, i.e., with a drain-source voltage of −2 V, the drain current shows a nearly ideal quadratic dependence on the gate-overdrive voltage (the difference between the gate-source voltage and the threshold voltage), an on/off current ratio of $10^{10}$, and a...
nearly gate voltage–independent effective carrier mobility ($\mu_{\text{eff}}$) of $\sim 3.6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (see Fig. 2B). The subthreshold swing is determined to be $(59 \pm 2)$ mV/decade by fitting the exponential region of the drain current between $V_{\text{GS}} = -0.5 \text{ V}$ and $-0.8 \text{ V}$ (see Fig. 2C).

We note that for the measurement temperature of 292 K, this is within the measurement error of the theoretical minimum (58.6 mV/decade) given as $\ln(10) k T/q$ where $k$ is the Boltzmann constant and $q$ is the elementary charge. The output characteristics show the
expected linear and saturation behavior (see Fig. 2D). The reproducibility of the fabrication process is illustrated in Fig. S2, where the measured transfer characteristics of 10 nominally identical DPh-DNTT TFTs with a channel length of 1.5 μm are shown. Figure S3 shows a comparison of the transfer and output characteristics of TFTs based on DPh-DNTT and C10-DNTT, illustrating the fact that similar TFT performance can be obtained with multiple semiconductors.

The TLM analysis of the transfer characteristics of DPh-DNTT TFTs with a channel width of 50 μm and channel lengths ranging from 1.0 to 10.5 μm in the linear regime shows a width-normalized contact resistance of 35 Ω·cm and an intrinsic channel mobility (μm) of 4.3 cm² V⁻¹ s⁻¹ at a gate-overdrive voltage of −2.5 V (see Fig. 2, E and F). These results are similar to those in our previous report (12), confirming the good reproducibility of the fabrication process.

**Static and dynamic circuit characteristics**

The performance characteristics of an inverter based on DPh-DNTT TFTs and of an 11-stage ring oscillator based on C10-DNTT TFTs, both fabricated on flexible PEN substrates, are summarized in Figs. 3 and 4, respectively. The critical dimensions of the TFTs are identical in both circuits (channel length, 1 μm; total gate-to-contact overlap, 4 μm), and both circuits use the biased-load design (26). An advantage of this design over single-power-rail designs is that the gate-source voltage of the load TFT can be kept above the threshold voltage at all times, facilitating more rapid discharging of the output node through the load TFT when the output node is switched from the high state (output voltage near the supply voltage) to the low state (output voltage near 0 V). As a result, the characteristic fall time and thus the total switching delay of biased-load circuit designs can be shorter than those of unipolar circuits without such an additional power supply. An additional advantage of the biased-load design is that it creates the possibility to tune the trip voltage (i.e., the input voltage at which the transition at the output occurs) independent of the supply voltage. To illustrate this, in Fig. 3 (A and B), we show transfer curves of the inverter. In Fig. 3A, the transfer curve is measured for a supply voltage (VDD) of 2 V and a bias voltage (Vbias) of −1 V, i.e., with the load TFT biased slightly above the threshold voltage. Figure 3B shows transfer curves of the same inverter measured for a supply voltage of 1 V and at bias voltages ranging from −1 to 0 V, illustrating that the trip voltage (indicated in Fig. 3B by open circles) can be tuned over a range of approximately 15% of the supply voltage.

The dynamic performance of the inverter was evaluated by applying a square-wave input signal with a frequency (f) of 2 MHz and an amplitude (Vin) of 1.5, 2.0, or 2.5 V (and adjusting the supply and bias voltages so that VDD = VDD = Vin for all measurements). The characteristic rise and fall time constants (τrise and τfall) of the switching events were determined by fitting simple exponential functions to the measured output-voltage transitions. The smallest time constants (19 and 56 ns) were observed for a supply voltage of 2.5 V (see Fig. 3C). The dependence of the time constants on the supply voltage is shown in Fig. 3D.

The results from an 11-stage ring oscillator based on C10-DNTT TFTs are summarized in Fig. 4. Figure 4 (A to C) show the schematic and a photograph of the circuit, a scanning electron microscopy (SEM) image of the channel region of one of the TFTs, and the measured output signal of the ring oscillator. The signal-propagation delay (τ), which was determined by fitting a sine wave to the measured output signal, is 143 ns per stage for a supply voltage of 1.6 V and 79 ns per stage for a supply voltage of 4.4 V (see Fig. 4D). This is the smallest signal delay reported to date for an organic TFT–based ring oscillator at a supply voltage of less than 50 V (see Fig. 1E) (27). From the signal-propagation delay, an equivalent frequency (fEQ = 1/2τ) can be calculated that provides an estimate of the average frequency at which the TFTs are switching in the ring oscillator and which can be used to approximate the TFTs’ transit frequency (fT) to within a factor of about 2 (7). For a supply voltage of 4.4 V, we obtain an equivalent frequency of 6.3 MHz, corresponding to a supply-voltage-normalized equivalent frequency of 1.4 MHz V⁻¹.

**Two-port network analysis**

While the dynamic performance of a ring oscillator provides a measure of the average switching frequency of the TFTs used in the circuit, more detailed information about the dynamic properties of individual TFTs can be provided by two-port network analysis (2). In particular, scattering-parameter (S-parameter) measurements are attractive for their capability of unambiguously assessing the high-frequency characteristics of organic TFTs (28, 29). These measurements can, e.g., provide access to the various contributions to the total gate

---

**Fig. 3. Static and dynamic inverter characteristics.** (A) Static transfer characteristics of an inverter based on two DPh-DNTT TFTs in a biased-load circuit design fabricated on a flexible PEN substrate for a supply voltage (VDD) of 2 V and bias voltage (Vbias) of −1 V. The TFTs have a channel length (L) of 1 μm and a total gate-to-contact overlap of 4 μm. The inset shows the circuit diagram and a photograph of the inverter. Photo credit: James W. Borchert, Max Planck Institute for Solid State Research. (B) Static transfer characteristics of the same inverter for bias voltages ranging from −1 to 0 V. The open circles indicate the trip voltage. (C) Dynamic characteristics of the inverter in response to a square-wave input signal with a frequency of 2 MHz, a duty cycle of 50%, and an amplitude of 2.5 V. Characteristic rise and fall time constants of the switching delays (τrise, τfall) were determined by fitting simple exponential functions to the measured output waveform. (D) Rise and fall time constants measured for supply voltages (VDD) of 1.5, 2.0, and 2.5 V. The amplitude of the square-wave input signal was identical to the supply voltage, and Vbias = −VDD for each measurement.
capacitance ($C_G$) by converting the $S$-parameters to admittance ($Y$) parameters \((30)\) and enable measurement of the unity-current-gain cutoff (or transit) frequency \((f_T)\) of individual TFTs \((28)\). Using this method, we performed detailed dynamic characterization of DPh-DNTT TFTs with channel lengths ranging from 0.6 to 10.5 µm, a total gate-to-contact overlap of 10 µm, and a channel width of 100 µm (see Fig. 5A). All measurements were performed with constant gate-source and drain-source voltages of −3 V, superimposed with a small-amplitude component (see Fig. 5B). To assess the high-frequency characteristics of the gate dielectric, we evaluated the gate-drain capacitance \((C_{GD})\) from the $Y$ parameters by noting that under saturation conditions, \(|Y_{21}| = 2\pi f C_{GD}\) according to the Meyer model (see Fig. 5C) \((2, 31)\). In all TFTs that were measured, the area-normalized gate-drain capacitance was found to be constant with frequency (with a decrease of less than 20% up to the maximum measurement frequency of 200 MHz) and closely corresponds to the value expected for the unit-area gate-dielectric capacitance \((C_{die}+)\) of 0.7 µF cm\(^{-2}\) \((31)\).

To obtain the transit frequency \((f_T)\), the $S$-parameters were used to calculate the hybrid parameter corresponding to the small-signal current gain \((|h_{21}| = |S_21|/|G_b|)\) (see Fig. 5, D and G). In Fig. 5D, since the gate-to-contact overlaps were approximately equivalent for all TFTs, it was possible to determine the transit frequency directly as the frequency at which \(|h_{21}| = 0\) dB. The transit frequencies determined for this set of TFTs ranged from 17.8 MHz for a channel length of 0.7 µm to 0.7 MHz for a channel length of 10.5 µm. The dependence of the transit frequency on the channel length \((L)\), the width-normalized contact resistance \((R_{C,W})\), and the intrinsic channel mobility \((\mu_0)\) is derived as \((see section S1)\)

\[
f_T = \frac{\mu_0 (V_{GS} - V_{th})}{2\pi (L + \frac{1}{3} C_{die} R_{C,W} (V_{GS} - V_{th})) (L_{ov,total} + \frac{2}{3} L)}
\]

Since the unit-area gate-dielectric capacitance \((C_{die}+)\) and the total gate-to-contact overlap \((L_{ov,total})\) are nominally identical for all TFTs considered here, the contact resistance and the intrinsic channel mobility can be extracted by fitting Eq. 1 to the empirical dependence of the transit frequency on the channel length, considering $R_{C,W}$ and $\mu_0$ as free parameters. Figure 5E shows that an excellent fit to the experimental data is achieved with $R_{C,W} = (10 \pm 2) \, \Omega\cdot\text{cm}$ and $\mu_0 = (6 \pm 1) \, \text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$. There is a notable discrepancy between the contact resistance determined using the TLM \((35 \, \Omega\cdot\text{cm}; see Fig. 2F)\) and the transit frequency method shown in Fig. 5E. This discrepancy is likely due to the fact that the lateral electric fields applied in the $S$-parameter measurements are substantially larger than the fields applied during TLM. It is not uncommon for the contact resistance of organic TFTs to show lateral-field dependence \((32)\). This effect could be caused by various nonidealities of the metal-organic semiconductor interface, such as diffusion-limited charge injection and image-force lowering \((33, 34)\).
Parasitic fringe-capacitance effects can arise in field-effect transistors when the semiconductor layer extends beyond the edges of the device (35). While operating a TFT in the saturation regime, these effects are isolated to the source side of the TFT, so that reducing the gate-to-source overlap \( \left( L_{ov,GS} \right) \) while keeping the total gate-to-contact overlap \( \left( L_{ov,total} \right) \) and the channel length constant will lead to a smaller total gate capacitance and thus a higher transit frequency (36). By fabricating an asymmetric TFT with a smaller \( L_{ov,GS} \) of 1.7 \( \mu \text{m} \) \( \left( L_{ov,total} = 10 \mu\text{m} \right) \) and a channel length of 0.6 \( \mu\text{m} \), a transit frequency of 21 MHz at \( V_{GS} = V_{DS} = -3 \text{ V} \) was obtained, compared to 17.8 MHz for a TFT with symmetric gate-to-contact overlaps (see Fig. 5, F to H). This is to our knowledge the highest transit frequency.
reported to date for an organic transistor fabricated on a flexible substrate. Normalized to the supply voltage (7 MHz V$^{-1}$), it is the highest voltage-normalized transit frequency reported to date for any organic transistors (see Fig. 1F and table S1) ($\mu$F cm$^{-2}$). The oxide/SAM gate dielectric is typically between 0.5 and 0.7 m$^{-1}$.

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

section

6


Acknowledgments: We acknowledge K. Takimiya (RIKEN Center for Emergent Matter Science, Wako, Saitama, Japan) as well as K. Ieda, Y. Sadamitsu, and S. Inoue (Nippon Kayaku, Tokyo, Japan) for providing the organic semiconductors OPh-DNTT and Cu2DNTT; T. Zaki and R. Rödel for designing the silicon stencil masks; and Z. Wu for assisting with the IRRAS measurements.

Funding: This work was partially funded by the German Research Foundation (DFG) under the grants KL 2223/6-1, KL 2223/6-2 (SPP FFlexCom), KL 2223/7-1, and INST 35/1429-1 (SFB 1249), R.T.W. acknowledges funding from the excellence initiative Nanosystems Initiative Munich (NIM), the Center for Nanoscience (CeNS), the Solar Technologies go Hybrid (SoITech) initiative, and additional funding by the DFG under Germany’s Excellence Strategy [EXC-2111–390814868 (MCGST) and EXC 2089/1–390762680]. M.C. and M.G. acknowledge the financial support by the European Research Council (ERC) under the European Union’s Horizon 2020 research and innovation program “HEROIC,” grant agreement 638059. Author contributions: J.W.B., U.Z., and H.K. devised the experimental details of the study. J.W.B. fabricated all devices and performed electrical and morphological measurements. M.G. performed the S-parameter measurements. J.W.B. and H.K. wrote the article, with contributions from M.C. and R.T.W. F.L. and J.N.B. manufactured the silicon stencil masks used for the fabrication of the TFTs and circuits. S.L. and H.K. supervised the project. All authors discussed the results and contributed to the development of the final manuscript. Competing interests: The authors declare that they have no competing interests.

Data and materials availability: All data needed to evaluate the conclusions in the paper are present in the paper and/or the Supplementary Materials. Additional data related to this paper may be requested from the authors.

Submitted 16 September 2019
Accepted 10 March 2020
Published 20 May 2020
10.1126/sciadv.aaz5156

Supplementary Materials for

Flexible low-voltage high-frequency organic thin-film transistors

James W. Borchert*, Ute Zschieschang, Florian Letzkus, Michele Giorgio, R. Thomas Weitz, Mario Cairoli, Joachim N. Burghartz, Sabine Ludwigs, Hagen Klauk*

*Corresponding author. Email: j.borchert@fkf.mpg.de (J.W.B.); h.klauk@fkf.mpg.de (H.K.)

Published 20 May 2020, Sci. Adv. 6, eaaz5156 (2020)
DOI: 10.1126/sciadv.aaz5156

This PDF file includes:

Section S1
Figs. S1 to S7
Table S1
References
S1: Contact resistance, carrier mobility and transit frequency

The contact resistance ($R_C$) in organic TFTs is typically evaluated in the linear regime of transistor operation using the transmission line method (TLM; see Figs. 2 and S4) (41). In TLM analyses, as well as for most other methods for determining $R_C$ (42), a requirement (and indeed a drawback) is that it is only valid for the linear regime of operation using vanishingly-small $V_{DS}$, since a key assumption of TLM is that $R_C$ is Ohmic and that the channel resistance is uniform over the entire channel region. This latter point by itself precludes any analysis of $R_C$ in the saturation regime using TLM because of the pinch-off of the channel that occurs when $V_{DS}$ is approximately equivalent to the overdrive voltage ($V_{GS} - V_{th}$). Experimental investigations have shown that $R_C$ in organic TFTs can vary significantly with $V_{DS}$ (32, 43). Especially for TFTs with small channel lengths ($L$), $R_C$ may be reduced by $V_{DS}$ due to effects such as image-force lowering (IFL) (33) or by drain-induced barrier lowering (DIBL) (35) of the injection barrier at the interface between the source contact and the semiconductor. Enhancements of the carrier mobility in the vicinity of the contacts through a Poole-Frenkel-like dependence of the mobility on the applied electric field may also lead to lower $R_C$, in part due to the nonlinear effects on both charge transport (44) and charge injection (45). For these reasons it is beneficial to be able to quantify the dependence of $R_C$ on $V_{DS}$.

Here, we estimate $R_C$ and the intrinsic channel mobility ($\mu_0$) in the saturation regime ($V_{DS} \leq V_{GS} - V_{th}$ for p-channel TFTs) by fitting the transit frequency ($f_T$) extracted from S-parameter measurements as a function of channel length ($L$). Similar to TLM, we use $\mu_0$ and the width-normalized contact resistance ($R_CW$) as fitting parameters. This approach has to our knowledge never been explicitly implemented, though comparisons of calculated $f_T$ to experimental results using $R_C$ determined from TLM have been reported (16, 36). In both approaches, the error in the extracted values is assessed simply as the calculated standard error from the fits. In the TLM, the width-normalized total source-to-drain resistance of the TFT ($RW$) is fit with a linear function with respect to $L$. In our method, the $f_T$ data as a function of $L$ is fit using the equation derived in the following.

The dependence of the effective mobility ($\mu_{eff}$) and the transit frequency ($f_T$) on $R_C$ can be illustrated with the following two equations for TFTs operated in the saturation regime (2, 46):

$$\mu_{eff} = \mu_0 \left[ 1 - \left( \frac{\mu_0 C_{dil} R_C W (V_{GS} - V_{th})}{L + \mu_0 C_{dil} R_C W (V_{GS} - V_{th})} \right)^2 \right]$$

(1)

$$f_T = \frac{\mu_{eff} (V_{GS} - V_{th})}{2\pi L (L_{ov \ total} + \frac{2L}{3})}$$

(2)

where $C_{dil}$ is the gate-dielectric capacitance per unit area and $L_{ov \ total}$ is the total gate-to-contact overlap length, which is simply the sum of the gate-to-source ($L_{ov, GS}$) and gate-to-drain ($L_{ov, GD}$) overlap lengths. In principle, the term $R_C$ encompasses contributions from both the source and drain contacts. Equation 1 can be simplified to (36)

$$\mu_{eff} = \frac{\mu_0}{1 + \frac{1}{2} \mu_0 C_{dil} R_C W (V_{GS} - V_{th})}$$

(3)

Combining Equations 2 and 3, we then obtain an expression for $f_T$ that includes the influence of the contact resistance:

$$f_T = \frac{\mu_0 (V_{GS} - V_{th})}{2\pi (L + \frac{1}{2} \mu_0 C_{dil} R_C W (V_{GS} - V_{th})) (L_{ov \ total} + \frac{2L}{3})}$$

(4)

For illustrative purposes, several curves of the transit frequency as a function of the channel length calculated using Equation 4 and assuming different values for $R_C W$ are shown in Fig. S7.
Fig. S1| Device fabrication process and materials characterization. (A) Schematic process flow for the fabrication of bottom-gate bottom-contact (inverted coplanar) organic TFTs. All metal and semiconductor layers are deposited by thermal evaporation or sublimation in vacuum and patterned using high-resolution silicon stencil masks. (B) Infrared reflection absorption spectroscopy (IRRAS) analysis of bulk pentafluorobenzenethiol (PFBT, black) and of a chemisorbed monolayer of PFBT on a gold surface (red). (C) AFM height scan of a thin film of the organic semiconductor DPh-DNTT deposited onto a hybrid AlOₓ/SAM gate dielectric on a flexible PEN substrate.
Fig. S2 | Static transistor characteristics and uniformity. (A) SEM micrograph of an individual DPh-DNTT TFT. (B) Measured transfer characteristics of 10 nominally identical TFTs having a channel length ($L$) of 1.5 µm, a total gate-to-contact overlap ($L_{ov,total}$) of 60 µm and a channel width ($W$) of 7.5 µm, with statistics for the effective carrier mobility ($\mu_{eff}$), threshold voltage ($V_{th}$) and subthreshold swing (SS). (C) Transfer characteristics of an individual TFT measured at a drain-source voltage ($V_{DS}$) of -3 V. The dotted blue line is a guide to the eye, indicating the ideal quadratic dependence of the drain current on the gate-overdrive voltage ($V_{GS} - V_{th}$) in the saturation regime. (D) Output characteristics for gate-source voltages ($V_{GS}$) from 0 to -3 V in steps of 0.5 V.
Fig. S3 | Static characteristics of TFTs based on DPh-DNTT (top row) and C\textsubscript{10}-DNTT (bottom row). Both TFTs have a channel length (L) of 8 µm, a total gate-to-contact overlap (L\textsubscript{ov,total}) of 4 µm and a channel width (W) of 200 µm. From left to right: Transfer characteristics, effective carrier mobility (\(\mu\)\textsubscript{eff}) plotted as a function of the gate-source voltage, and output characteristics for gate-source voltages (V\textsubscript{GS}) from 0 to -3 V in steps of 0.5 V. (Note that these TFTs were fabricated separately from the TFTs shown in Fig. S2.)
Fig. S4 | Transistors for TLM analysis. (A) Transfer characteristics of DPh-DNTT TFTs with channel lengths ($L$) ranging from 1 to 10.5 µm and a channel width ($W$) of 50 µm, measured with a drain-source voltage ($V_{DS}$) of -0.1 V. (B) Effective carrier mobility ($\mu_{eff}$) in the linear regime determined for each TFT as a function of the channel length ($L$). The line is a fit to the data using the equation $\mu_{eff} = \mu_0 \left(1 + \frac{L_{1/2}}{L}\right)^{-1}$ where $\mu_0$ is the intrinsic channel mobility and $L_{1/2}$ is the channel length at which $\mu_{eff} = \frac{1}{2} \mu_0$. (C) SEM micrographs of the channel region of the TFTs. (Note that these TFTs were fabricated separately from the TFTs shown in Fig. S2.)
Fig. S5 | Transistors for S-parameter measurements. (A) Transfer characteristics of DPh-DNTT TFTs with channel lengths ($L$) ranging from 0.7 to 10.5 µm, a total gate-to-contact overlap ($L_{ov, total}$) of 10 µm and a channel width ($W$) of 100 µm, measured with a drain-source voltage ($V_{DS}$) of -3 V. (B) Output characteristics of each TFT for a gate-source voltage ($V_{GS}$) of -3 V. (C) Channel-width-normalized peak transconductance ($g_m$) at a gate-source voltage ($V_{GS}$) of -3 V as a function of the inverse of the channel length. (D) SEM micrographs of the channel region of the TFTs. (Note that these TFTs were fabricated separately from the TFTs shown in Fig. S2.)
Fig. S6| DPh-DNTT TFT showing a transit frequency of 21 MHz. The TFT has a channel length ($L$) of 0.6 µm, a total gate-to-contact overlap ($L_{ov,\text{total}}$) of 10 µm and a channel width ($W$) of 100 µm. (A) Output characteristics for gate-source voltages ($V_{GS}$) from 0 to -3 V in steps of 0.5 V. (B) SEM micrographs of the channel region of the TFT.

Fig. S7| Relation between channel length, contact resistance and transit frequency. The curves were calculated using Equation (4) for width-normalized contact resistances ($R_{C}W$) of 10, 50 and 100 Ωcm, gate-to-source and gate-to-drain overlaps ($L_{ov,GS}$, $L_{ov,GD}$) of 5 µm, an intrinsic channel mobility ($\mu_0$) of 5 cm$^2$ V$^{-1}$ s$^{-1}$ and a gate-overdrive voltage ($|V_{GS}-V_{th}|$) of 2 V.
<table>
<thead>
<tr>
<th>Reference</th>
<th>Substrate</th>
<th>Device</th>
<th>Voltage (V)</th>
<th>( f_T/V ) (MHz V(^{-1}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Crone, J. Appl. Phys., vol. 89, p. 5125, 2001</td>
<td>Rigid</td>
<td>RO*</td>
<td>100</td>
<td>5 \times 10^{-4}</td>
</tr>
<tr>
<td>Sheraw, Int’l Electr. Dev. Meeting 2000</td>
<td>Flexible</td>
<td>RO*</td>
<td>20</td>
<td>0.00125</td>
</tr>
<tr>
<td>Fix, Appl. Phys. Lett., vol. 81, p. 1735, 2002</td>
<td>Flexible</td>
<td>RO*</td>
<td>80</td>
<td>0.0092</td>
</tr>
<tr>
<td>Wagner, Appl. Phys. Lett., vol. 89, p. 243515, 2006</td>
<td>Rigid</td>
<td>RO*</td>
<td>10</td>
<td>0.2</td>
</tr>
<tr>
<td>Heremans, Int’l Electr. Dev. Meeting 2009</td>
<td>Flexible</td>
<td>RO*</td>
<td>20</td>
<td>0.2</td>
</tr>
<tr>
<td>Zschieschang, Org. Electronics, vol. 14, p. 1516, 2013</td>
<td>Flexible</td>
<td>RO*</td>
<td>4</td>
<td>0.42</td>
</tr>
<tr>
<td>Kitamura, Appl. Phys. Lett., vol. 95, p. 023503, 2009</td>
<td>Rigid</td>
<td>TFT(^a)</td>
<td>25</td>
<td>0.8</td>
</tr>
<tr>
<td>Kitamura, Jpn. J. Appl. Phys., vol. 50, p. 01BC01, 2011</td>
<td>Rigid</td>
<td>TFT(^a)</td>
<td>25</td>
<td>1.11</td>
</tr>
<tr>
<td>Yamamura, Sci. Adv., vol. 4, p. eaao5758, 2018</td>
<td>Rigid</td>
<td>TFT(^a)</td>
<td>10</td>
<td>2</td>
</tr>
<tr>
<td>Perinot, Adv. Sci., vol. 6, p. 1801566, 2019</td>
<td>Flexible</td>
<td>TFT(^a)</td>
<td>14</td>
<td>2.06</td>
</tr>
<tr>
<td>Borchert, Int’l Electr. Dev. Meeting 2018</td>
<td>Flexible</td>
<td>TFT(^b)</td>
<td>3</td>
<td>2.23</td>
</tr>
<tr>
<td>Kheradmam-Boroujeni, Sci. Rep., vol. 8, p. 7643, 2018</td>
<td>Rigid</td>
<td>TFT(^c)</td>
<td>8.6</td>
<td>4.65</td>
</tr>
<tr>
<td>This work</td>
<td>Flexible</td>
<td>TFT(^b)</td>
<td>3</td>
<td>7</td>
</tr>
</tbody>
</table>

\(^{a}\) Small-signal currents directly measured to evaluate \( f_T \).

\(^{b}\) S-parameter measurement to evaluate \( f_T \).

\(^{c}\) Pulsed-bias measurement circuit to evaluate \( f_T \).

*In cases where the data were obtained from measurements on ring oscillators (RO), the equivalent frequency \( f_{eq} = 1/(2\tau) \) is normalized to the supply voltage.
REFERENCES


